To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

2SK3454

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3454 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3454	Isolated TO-220

FEATURES

- Gate voltage rating ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.63 Ω MAX. (V_{GS} = 10 V, I_D = 4.0 A)
- Low input capacitance
  C_{iss} = 400 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Built-in gate protection diode
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	250	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current(DC) (T_C = 25°C)	$I_{D(DC)}$	±7.0	A
Drain Current(pulse) Note1	$I_{D(pulse)}$	±21	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	2.0	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	30	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	7.0	A
Single Avalanche Energy Note2	E_{AS}	49	mJ

Notes1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 125 V, R_G = 25 Ω , V_{GS} = 20 V→0 V

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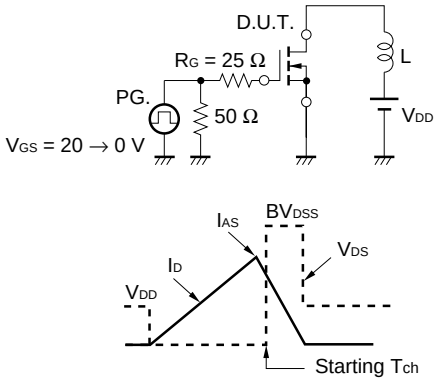
Printed in Japan

The mark ★ shows major revised points.

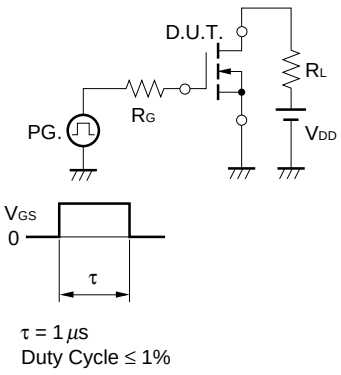
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain Leakage Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		4.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 4.0 A	1.0			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.0 A		0.5	0.63	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		400		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		110		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		55		pF
Turn-on Delay Time	$T_{d(on)}$	V_{DD} = 125 V, I_D = 4.0 A		11		ns
Rise Time	T_r	$V_{GS(on)}$ = 10 V		18		ns
Turn-off Delay Time	$T_{d(off)}$	R_G = 10 Ω		32		ns
Fall Time	T_f			15		ns
Total Gate Charge	Q_G	V_{DD} = 200 V		18		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		3.5		nC
Gate to Drain Charge	Q_{GD}	I_D = 7.0 A		10		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	T_{rr}	I_F = 7.0 A, V_{GS} = 0 V		250		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		1.0		μC

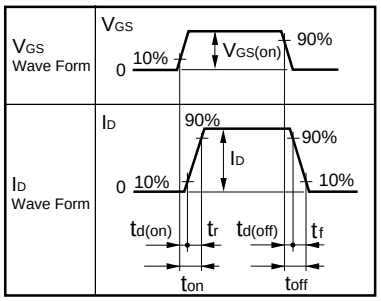
TEST CIRCUIT 1 AVALANCHE CAPABILITY



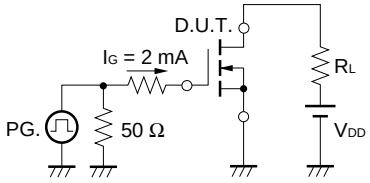
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

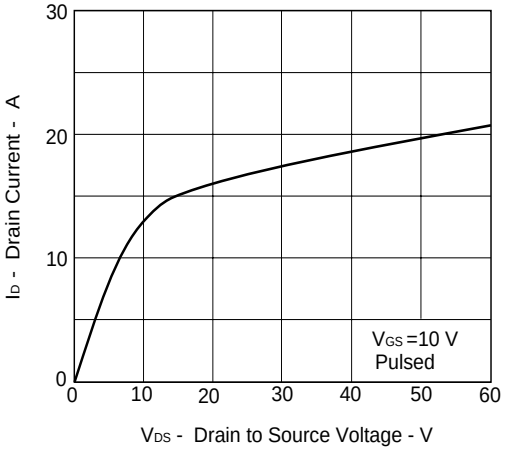


TEST CIRCUIT 3 GATE CHARGE

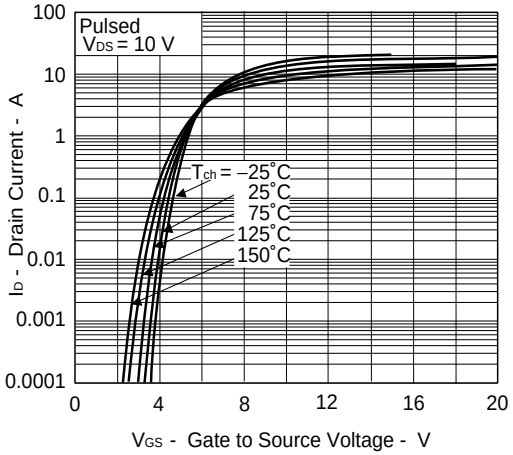


TYPICAL CHARACTERISTICS

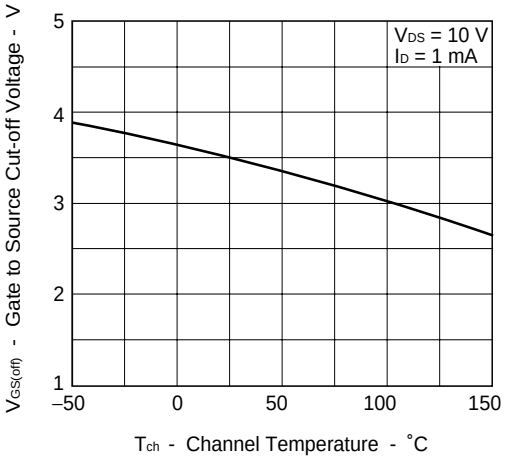
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



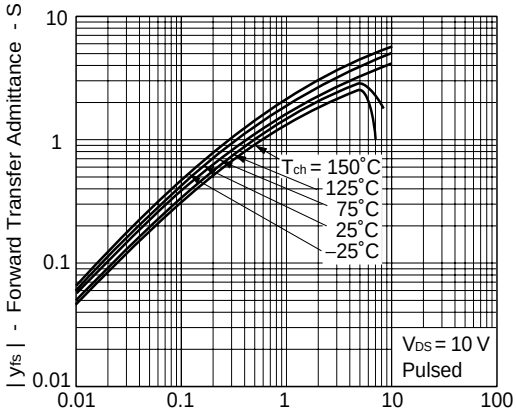
FORWARD TRANSFER CHARACTERISTICS



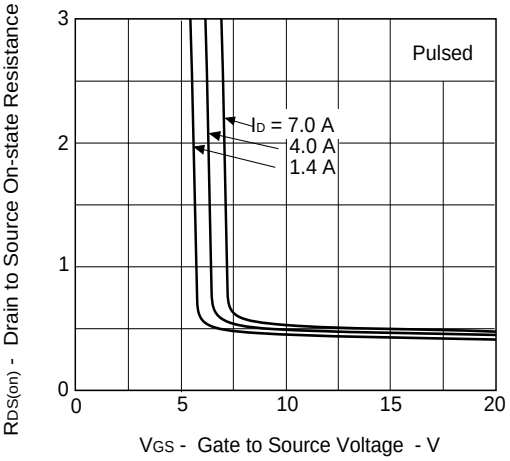
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



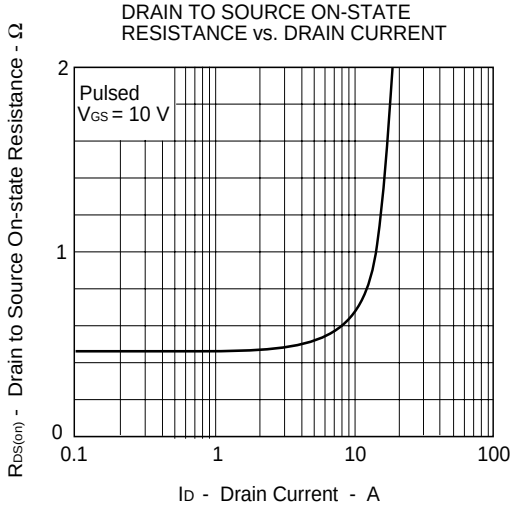
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



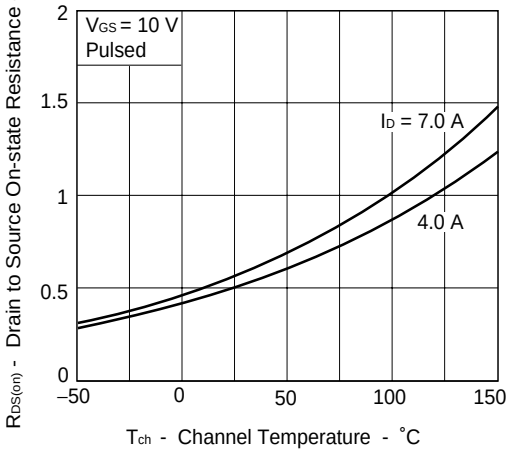
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



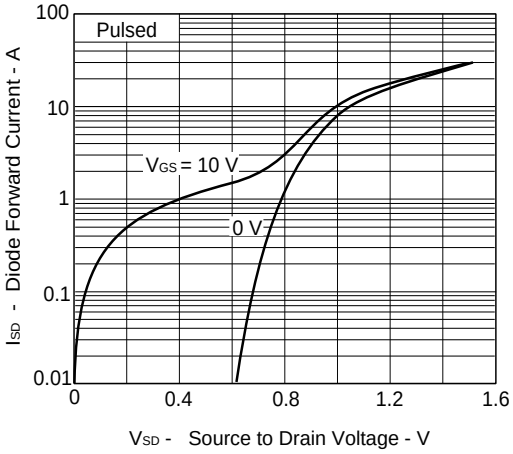
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



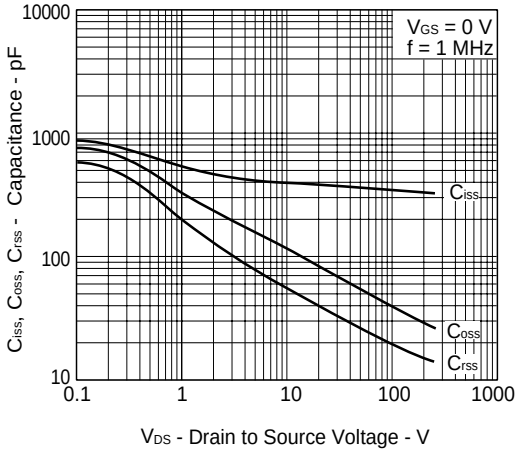
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



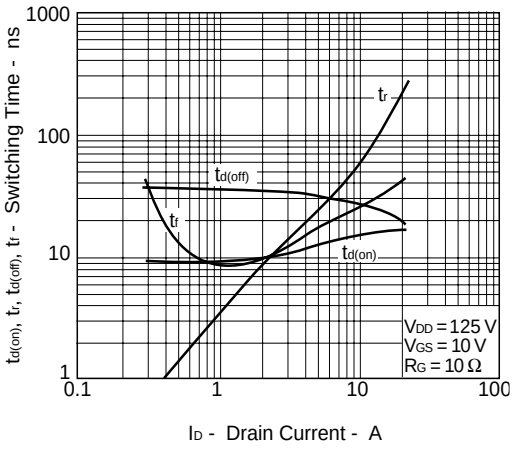
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



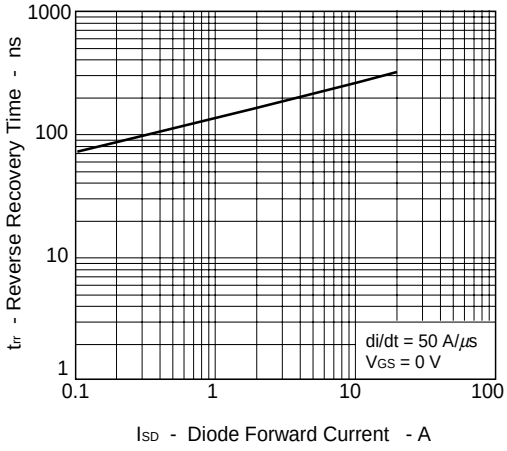
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



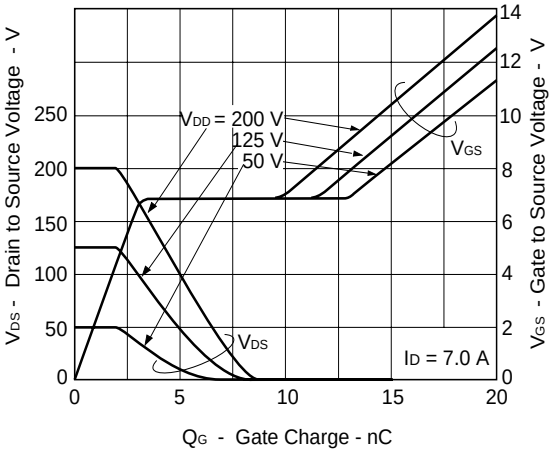
SWITCHING CHARACTERISTICS



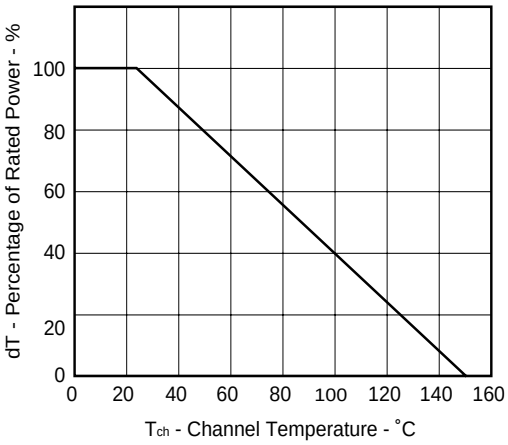
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



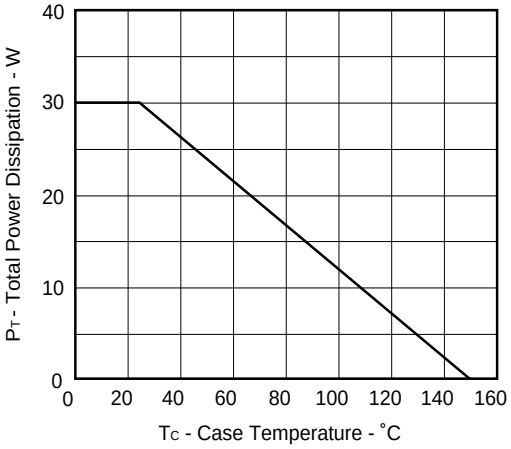
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



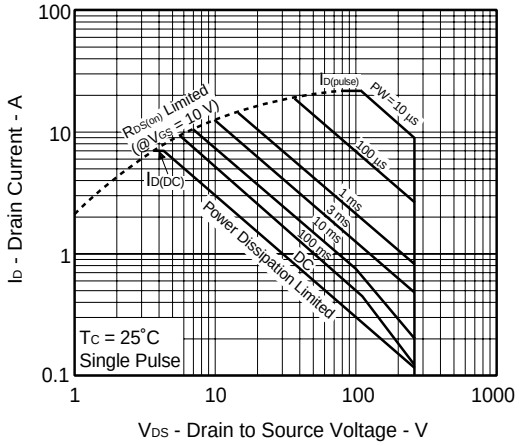
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



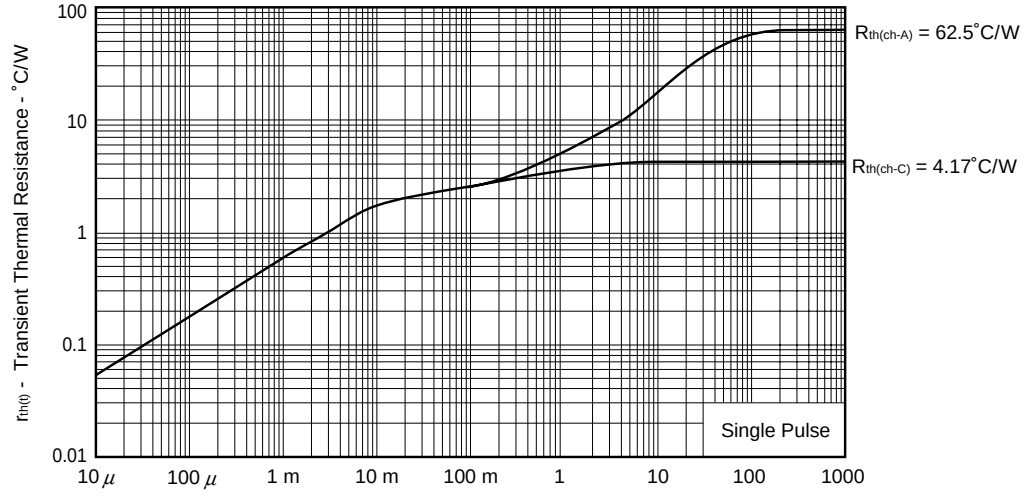
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



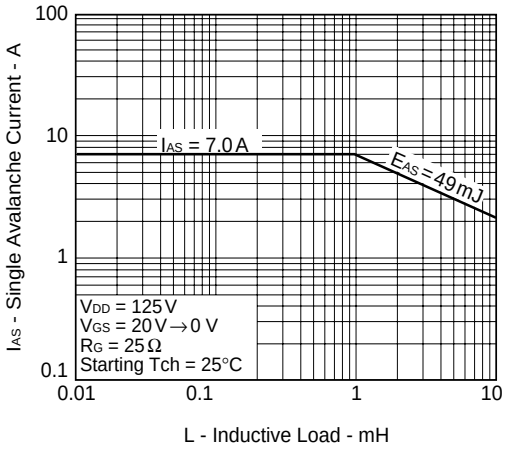
★ FORWARD BIAS SAFE OPERATING AREA



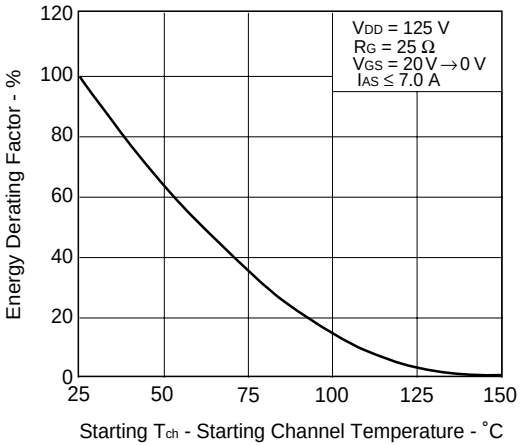
★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

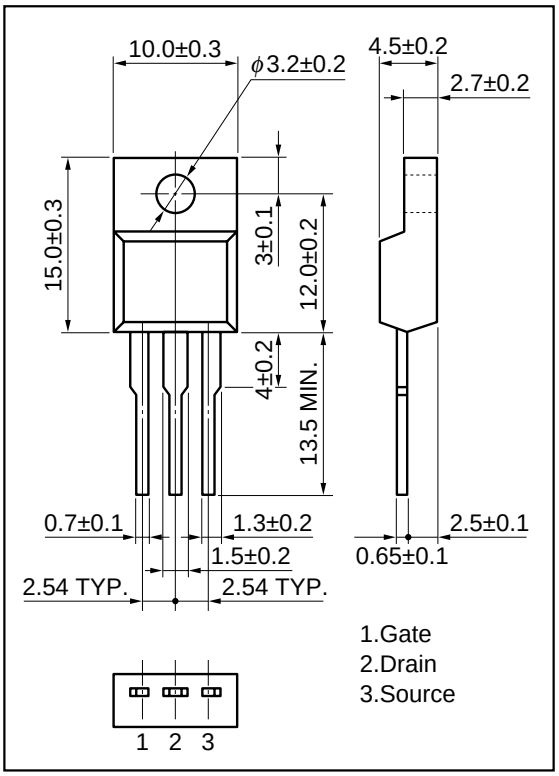


SINGLE AVALANCHE ENERGY
DERATING FACTOR

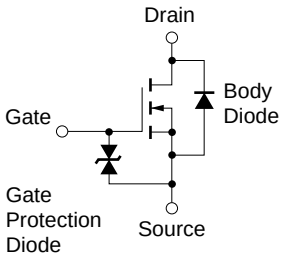


PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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