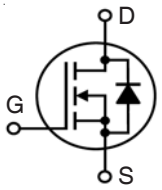
IXYS

X3-Class HiPerFET™ Power MOSFET

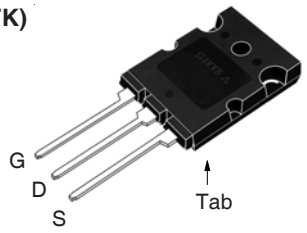
IXFK210N30X3
IXFX210N30X3

V_{DSS} = 300V
I_{D25} = 210A
$R_{DS(on)}$ ≤ 5.5mΩ

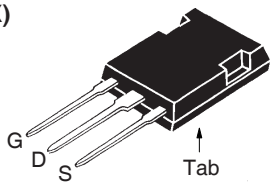
N-Channel Enhancement Mode
Avalanche Rated



TO-264 (IXFK)



PLUS247 (IXFX)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	300	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	300	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	210	A
$I_{L(RMS)}$	External Lead Current Limit	160	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	650	A
I_A	T_C = 25°C	105	A
E_{AS}	T_C = 25°C	3	J
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	50	V/ns
P_D	T_C = 25°C	1250	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in
F_C	Mounting Force (PLUS247)	20..120 /4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA	2.5		4.5	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			25	μA
	T_J = 125°C			2.5	mA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1		4.3	5.5	mΩ

Features

- International Standard Packages
- Low $R_{DS(ON)}$ and Q_G
- Avalanche Rated
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
g_{fs}	V_{DS} = 10V, I_D = 60A, Note 1	84	140		S
R_{Gi}	Gate Input Resistance		2		Ω
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		24.2		nF
C_{oss}			3.1		nF
C_{rss}			7.7		pF
	Effective Output Capacitance				
$C_{o(er)}$	Energy related; V_{GS} = 0V, V_{DS} = 0.8 • V_{DSS}		1100		pF
$C_{o(tr)}$	Time related; V_{GS} = 0V, V_{DS} = 0.8 • V_{DSS}		4600		pF
$t_{d(on)}$	**Resistive Switching Times**		38		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		40		ns
$t_{d(off)}$	R_G = 1Ω (External)		210		ns
t_f			15		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		375		nC
Q_{gs}			107		nC
Q_{gd}			100		nC
R_{thJC}				0.10	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
I_S	V_{GS} = 0V			210	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			840	A
V_{SD}	I_F = 100A, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 105A, -di/dt = 100A/μs		190		ns
Q_{RM}	V_R = 100V		1.4		μC
I_{RM}			15		A

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

Fig. 1. Output Characteristics @ T_J = 25°C

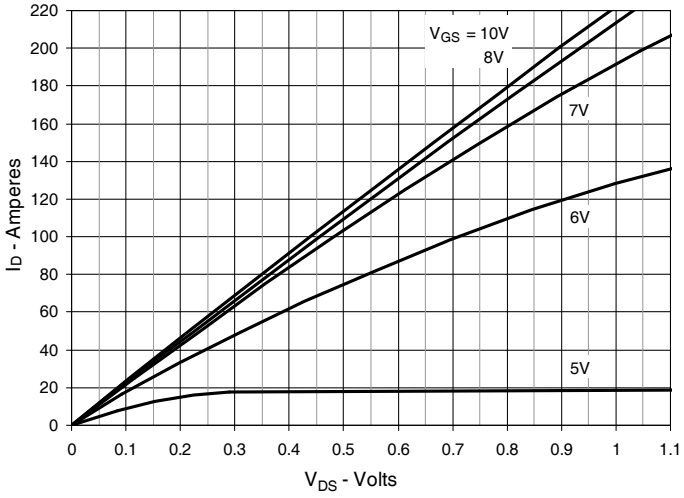


Fig. 2. Extended Output Characteristics @ T_J = 25°C

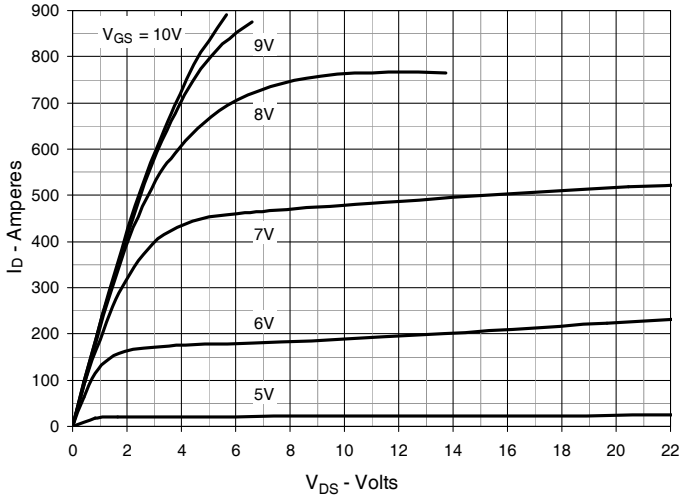


Fig. 3. Output Characteristics @ T_J = 125°C

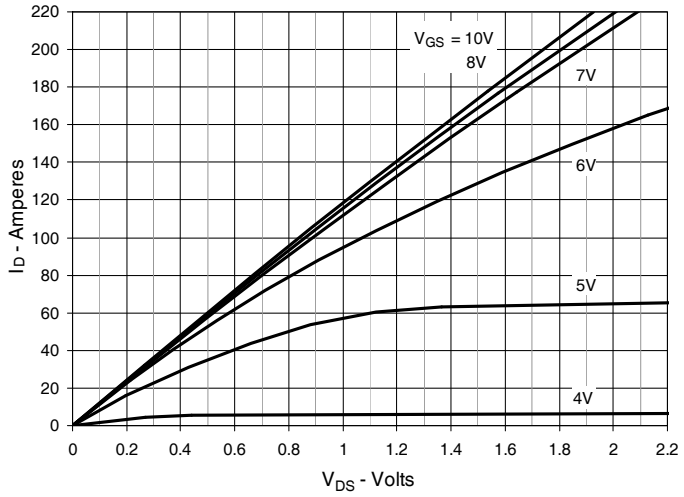


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 105A Value vs. Junction Temperature

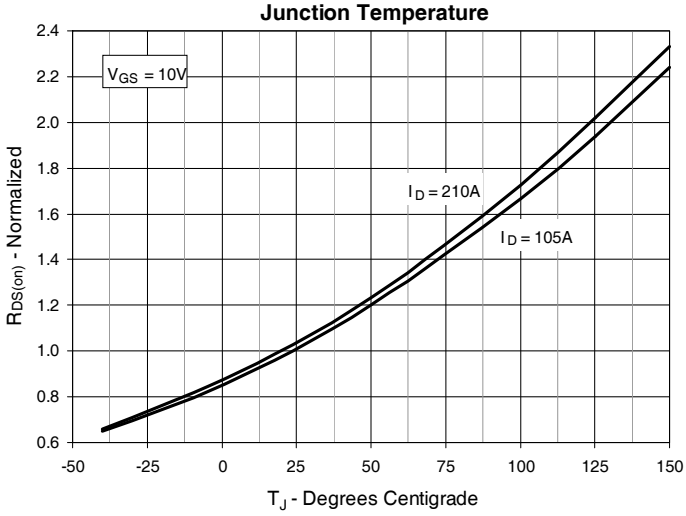


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 105A Value vs. Drain Current

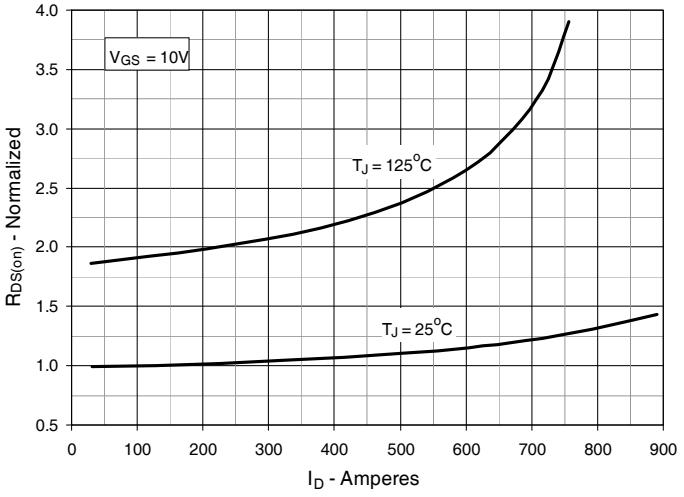


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

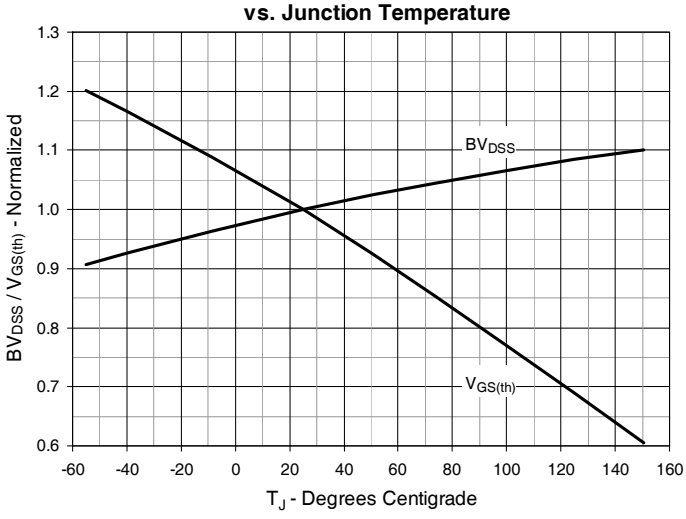


Fig. 7. Maximum Drain Current vs. Case Temperature

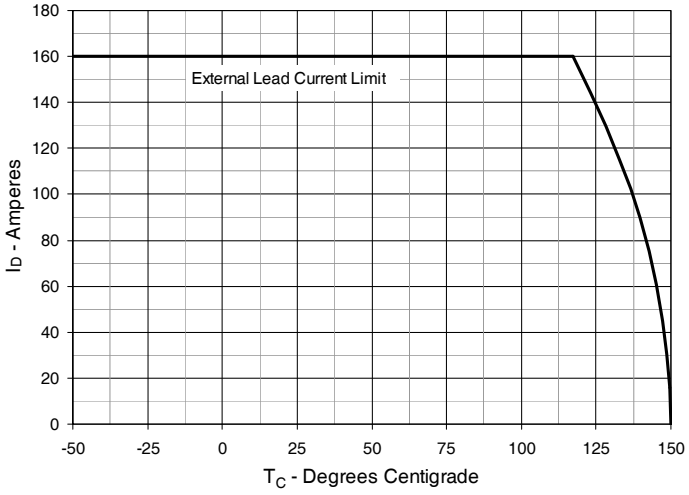


Fig. 8. Input Admittance

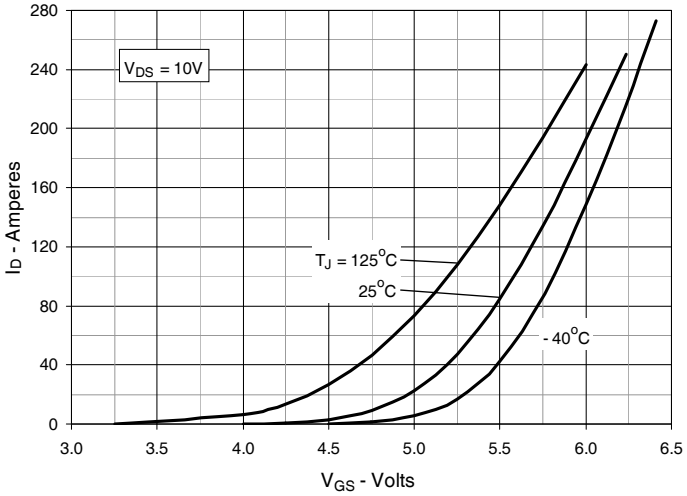


Fig. 9. Transconductance

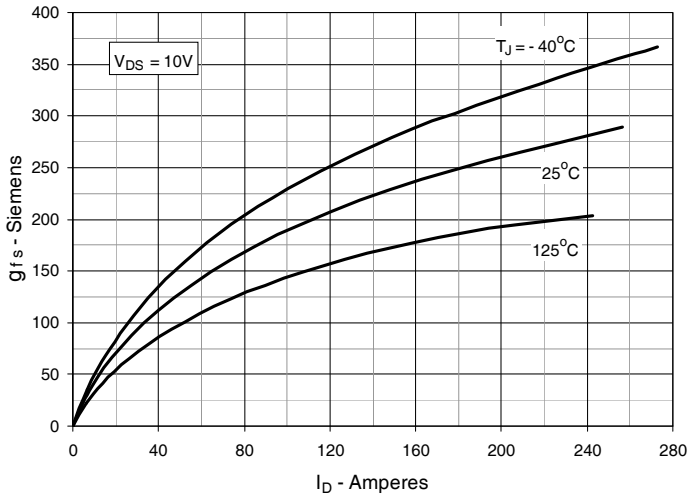


Fig. 10. Forward Voltage Drop of Intrinsic Diode

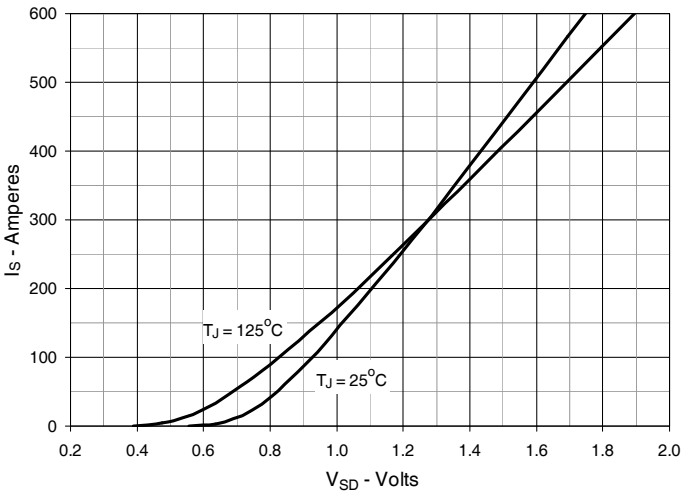


Fig. 11. Gate Charge

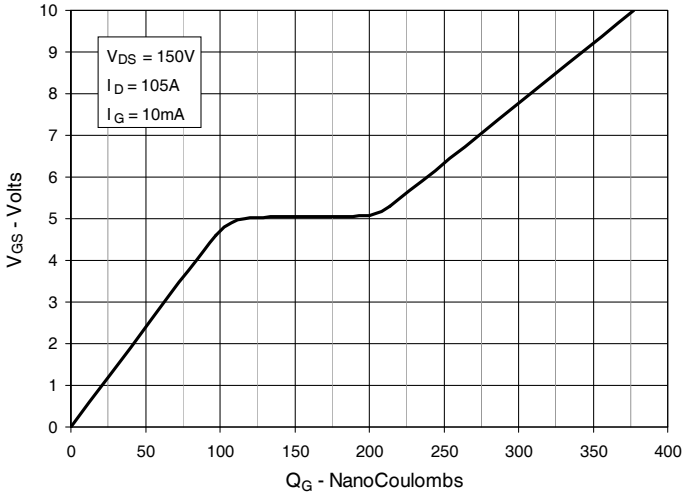


Fig. 12. Capacitance

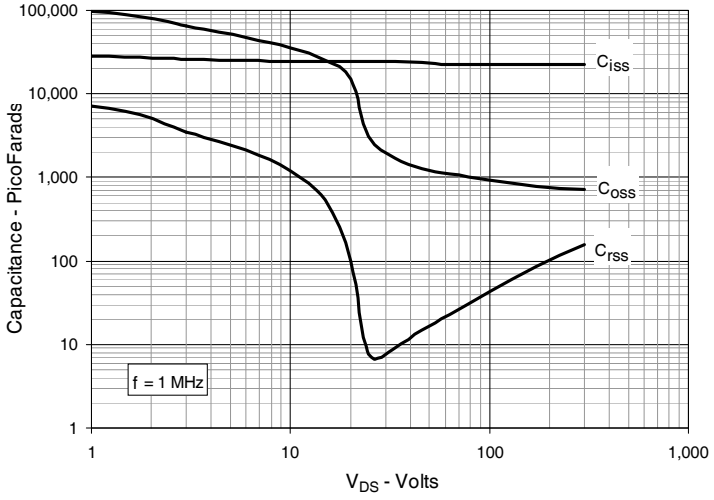


Fig. 13. Output Capacitance Stored Energy

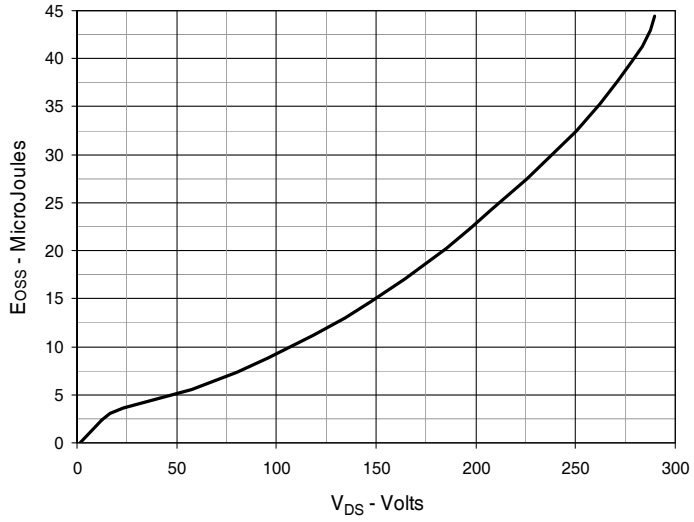


Fig. 14. Forward-Bias Safe Operating Area

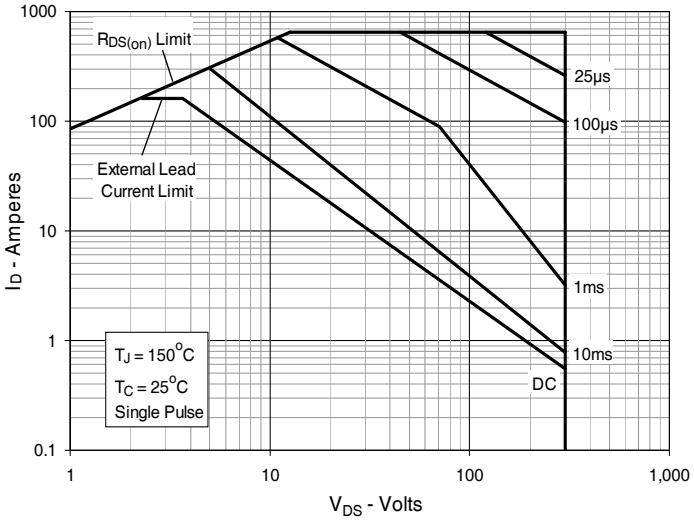
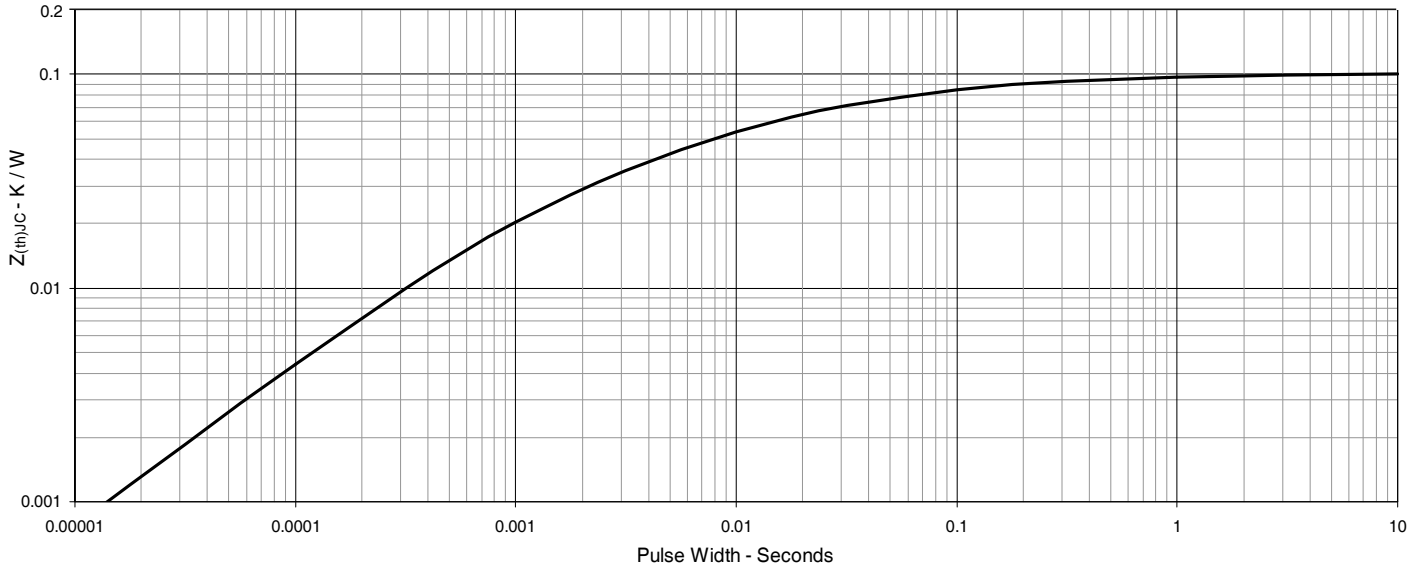
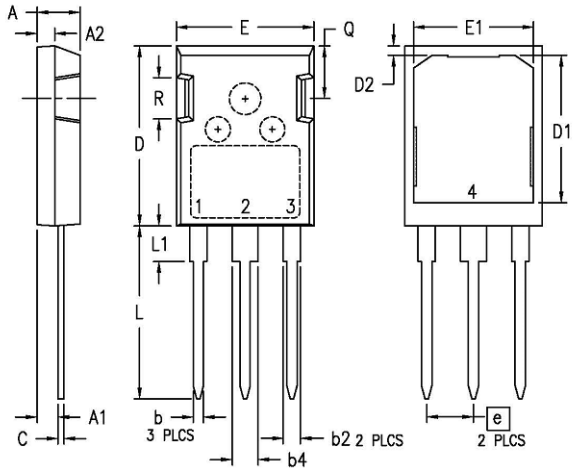


Fig. 15. Maximum Transient Thermal Impedance



PLUS247 Outline

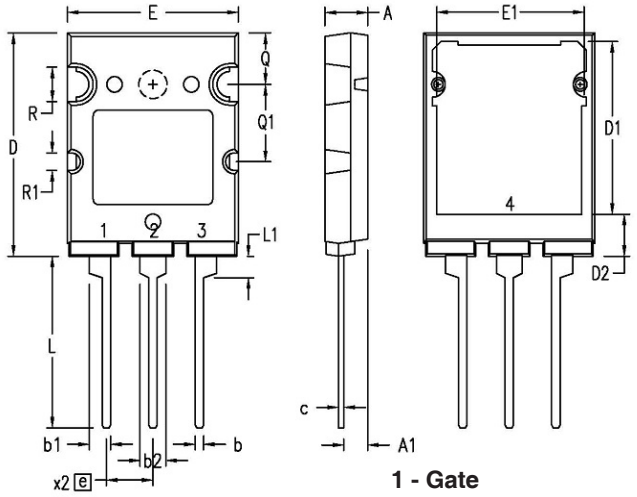


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.520	.560	13.08	14.22
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83

1 - Gate
2,4 - Drain
3 - Source

NOTE:
1. This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD (R-PSIP-F3) except screw mounting hole.
2. Pin #2 is connected to the bottom heatsink (#4).
3. Lead finish – One of the following depending on the packaging plants.
   3.1 Matte pure tin plating on the leads and back heatsink.
   3.2 Pb free solder dip on the leads and pre Ni plated back heatsink.

TO-264 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.30
A1	.102	.118	2.60	3.00
b	.035	.049	0.90	1.25
b1	.091	.106	2.30	2.70
b2	.110	.126	2.80	3.20
c	.020	.033	0.50	0.85
D	1.012	1.035	25.70	26.30
D1	.783	.799	19.90	20.30
D2	.185	.205	4.70	5.20
E	.776	.799	19.70	20.30
E1	.661	.677	16.80	17.20
e	.215 BSC		5.46 BSC	
L	.768	.807	19.50	20.50
L1	.091	.106	2.30	2.70
Q	.228	.244	5.80	6.20
Q1	.346	.362	8.80	9.20
øR	.150	.165	3.80	4.20
øR1	.071	.087	1.80	2.20

1 - Gate
2,4 - Drain
3 - Source

NOTE: Leads and back heatsink are Matte Pure Tin plated.