

Vishay Siliconix

# N-Channel 200 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY						
V <sub>DS</sub> (V)	200					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0150					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.0165					
Q <sub>g</sub> typ. (nC)	58					
I <sub>D</sub> (A)	90					
Configuration	Single					

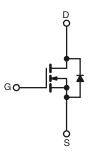
#### **FEATURES**

- ThunderFET® power MOSFET
- Maximum 175 °C junction temperature
- 100 % R<sub>q</sub> and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



#### **APPLICATIONS**

- Power supplies:
  - Uninterruptible power supplies
  - AC/DC switch-mode power supplies
  - Lighting
- Synchronous rectification
- DC/DC converter
- Motor drive switch
- DC/AC inverter
- · Solar micro inverter
- · Class D audio amplifier



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and halogen-free	SUM90142E-GE3

<b>ABSOLUTE MAXIMUM RATI</b>	NGS (T <sub>A</sub> = 25 °C, u	nless other	wise noted)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	200	V
Gate-source voltage		V <sub>GS</sub>	± 20	V
Continuous drain current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	90	
	T <sub>C</sub> = 125 °C		52	
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	240	Α
Continuous source-drain diode current		I <sub>S</sub>	90	
Single pulse avalanche current <sup>a</sup>	L = 0.1 mH	I <sub>AS</sub>	60	
Single pulse avalanche energy <sup>a</sup>	L = 0.1 mm	E <sub>AS</sub>	180	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	375 <sup>b</sup>	14/
	T <sub>C</sub> = 125 °C		125 <sup>b</sup>	W
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	00
Soldering recommendations (peak temperature) <sup>c</sup>			260	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	MAXIMUM	UNIT	
Maximum junction-to-ambient (PCB mount) <sup>c</sup>		R <sub>thJA</sub>	40	°C/W	
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	0.4	C/VV	

#### **Notes**

- a. Duty cycle ≤ 1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR4 material).
- d. Package limited.



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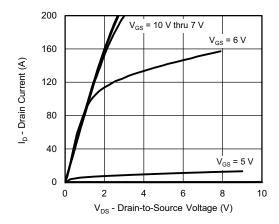
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	2	-	4	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	250	nA	
	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	-	-	1	μА	
Zero gate voltage drain current		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	150		
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	5	mA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	60	-	-	Α	
During and a solution of the s		$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$	-	0.0123	0.0150		
Drain-source on-state resistance a	R <sub>DS(on)</sub>	$V_{GS} = 7.5 \text{ V}, I_D = 30 \text{ A}$	-	0.0130	0.0165	Ω	
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	-	63	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	3120	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	280	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	24	-		
Total gate charge	Qg		-	58	87	nC	
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$	-	17.6	-		
Gate-drain charge	Q <sub>gd</sub>		-	17.2	-		
Output charge	Q <sub>oss</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	-	108	162		
Gate resistance	R <sub>q</sub>	f = 1 MHz	1.5	3	5	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	14	28		
Rise time	t <sub>r</sub>	$V_{DD} = 100 \text{ V}, R_{I} = 1.66 \Omega, I_{D} \cong 60 \text{ A},$	-	125	250	1	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	27	54	ns	
Fall time	t <sub>f</sub>		-	80	150		
Drain-Source Body Diode Characteristic	cs						
Pulse diode forward current (t = 100 μs)	I <sub>SM</sub>		-	-	240	Α	
Body diode voltage	$V_{SD}$	$I_F = 30 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.85	1.5	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	150	300	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	1 00 4 41/-11 400 47 -	-	0.9	1.8	nC	
Reverse recovery fall time	ta	$I_F = 30 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$	-	125	-		
Reverse recovery rise time	t <sub>b</sub>		-	25	-	ns	
Body diode peak reverse recovery charge	I <sub>RM(REC)</sub>		-	11.5	20	Α	

#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





#### **Output Characteristics**

V<sub>GS</sub> = 7.5 V

0.016

0.015

0.014

0.013

0.012

0.011

0

20

R<sub>DS(on)</sub> - On-Resistance (Ω)





I<sub>D</sub> - Drain Current (A)

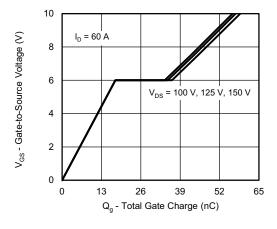
40

V<sub>GS</sub> = 10 V

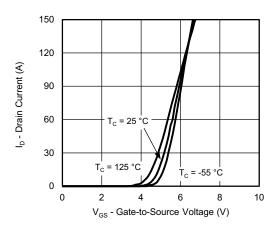
60

80

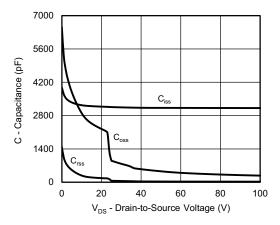
100



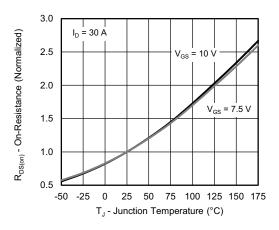
**Gate Charge** 



**Transfer Characteristics** 

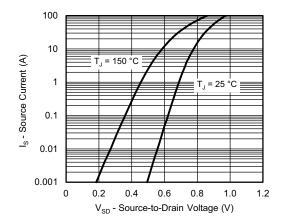


Capacitance

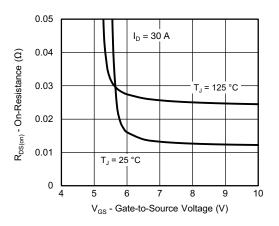


On-Resistance vs. Junction Temperature

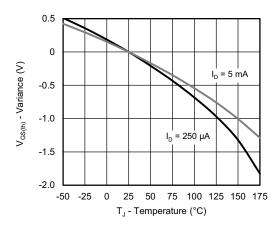




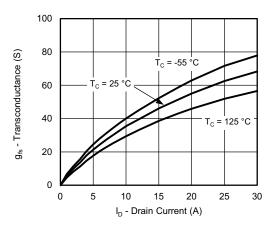
Source-Drain Diode Forward Voltage



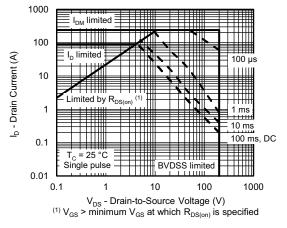
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

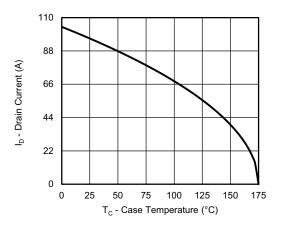


Transconductance

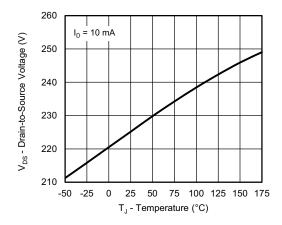


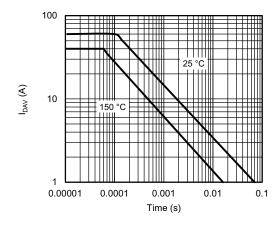
Safe Operating Area, Junction-to-Ambient





#### Current Derating a





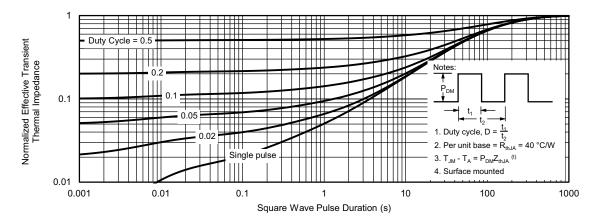
Drain Source Breakdown vs. Junction Temperature

I<sub>DAV</sub> vs. Time

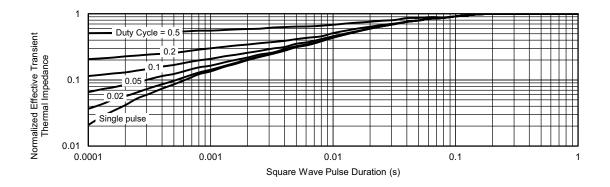
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

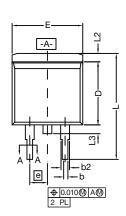


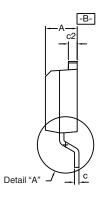
Normalized Thermal Transient Impedance, Junction-to-Case

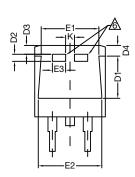
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# TO-263 (D<sup>2</sup>PAK): 3-LEAD

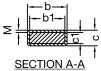








DETAIL A (ROTATED 90°)



_   <del>  -</del> b1 <del></del>    , , ,	
≥ <del>                                    </del>	- -

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6. This feature is for thick lead.

		INCHES		MILLIMETERS		
	DIM.	MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.045 0.055		1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380 0.4		9.652	10.414	
	E1	0.245	-	6.223	=	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
е		0.100 BSC		2.54 BSC		
	K	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





# RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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