

October 1997

Features

- 70A, 30V
- $r_{DS(ON)} = 0.010\Omega$
- *Temperature Compensating PSPICE Model*
- *Peak Current vs Pulse Width Curve*
- *UIS Rating Curve (Single Pulse)*
- 175°C Operating Temperature
- **Related Literature**
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFP70N03	TO-220AB	RFP70N03
RF1S70N03	TO-262AA	F1S70N03
RF1S70N03SM	TO-263AB	F1S70N03

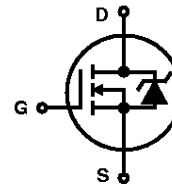
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g., RF1S70N03SM9A

Description

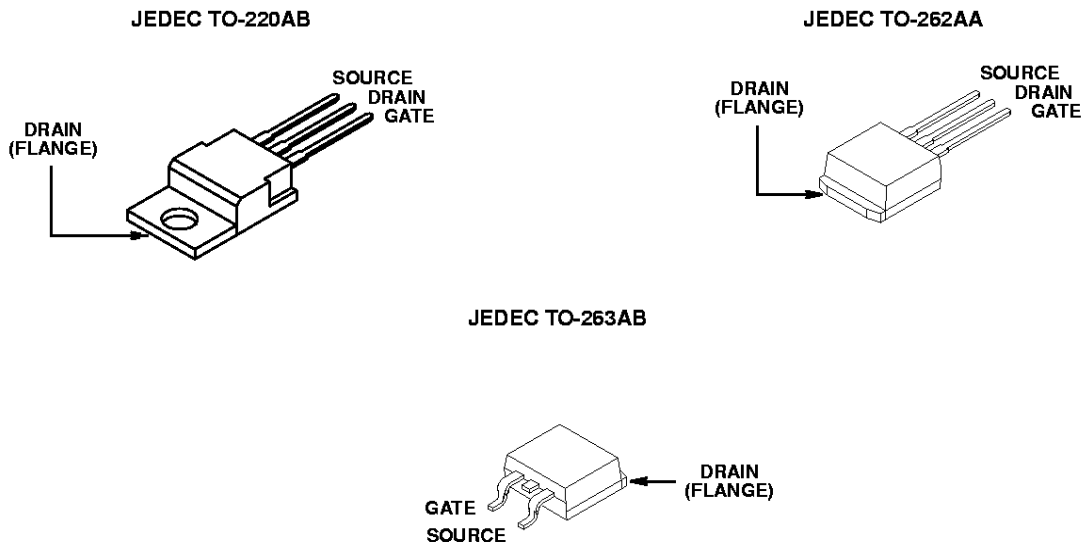
These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49025.

Symbol



Packaging



RFP70N03, RF1S70N03, RF1S70N03SM

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	70	A
Pulsed Drain Current	I_{DM}	200	A
Pulsed Avalanche Rating	E_{AS}	Figures 5, 13, 14	
Power Dissipation	P_D	150	W
Derate Above 25°C		1.0	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	$^\circ\text{C}$
Package Body for 10s, see Techbrief 334	T_{pkg}	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 10)	30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 9)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 70\text{A}, V_{GS} = 10\text{V}$ (Figure 8)	-	-	0.010	Ω
Turn-On Time	t_{ON}	$V_{DD} = 15\text{V}, I_D \cong 70\text{A},$ $R_L = 0.214\Omega, V_{GS} = 10\text{V},$ $R_{GS} = 2.5\Omega$ (Figures 17, 18)	-	-	80	ns
Turn-On Delay Time	$t_{d(ON)}$		-	20	-	ns
Rise Time	t_r		-	20	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	-	ns
Fall Time	t_f		-	25	-	ns
Turn-Off Time	t_{OFF}		-	-	125	ns
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V to } 20\text{V}$	-	215	260	nC
Gate Charge at 10V	$Q_g(10)$	$V_{GS} = 0\text{V to } 10\text{V}$				
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V to } 2\text{V}$				
		$V_{DD} = 24\text{V},$ $I_D \cong 70\text{A},$ $R_L = 0.343\Omega$ $I_g(REF) = 1.0\text{mA}$ (Figures 12,15,16)				
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$ (Figure 11)	-	3300	-	pF
Output Capacitance	C_{OSS}		-	1750	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	750	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	1.0	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220, TO-262, TO-263	-	-	62	$^\circ\text{C}/\text{W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 70\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 70\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves

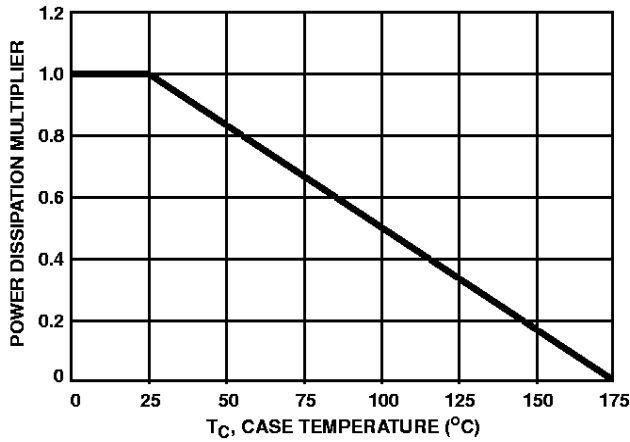


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

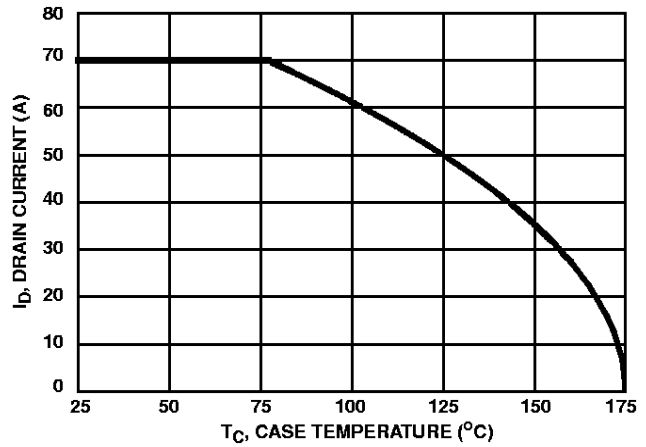


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

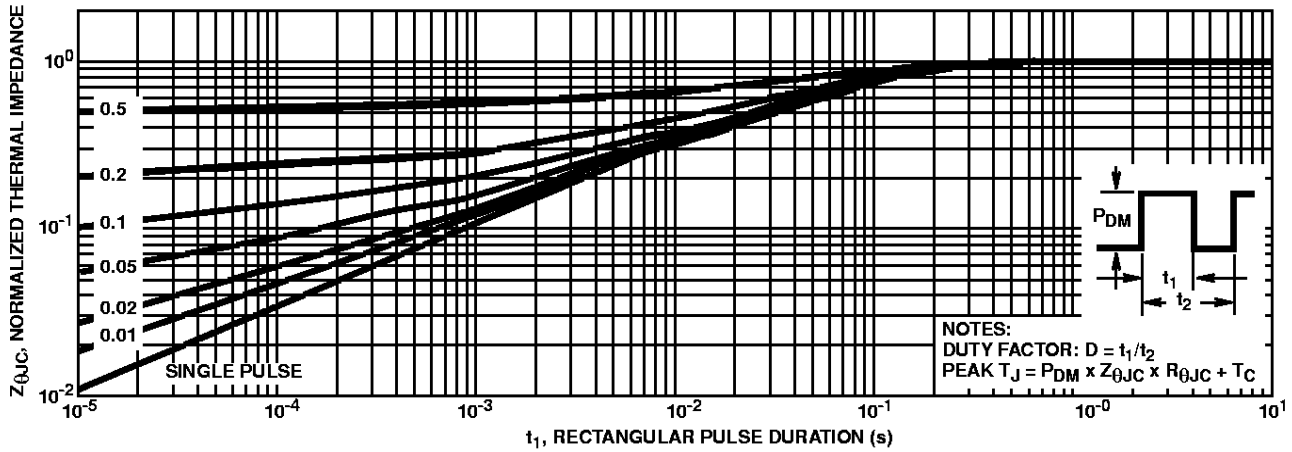


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

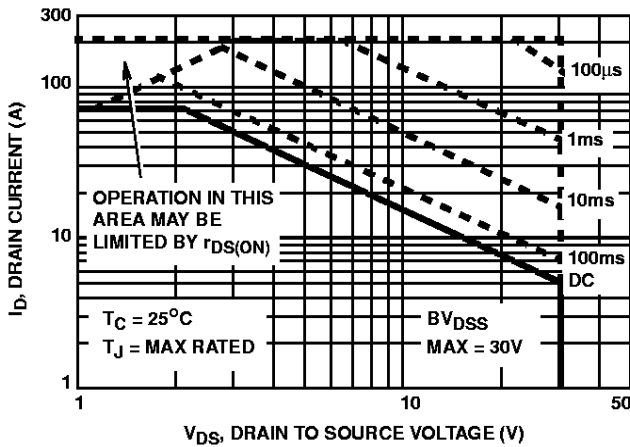
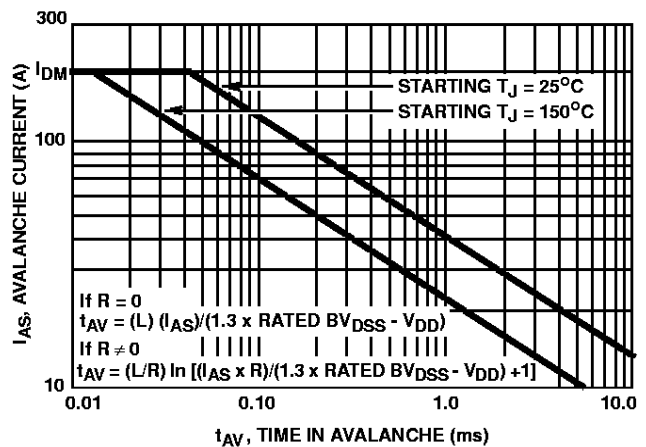


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Harris Application Notes 9321 and 9322.

FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

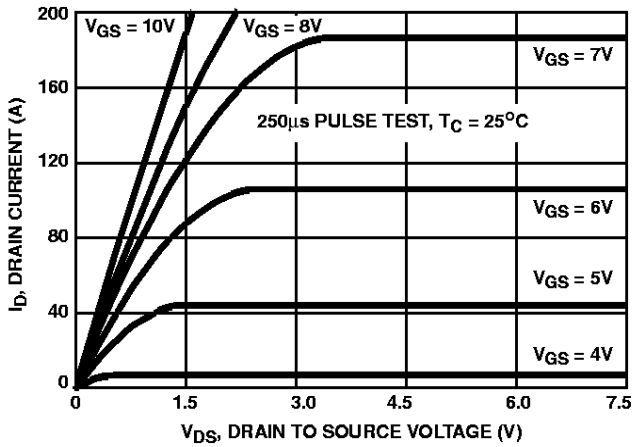


FIGURE 6. SATURATION CHARACTERISTICS

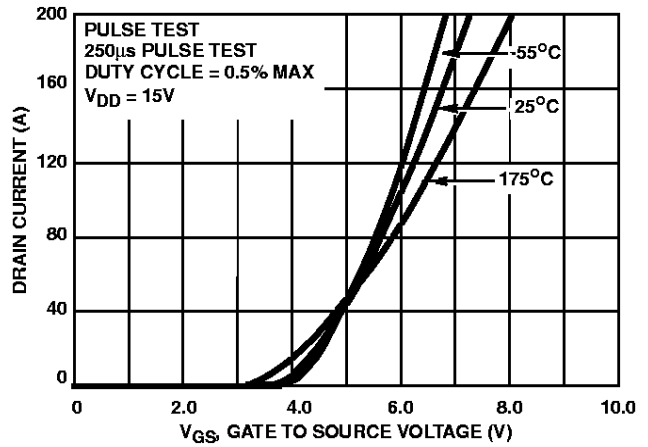


FIGURE 7. TRANSFER CHARACTERISTICS

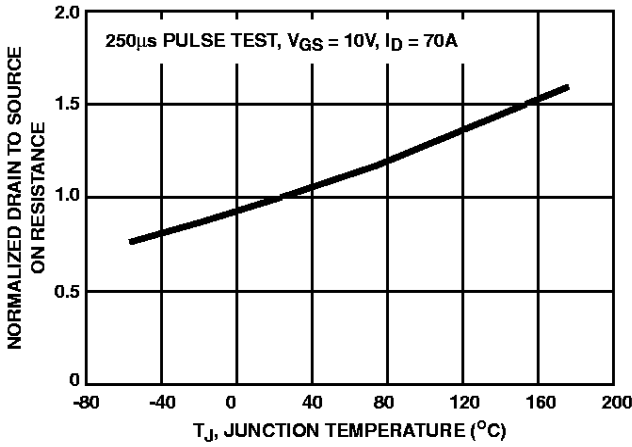


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

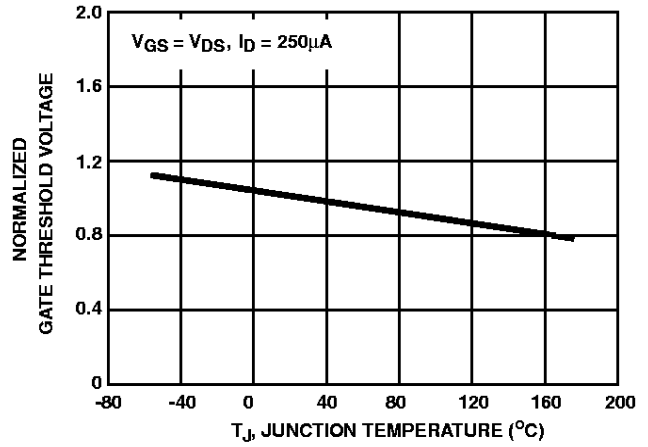


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

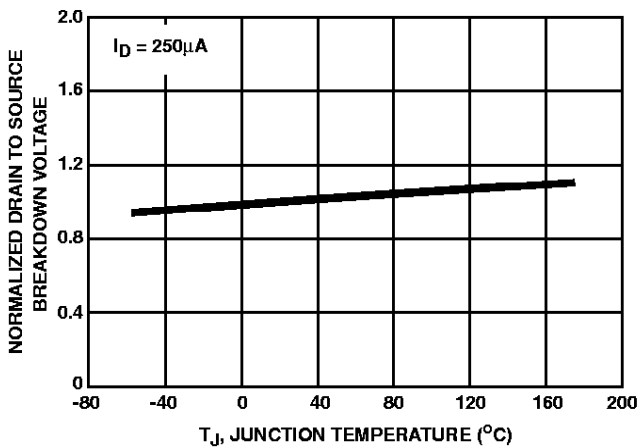


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

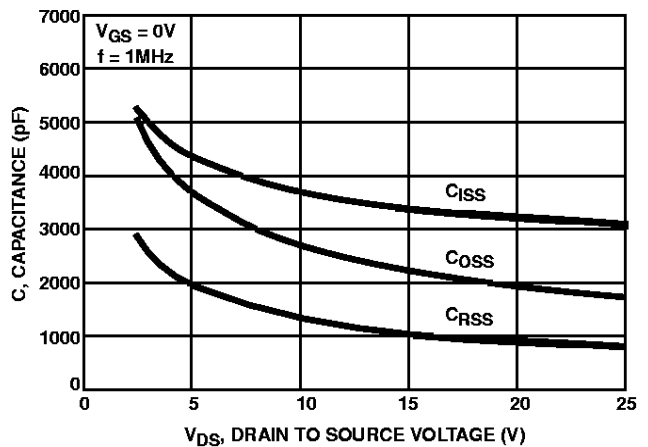
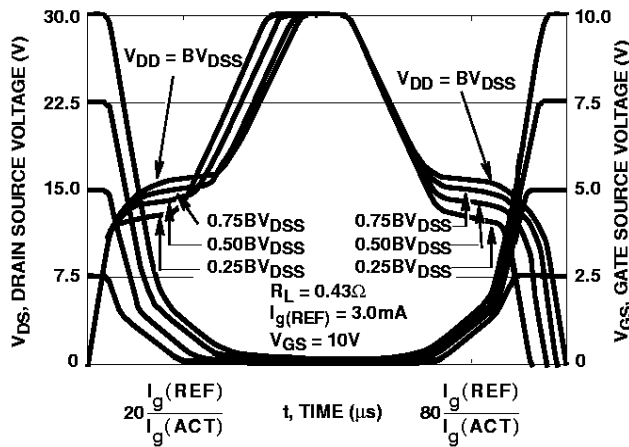


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 12. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

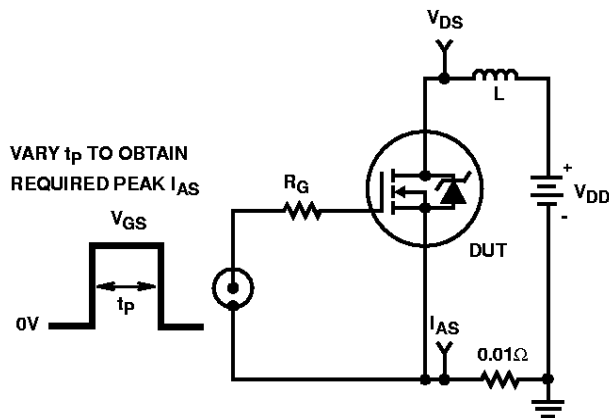


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

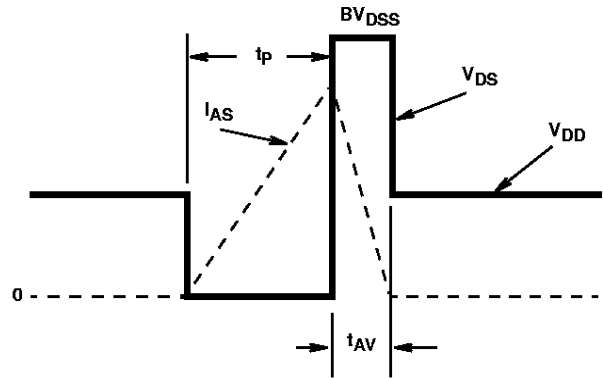


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

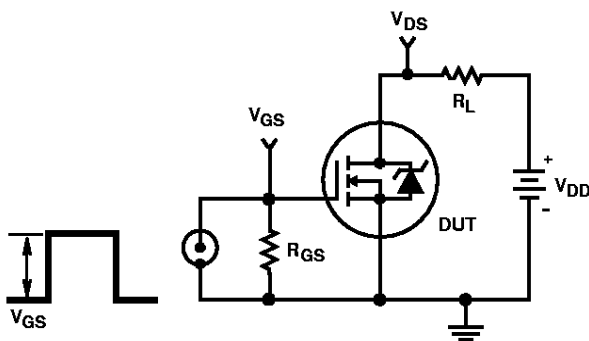


FIGURE 15. SWITCHING TIME TEST CIRCUIT

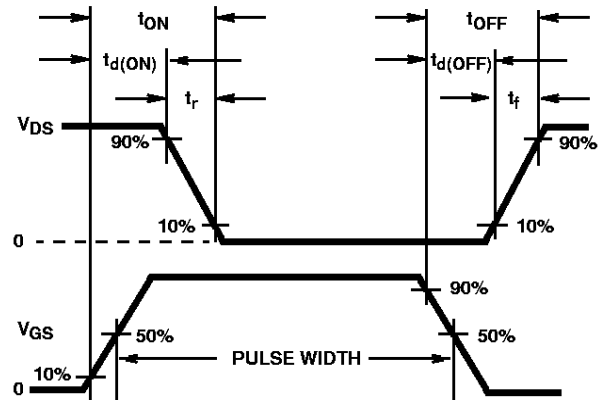


FIGURE 16. SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

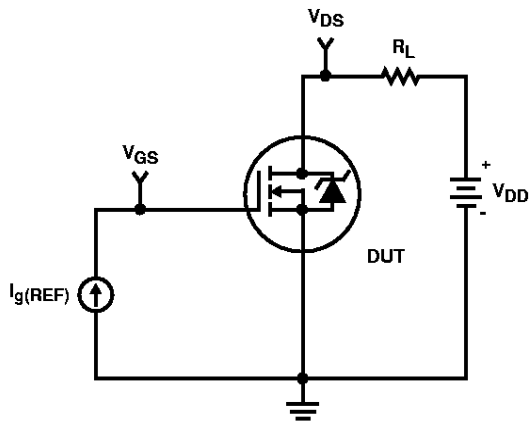


FIGURE 17. GATE CHARGE TEST CIRCUIT

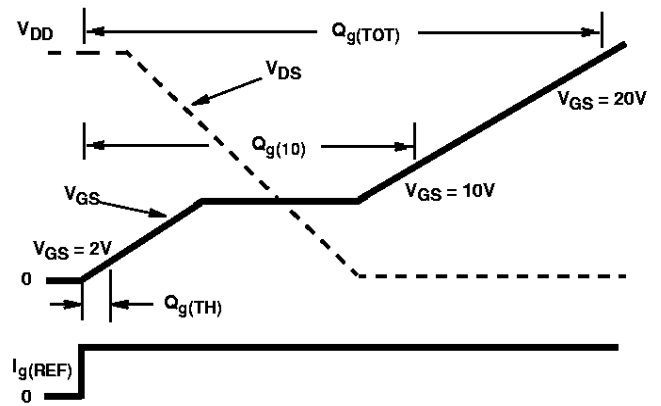


FIGURE 18. GATE CHARGE WAVEFORM

