

NP90N06VDK

60 V – 90 A – N-channel Power MOS FET

R07DS1297EJ0200 Rev.2.00 May 24, 2018

Data Sheet

Application: Automotive

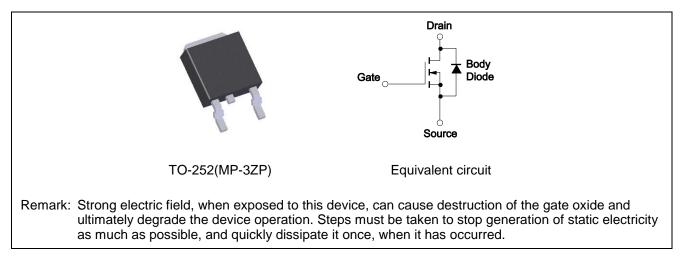
Description

NP90N06VDK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
- ---- $R_{DS(on)1} = 5.3 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 45 \text{ A}$)
- Low C_{iss} : $C_{iss} = 4000 \text{ pF TYP}$. ($V_{DS} = 25 \text{ V}$)
- Designed for automotive application and AEC-Q101 qualified

Outline



Ordering Information

Part No.	Lead Plating	Pac	Package		
NP90N06VDK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252(MP-3ZP)	
NP90N06VDK-E2-AY *1		Tape 2500 p/teel	Taping (E2 type)	10-252(1017-527)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)



Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 V$)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) ($T_c = 25^{\circ}C$)	I _{D(DC)}	±90	A
Drain Current (pulse) *1*3	I _{D(pulse)}	±360	A
Total Power Dissipation ($T_C = 25^{\circ}C$)	P _{T1}	147	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	P _{T2}	1.2	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *2*3	I _{AR}	33	A
Repetitive Avalanche Energy *2*3	E _{AR}	108	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *3	1.02	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A) *3	125	°C/W

Notes: *1. T_C = 25°C, PW \leq 10 $\mu s,$ Duty Cycle \leq 1%

- *2. R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V
- *3. Not subject of production test. Verified by design/characterization.



Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	V _{GS(th)}	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$
Forward Transfer Admittance *1	y _{fs}	40	80		S	$V_{DS} = 5 V, I_D = 45 A$
Drain to Source On-state	R _{DS(on)1}		3.8	5.3	mΩ	$V_{GS} = 10 \text{ V}, I_D = 45 \text{ A}$
Resistance *1	R _{DS(on)2}		4.9	8.2	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 23 \text{ A}$
Input Capacitance*2	Ciss		4000	6000	pF	$V_{DS} = 25 V,$
Output Capacitance*2	Coss		360	540	pF	$V_{GS} = 0 V,$
Reverse Transfer Capacitance*2	C _{rss}		110	200	pF	f = 1 MHz
Turn-on Delay Time*2	t _{d(on)}		24	60	ns	$V_{DD} = 30 \text{ V}, \text{ I}_{D} = 45 \text{ A},$
Rise Time*2	tr		7	20	ns	Vgs = 10 V,
Turn-off Delay Time*2	t _{d(off)}		60	120	ns	R _G = 0 Ω
Fall Time*2	t _f		6	20	ns	_
Total Gate Charge*2	Q _G		63	95	nC	$V_{DD} = 48 V,$
Gate to Source Charge	Q _{GS}		15		nC	V _{GS} = 10 V,
Gate to Drain Charge	Q _{GD}		12		nC	I _D = 90 A
Body Diode Forward Voltage *1	VF(S-D)		0.9	1.5	V	I _F = 90 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		40		ns	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Qrr		45		nC	di/dt = 100 A/µs

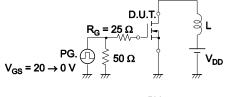
Electrical Characteristics (T_A = 25°C)

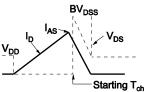
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

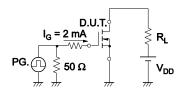
TEST CIRCUIT 1 AVALANCHE CAPABILITY

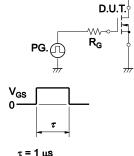
TEST CIRCUIT 2 SWITCHING TIME



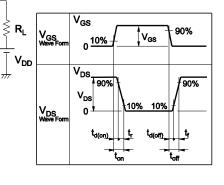


TEST CIRCUIT 3 GATE CHARGE



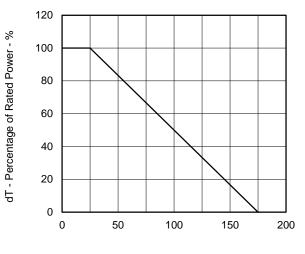






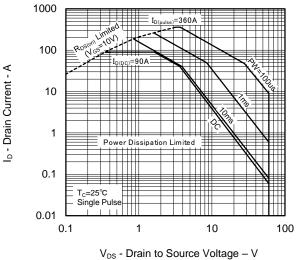
Typical Characteristics (T_A = 25°C)

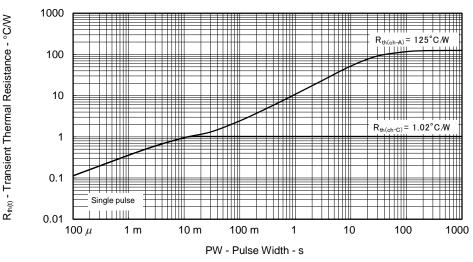
DERATING FACTOR OF FORWARD BIAS SAFE **OPERATING AREA**

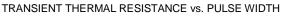


T_c - Case Temperature - °C



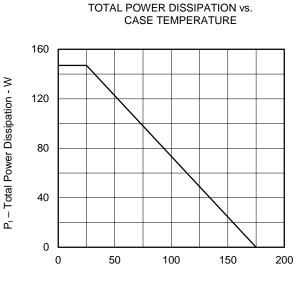




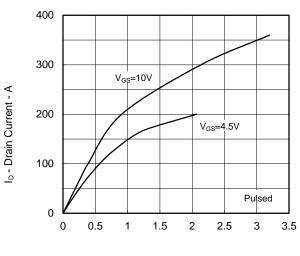


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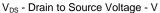


T_c - Case Temperature - °C

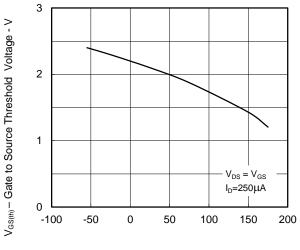


DRAIN CURRENT vs.

DRAIN TO SOURCE VOLTAGE

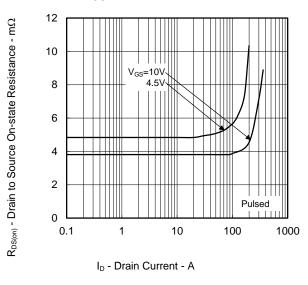


GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

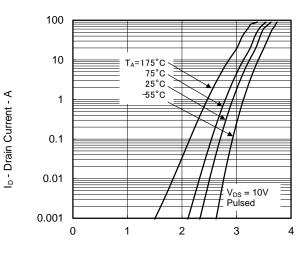


T_{ch} - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

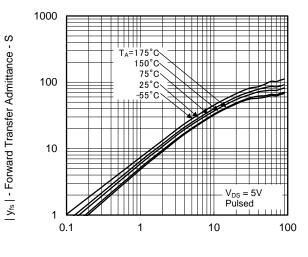


FORWARD TRANSFER CHARACTERISTICS

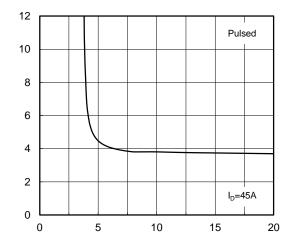


V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



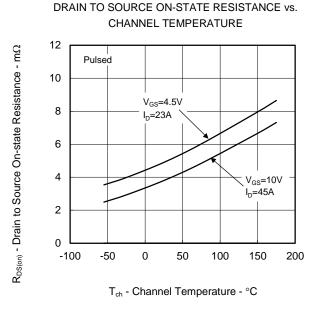
I_D - Drain Current - A



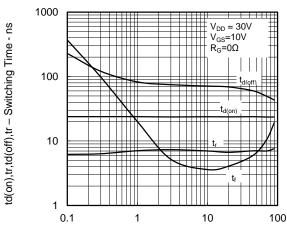
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

 V_{GS} - Gate to Source Voltage - V

 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

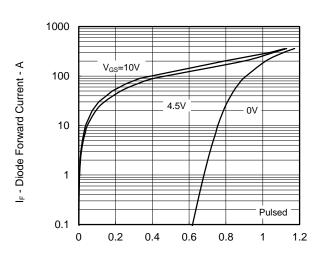


SWITCHING CHARACTERISTICS



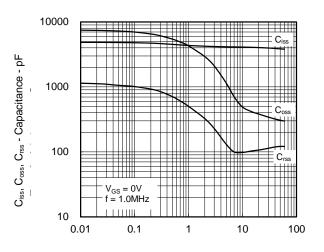
I_D - Drain Current - A

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



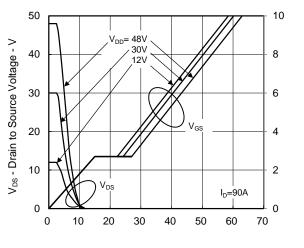
 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

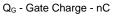
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



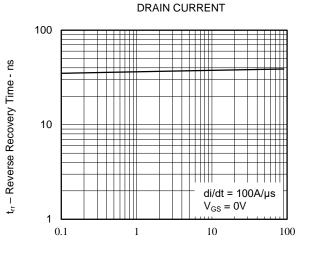
V_{DS} - Drain to Source Voltage - V







REVERSE RECOVERY TIME vs.



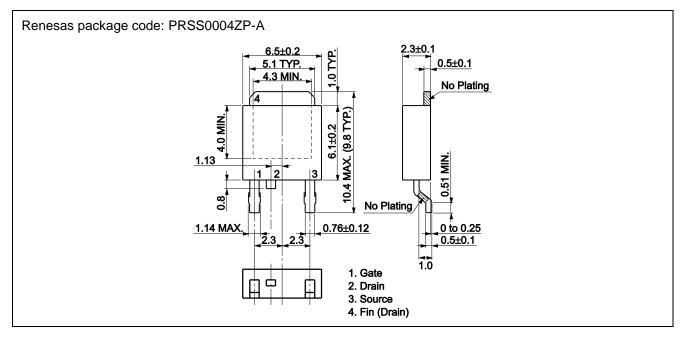
IF - Drain Current - A

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Package Drawings (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.3 g TYP.)





Revision History

NP90N06VDK Data Sheet

		Description				
Rev.	Date	Page	Summary			
1.00	Oct. 26, 2015	—	First Edition Issued			
2.00	May 24 ,2018	2	Note 3 was added			
		3	Note 2 was added			

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