

**50A, 60V, 0.022 Ohm, ESD Rated, Logic Level N-Channel Power MOSFETs**

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49164.

**Ordering Information**

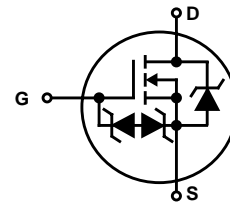
PART NUMBER	PACKAGE	BRAND
RFG50N06LE	TO-247	FG50N06L
RFP50N06LE	TO-220AB	FP50N06L
RF1S50N06LESM	TO-263AB	F50N06LE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. RF1S45N06SM9A.

**Features**

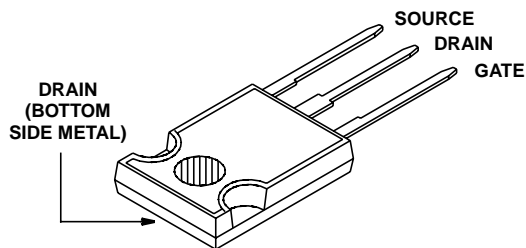
- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- 2kV ESD Protected
- Temperature Compensating PSPICE™ Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**

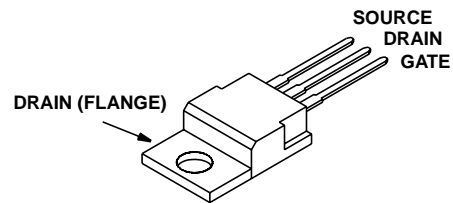


**Packaging**

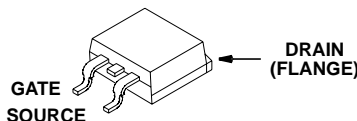
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



# RFG50N06LE, RFP50N06LE, RF1S50N06LESM

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFG50N06LE, RFP50N06LE, RF1S50N06LESM	UNITS
Drain to Source Voltage (Note 1) . . . . .	60	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	60	V
Gate to Source Voltage . . . . .	$\pm 10$	V
Continuous Drain Current . . . . .	50	A
Pulsed Drain Current (Note 3) . . . . .	Refer to Peak Current Curve	
Pulsed Avalanche Rating . . . . .	Refer to UIS Curve	
Power Dissipation . . . . .	142	W
Derate Above $25^\circ\text{C}$ . . . . .	0.95	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	-55 to 175	$^\circ\text{C}$
Electrostatic Discharge Rating MIL-STD-883, Category B(2) . . . . .	2	kV
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	260	$^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ , Figure 13	60	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ , Figure 12	1	-	2	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
			$T_C = 150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10\text{V}$	-	-	10	$\mu\text{A}$	
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 50\text{A}$ , $V_{GS} = 5\text{V}$ , Figure 11	-	-	0.022	$\Omega$	
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}$ , $I_D = 50\text{A}$ , $R_L = 0.6\Omega$ , $V_{GS} = 5\text{V}$ , $R_{GS} = 2.5\Omega$ Figures 10, 18, 19	-	-	230	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	20	-	ns	
Rise Time	$t_r$		-	170	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	48	-	ns	
Fall Time	$t_f$		-	90	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	165	ns	
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$	$V_{DD} = 48\text{V}$ , $I_D = 50\text{A}$ , $R_L = 0.96\Omega$ Figures 21, 21	-	96	120	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V}$ to $5\text{V}$		-	57	70	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $1\text{V}$		-	2.2	2.7	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ Figure 14	-	2100	-	pF	
Output Capacitance	$C_{OSS}$		-	600	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	230	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.05	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C/W}$	
		TO-220 and TO-263	-	-	80	$^\circ\text{C/W}$	

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 45\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 45\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

**NOTES:**

2. Pulse test: pulse width  $\leq 80\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. Gate to source diodes are designed for ESD Protection. Operation in continuous breakdown mode is not recommended.

Typical Performance Curves Unless Otherwise Specified

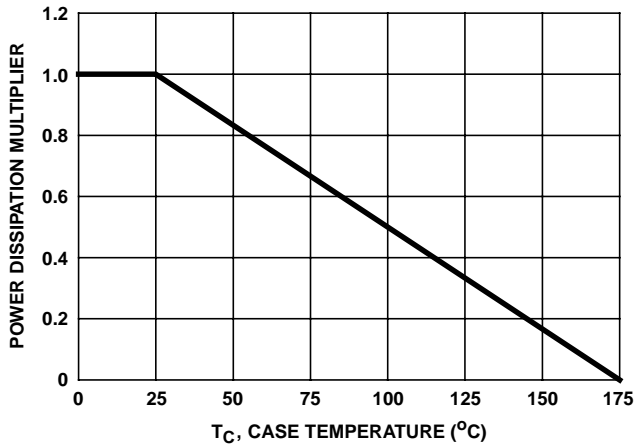


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

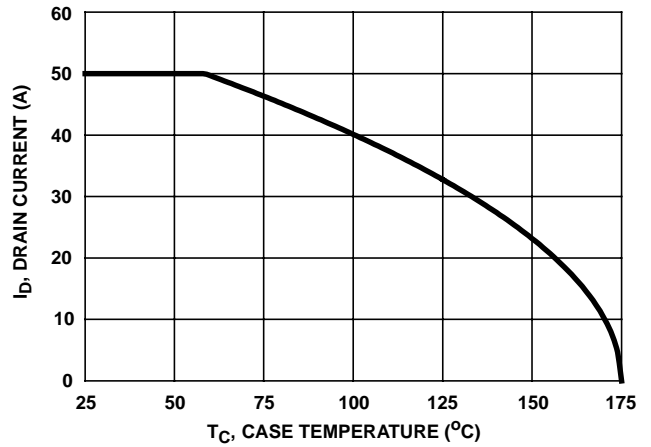


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

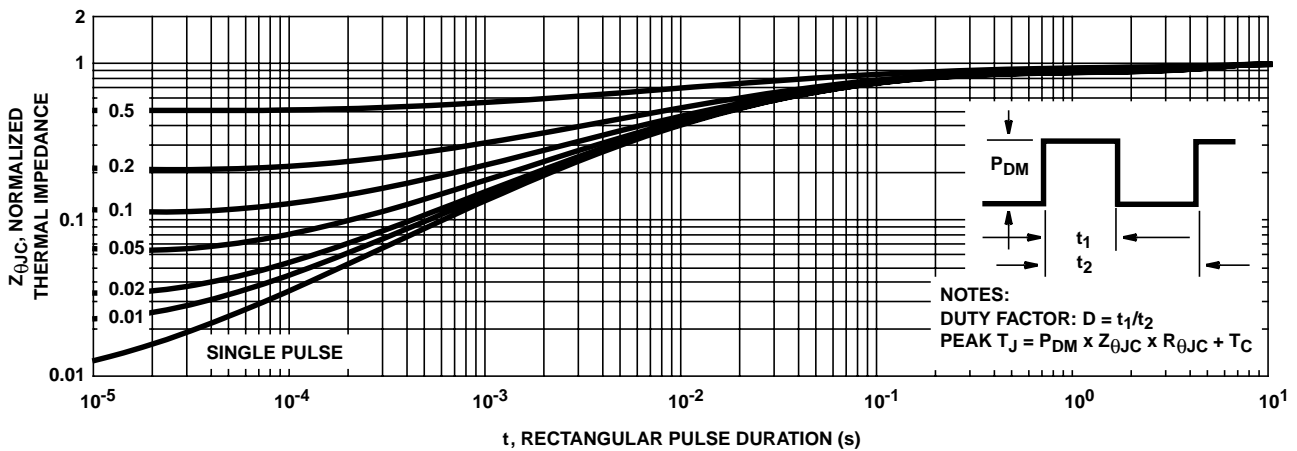


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

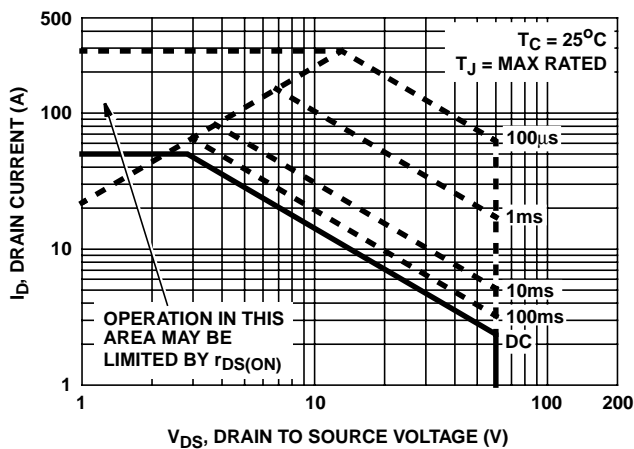


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

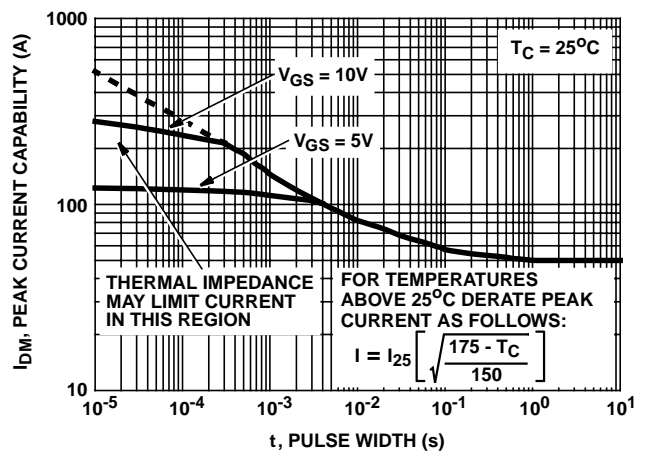
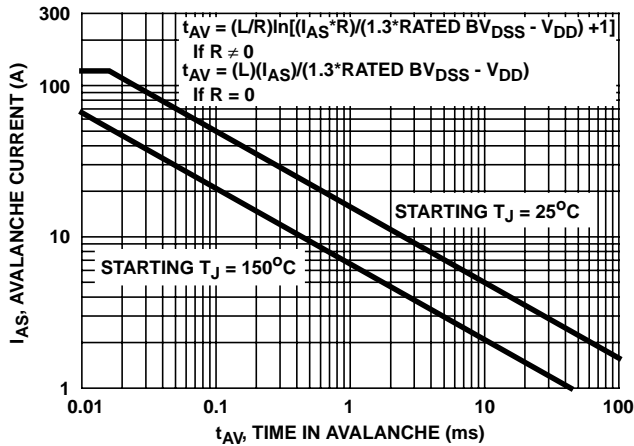


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

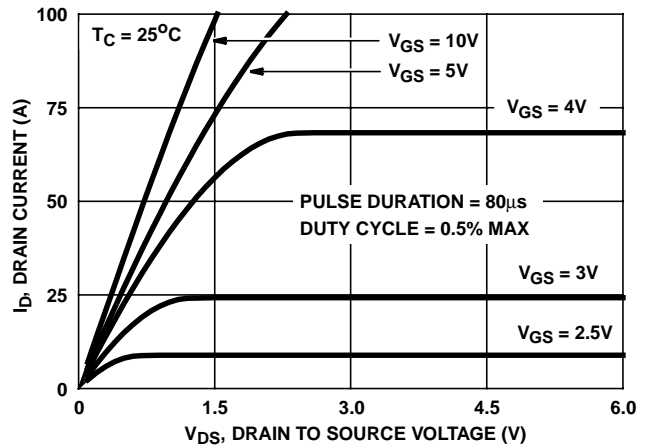


FIGURE 7. SATURATION CHARACTERISTICS

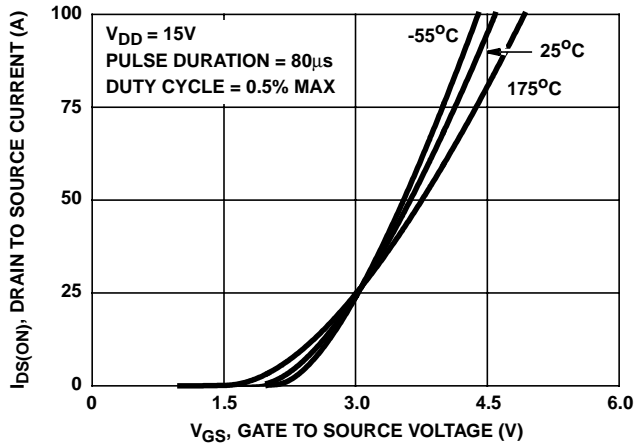


FIGURE 8. TRANSFER CHARACTERISTICS

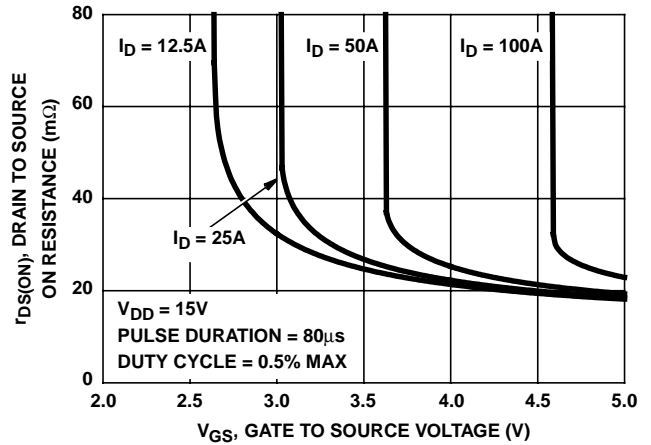


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

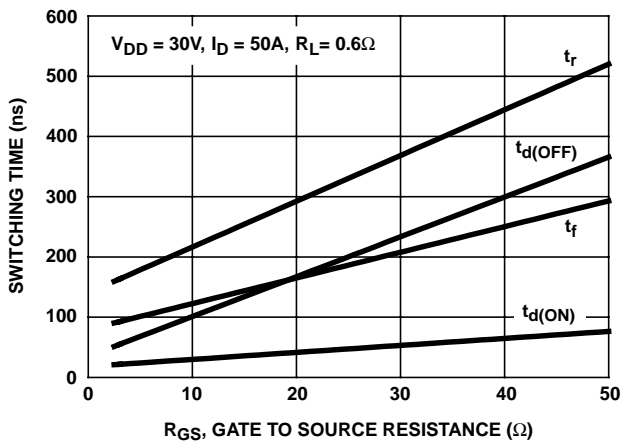


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

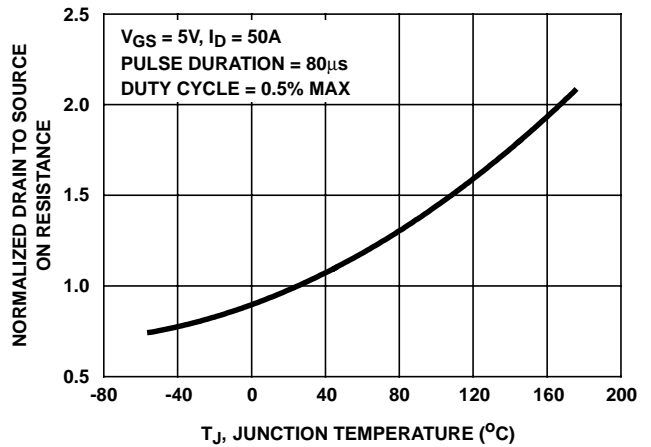


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

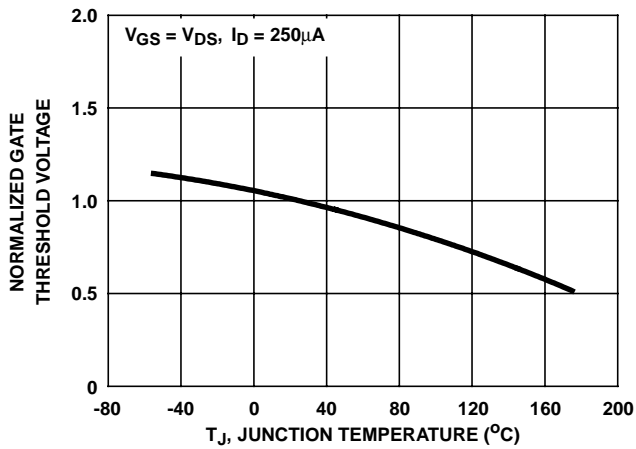


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

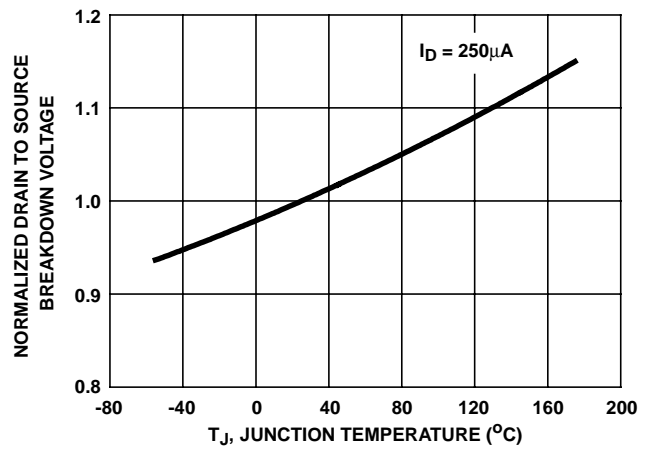


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

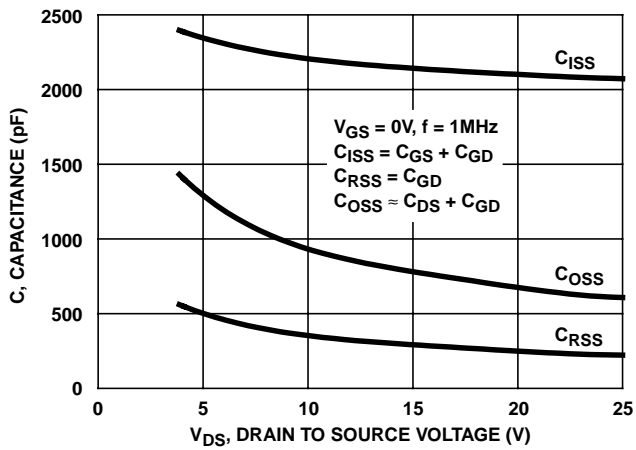
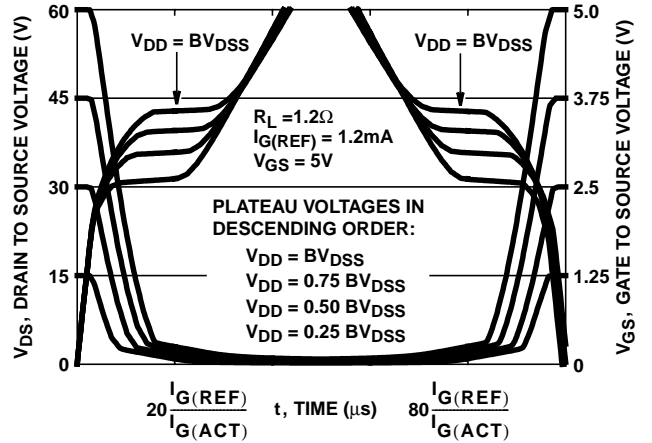


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

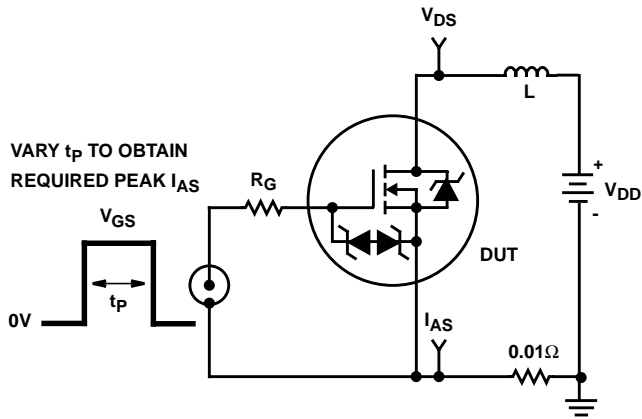


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

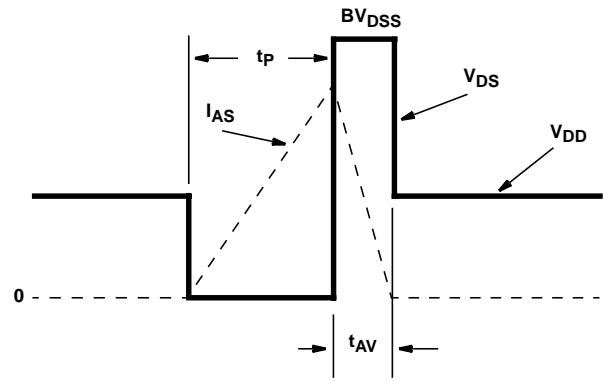


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

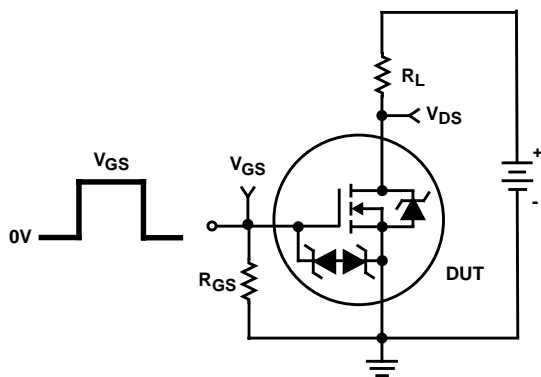


FIGURE 18. SWITCHING TIME TEST CIRCUIT

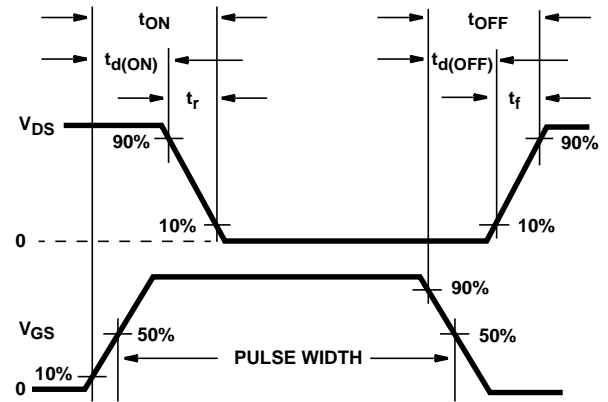


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

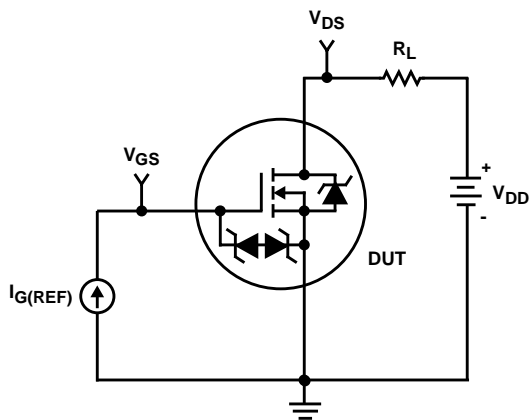


FIGURE 20. GATE CHARGE TEST CIRCUIT

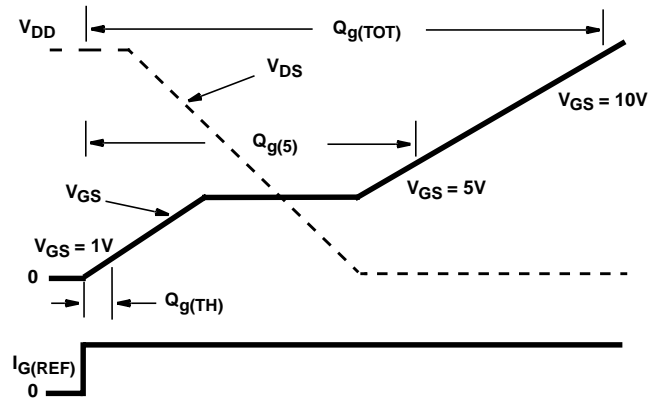


FIGURE 21. GATE CHARGE WAVEFORMS

**PSPICE Electrical Model**

SUBCKT 50N06LE 2 1 3 ; rev 8/11/95  
 CA 12 8 7.0e-9  
 CB 15 14 7.0e-9  
 CIN 6 8 1.85e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DESD1 91 9 DESD1MOD  
 DESD2 91 7 DESD2MOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.3

EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 7.29e-9  
 LSOURCE 3 7 6.16e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 3.95e-3  
 RGATE 9 20 1.18

RLDRAIN 2 5 10  
 RLGATE 1 9 72.9  
 RLSOURCE 3 7 61.6  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 8.0e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*185),4.2))}

.MODEL DBODYMOD D (IS = 1.98e-12 RS = 4.90e-3 TRS1 = 2.75e-3 TRS2 = -4.08e-6 CJO = 1.90e-9 TT = 7.15e-8 M = 0.49)

.MODEL DBREAKMOD D (RS = 1.26e-1 TRS1 = 2.75e-3 TRS2 = -1.17e-5)

.MODEL DESD1MOD D (BV = 12.75 TBV1 = 0 TBV2 = 0 RS = 0 TRS1 = 0 TRS2 = 0)

.MODEL DESD2MOD D (BV = 12.75 TBV1 = 0 TBV2 = 0 RS = 54 TRS1 = 0 TRS2 = 0)

.MODEL DPLCAPMOD D (CJO = 1.36e-9 IS = 1e-30 N = 10 M = 0.56)

.MODEL MMEDMOD NMOS (VTO = 1.56 KP = 3.50 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.18)

.MODEL MSTROMOD NMOS (VTO = 1.88 KP = 50.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)

.MODEL MWEAKMOD NMOS (VTO = 1.34 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 11.8 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 9.02e-4 TC2 = 9.18e-7)

.MODEL RDRAINMOD RES (TC1 = 1.41e-2 TC2 = 7.94e-5)

.MODEL RSLCMOD RES (TC1 = 3.0e-3 TC2 = 2.0e-6)

.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)

.MODEL RVTHRESMOD RES (TC1 = -9.50e-4 TC2 = -9.53e-6)

.MODEL RVTEMPMOD RES (TC1 = -1.54e-3 TC2 = 1.21e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.95 VOFF = -1.95)

.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.95 VOFF = -4.95)

.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.43 VOFF = 1.57)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.57 VOFF = -1.43)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records; authors William J. Hepp and C. Frank Wheatley, 1991.

