HARRIS

IRFP244, IRFP245 IRFP246, IRFP247

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 15A and 14A, 275V - 250V
- $r_{DS(on)}$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275V, 250V DC Rated - 120V AC Line System Operation

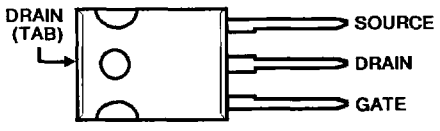
Description

The IRFP244, IRFP245, IRFP246, and IRFP247 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

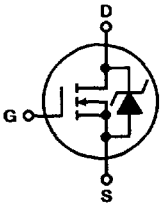
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

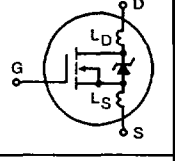
	IRFP244	IRFP245	IRFP246	IRFP247	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	15	14	15	14	A
T_C = +100°C ..... I_D	9.7	8.8	9.7	8.8	A
Pulsed Drain Current (3) ..... I_{DM}	60	56	60	56	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	550	550	550	550	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

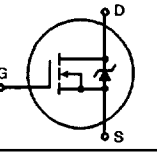
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, I_{PEAK} = 15A. See Figures 14 and 15.

File Number 2211.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP244, IRFP245	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	250	-	-	V
IRFP246, IRFP247			275	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFP244, IRFP246	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	15	-	-	A
IRFP245, IRFP247			14	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP244, IRFP246	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	-	0.20	0.28	Ω
IRFP245, IRFP247			-	0.24	0.34	V
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 10A	6.7	11	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1300	-	pF
Output Capacitance	C_{OSS}		-	320	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	69	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 15A, R_G = 9.1Ω, See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	16	24	ns
Rise Time	t_r		-	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	53	80	ns
Fall Time	t_f		-	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 15A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	39	59	nC
Gate-Source Charge	Q_{gs}		-	6.6	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	20	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	15	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	60	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 15A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	1.6	3.4	7.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, I_{PEAK} = 15A. (See Figures 14 & 15)

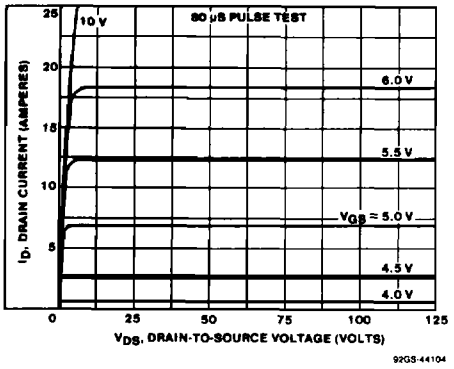


Fig. 1 - Typical output characteristics.

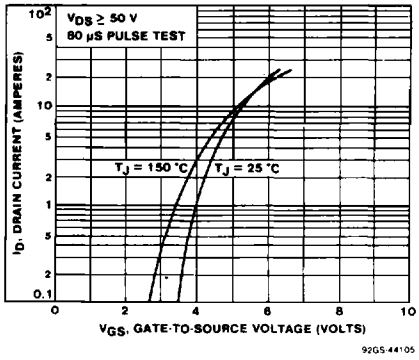


Fig. 2 - Typical transfer characteristics.

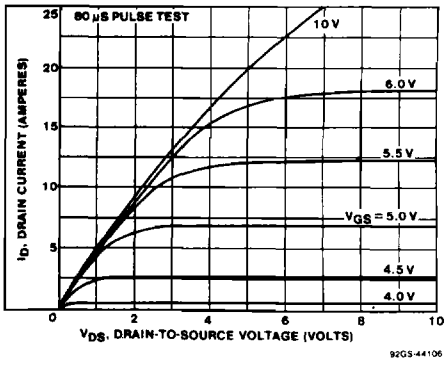


Fig. 3 - Typical saturation characteristics.

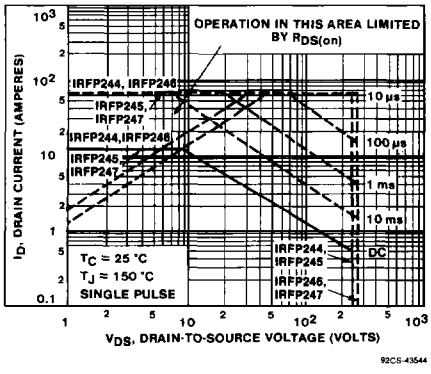


Fig. 4 - Maximum safe operating area.

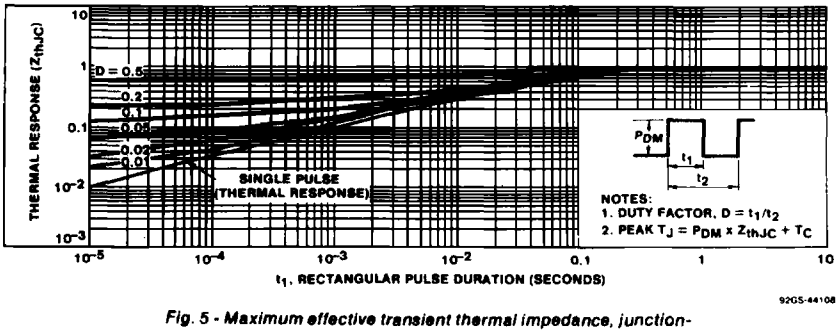


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

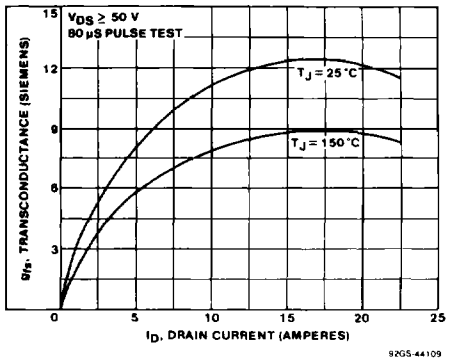


Fig. 6 - Typical transconductance vs. drain current.

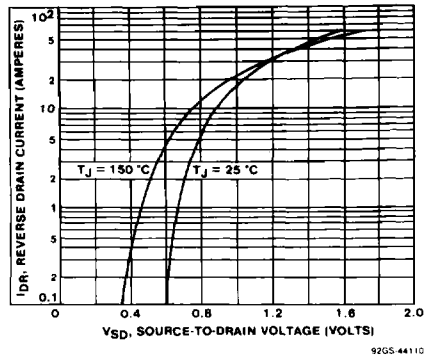


Fig. 7 - Typical source-drain diode forward voltage.

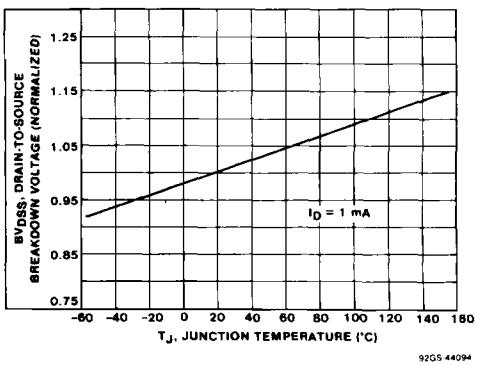


Fig. 8 - Breakdown voltage vs. temperature.

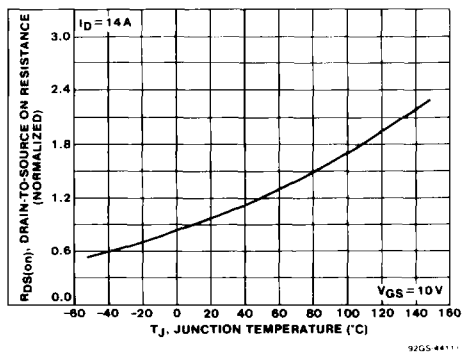


Fig. 9 - Normalized on-resistance vs. temperature.

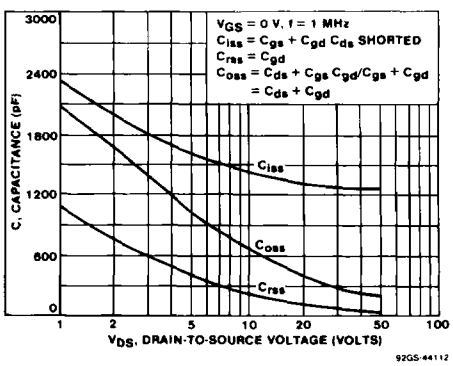


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

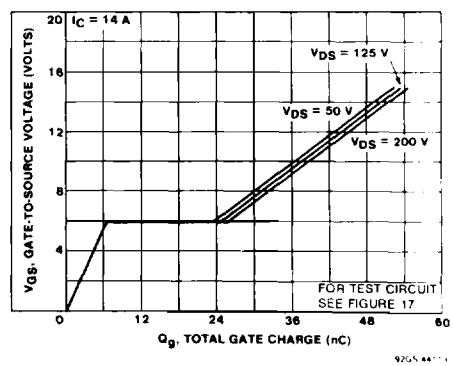


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

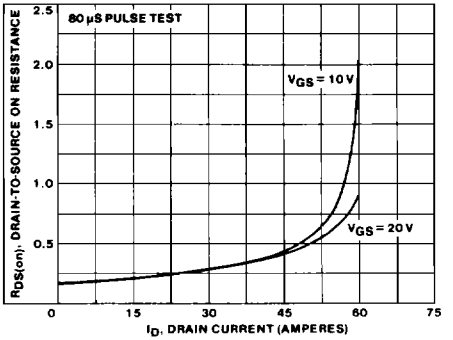


Fig. 12 - Typical on-resistance vs. drain current.

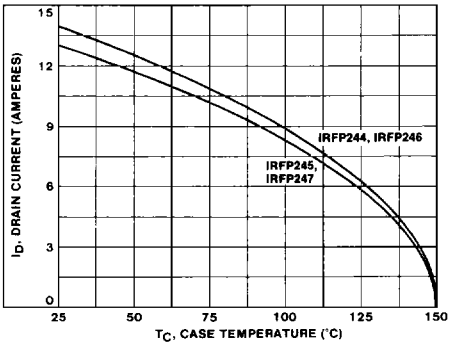


Fig. 13 - Maximum drain current vs case temperature.

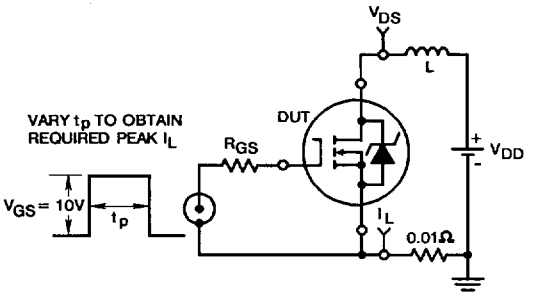


Fig. 14 - Unclamped energy test circuit.

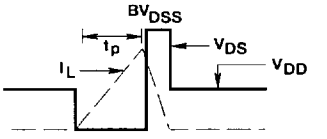


Fig. 15 - Unclamped energy waveforms.

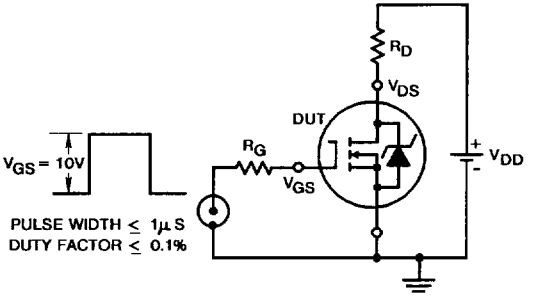


Fig. 16 - Switching time test circuit.

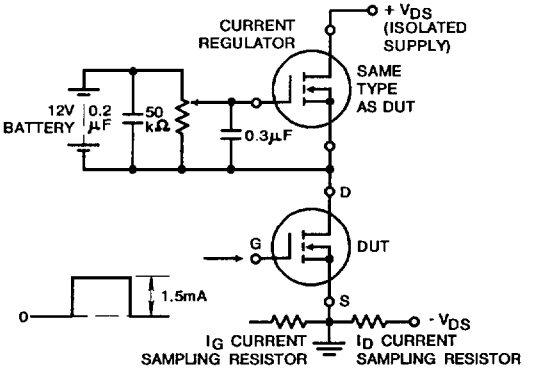


Fig. 17 - Gate charge test circuit.