HARRIS

IRFP140R, IRFP141R IRFP142R, IRFP143R

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 27A and 31A, 80V - 100V
- $r_{DS(on)}$ = 0.077Ω and 0.099Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

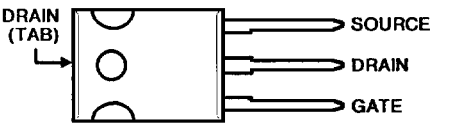
Description

The IRFP140R, IRFP141R, IRFP142R, and IRFP143R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

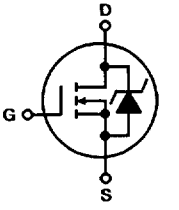
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP140R	IRFP141R	IRFP142R	IRFP143R	UNITS
Drain-Source Voltage (1)	V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	100	80	100	80	V
Continuous Drain Current						
T_C = +25°C	I_D	31	31	27	27	A
T_C = +100°C	I_D	22	22	19	19	A
Pulsed Drain Current (3)	I_{DM}	120	120	110	110	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	180	180	180	180	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	100	100	100	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

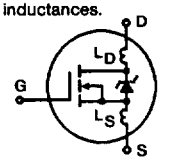
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 160μH, R_{GS} = 50Ω, I_{PEAK} = 31A. See Figures 14 and 15.

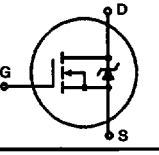
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2086.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP140R, IRFP142R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRFP141R, IRFP143R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFP140R, IRFP141R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	31	-	-	A
IRFP142R, IRFP143R			27	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP140R, IRFP141R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 19A	-	0.055	0.077	Ω
IRFP142R, IRFP143R			-	0.077	0.099	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 19A	9.3	14	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1275	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \approx$ 28A, R_G = 9.1Ω, RD = 1.8Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	23	ns
Rise Time	t_r		-	72	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	60	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	59	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	21	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	31	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	120	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 31A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/µs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/µs	0.44	0.91	1.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 160µH, R_{GS} = 50Ω, I_{PEAK} = 31A. (See Figures 14 & 15)

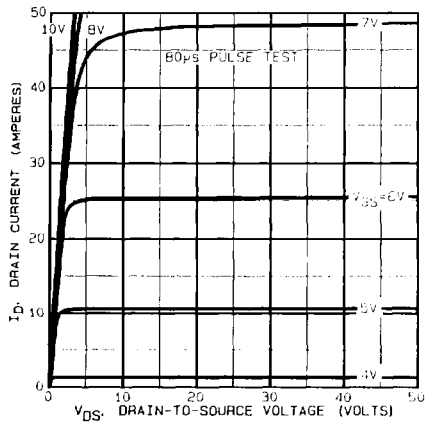


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

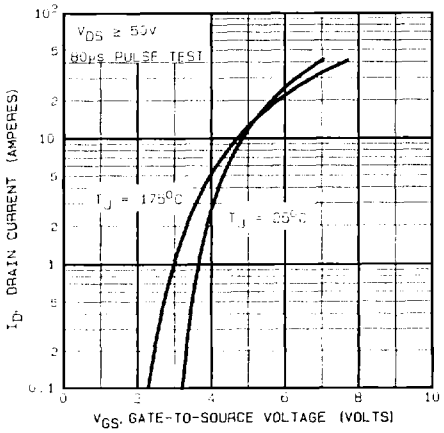


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

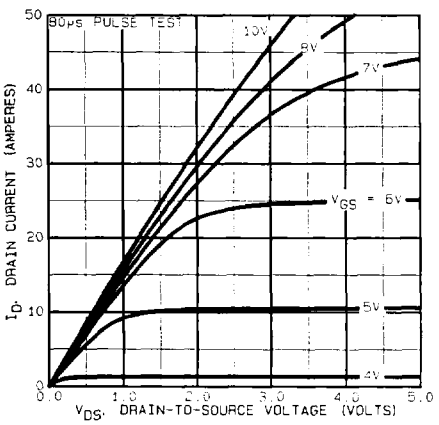


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

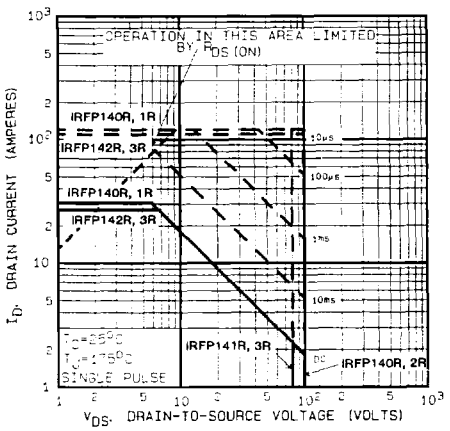


FIGURE 4. MAXIMUM SAFE OPERATING AREA

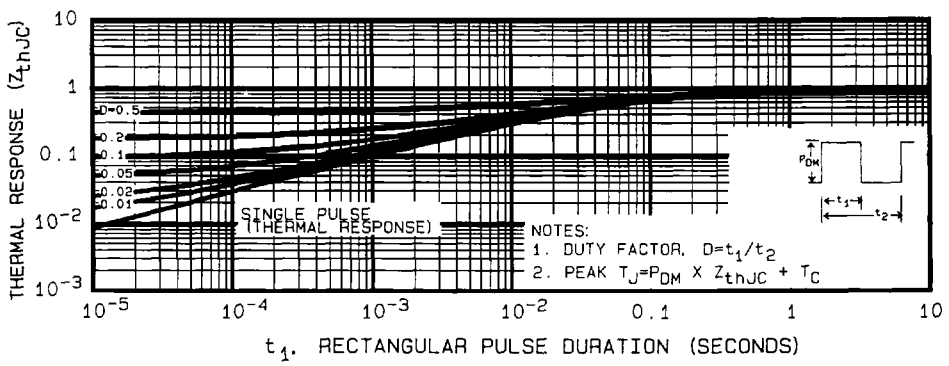


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

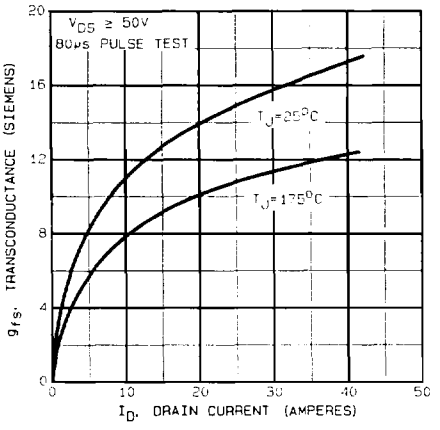


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

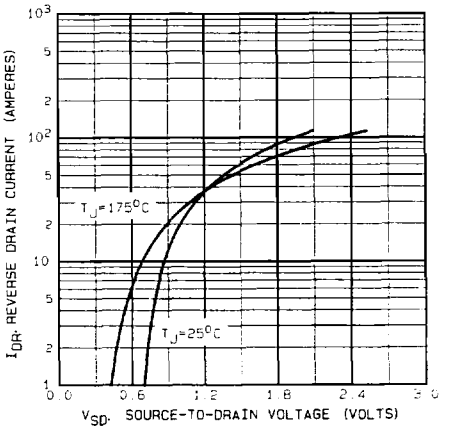


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

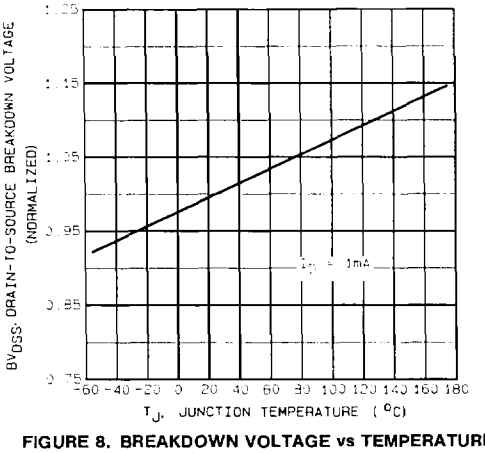


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

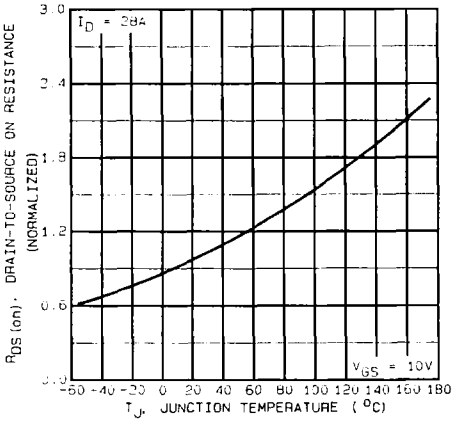


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

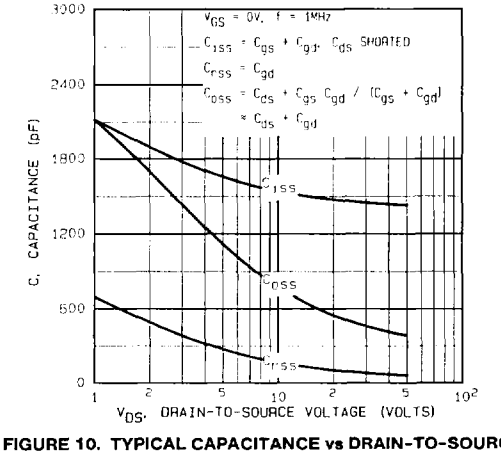


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

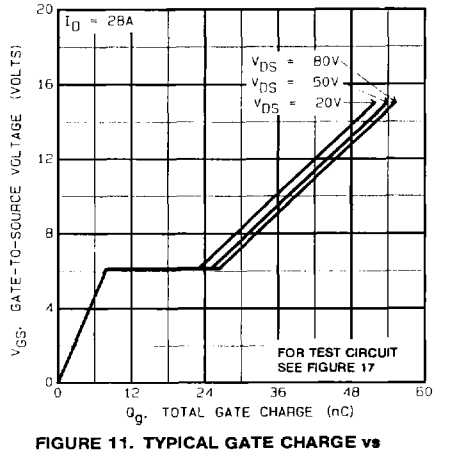


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

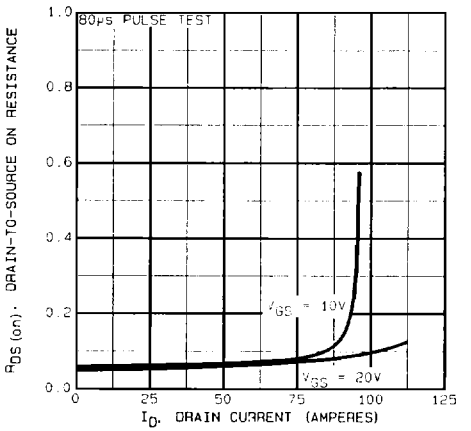


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

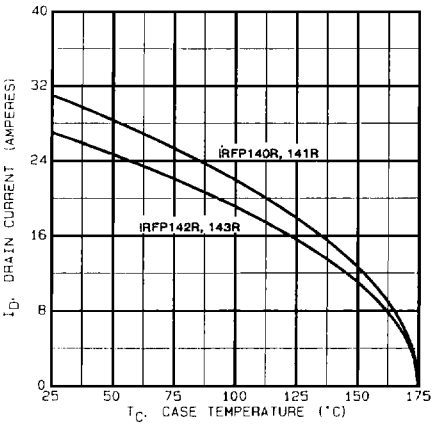


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

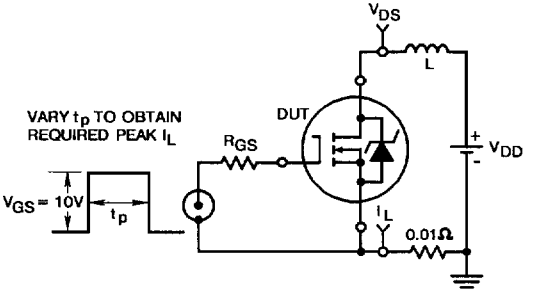


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

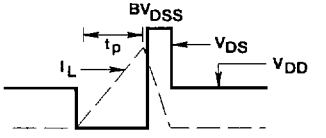


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

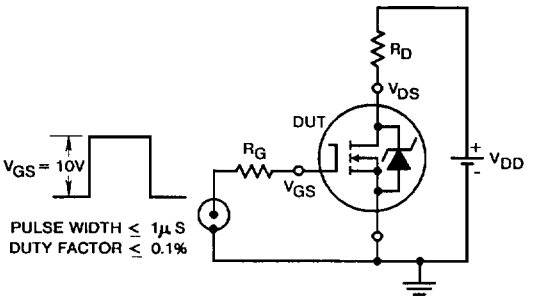


FIGURE 16. SWITCHING TIME TEST CIRCUIT

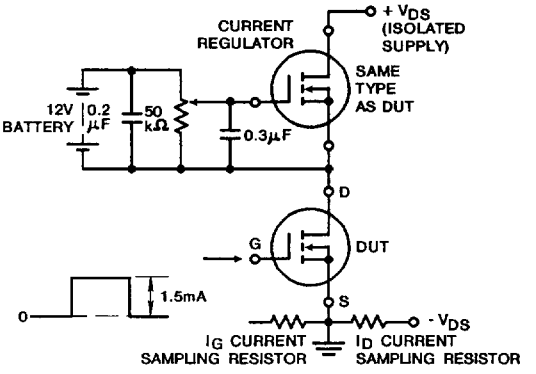


FIGURE 17. GATE CHARGE TEST CIRCUIT