

August 1991

Features

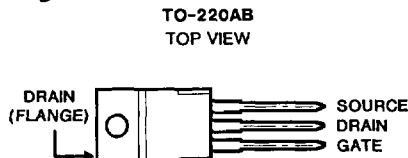
- 4.0A and 5.0A, 150V - 200V
- $r_{DS(on)} = 0.8\Omega$ and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA Is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRF620, IRF621, IRF622, and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF620R, IRF621R, IRF622R and IRF623R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

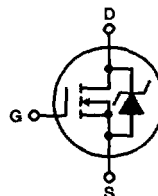
The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRF620 IRF620R	IRF621 IRF621R	IRF622 IRF622R	IRF623 IRF623R	UNITS
Drain-Source Voltage (1)	V_{DS} 200	150	200	150	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 200	150	200	150	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 5.0	5.0	4.0	4.0	A
$T_C = +100^\circ\text{C}$	I_D 3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3)	I_{DM} 20	20	16	16	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$	P_D 40	40	40	40	W
Linear Derating Factor	0.32	0.32	0.32	0.32	W/°C
Inductive Current, Clamped	I_{LM} 20	20	16	16	A
(See Figure 14, $L = 100\mu\text{H}$)					
Single Pulse Avalanche Energy Rating (4)	E_{AS}^* 85	85	85	85	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	°C
(0.063" (1.6mm) from case for 10s)					

NOTES:

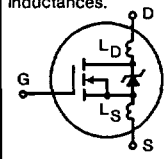
- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
 - Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
 - Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
 - $V_{DD} = 10\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 6.18\text{mH}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 5\text{A}$. See Figure 15.
- *R Suffix Types Only

IRF620, IRF621, IRF622, IRF623 IRF620R, IRF621R, IRF622R, IRF623R

Electrical Characteristics $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF620/622, IRF620R/622R IRF621/623, IRF621R/623R	BV _{DSS}	V _{GS} = 0V, I _D = 250 μ A	200	-	-	V
			150	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250 μ A	2.0	-	4.0	V
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _J = +125 $^\circ$ C	-	-	250	μ A
			-	-	1000	μ A
On-State Drain Current (Note 2) IRF620/621, IRF620R/621R IRF622/623, IRF622R/623R	I _{D(ON)}	V _{DS} > I _{D(ON)} x R _{DS(ON)} Max, V _{GS} = 10V	5.0	-	-	A
			4.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF620/621, IRF620R/621R IRF622/623, IRF622R/623R	r _{DS(ON)}	V _{GS} = 10V, I _D = 2.5A	-	0.5	0.8	Ω
			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} > I _{D(ON)} x R _{DS(ON)} Max, I _D = 2.5A	1.3	2.5	-	S(Ω)
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	-	450	-	pF
Output Capacitance	C _{OSS}	See Figure 10	-	150	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	40	-	pF
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 2.5BV _{DSS} , I _D = 5.0A, R _G = 9.1 Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t _r		-	30	60	ns
Turn-Off Delay Time	t _{d(OFF)}		-	50	100	ns
Fall Time	t _f		-	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	V _{GS} = 10V, I _D = 5.0A, V _{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	11	15	nC
Gate-Source Charge	Q _{gs}		-	5.0	-	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	6.0	-	nC
Internal Drain Inductance	L _D	Measured from the contact screw on tab to center of die	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from pack- age to center of die	-	4.5	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	R _{θJC}		-	-	3.12	$^\circ\text{C/W}$
Case-to-Sink	R _{θCS}	Mounting surface flat, smooth and greased	-	0.5	-	$^\circ\text{C/W}$
Junction-to-Ambient	R _{θJA}	Free air operation	-	-	80	$^\circ\text{C/W}$

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N-CHANNEL
POWER MOSFETS



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	5.0	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	20	A
Diode Forward Voltage (Note 2)	V _{SD}	T _J = +25 $^\circ$ C, I _S = 5.0A, V _{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t _{rr}	T _J = +150 $^\circ$ C, I _F = 5.0A, dI _F /dt = 100A/ μ s	-	350	-	ns
Reverse Recovered Charge	Q _{RR}	T _J = +150 $^\circ$ C, I _F = 5.0A, dI _F /dt = 100A/ μ s	-	2.3	-	μ C
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES: 1. T_J = +25 $^\circ$ C to +150 $^\circ$ C
 2. Pulse Test: Pulse width \leq 300 μ s,
 Duty Cycle \leq 2%
 3. Repetitive Rating: Pulse width limited by max.
 junction temperature. See Transient Thermal
 Impedance Curve (Figure 5)
 4. V_{DD} = 10V, Start T_J = +25 $^\circ$ C, L = 6.18mH,
 R_{GS} = 50 Ω , I_{PEAK} = 5A (See Figure 15)

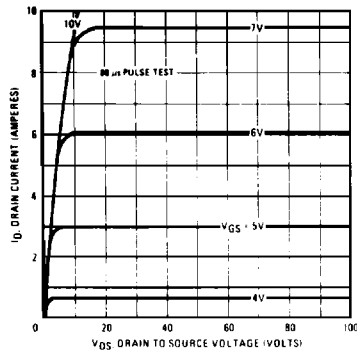


Fig. 1 - Typical Output Characteristics

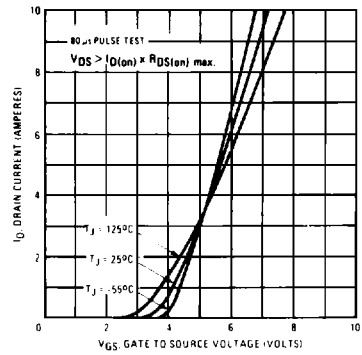


Fig. 2 - Typical Transfer Characteristics

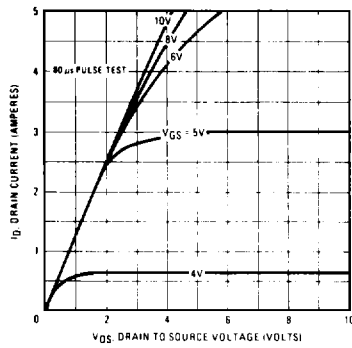


Fig. 3 - Typical Saturation Characteristics

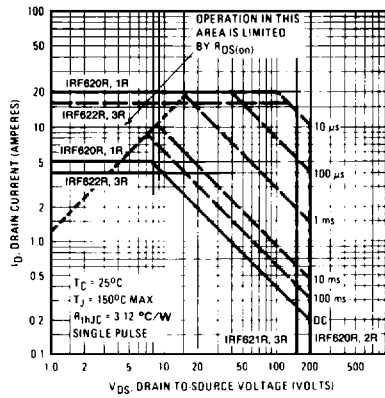


Fig. 4 - Maximum Safe Operating Area

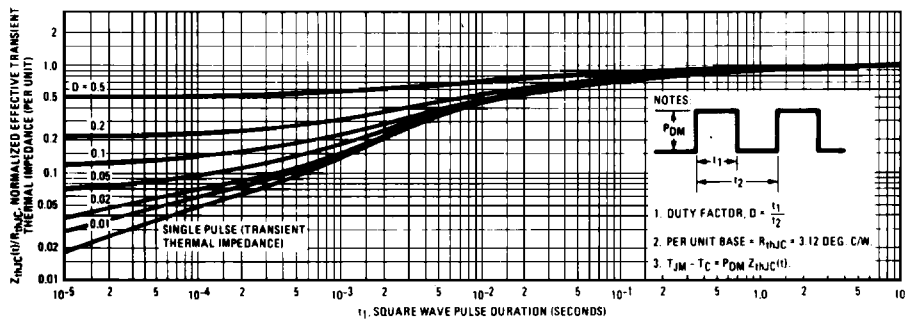


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

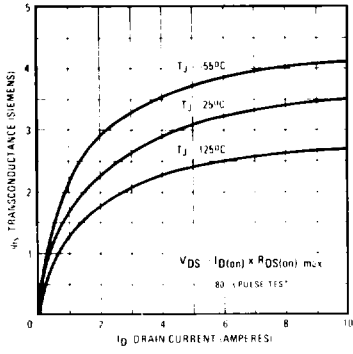


Fig. 6 – Typical Transconductance Vs. Drain Current

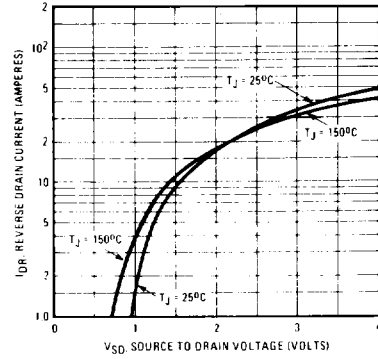


Fig. 7 – Typical Source-Drain Diode Forward Voltage

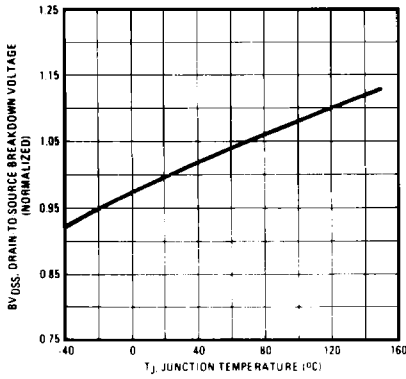


Fig. 8 – Breakdown Voltage Vs. Temperature

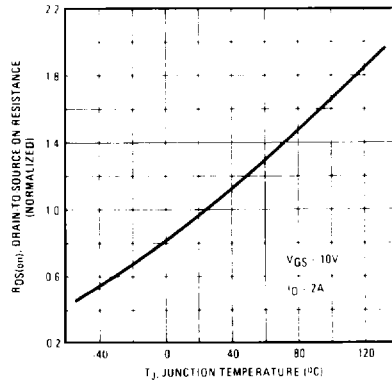


Fig. 9 – Normalized On-Resistance Vs. Temperature

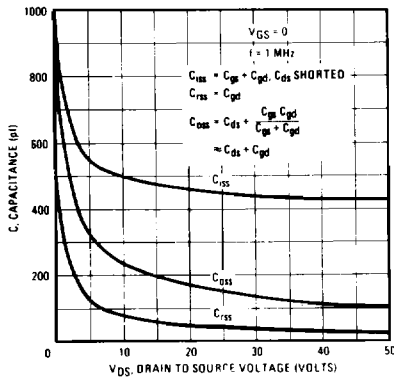


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

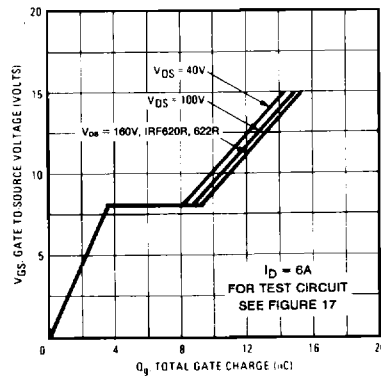


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

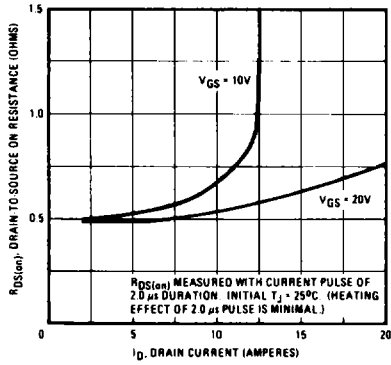


Fig. 12 — Typical On-Resistance Vs. Drain Current

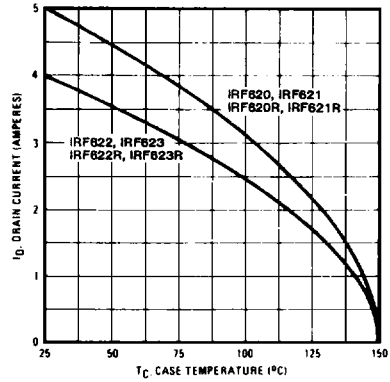


Fig. 13 — Maximum Drain Current Vs. Case Temperature

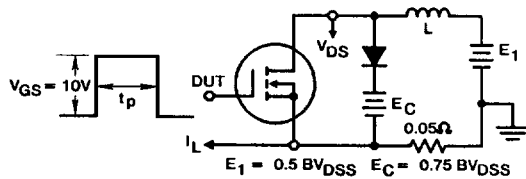


Fig. 14a — Clamped Inductive Test Circuit

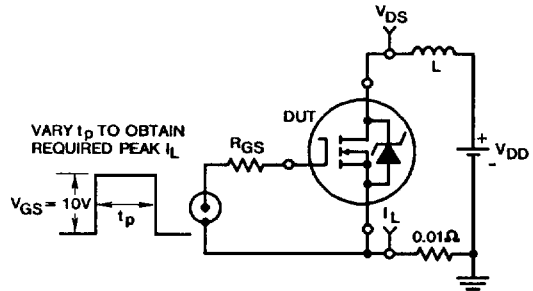


Fig. 15a — Unclamped Energy Test Circuit

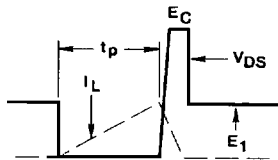


Fig. 14b — Clamped Inductive Waveforms

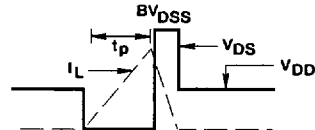


Fig. 15b — Unclamped Energy Waveforms

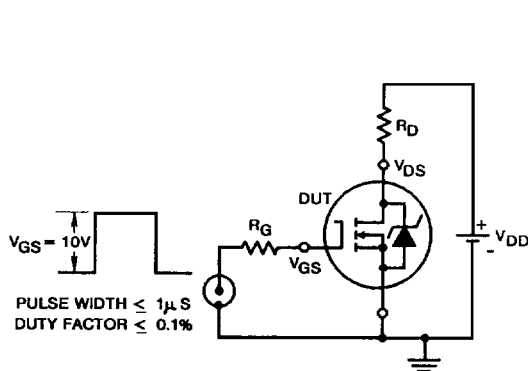


Fig. 16 — Switching Time Test Circuit

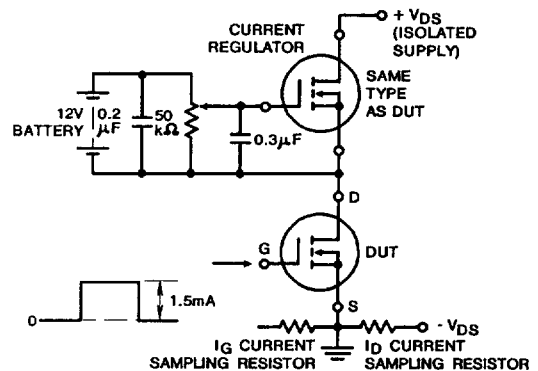


Fig. 17 — Gate Charge Test Circuit