HARRIS

RFD15P05/05SM
RFP15P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

May 1992

Features

- -15A, -50V
- $r_{DS(on)}$ = 0.150 Ω
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

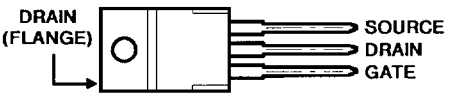
Description

The RFD15P05, RFD15P05SM and RFP15P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

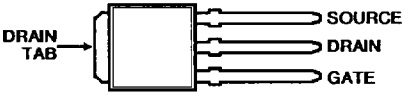
The RFD15P05 is supplied in the JEDEC TO-251AA plastic package and the RFD15P05SM in the TO-252AA plastic package. The RFP15P05 is supplied in the JEDEC TO-220AB plastic package.

Packages

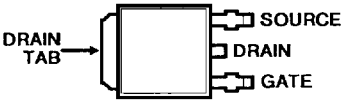
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW

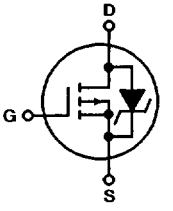


TO-252AA
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-50V
Drain-Gate Voltage, (R_{GS} = 1MΩ), V_{DGR}	-50V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-15A
Pulsed, I_{DM}	-40A
Avalanche Current, I_{AS}	See Figure 2
Power Dissipation, P_D:	
T_C = +25°C	80W
Derate Above T_C = +25°C	0.533W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55°C to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

File Number **2387.1**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V	-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	-	1	µA
		T_C = 150°C		50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V	-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 15A, V_{GS} = -10V	-	0.150	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 7.5A Ig1 = Ig2 = 0.4A V_{GS} (clamp): -10V, +0.6V R_L = 3.3Ω (See Figure 12)	-	60	ns
Turn-On Delay Time	$t_{d(on)}$		-	16 (typ)	ns
Rise Time	t_r		-	30 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$		-	50 (typ)	ns
Fall Time	t_f			20 (typ)	ns
Turn-Off Time	$t_{(off)}$		-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V, V_{DD} = -40V	-	150	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V, I_D = 15A	-	75	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V, R_L = 2.67Ω	-	3.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 15A, V_{DS} = -15V	-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 7.5A, R_L = 3.33Ω L = 0.2µH, Ig1 = Ig2 = 0.4A V_{GS} (clamp): -10V, +0.6V	-	17	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA	-	1.875	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA	-	100	°C/W
		TO-220AB	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 15A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 15A, d_{ISD}/dt = 100A/µs	-	125	ns

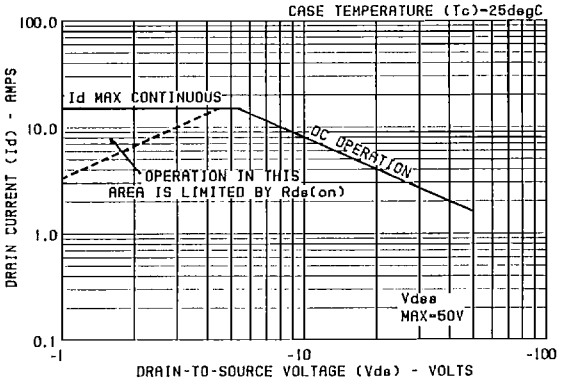


Figure 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

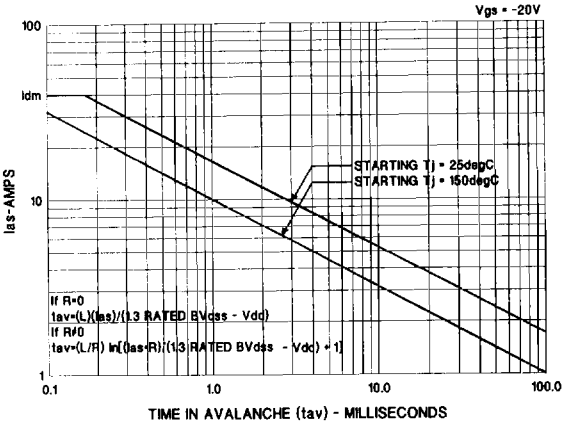


Figure 2 - Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

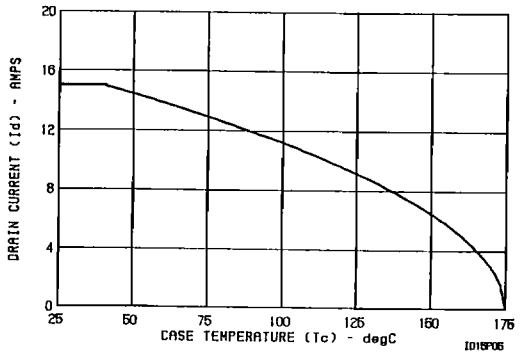


Figure 3 - Maximum continuous drain current vs. temperature.

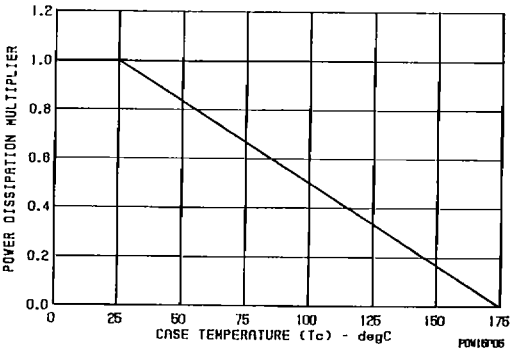


Figure 4 - Normalized power dissipation vs temperature derating curve.

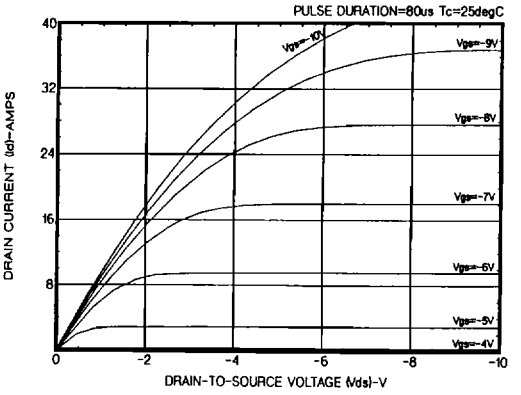


Figure 5 - Typical saturation characteristics.

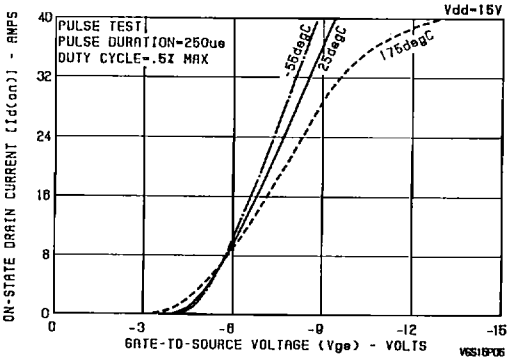


Figure 6 - Typical transfer characteristics.

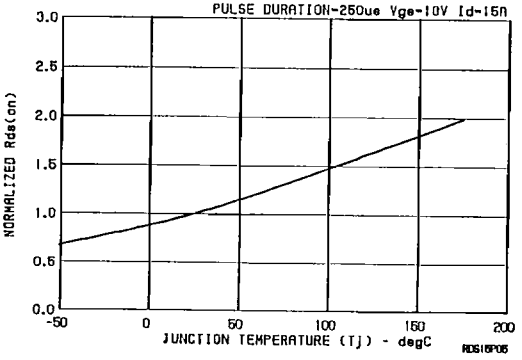


Figure 7 - Normalized rDS(on) vs junction temperature.

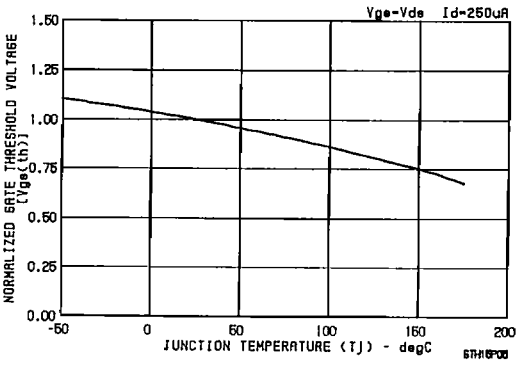


Figure 8 - Normalized gate threshold voltage.

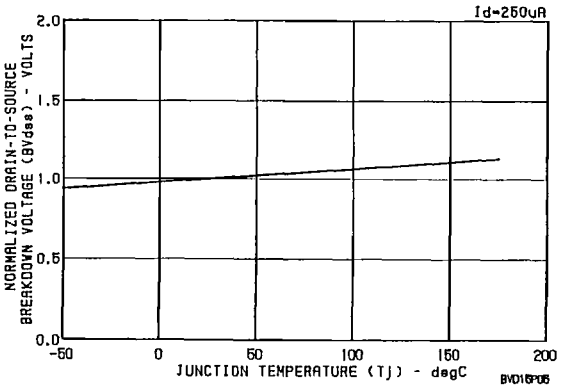


Figure 9 - Normalized drain source breakdown voltage vs temperature.

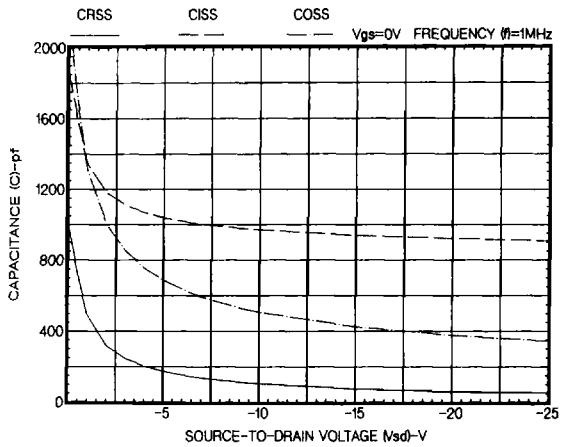


Figure 10 - Typical capacitance vs voltage.

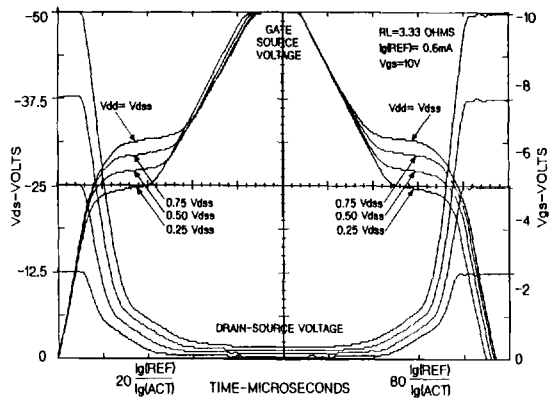


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

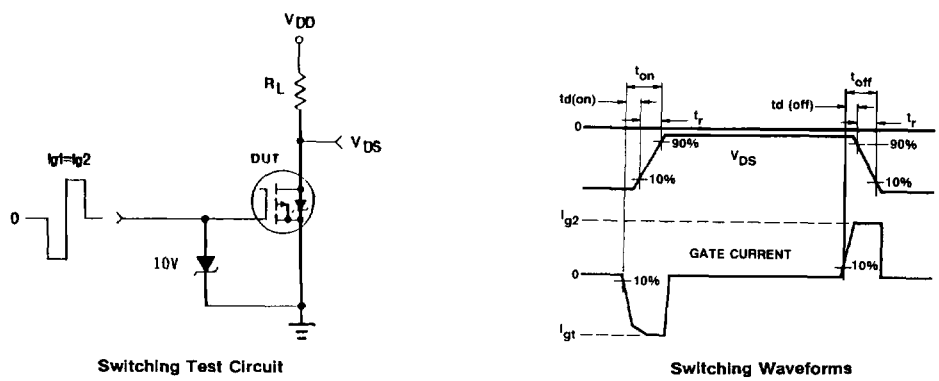


Figure 12 - Resistive switching.

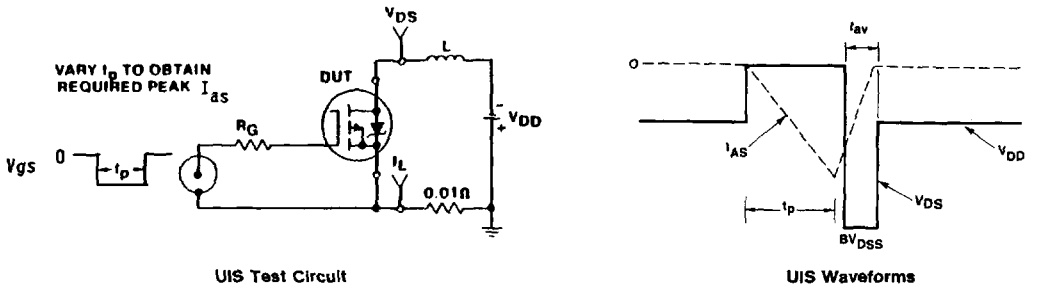


Figure 13 - Unclamped-inductive-switching test.