HARRIS

IRF624, IRF625 IRF626, IRF627

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 3.8A and 3.3A, 250V - 275V
- $r_{DS}(on)$ = 1.1Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 250/275V DC Rating - 120V AC Line System Operation

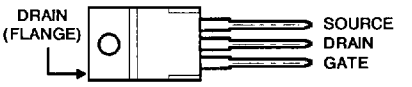
Description

The IRF624, IRF625, IRF626, and IRF627 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

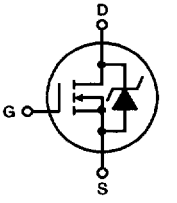
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

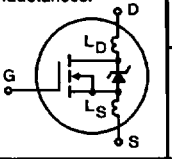
		IRF624	IRF625	IRF626	IRF627	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	3.8	3.3	3.8	3.3	A
T_C = +100°C	I_D	2.4	2.1	2.4	2.1	A
Pulsed Drain Current (3)	I_{DM}	15	13	15	13	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	40	40	40	40	W
Linear Derating Factor		0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{AS}	120	120	120	120	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

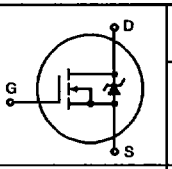
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 13.6mH, R_{GS} = 25Ω, I_{PEAK} = 3.8A. See Figures 14 & 15.

File Number 2167.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF624, IRF626	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	275	-	-	V
IRF625, IRF627			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF624, IRF626	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	3.8	-	-	A
IRF625, IRF627			3.3	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF624, IRF626	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	-	0.8	1.1	Ω
IRF625, IRF627			-	1.05	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} = 2 \times V_{GS}$, I_{DS} = 1.9A	1.4	2.1	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	340	-	pF
Output Capacitance	C_{OSS}		-	110	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	32	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 3.8A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	11	17	ns
Rise Time	t_r		-	24	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	21	32	ns
Fall Time	t_f		-	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	15	22	nC
Gate-Source Charge	Q_{gs}		-	4.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7.2	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	3.8	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	15	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.8A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.8A, dI_F/dt = 100A/µs	81	180	370	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.8A, dI_F/dt = 100A/µs	0.44	0.93	2.0	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

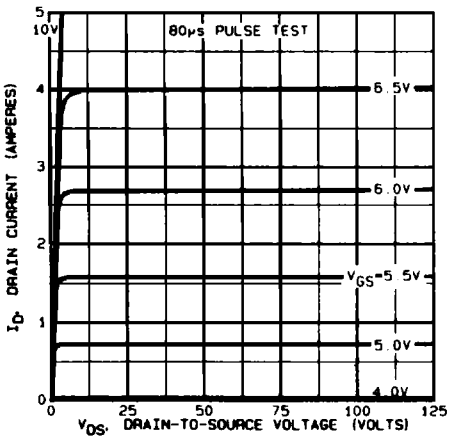


Fig. 1 — Typical Output Characteristics

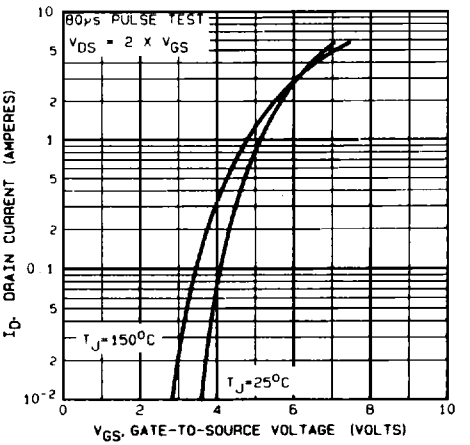


Fig. 2 — Typical Transfer Characteristics

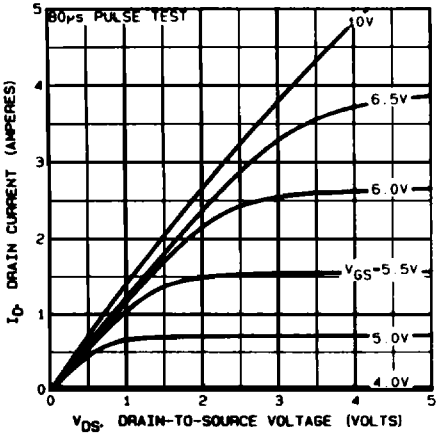


Fig. 3 — Typical Saturation Characteristics

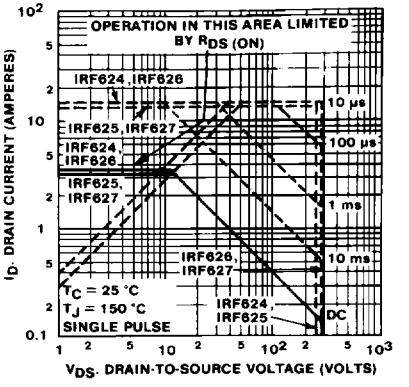


Fig. 4 — Maximum Safe Operating Area

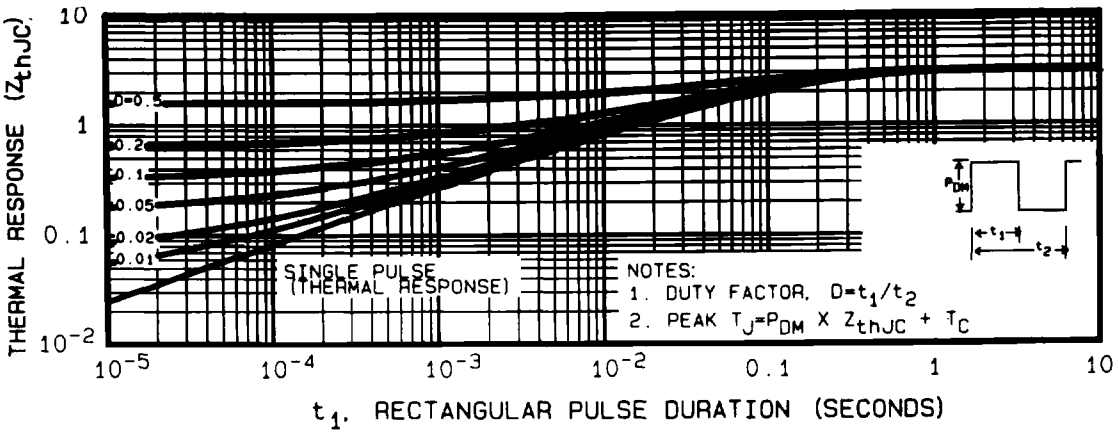


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

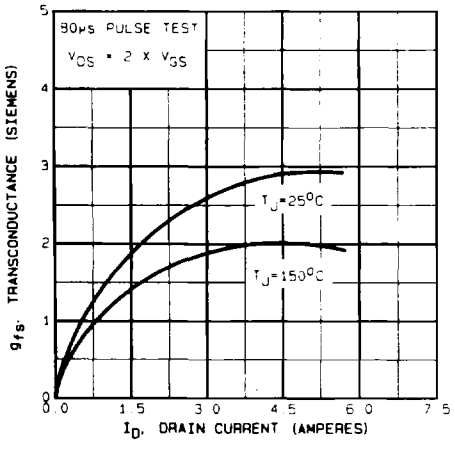


Fig. 6 — Typical Transconductance Vs. Drain Current

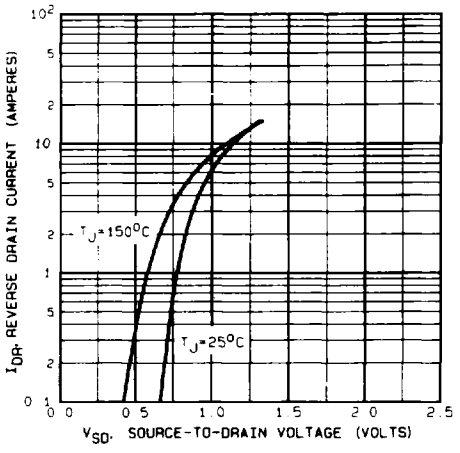


Fig. 7 — Typical Source-Drain Diode Forward Voltage

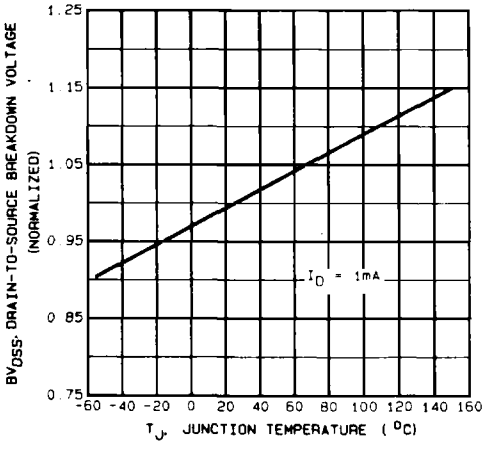


Fig. 8 — Breakdown Voltage Vs. Temperature

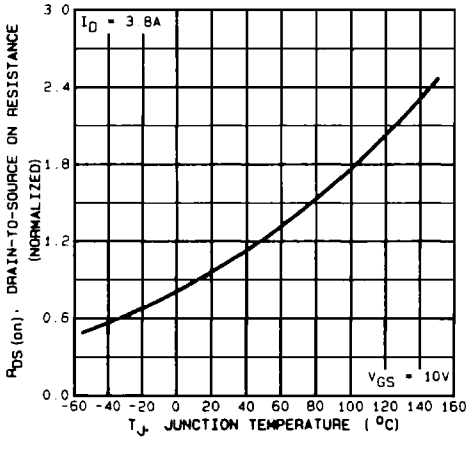


Fig. 9 — Normalized On-Resistance Vs. Temperature

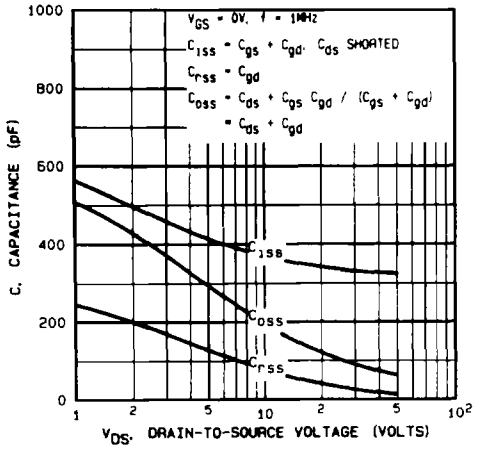


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

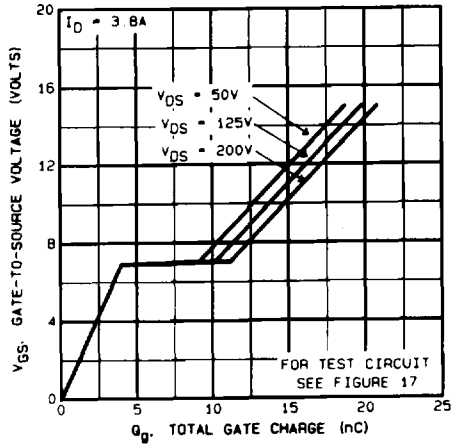


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

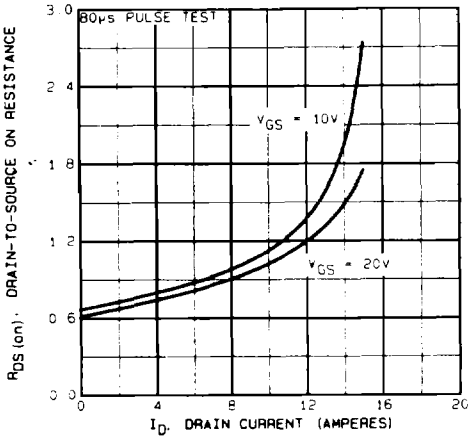


Fig. 12 — Typical On-Resistance Vs. Drain Current

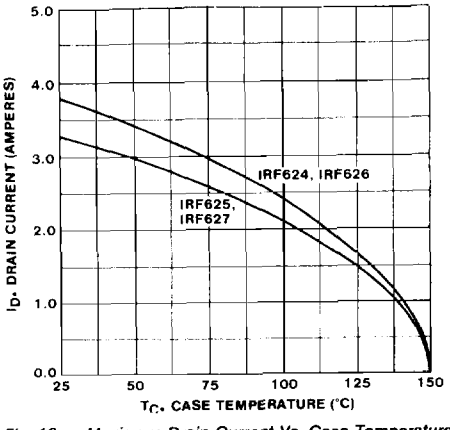


Fig. 13 — Maximum Drain Current Vs. Case Temperature

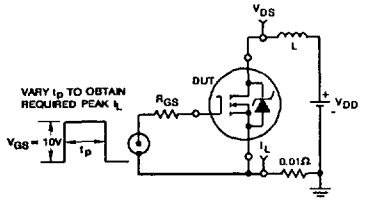


Fig. 14 — Unclamped Energy Test Circuit

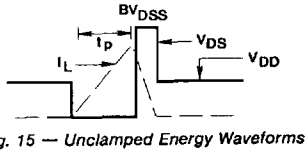


Fig. 15 — Unclamped Energy Waveforms

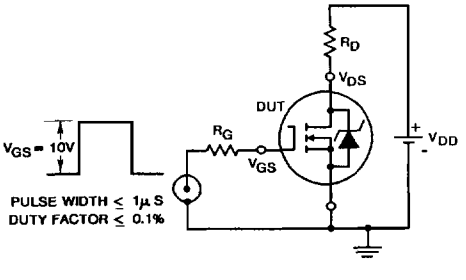


Fig. 16 — Switching Time Test Circuit

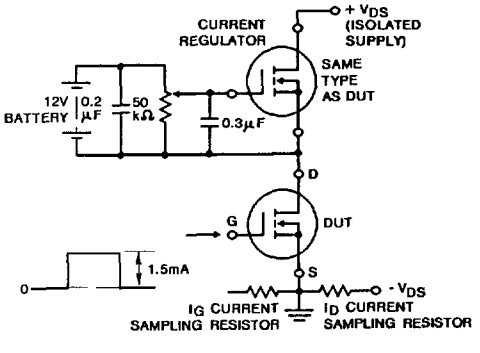


Fig. 17 — Gate Charge Test Circuit