



HARRIS

# IRFF9230, IRFF9231 IRFF9232, IRFF9233

Avalanche Energy Rated  
P-Channel Power MOSFETs

August 1991

### Features

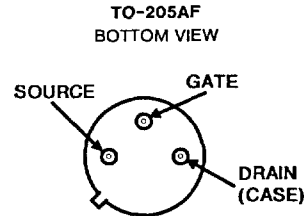
- -3.5A and -4.0A, -150V and -200V
- $r_{DS(ON)} = 0.8\Omega$  and  $1.20\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

### Description

The IRFF9230, IRFF9231, IRFF9232 and IRFF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

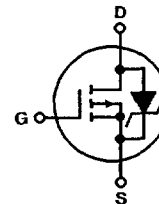
The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

### Package



### Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



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P-CHANNEL  
POWER MOSFETs

### Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ ) Unless Otherwise Specified

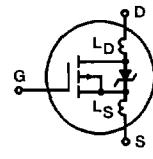
	IRFF9230	IRFF9231	IRFF9232	IRFF9233	UNITS
Drain-Source Voltage (1) . . . . . $V_{DS}$	-200	-150	-200	-150	V
Drain-Gate Voltage ( $R_{GS} = 20k\Omega$ ) (1) . . . . . $V_{DGR}$	-200	-150	-200	-150	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ . . . . . $I_D$	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3) . . . . . $I_{DM}$	-16	-16	-14	-14	A
Gate-Source Voltage . . . . . $V_{GS}$	$\pm 20$	$\pm 20$	$\pm 20$	$\pm 20$	V
Maximum Power Dissipation . . . . . $P_D$ (See Figure 14)	25	25	25	25	W
Linear Derating Factor . . . . . (See Figure 14)	0.2	0.2	0.2	0.2	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (4) . . . . . $E_{as}$	500	500	500	500	mJ
Operating and Storage Junction Temperature Range . . . . . $T_J, T_{STG}$	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) . . . . . $T_L$	300	300	300	300	$^\circ\text{C}$

#### NOTES:

- $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$
- Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
- $V_{DD} = 50\text{V}$ , Start  $T_J = +25^\circ\text{C}$ ,  $L = 46.9\text{mH}$ ,  $R_G = 25\Omega$ , Peak  $I_L = 4.0\text{A}$   
(See Figures 15 and 16)

## Specifications IRFF9230, IRFF9231, IRFF9232, IRFF9233

**Electrical Characteristics**  $T_C = +25^\circ\text{C}$ , Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRFF9230, IRFF9232 IRFF9231, IRFF9233	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-200 -150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2.0	-	-4.0	V
Gate-Source Leakage Forward	$I_{GSS}$	$V_{GS} = -20V$	-	-	-100	nA
Gate-Source Leakage Reverse	$I_{GSS}$	$V_{GS} = 20V$	-	-	100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$ $V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V,$ $T_C = +125^\circ\text{C}$	-	-	-250 -1000	$\mu A$
On-State Drain Current (Note 2) IRFF9230, IRFF9231 IRFF9232, IRFF9233	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, V_{GS} = -10V$	-4.0 -3.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9230, IRFF9231 IRFF9232, IRFF9233	$r_{DS(ON)}$	$V_{GS} = -10V, I_D = -2.0A$	-	0.5 0.8	0.8 1.2	$\Omega$
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, I_D = -2.0A$	2.2	3.5	-	S( $\Omega$ )
Input Capacitance	$C_{ISS}$	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$	-	550	-	pF
Output Capacitance	$C_{OSS}$	See Figure 10	-	170	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 BV_{DSS}, I_D = -4.0A, R_G = 9.1\Omega$ See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	$t_r$		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	$t_f$		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	$Q_g$	$V_{GS} = -10V, I_D = -4.0V_{DS} = 0.8 \text{ Max}$ Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	$Q_{gs}$		-	18	-	nC
Gate-Drain ("Miller") Charge	$Q_{gd}$		-	13	-	nC
Internal Drain Inductance	$L_D$	Measured from the drain lead, 5mm (0.2") from header to center of die.	-	5.0	-	nH
Internal Source Inductance	$L_S$	Measured from the source lead, 5mm (0.2") from header to source bonding pad.	-	15	-	nH
						
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	$^\circ\text{C/W}$

### Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	$I_S$	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-4.0	A
Pulse Source Current (Body Diode) (Note 3)	$I_{SM}$		-	-	-16	A
Diode Forward Voltage (Note 2)	$V_{SD}$	$T_C = +25^\circ\text{C}, I_S = -4.0A, V_{GS} = 0V$	-	-	-1.5	V
Reverse Recovery Time	$t_{rr}$	$T_J = +150^\circ\text{C}, I_F = -4.0A, dI_F/dt = 100A/\mu s$	-	400	-	ns
Reverse Recovered Charge	$Q_{RR}$	$T_J = +150^\circ\text{C}, I_F = -4.0A, dI_F/dt = 100A/\mu s$	-	2.6	-	$\mu\text{C}$
Forward Turn-on Time	$t_{ON}$	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$ .	-	-	-	-

NOTES: 1.  $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$

2. Pulse Test: Pulse width  $\leq 300\mu s$ ,  
Duty Cycle  $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max.  
junction temperature. See Transient Thermal  
Impedance Curve (Figure 5)

4.  $V_{DD} = 50V$ , Start  $T_J = +25^\circ\text{C}$ ,  $L = 46.9\text{mH}$ ,  
 $R_G = 25\Omega$ , Peak  $I_L = 4.0A$  (See Figures 15  
and 16)

# IRFF9230, IRFF9231, IRFF9232, IRFF9233

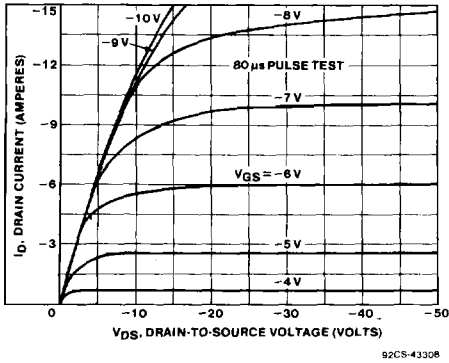


Fig. 1 - Typical output characteristics.

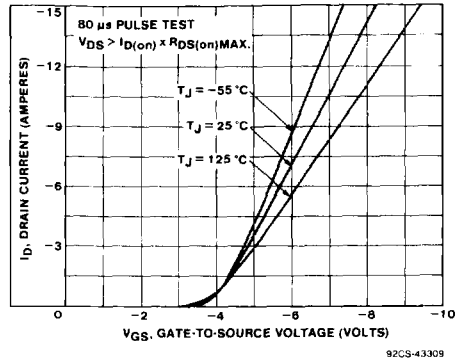


Fig. 2 - Typical transfer characteristics.

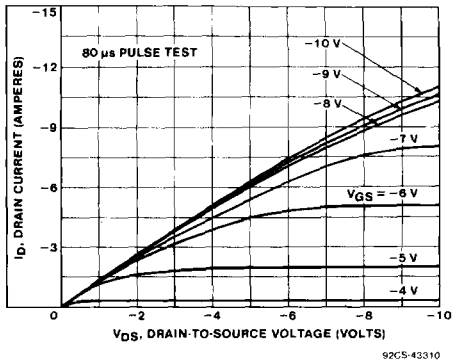


Fig. 3 - Typical saturation characteristics.

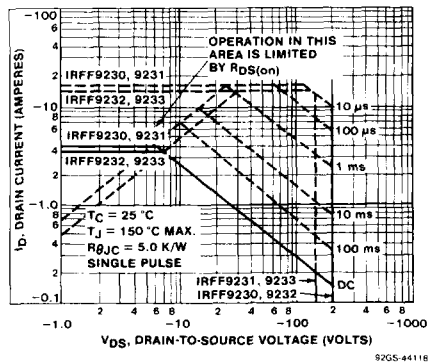


Fig. 4 - Maximum safe operating area.

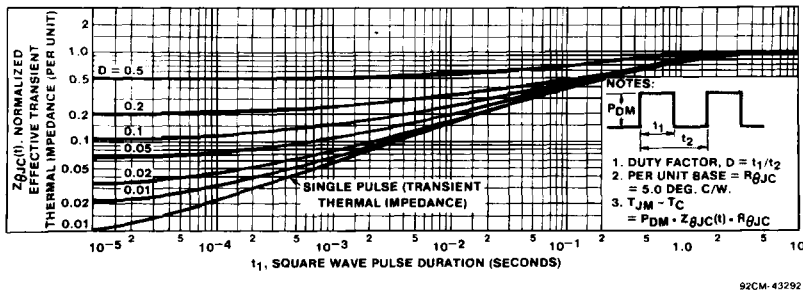


Fig. 5 - Maximum effective transient thermal impedance, junction-

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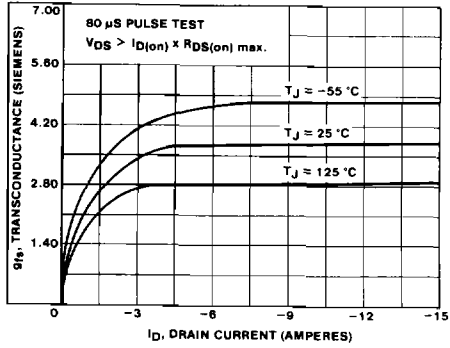


Fig. 6 - Typical transconductance vs. drain current.

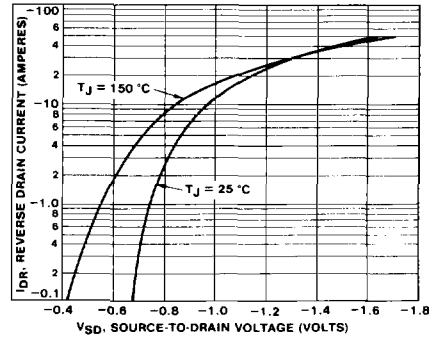


Fig. 7 - Typical source-drain diode forward voltage.

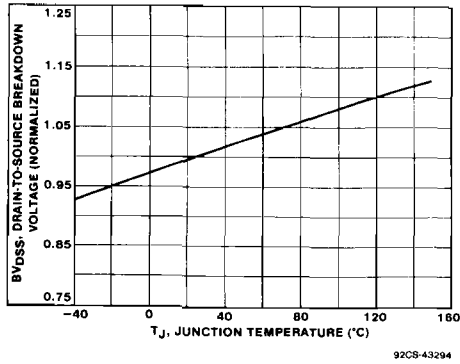


Fig. 8 - Breakdown voltage vs. temperature.

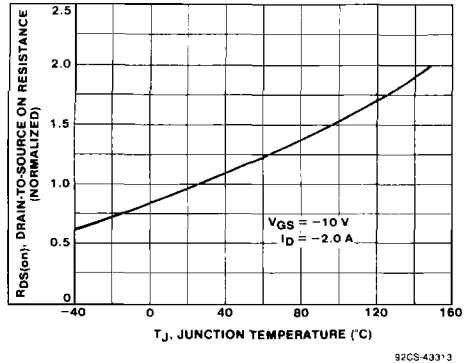


Fig. 9 - Normalized on-resistance vs. temperature.

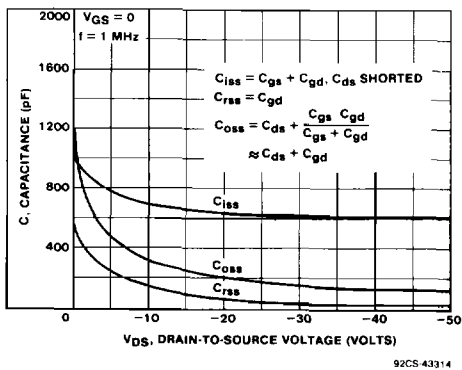


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

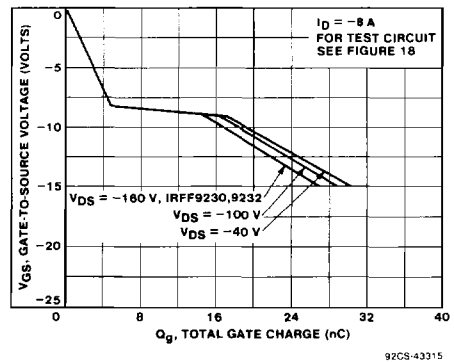


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

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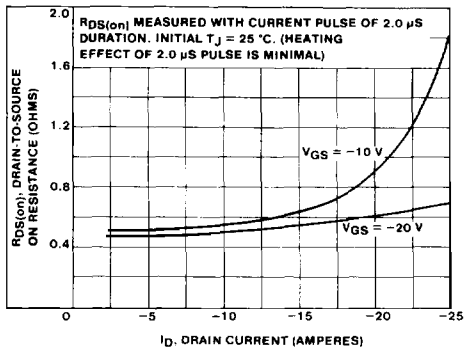


Fig. 12 - Typical on-resistance vs. drain current.

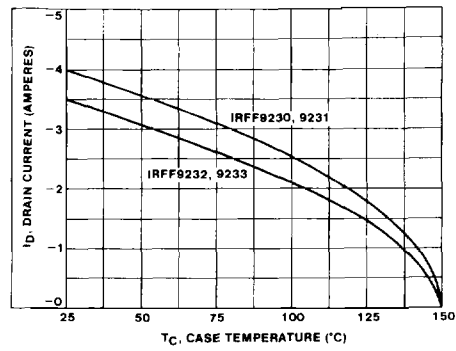


Fig. 13 - Maximum drain current vs. case temperature.

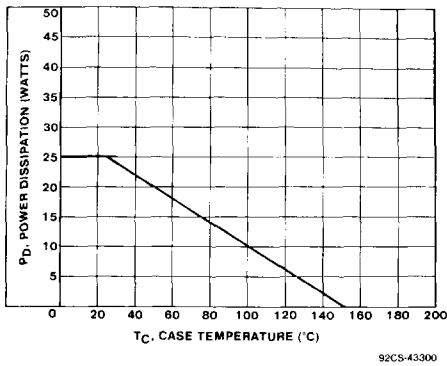


Fig. 14 - Power vs. temperature derating curve.

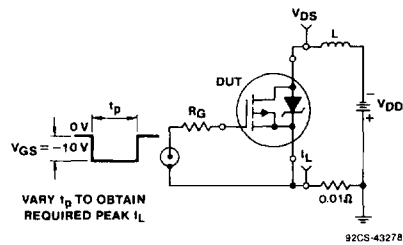


Fig. 15 - Unclamped inductive test circuit.

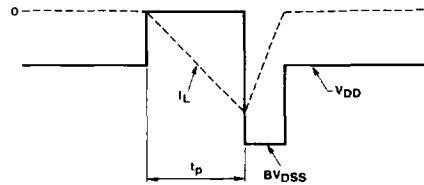


Fig. 16 - Unclamped inductive waveforms.

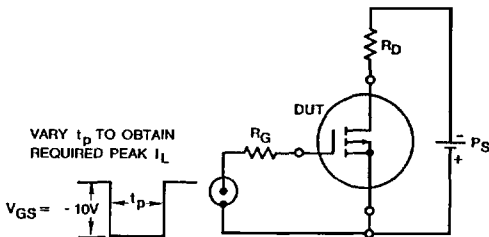


Fig. 17 - Switching time test circuit.

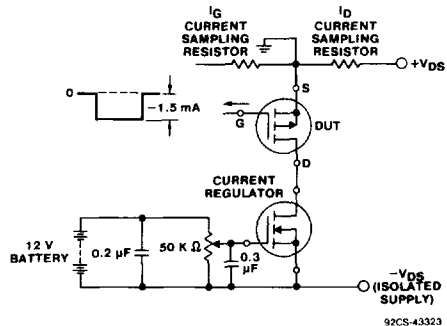


Fig. 18 - Gate charge test circuit.

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