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Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	40
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0034
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0043
I _D (A)	75
Configuration	Single

FEATURES

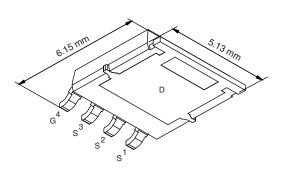
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- AEC-Q101 Qualified^c
- Material categorization:
 For definitions of compliance please see www.vishay.com/doc?99912

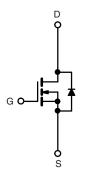




ROHS COMPLIANT HALOGEN FREE

PowerPAK® SO-8L Single





N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ422EP-T1-GE3

ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	d)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	40	V	
Gate-Source Voltage		V _{GS}	± 20	V	
Continuous Drain Current	T _C = 25 °C	1	75		
Continuous Drain Current	T _C = 125 °C	I _D	62		
Continuous Source Current (Diode Conduct	I _S	75	Α		
Pulsed Drain Current ^a		I _{DM}	300		
ulsed Drain Current ^a ngle Pulse Avalanche Current L = 0.1 ml		I _{AS}	46		
Single Pulse Avalanche Energy	L = U.1 IIII	E _{AS}	105	mJ	
Maximum Dawar Dissination	T _C = 25 °C 83	14/			
Maximum Power Dissipation ^a	T _C = 125 °C	P_{D}	27	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		-	260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^b	R_{thJA}	65	°C/W
Junction-to-Case (Drain)		R_{thJC}	1.8	C/VV

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. When mounted on 1" square PCB (FR-4 material).
- c. Parametric verification ongoing.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	1			l .		ı	ı
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-		Α
		V _{GS} = 10 V	I _D = 18 A	-	0.0028	0.0034	
Drain Cauras On State Resistance	V _{DS} V _{GS(th)} I _{GSS} I _{DSS} I _{D(on)} R _{DS(on)} September 1 September 2 September 2 September 3 September 2 September 3 September 3 September 3 September 3 September 4 September 3 September 4 September 3 September 4 Sept	V _{GS} = 4.5 V	I _D = 16 A	-	0.0035	0.0043	
Drain-Source On-State Resistance ^a	H _{DS(on)}	V _{GS} = 10 V	I _D = 18 A, T _J = 125 °C	-	-	0.0071	Ω
		V _{GS} = 10 V	I _D = 18 A, T _J = 175 °C	-	-	0.0089	1
Forward Transconductanceb	9 _{fs}	V _{DS}	= 15 V, I _D = 18 A	-	117	-	S
Dynamic ^b							
Input Capacitance	C _{iss}			-	3730	4660	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = 20 \text{ V, f} = 1 \text{ MHz}$	-	553	691	pF
Reverse Transfer Capacitance	C _{rss}]		-	223	278	
Total Gate Charge ^c				-	67	100	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 10 \text{ A}$	-	11.25	-	nC
Gate-Drain Charge ^c	Q _{gd}]		-	10.31		
Gate Resistance	R _g		f = 1 MHz	0.30	0.63	1.10	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	13	19	
Rise Time ^c	t _r	V _{DD} :	= 20 V, $R_1 = 20 \Omega$	-	10	15	
Turn-Off Delay Time ^c	t _{d(off)}		$V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$	-	29	44	ns
Fall Time ^c				-	8	12	
Source-Drain Diode Ratings and Char	acteristics ^b						
Pulsed Current ^a	I _{SM}			-	-	300	Α
Forward Voltage	V _{SD}	I _F :	= 12 A, V _{GS} = 0	-	0.75	1.1	V

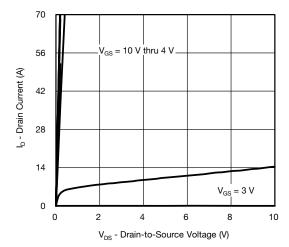
Notes

- a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

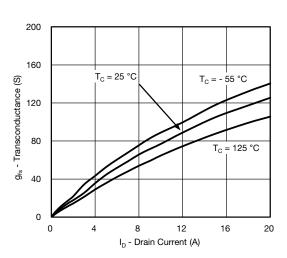
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



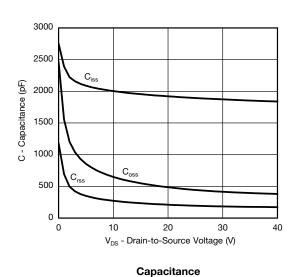
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



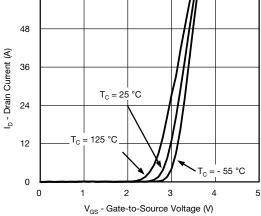
Output Characteristics



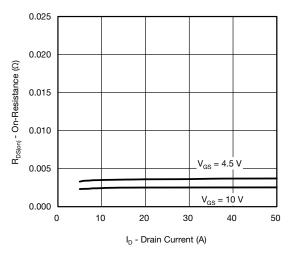
Transconductance



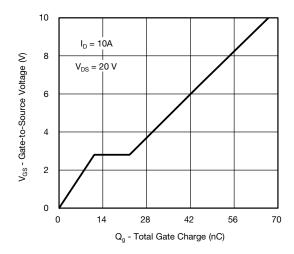
60 48



Transfer Characteristics

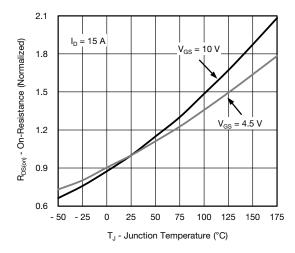


On-Resistance vs. Drain Current

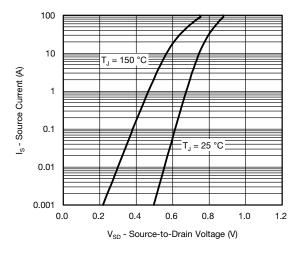




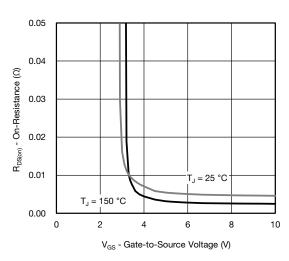
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



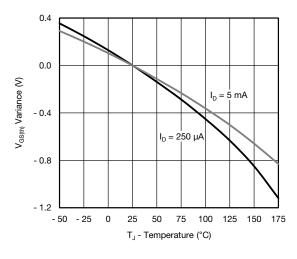
On-Resistance vs. Junction Temperature



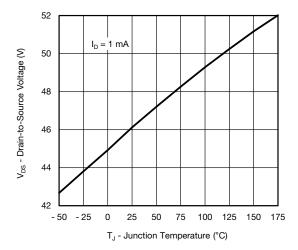
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

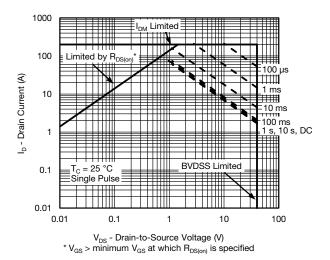


Drain Source Breakdown vs. Junction Temperature

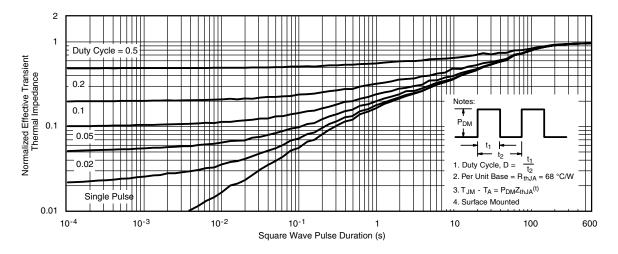
ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



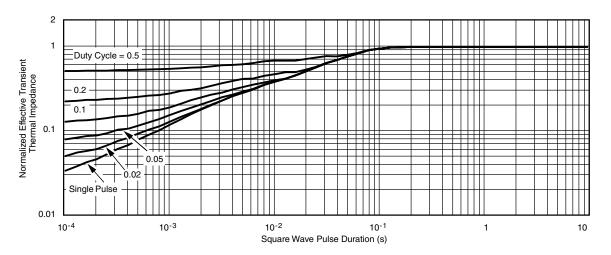
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

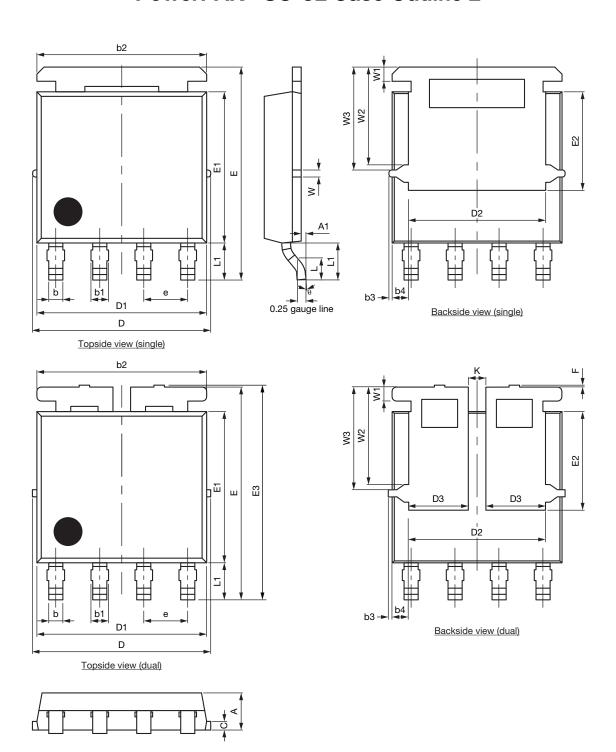
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63989.



PowerPAK® SO-8L Case Outline 2





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DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX	
Α	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094			0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC		0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
E3	6.05	6.22	6.40	0.238	0.245	0.252	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51		0.020			
W	0.23			0.009			
W1		0.41		0.016			
W2	2.82		0.111				
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

DWG: 6044

Note

• Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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