PAL16RP8A Series

16P8A, 16RP8A 16RP6A, 16RP4A

Features/Benefits

- Programmable polarity
- High speed at 25 ns tPD
- Register preload
- Power-up reset
- Security fuse

Description

The PAL16RP8A Series is equivalent to the PAL16R8A Series, with the addition of programmable polarity. With programmable polarity unused, these devices are equivalent to the PAL16R8A Series.

Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The combinatorial device has ten dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied directly to VCC or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with programmable three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any combination of device inputs or output feedback. The output provides a bidirectional I/O pin in the combinatorial configuration, and may be configured as a dedicated input if the buffer is always disabled.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops which are loaded on the low-to-high transition of the clock input.

Ordering Information

PAL16RP8A C N STD

- PROGRAMMABLE ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - RP = Registered with Programmable Polarity
  - P = Combinatorial with Programmable Polarity
- NUMBER OF OUTPUTS
- PROCESSING
  - STD = Standard
  - XXXX = Other
- PACKAGE
  - N = Plastic DIP
  - J = Ceramic DIP
  - NL = Plastic Leaded Chip Carrier
  - SG = Small-Outline Gull-wing
- OPERATING CONDITIONS
  - C = Commercial
- HIGH SPEED

Polarity

Each of these devices offers programmable polarity on each output. If the polarity fuse is unused, the output is active low. If the polarity fuse is programmed, the output is inverted to active high.

Preload and Power-Up Reset

Each device also offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages in order to simplify functional testing. This series also offers Power-Up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

Performance

Performance varies according to the use of the programmable polarity. Active low outputs have a tPD of 25 ns, while active high outputs have a tPD of 30 ns due to the extra inversion. All devices consume 180 mA maximum ICC.

Packages

The commercial PAL16RP8A Series is available in the plastic DIP (N), ceramic DIP (J), plastic leaded chip carrier (NL), and small outline (SG) packages.

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PAL16RP8A Series

	ARRAY INPUTS	OUTPUTS		t_{PD}* (ns)	I_{CC} (mA)
		COMBINATORIAL	REGISTERED		
PAL16P8A	16	8	0	25/30	180
PAL16RP8A	16	0	8	25/30	180
PAL16RP6A	16	6	2	25/30	180
PAL16RP4A	16	4	4	25/30	180

*25 ns active low, 30 ns active high

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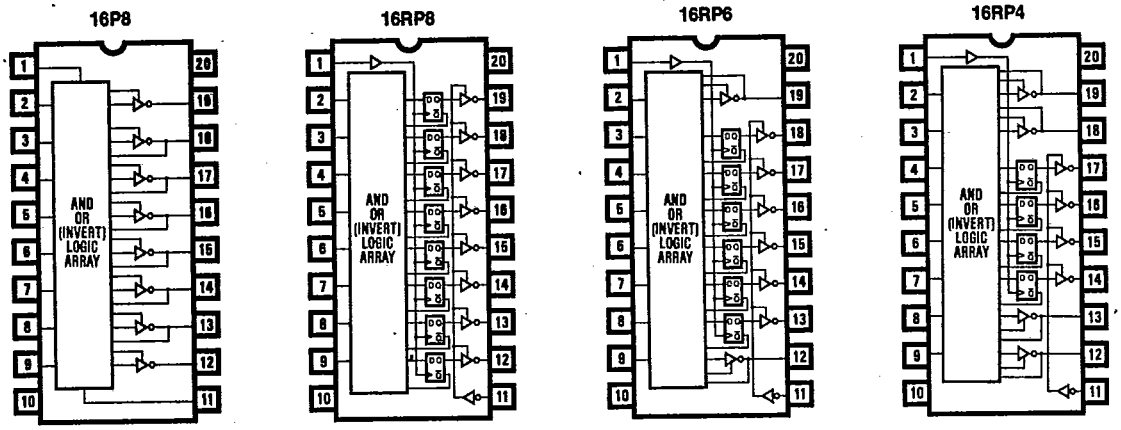
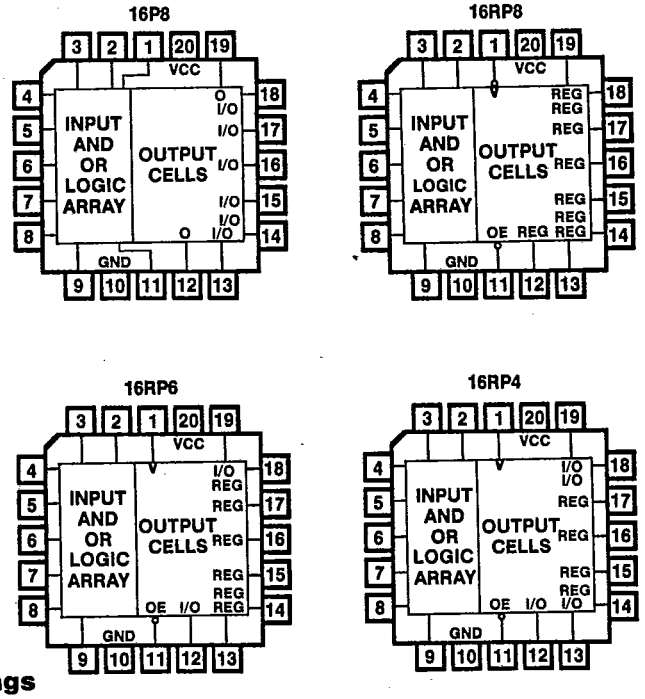
DIP/SO Pinouts



PLCC Pinouts



Package Drawings

(refer to PAL Device Package Outlines, page 3-179)

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low		20	14		ns
		High		10	6		
t_{su}	Set up time from input or feedback to clock	16RP8A 16RP6A 16RP4A	Polarity fuse intact	25	15		ns
			Polarity fuse programmed	30	20		
t_h	Hold time			0	-10		ns
T_A	Operating free-air temperature			0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -3.2 mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	µA
I_{OZH}[3]			V_O = 2.4 V			100	µA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

1. The PAL16RP8A Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 16P8A, 16RP6A, 16RP4A		Polarity fuse intact	R_1 = 200 Ω R_2 = 390 KΩ		15	25	ns
			Polarity fuse programmed			20	30	
t_{CLK}	Clock to output					10	15	ns
t_{CF}	Clock to feedback					8	10	ns
t_{PZX}	Pin 11 to output enable except 16P8A					10	20	ns
t_{PXZ}	Pin 11 to output disable except 16P8A					11	20	ns
t_{EA}	Input to output enable		16P8A, 16RP6A, 16RP4A			10	25	ns
t_{ER}	Input to output disable		16P8A, 16RP6A, 16RP4A			13	25	ns
f_{MAX}	Maximum frequency 16RP8A, 16RP6A, 16RP4A	External	Polarity fuse intact		25	40		MHz
			Polarity fuse programmed		22	33		
		Internal	Polarity fuse intact		28.5	43		
			Polarity fuse programmed		25	35		
		No feedback			33	50		

Switching Test Load
(refer to page 5-164)

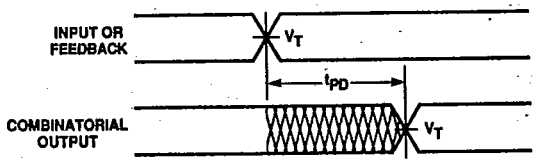
Programmers/Development Systems
(refer to Programmer Reference Guide, page 3-81)

Register Preload Waveform
(refer to page 5-164)

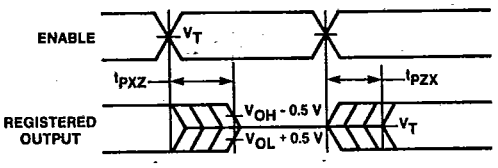
Power-Up Reset Waveform
(refer to page 5-164)

Schematic of Inputs and Outputs
(refer to page 5-164)

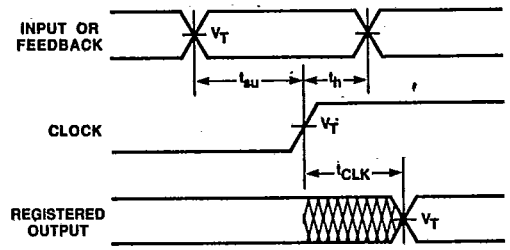
Switching Waveforms



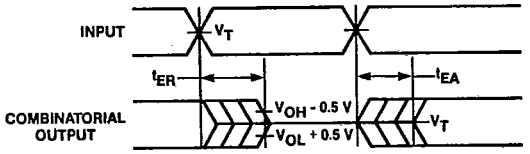
Combinatorial Output



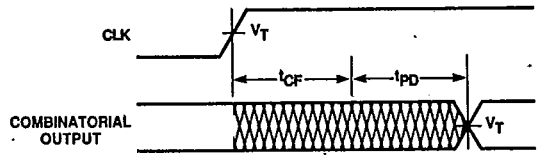
Pin 11 to Output Disable/Enable



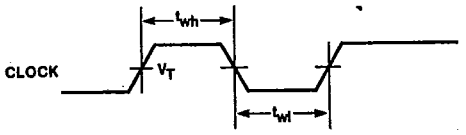
Registered Output



Input to Output Disable/Enable



Clock to Feedback to Combinatorial Output (see path below)



Clock Width

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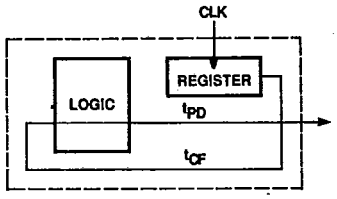
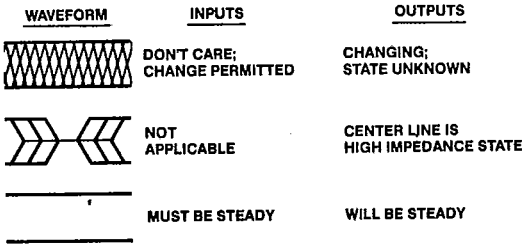


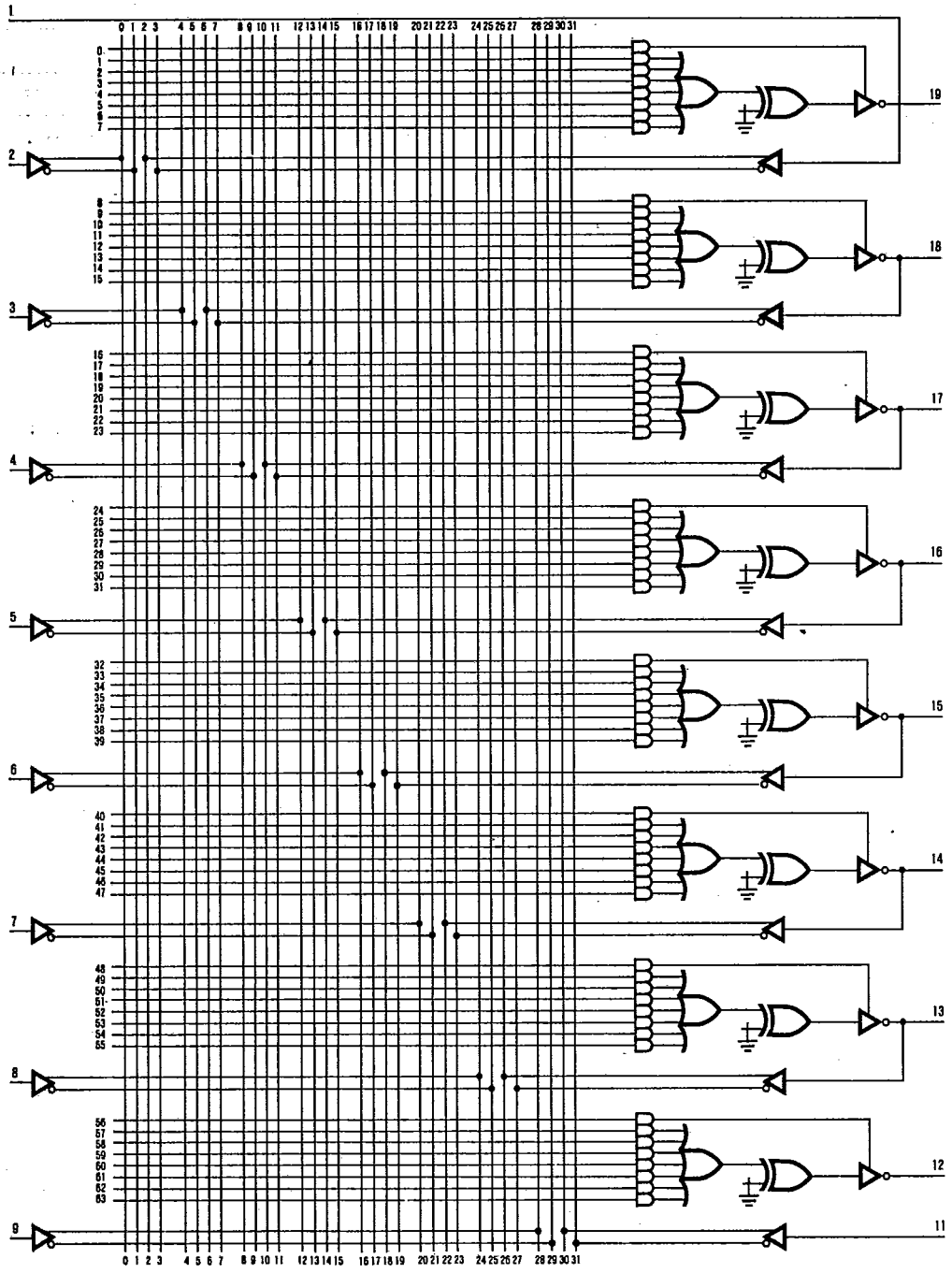
Key to Timing Diagrams



Notes:
1. VT=1.5V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2-5 ns typical

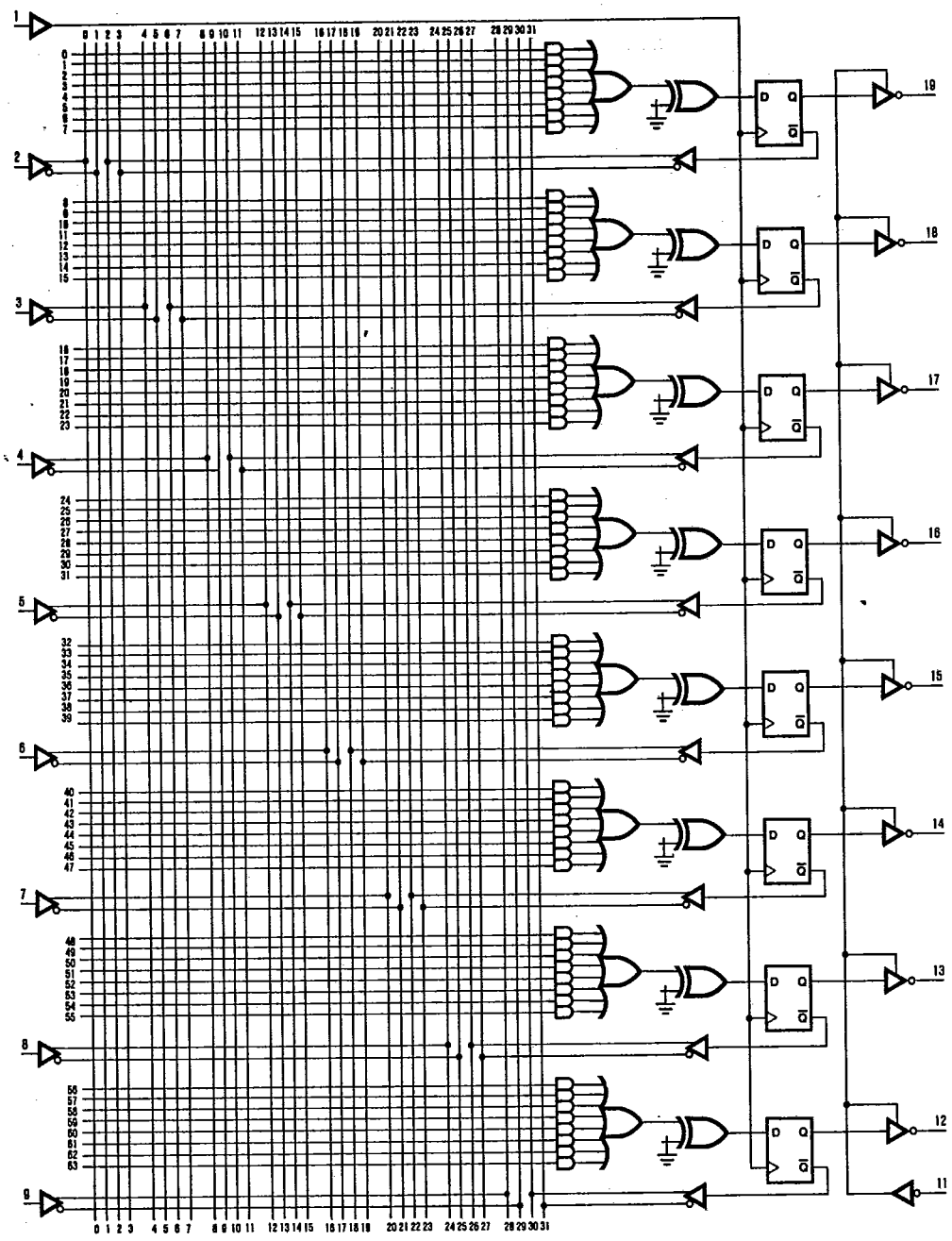
Logic Diagram

16P8A



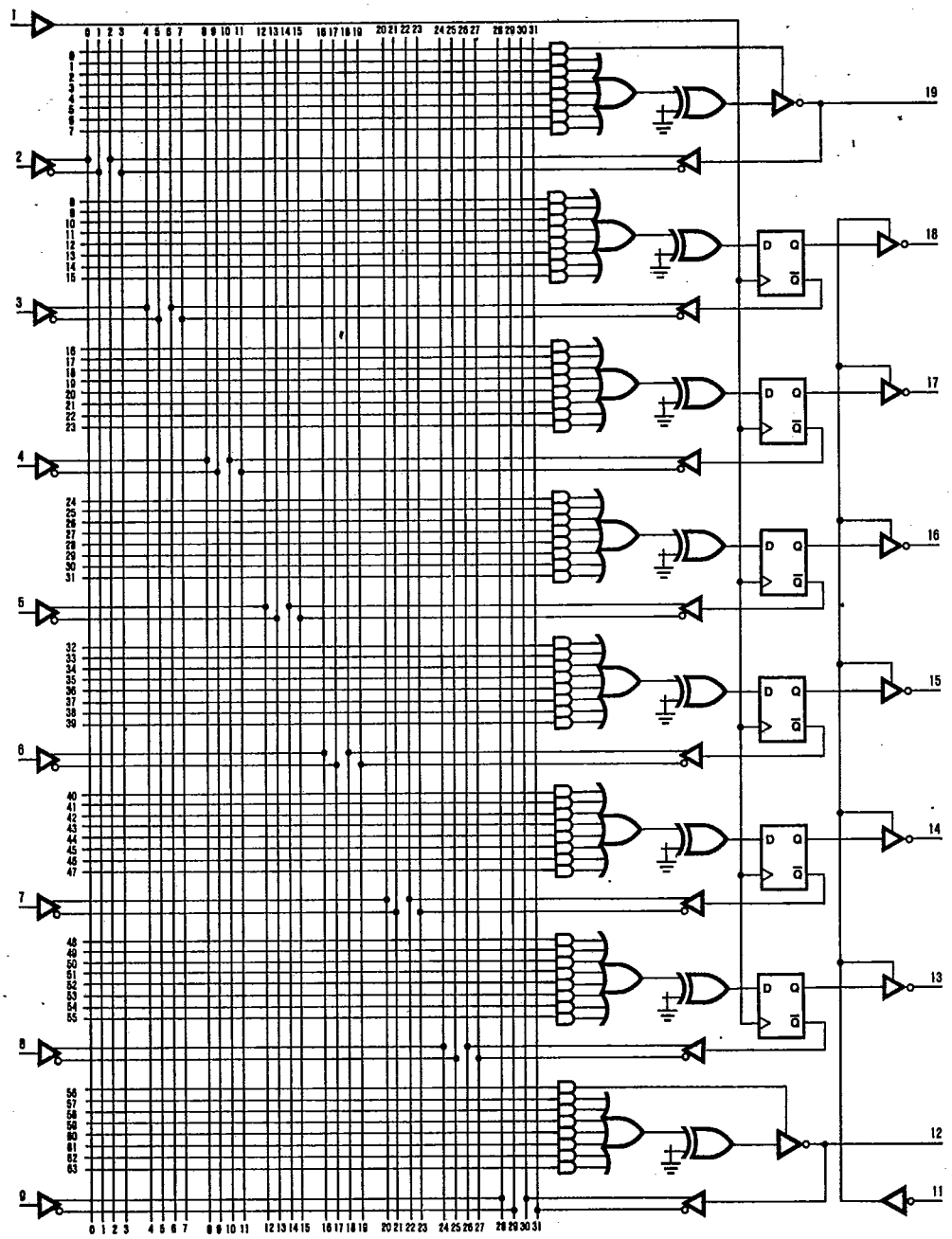
Logic Diagram

16RP8A



Logic Diagram

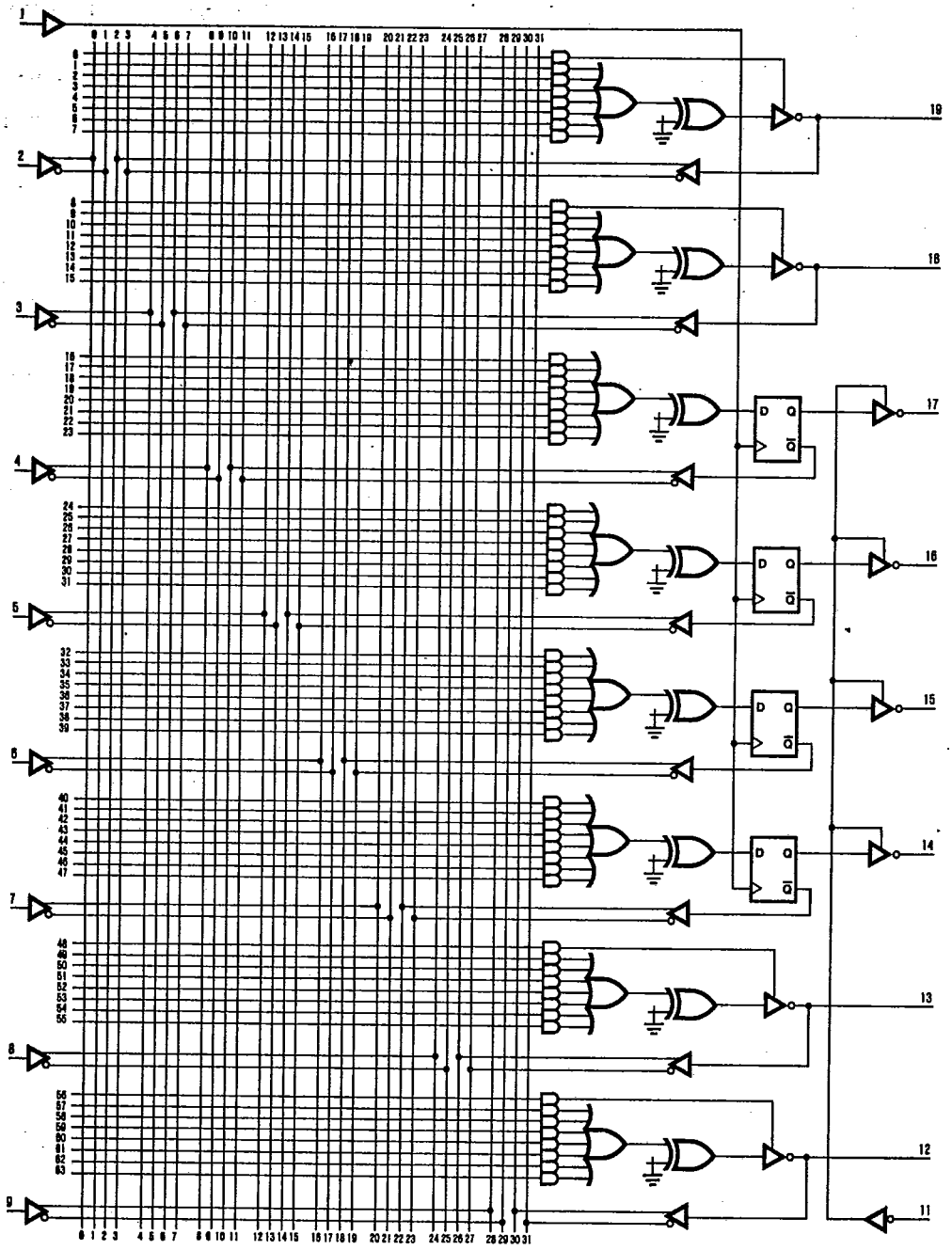
16RP6A



Logic Diagram

16RP4A

T-46-13-47



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