

## Automotive MOSFET

## OptiMOS™-5 Power-Transistor



## Features

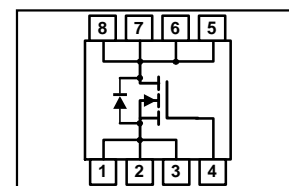
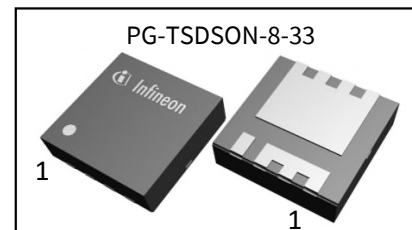
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



## Product Summary

$V_{DS}$	60	V
$R_{DS(on)}$	5	mΩ
$I_D$ (chip limited)	90	A

Type	Package	Marking
IAUZ40N06S5L050	PG-TSDSON-8-33	5N6L050



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , Chip limitation <sup>1,2)</sup>	90	A
		$V_{GS}=10\text{V}$ , DC current <sup>3)</sup>	40	
		$T_a=85\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,4)</sup>	12	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$ , $t_p=100\text{ }\mu\text{s}$	252	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=20\text{ A}$	115	mJ
Avalanche current, single pulse	$I_{AS}$	–	40	A
Gate source voltage	$V_{GS}$	–	$\pm 16$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	71	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

## Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	2.1	K/W
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	–	–	38.5	–	

## Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	60	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=29\text{ }\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	–	–	1	$\mu\text{A}$
		$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=100\text{ °C}^{2)}$	–	–	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=16\text{ V}$ , $V_{DS}=0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$	–	5.3	6.4	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$	–	4.0	5.0	
Gate resistance <sup>2)</sup>	$R_G$	–	–	1.35	–	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Dynamic characteristics<sup>2)</sup></b>						
Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$	-	1923	2500	pF
Output capacitance	$C_{oss}$		-	356	463	
Reverse transfer capacitance	$C_{rss}$		-	18	27	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=20\text{ A}, R_G=3.5\ \Omega$	-	3.3	-	ns
Rise time	$t_r$		-	0.9	-	
Turn-off delay time	$t_{d(off)}$		-	14.6	-	
Fall time	$t_f$		-	8.0	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=30\text{ V}, I_D=20\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	5.6	7.3	nC
Gate to drain charge	$Q_{gd}$		-	4.3	6.5	
Gate charge total	$Q_g$		-	28.2	36.7	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ °C}$	-	-	40	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	-	-	252	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ °C}$	-	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=30\text{ V}, I_F=40\text{ A}, di_f/dt=100\text{ A}/\mu\text{s}$	-	33	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	23	-	nC

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

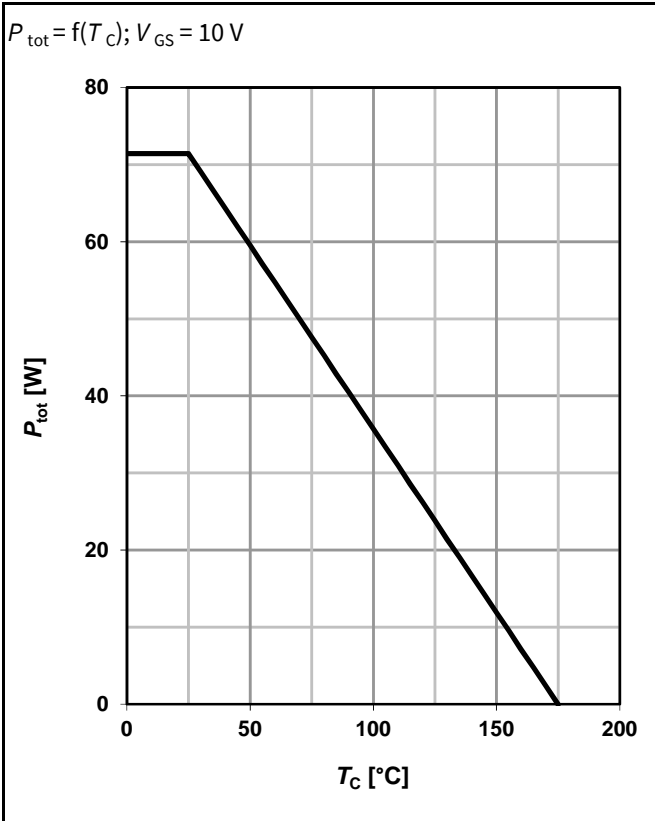
<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Current is limited by the package.

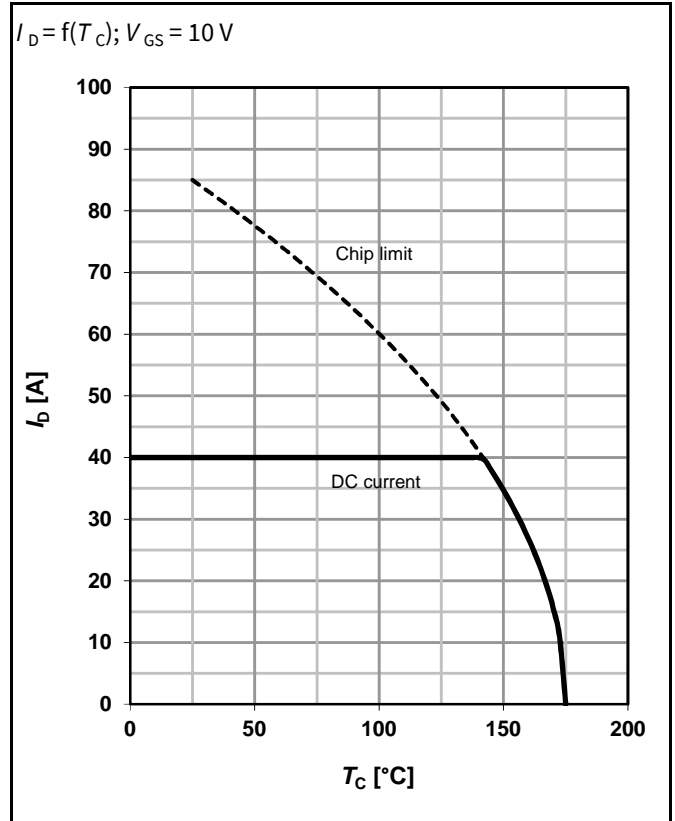
<sup>4)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

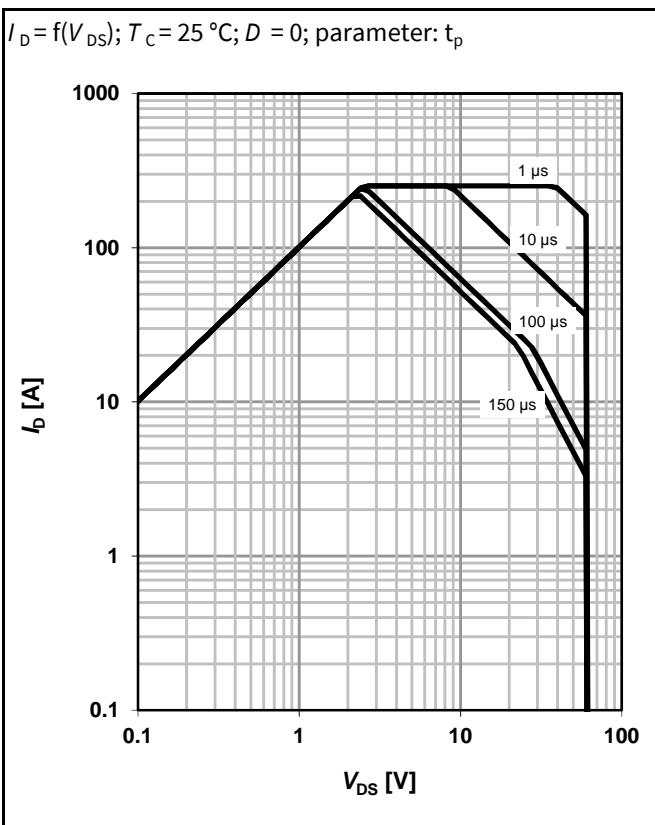
### 1 Power dissipation



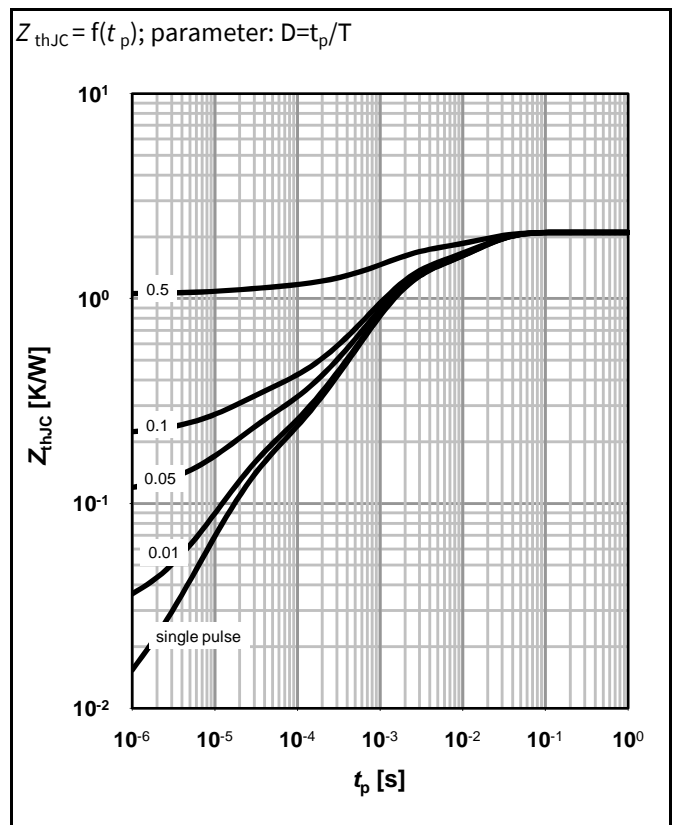
### 2 Drain current



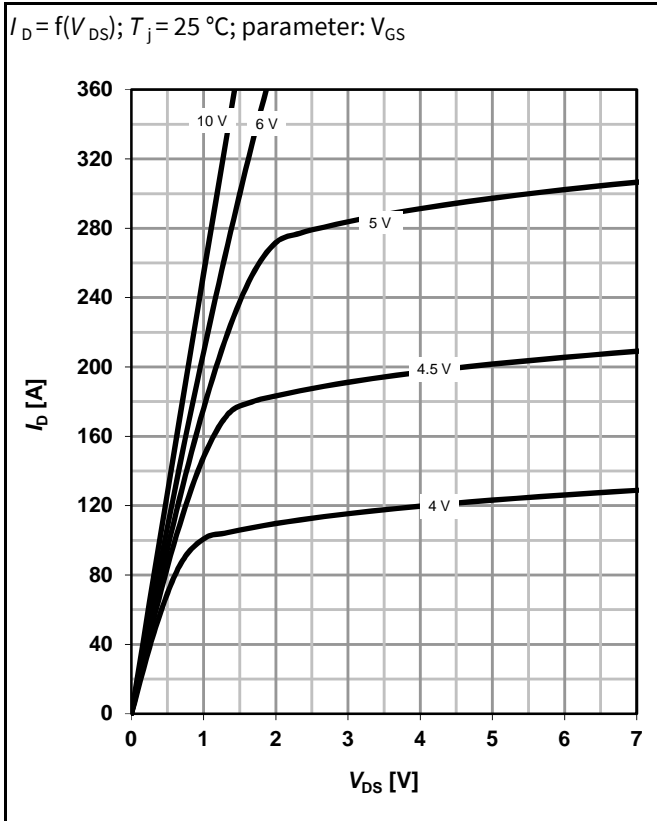
### 3 Safe operating area



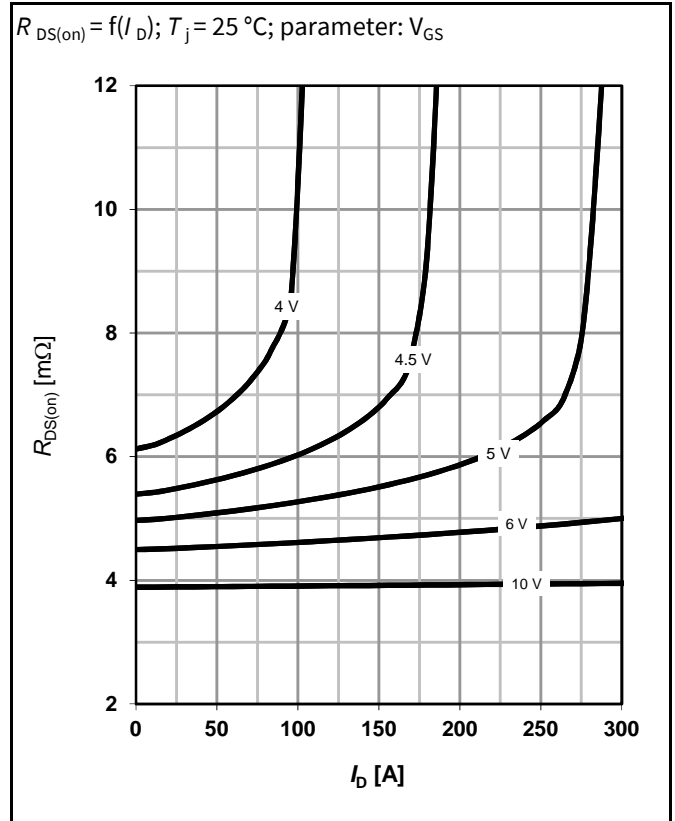
### 4 Max. transient thermal impedance



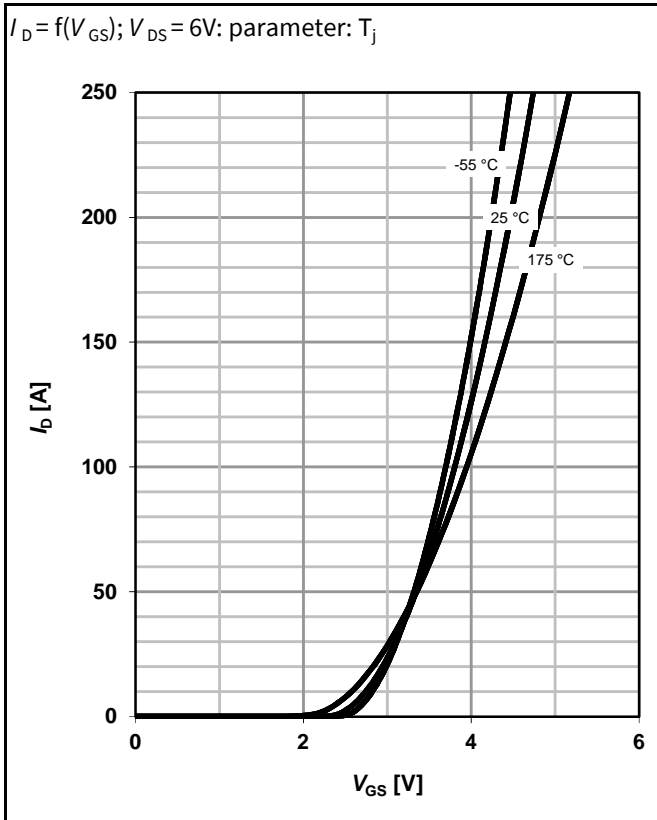
5 Typ. output characteristics



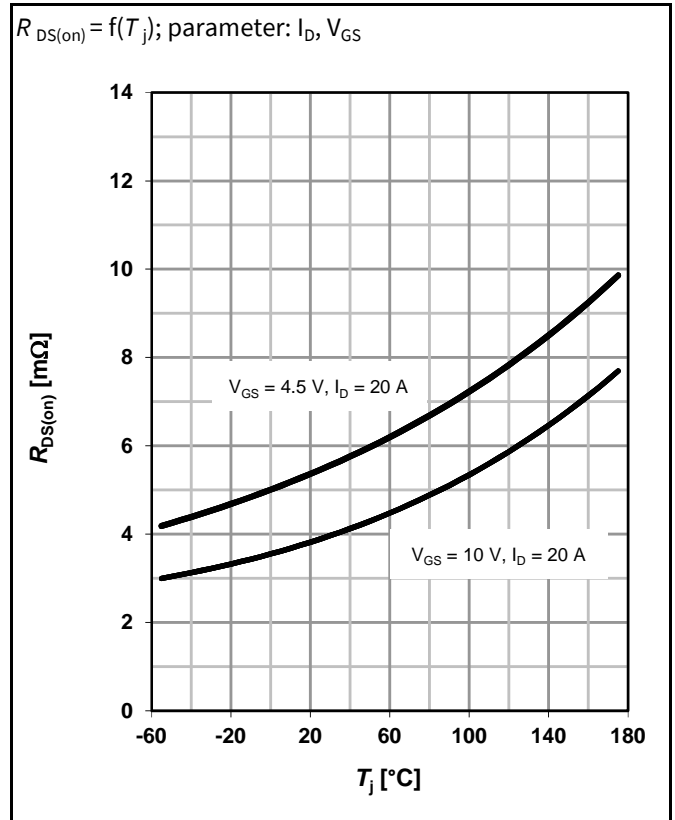
6 Typ. drain-source on-state resistance



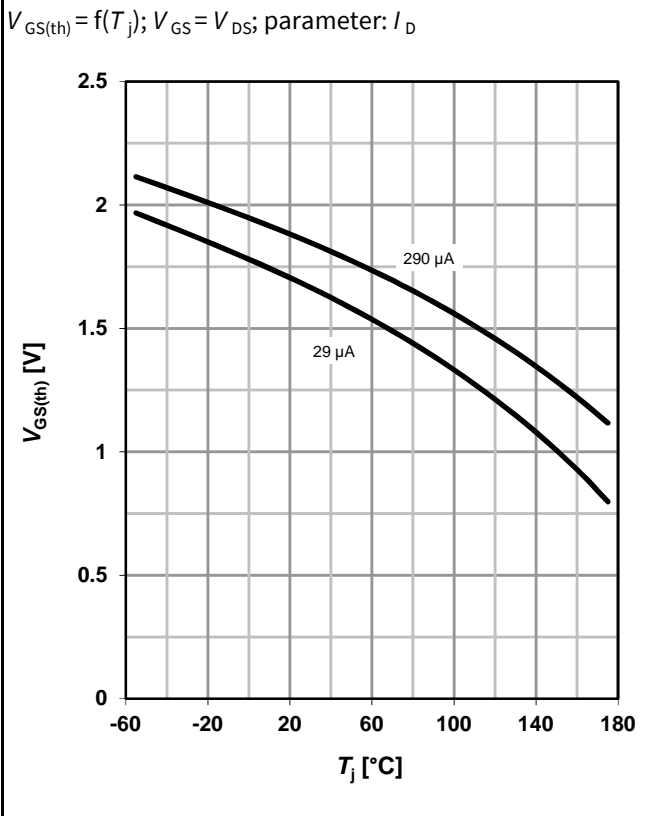
7 Typ. transfer characteristics



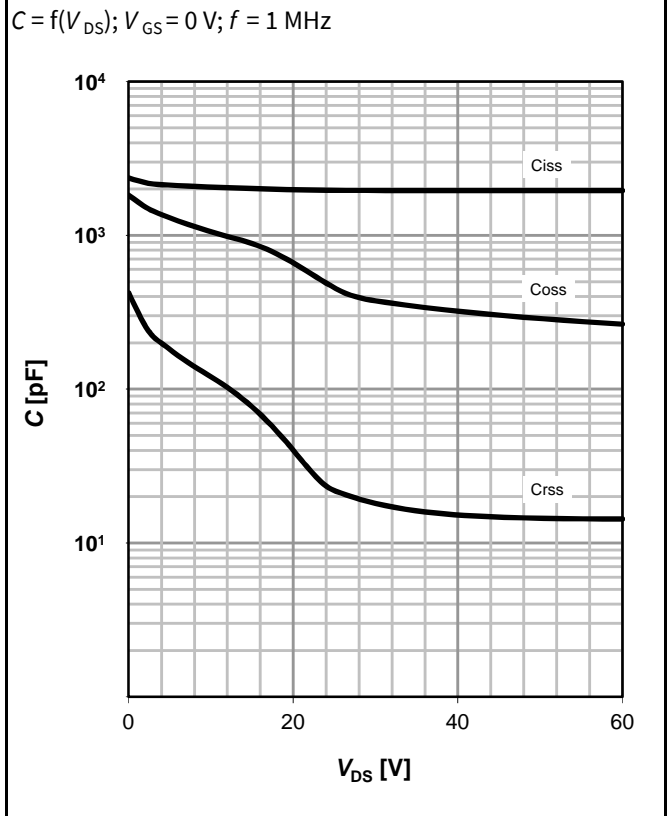
8 Typ. drain-source on-state resistance



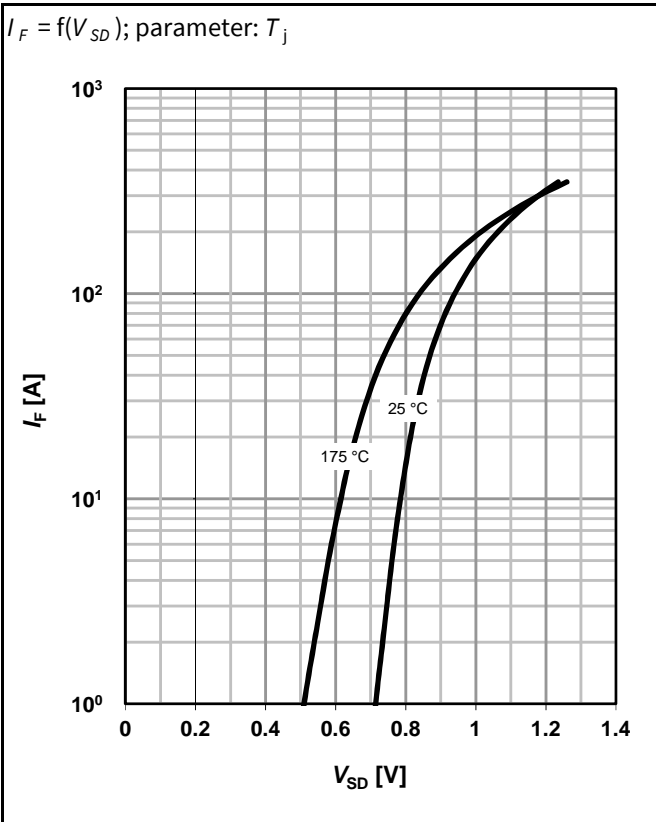
9 Typ. gate threshold voltage



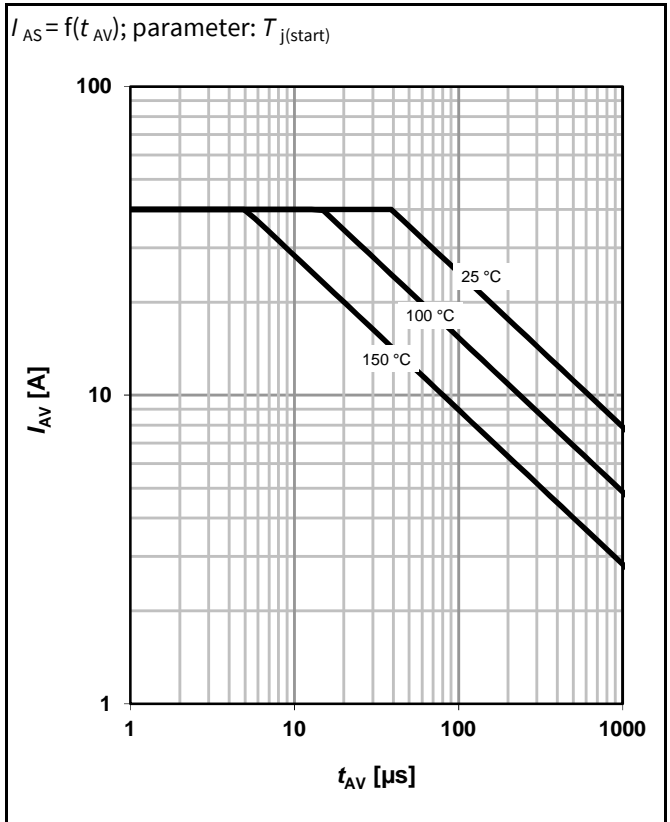
10 Typ. capacitances



11 Typical forward diode characteristics

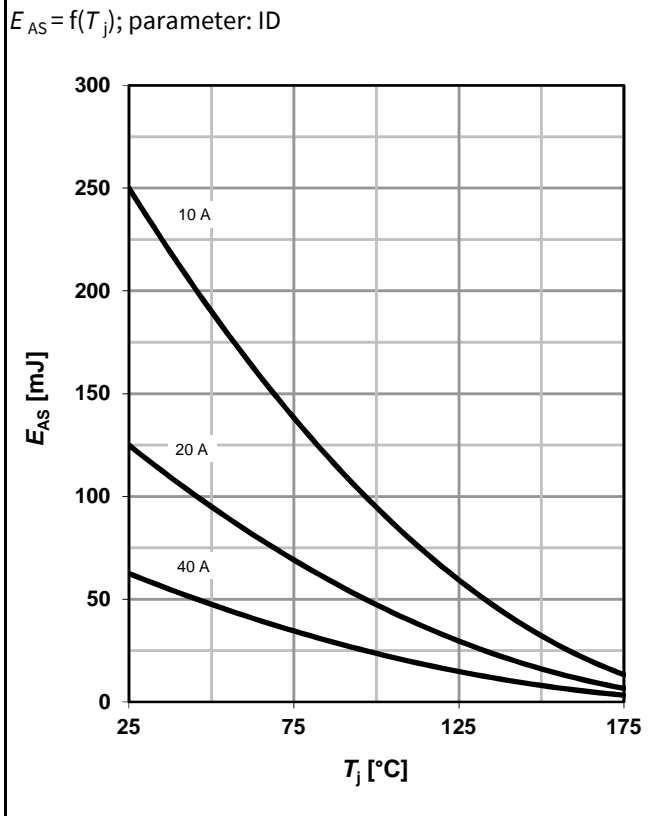


12 Typ. avalanche characteristics

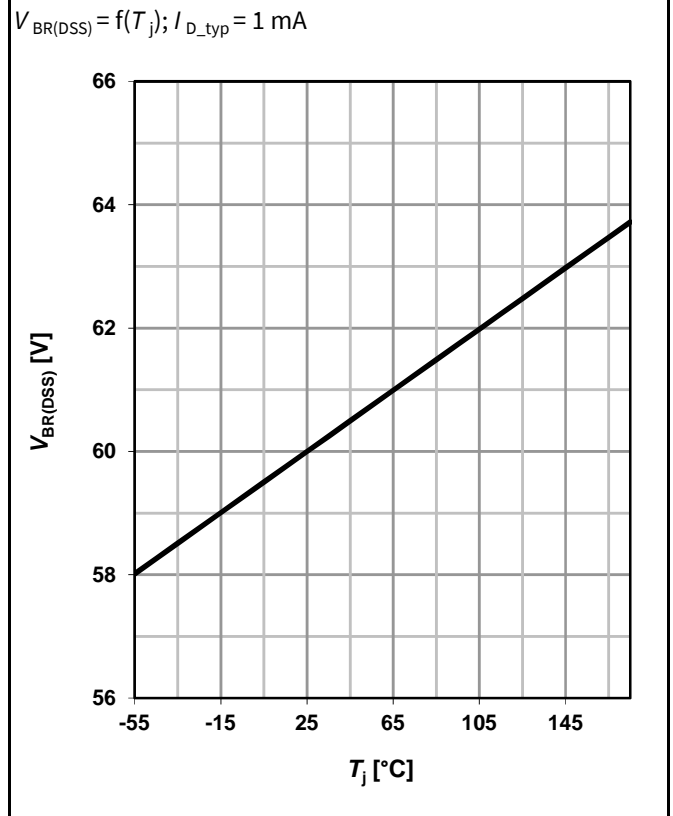




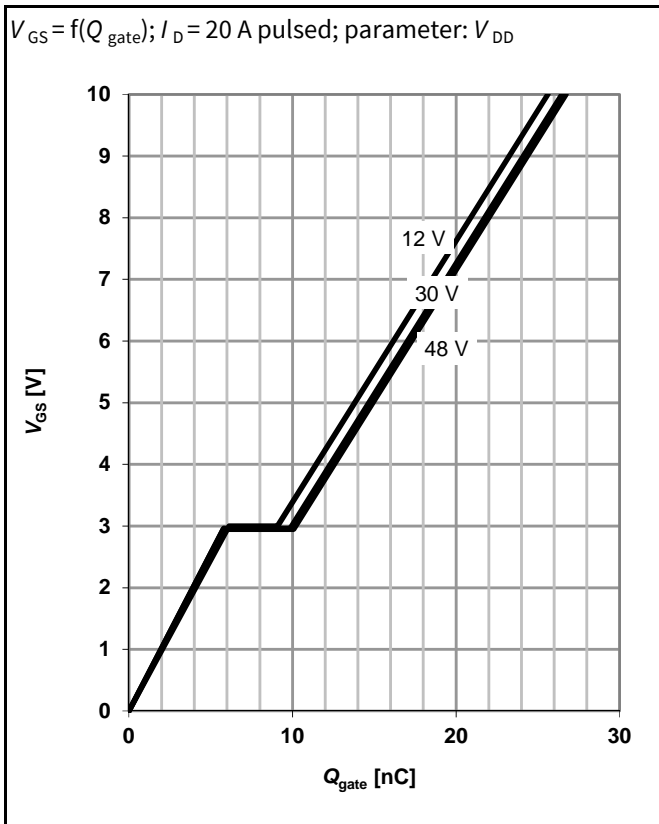
13 Typical avalanche energy



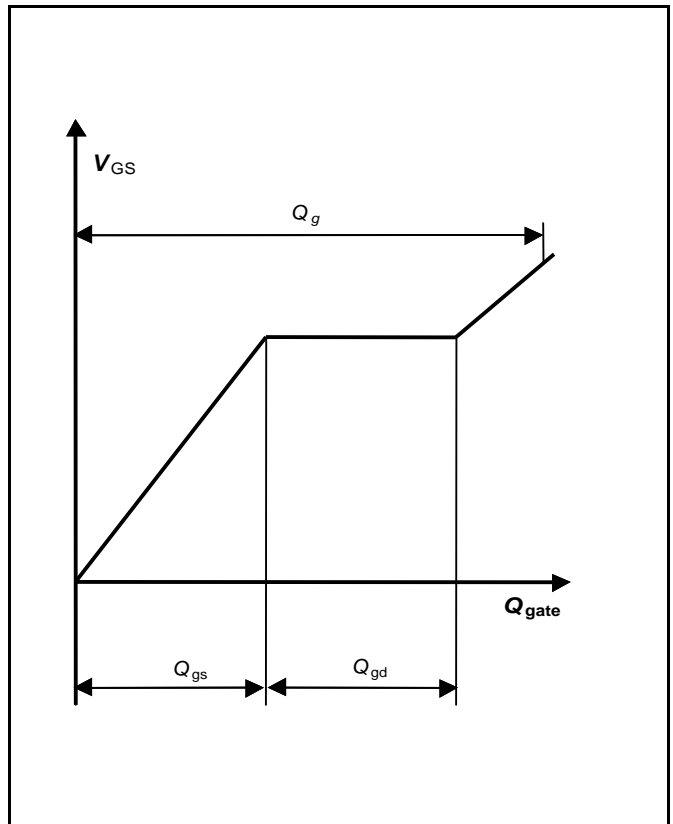
14 Drain-source breakdown voltage



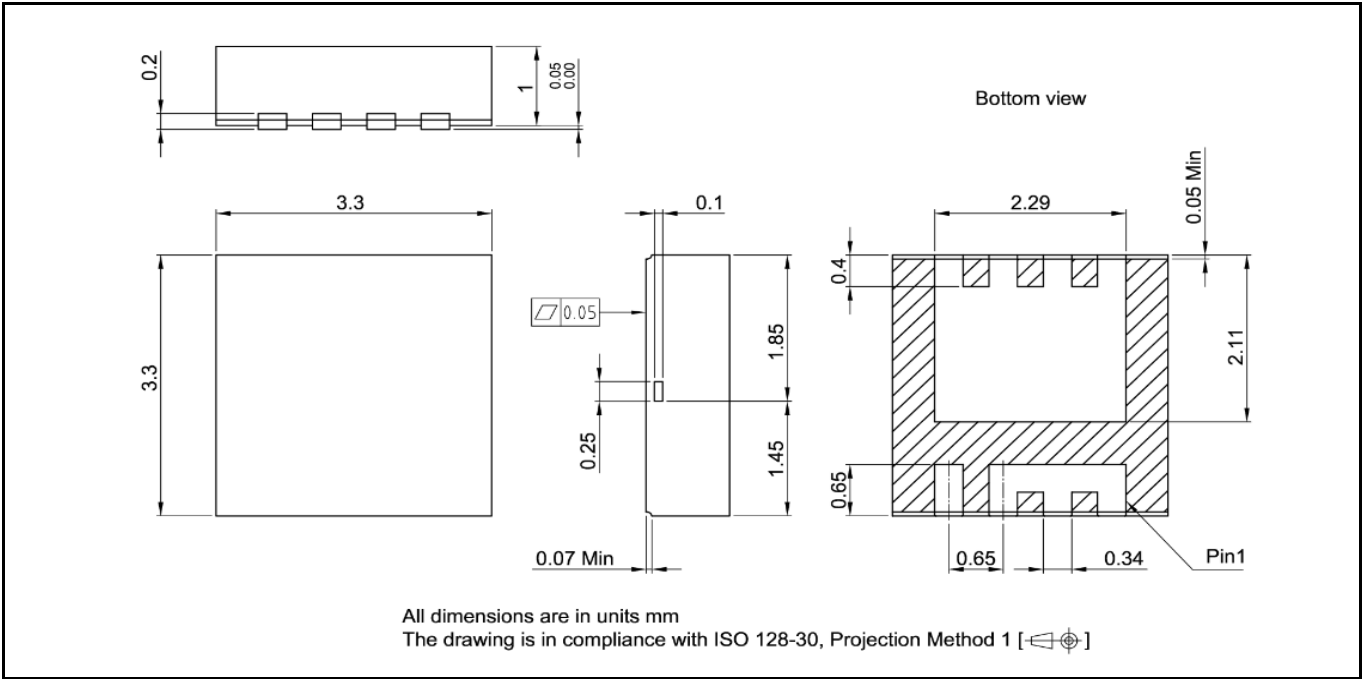
15 Typ. gate charge



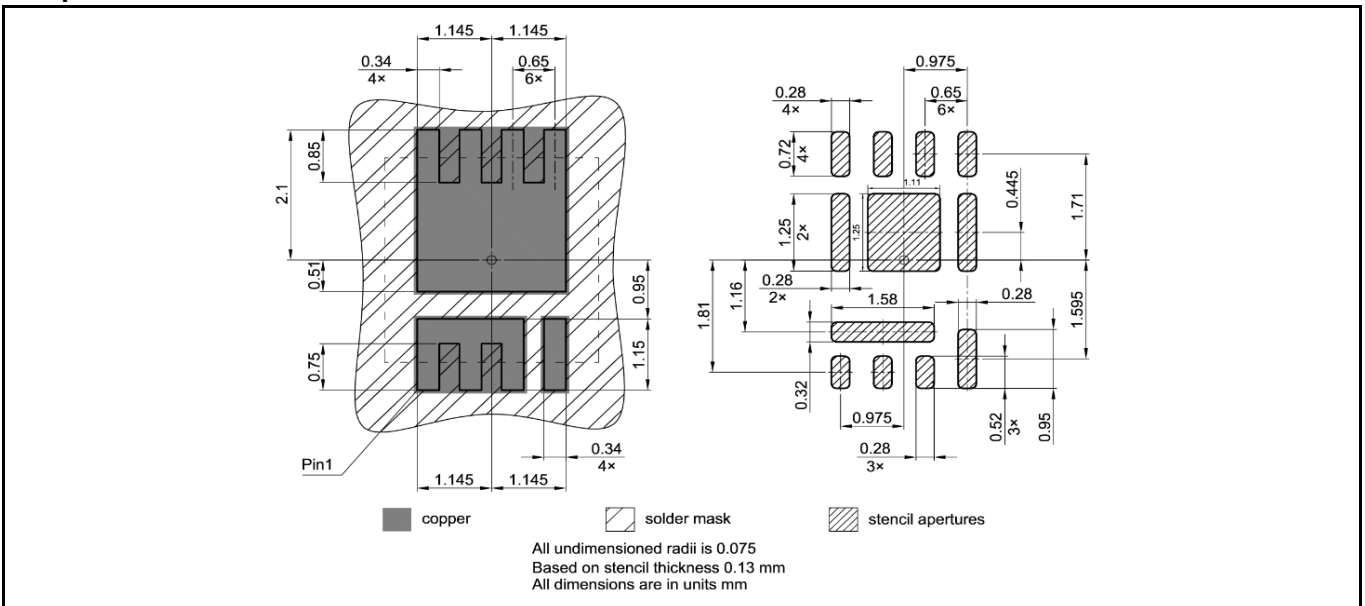
16 Gate charge waveforms



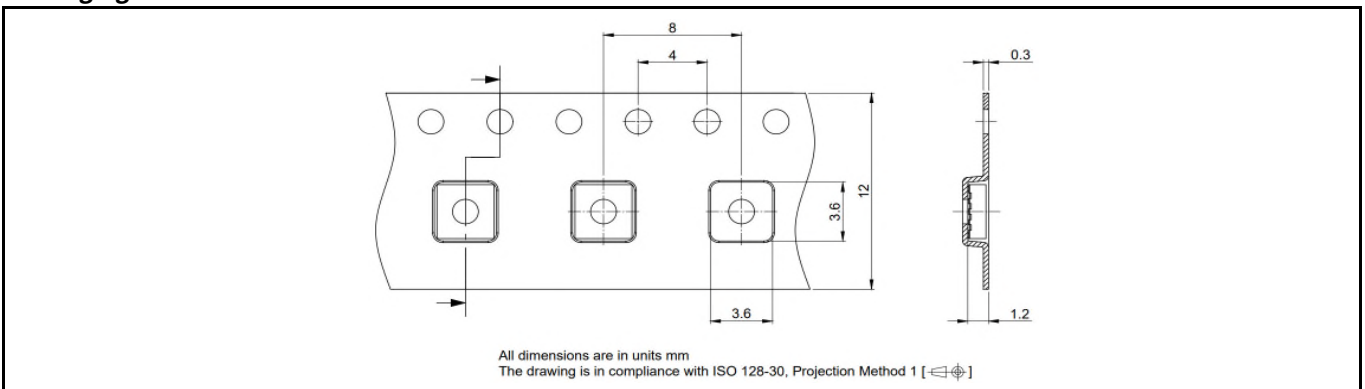
## Package Outline



## Footprint



## Packaging



**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
Revision 1.0	04.05.2021	final data sheet
Revision 1.1	07.05.2021	marking (page 1)
Revision 1.2	01.10.2021	normal level -> logic level (page 1)
Revision 1.3	27.01.2022	update image for pin layout (page 1), update thermal characteristics (page 4)

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