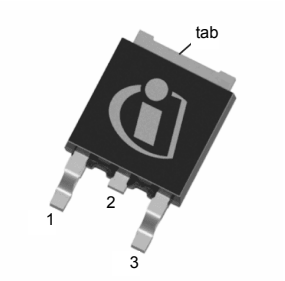
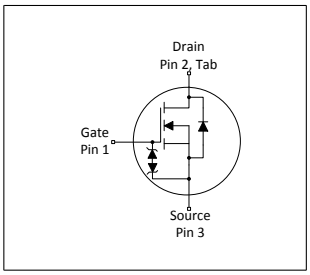
MOSFET

700V CoolMOS™ P7 Power Transistor

DPAK



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.
The latest CoolMOS™ P7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, lighting, TV, etc.
The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



Features

- Extremely low losses due to very low FOM $R_{DS(on)}$*Q_g and $R_{DS(on)}$*E_{oss}
- Excellent thermal behavior
- Integrated ESD protection diode
- Low switching losses (E_{oss})
- Product validation acc. JEDEC Standard

Benefits

- Cost competitive technology
- Lower temperature
- High ESD ruggedness
- Enables efficiency gains at higher switching frequencies
- Enables high power density designs and small form factors

Potential applications

Recommended for Flyback topologies for example used in Chargers, Adapters, Lighting Applications, etc.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j=25°C}$	700	V
$R_{DS(on),max}$	0.6	Ω
$Q_{g,typ}$	10.5	nC
$I_{D,pulse}$	20.5	A
E_{oss} @ 400V	1.2	µJ
$V_{(GS)th,typ}$	3	V
ESD class (HBM)	2	

Type / Ordering Code	Package	Marking	Related Links
IPD70R600P7S	PG-TO 252-3	70S600P7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	8.5 5.0	A	T_C = 20°C T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	20.5	A	T_C=25°C
Application (Flyback) relevant avalanche current, single pulse[3]	I_{AS}	-	-	3.2	A	measured with standard leakage inductance of transformer of 7µH
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS} =0...400V
Gate source voltage	V_{GS}	-16 -30	- -	16 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	43.1	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-
Continuous diode forward current	I_S	-	-	5.9	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	20.5	A	T_C = 25°C
Reverse diode dv/dt[4]	dv/dt	-	-	1	V/ns	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed[4]	di_f/dt	-	-	50	A/µs	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction	R_{thJC}	-	-	2.9	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	Device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm^2 (one layer 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL3

[1] Limited by $T_{j\,max}$. T_j = 20°C. Maximum duty cycle D=0.5
[2] Pulse width t_p limited by $T_{j,max}$
[3] Proven during verification test. For explanation please read AN - CoolMOS™ 700V P7.
[4] V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	V_{DS}=V_{GS}, I_D=0.09mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=700V, V_{GS}=0V, T_j=25°C V_{DS}=700V, V_{GS}=0V, T_j=150°C
Gate-source leakage current incl. Zener diode	I_{GSS}	-	-	1	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.49 1.03	0.60 -	Ω	V_{GS}=10V, I_D=1.8A, T_j=25°C V_{GS}=10V, I_D=1.8A, T_j=150°C
Gate resistance	R_G	-	10	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	364	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	7	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	17	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	200	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=5.3Ω
Rise time	t_r	-	5.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=5.3Ω
Turn-off delay time	$t_{d(off)}$	-	63	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=5.3Ω
Fall time	t_f	-	23	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=5.3Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.6	-	nC	V_{DD}=400V, I_D=1.4A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	3.7	-	nC	V_{DD}=400V, I_D=1.4A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	10.5	-	nC	V_{DD}=400V, I_D=1.4A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	V_{DD}=400V, I_D=1.4A, V_{GS}=0 to 10V

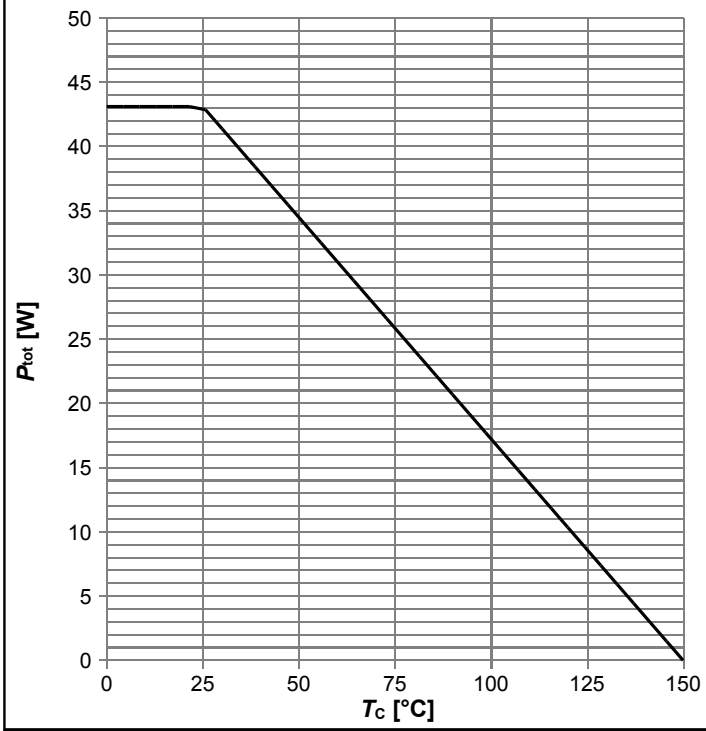
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=2.5A, T_j=25°C
Reverse recovery time	t_{rr}	-	190	-	ns	V_R=400V, I_F=1.4A, di_F/dt=50A/µs
Reverse recovery charge	Q_{rr}	-	0.8	-	µC	V_R=400V, I_F=1.4A, di_F/dt=50A/µs
Peak reverse recovery current	I_{rrm}	-	9	-	A	V_R=400V, I_F=1.4A, di_F/dt=50A/µs

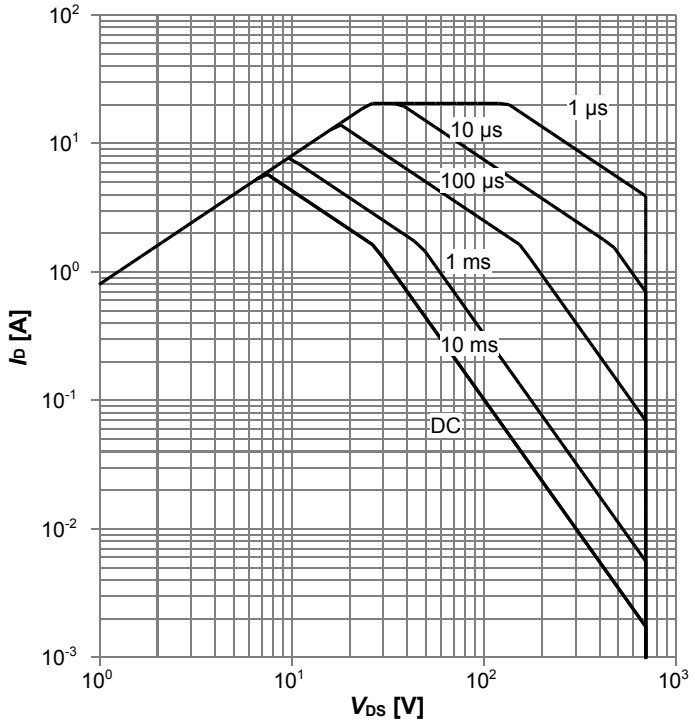
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



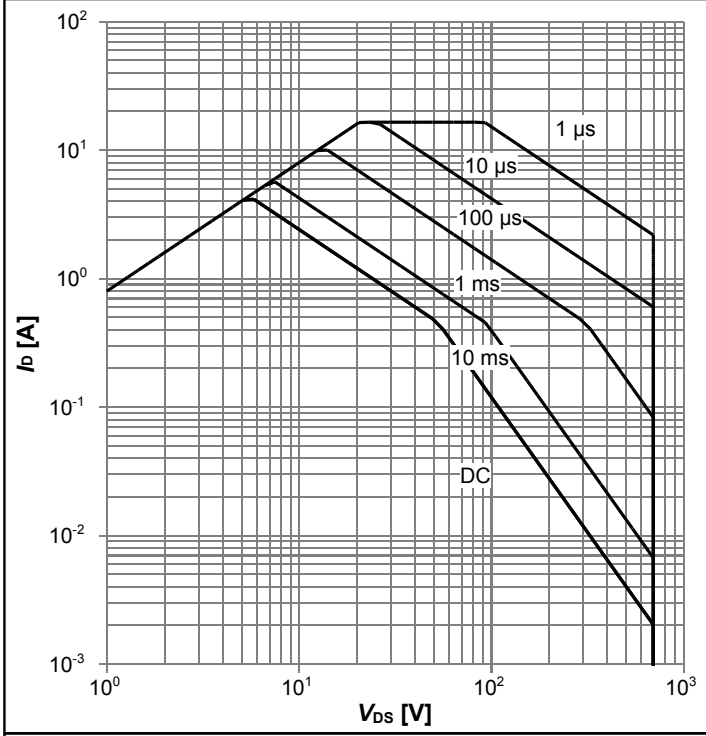
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



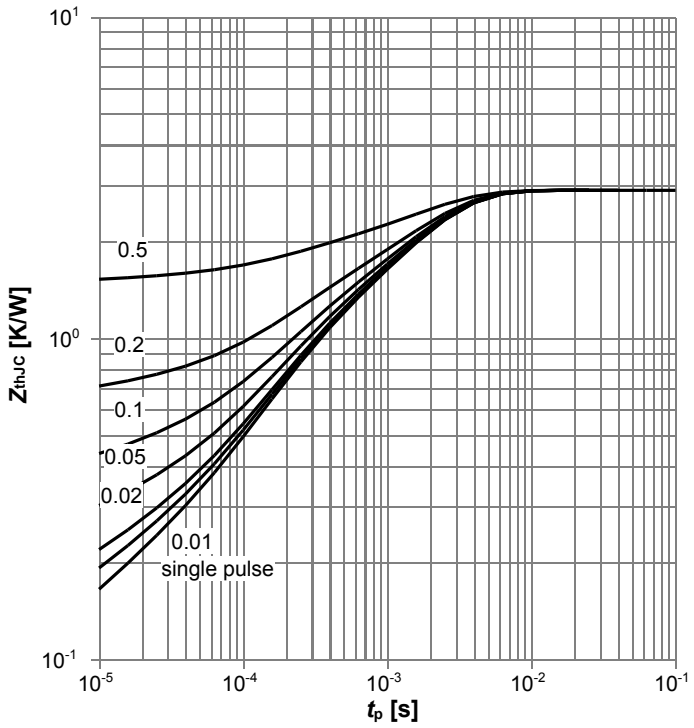
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 3: Safe operating area



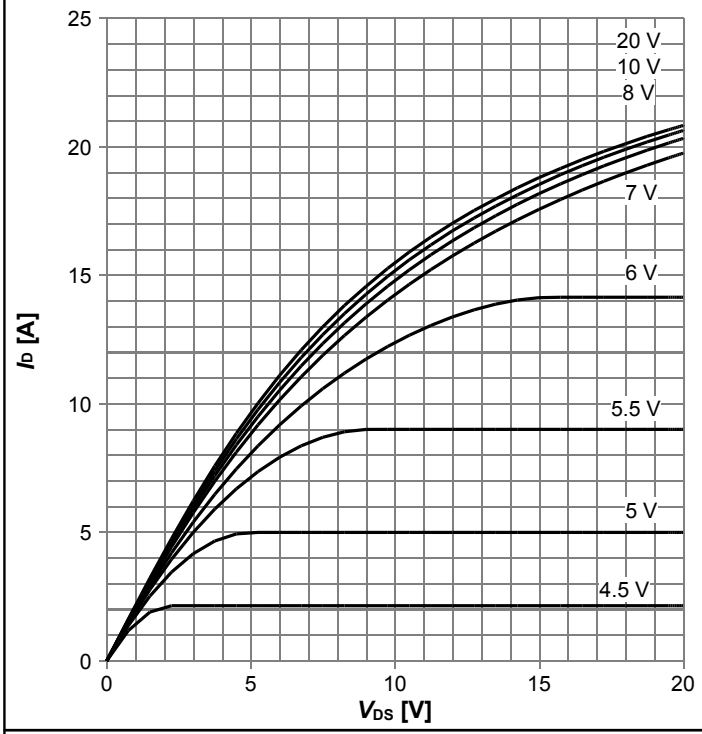
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



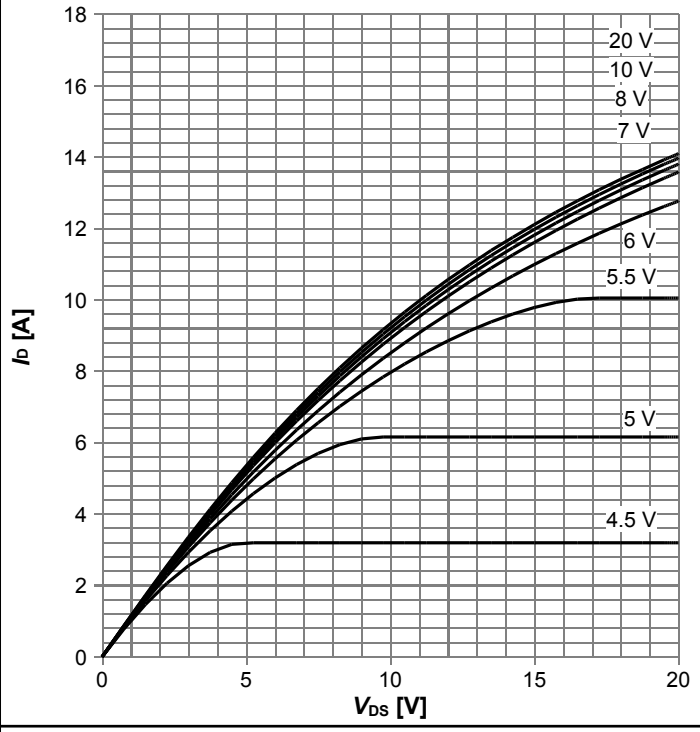
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



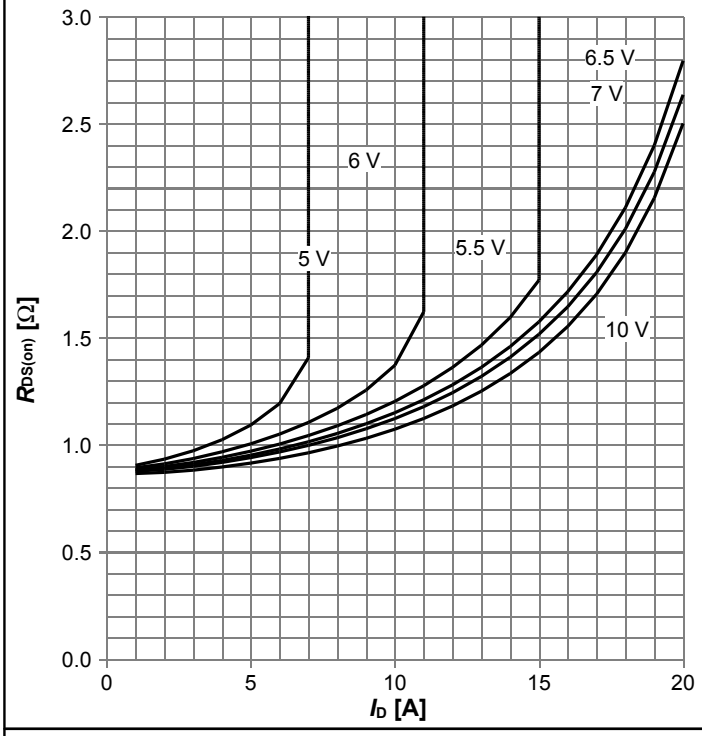
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



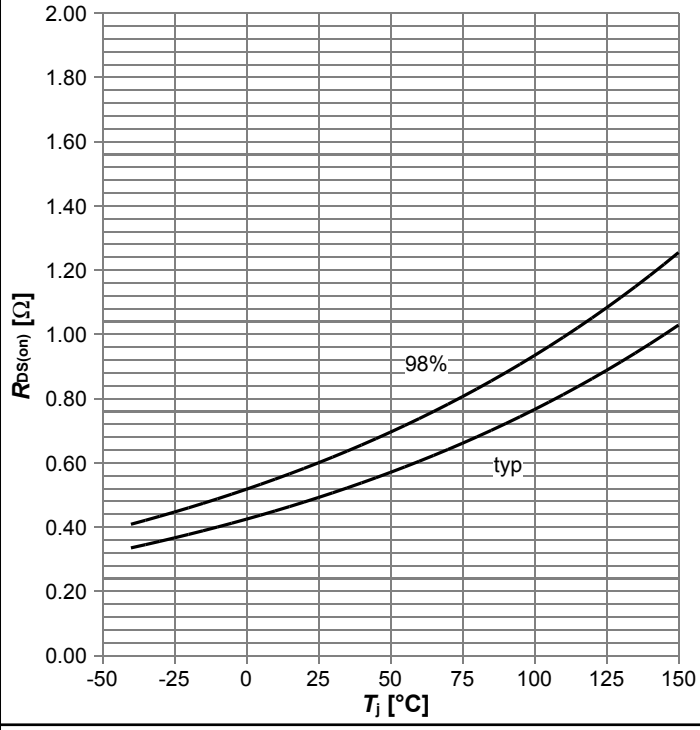
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



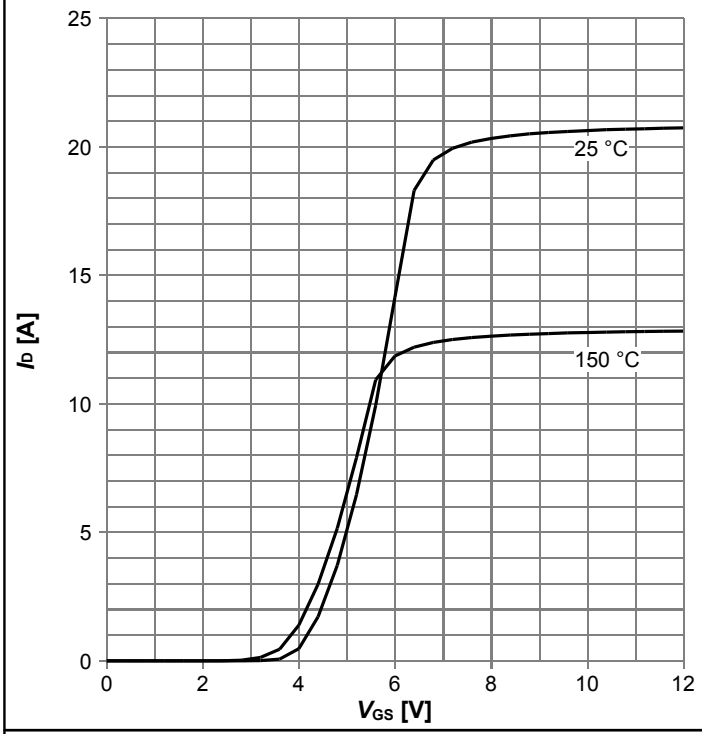
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



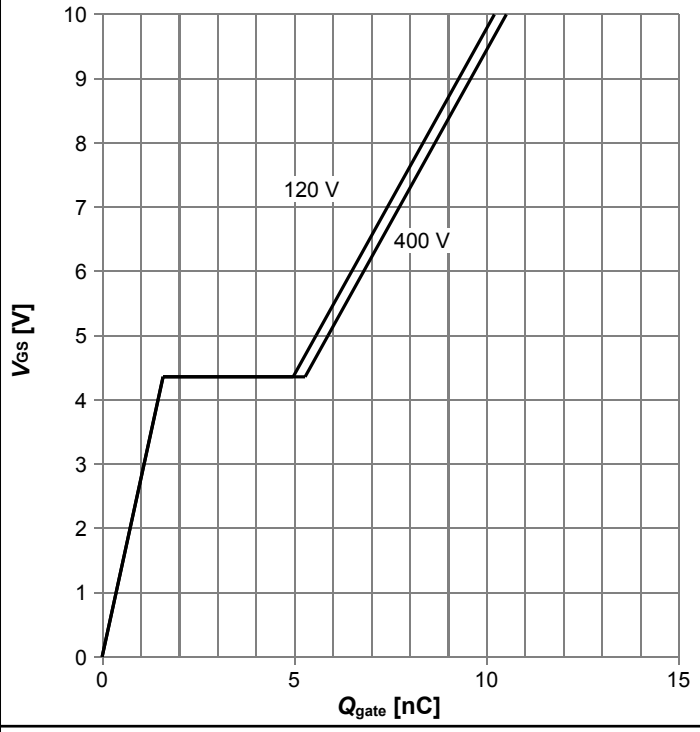
$R_{DS(on)}=f(T_j)$; $I_D=1.8$ A; $V_{GS}=10$ V

Diagram 9: Typ. transfer characteristics



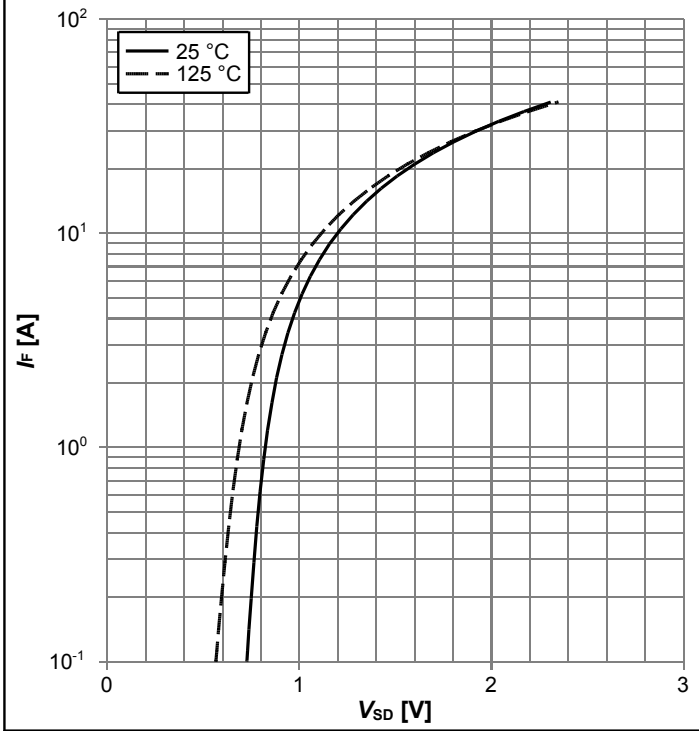
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



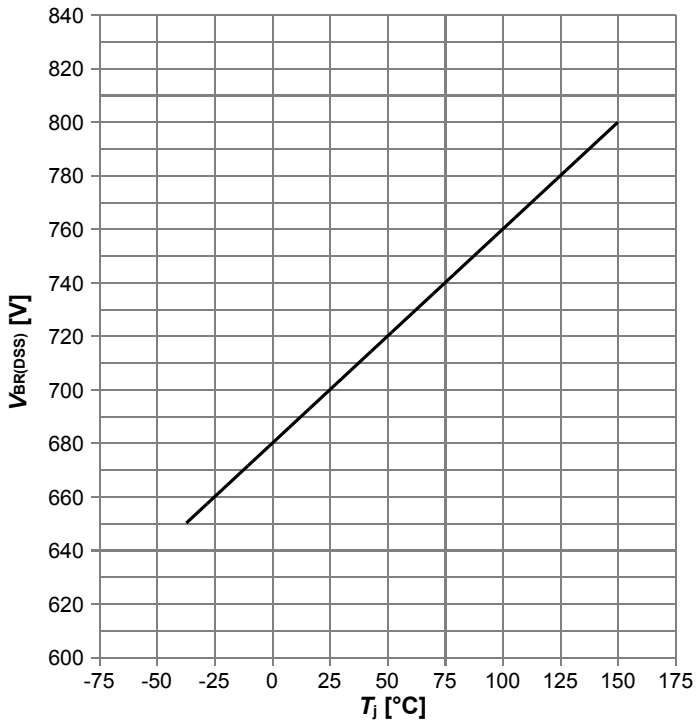
V_{GS}=f(Q_{gate}); I_D=1.4 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



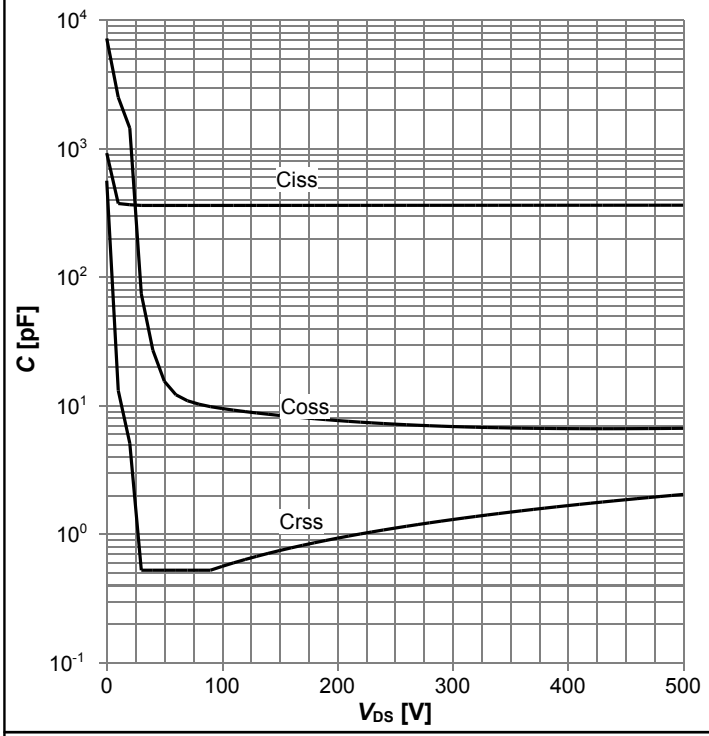
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Drain-source breakdown voltage



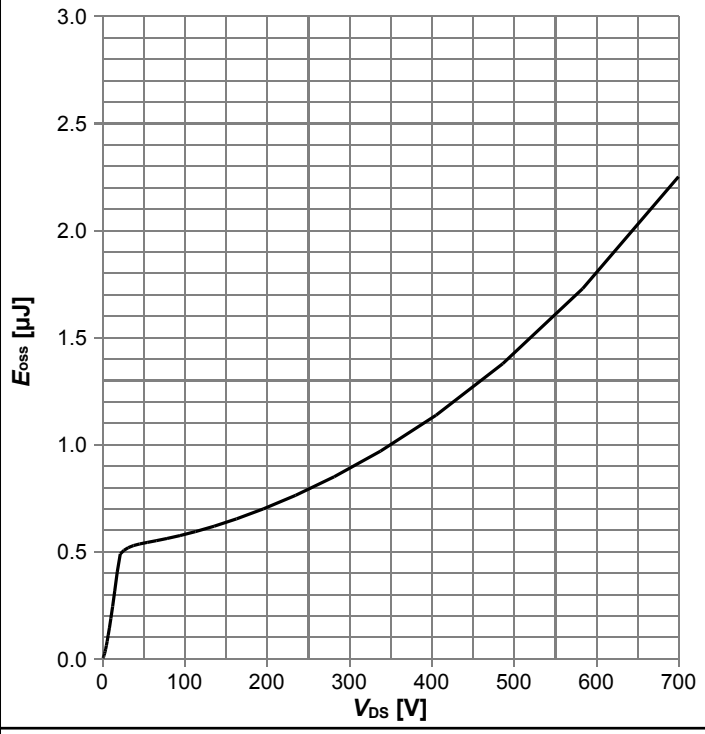
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

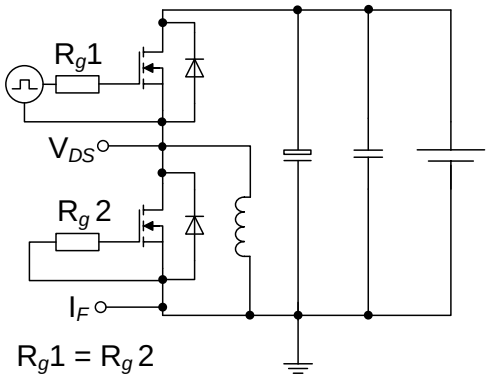
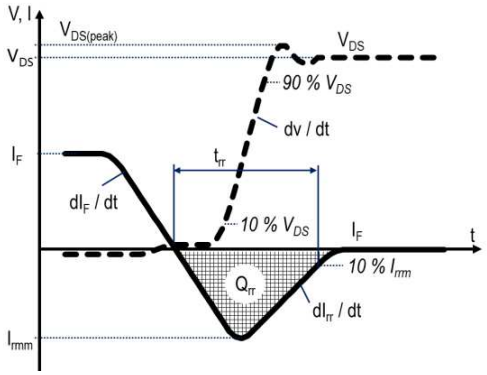
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

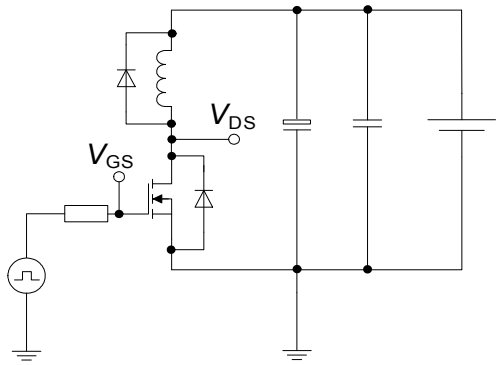
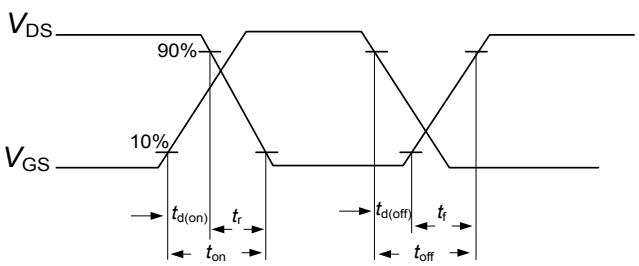
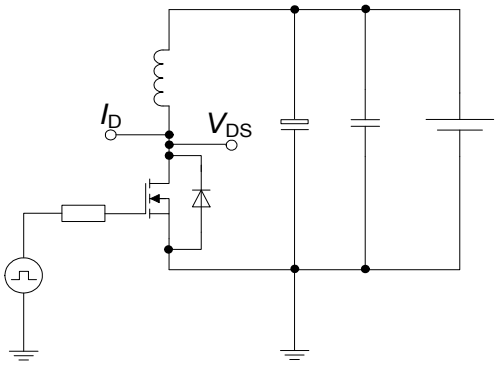
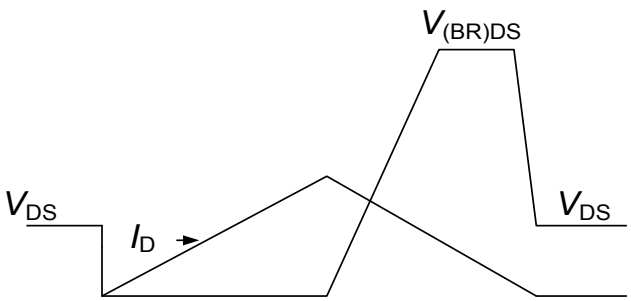
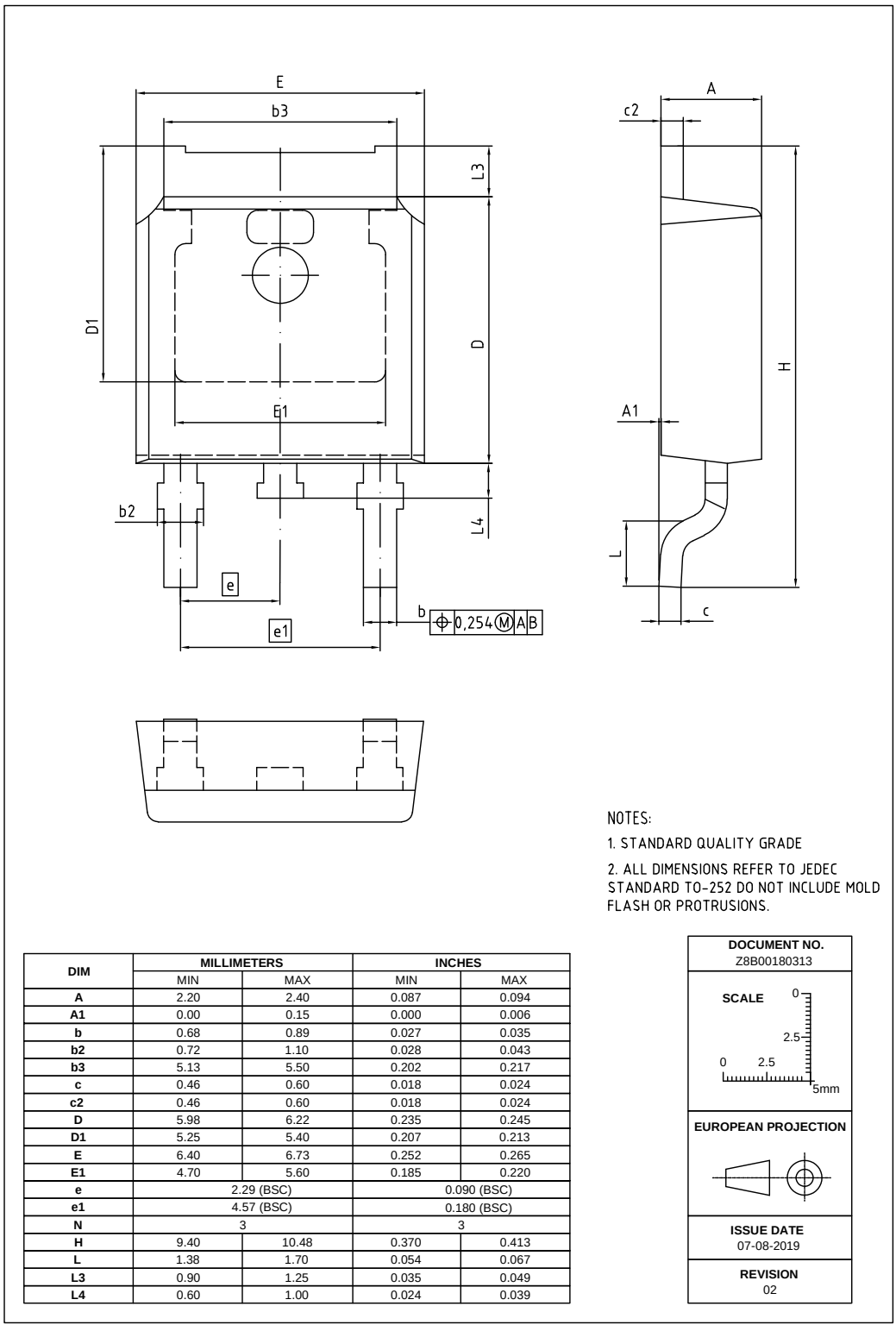
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
A1	0.00	0.15	0.000	0.006
b	0.68	0.89	0.027	0.035
b2	0.72	1.10	0.028	0.043
b3	5.13	5.50	0.202	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.60	0.018	0.024
D	5.98	6.22	0.235	0.245
D1	5.25	5.40	0.207	0.213
E	6.40	6.73	0.252	0.265
E1	4.70	5.60	0.185	0.220
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.38	1.70	0.054	0.067
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039

Figure 1 Outline PG-TO 252-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ P7 Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPD70R600P7S

Revision: 2019-08-09, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-10-11	Release of final version
2.1	2018-02-12	Corrected front page text
2.2	2019-08-09	Updated package outline

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