

RJK03M8DNS

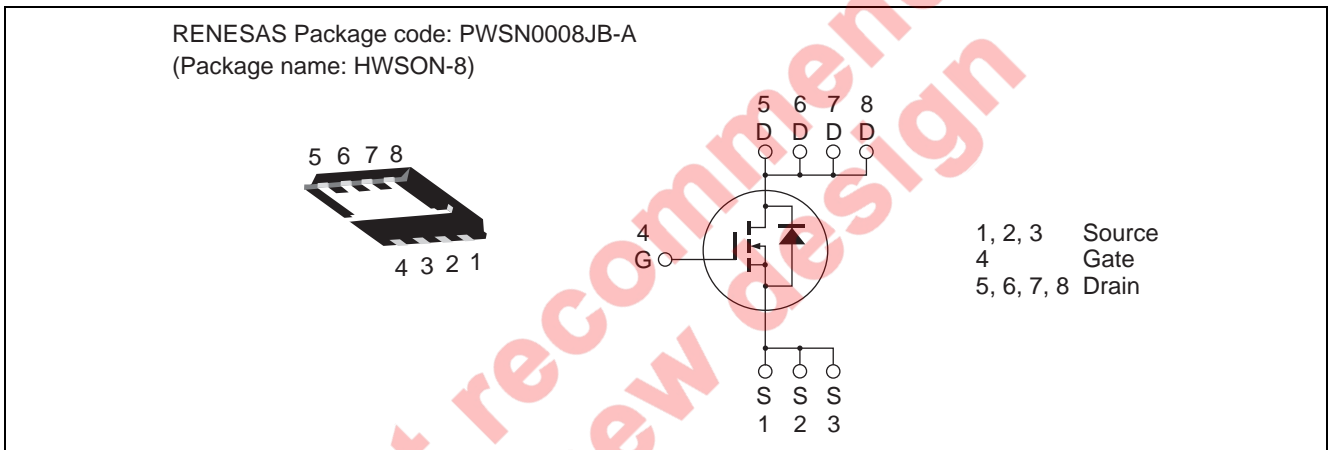
Silicon N Channel Power MOS FET
Power Switching

R07DS0774EJ0110
Rev.1.10
May 29, 2012

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 4.3 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	120	A
Body-drain diode reverse drain current	I_{DR}	30	A
Avalanche current	I_{AP} ^{Note 2}	13	A
Avalanche energy	E_{AS} ^{Note 2}	16.9	mJ
Channel dissipation	P_{ch} ^{Note 3}	20	W
Channel to case thermal impedance	θ_{ch-c} ^{Note 3}	6.25	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

Electrical Characteristics

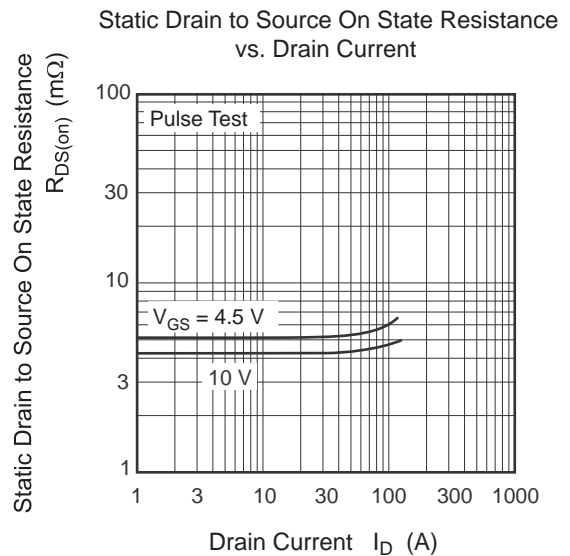
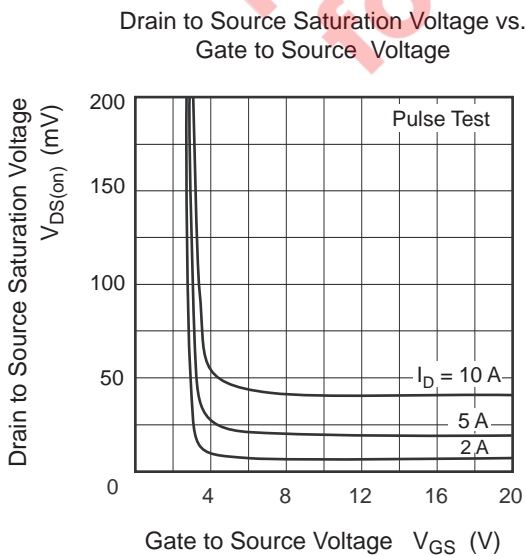
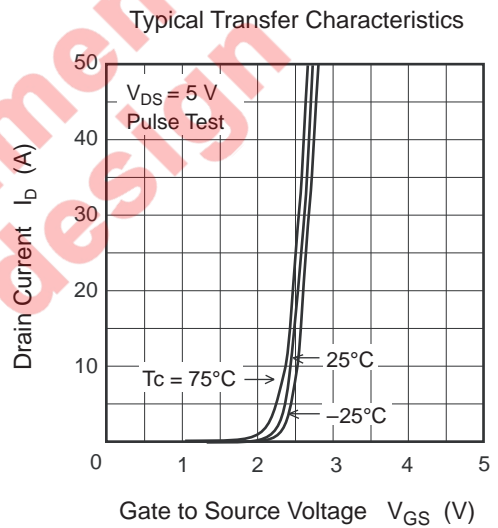
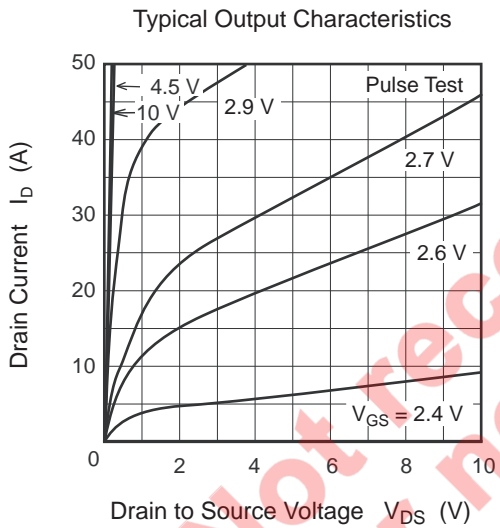
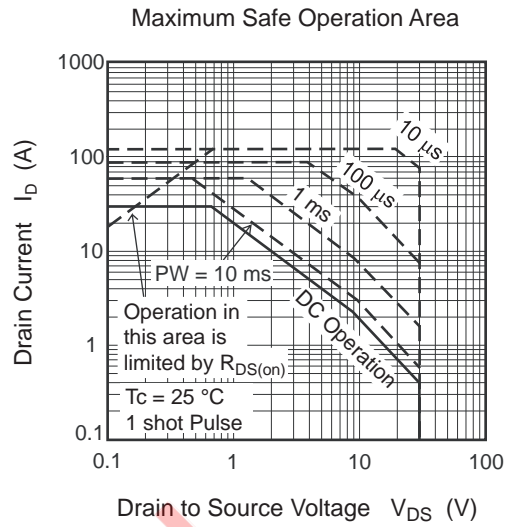
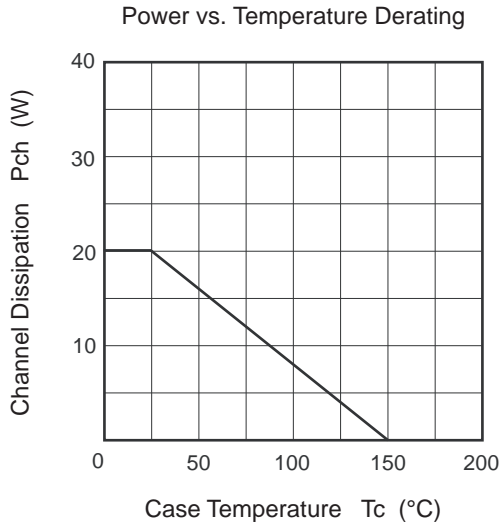
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.5	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 24 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.3	5.2	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	5.1	6.7	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	70	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1850	2590	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	290	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	150	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.5	3.0	Ω	
Total gate charge	Q_g	—	14.5	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	4.6	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	4.5	—	nC	$I_D = 16 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	4.2	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$
Rise time	t_r	—	3.6	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	30	—	ns	$R_L = 0.66 \Omega$
Fall time	t_f	—	9.0	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.84	1.09	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	9.3	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

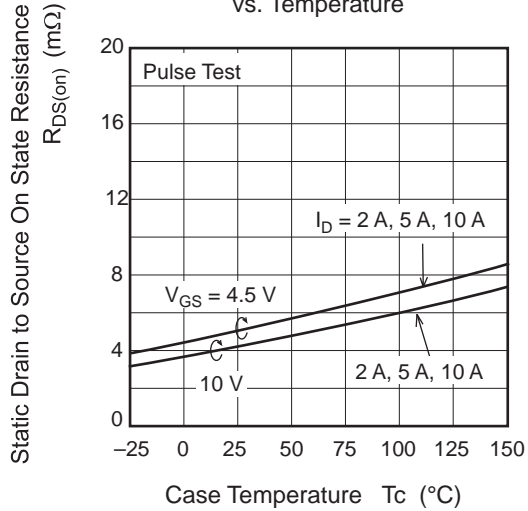
Notes: 4. Pulse test

Not recommended for new designs

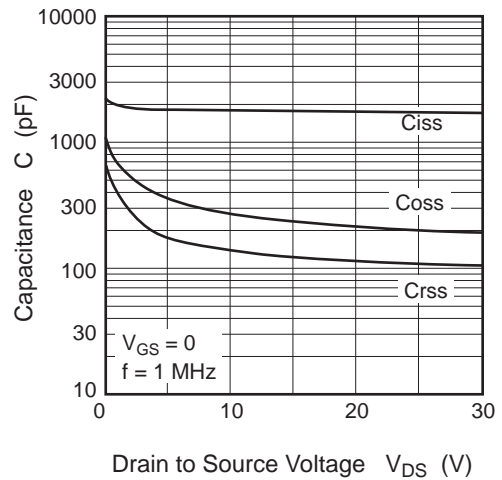
Main Characteristics



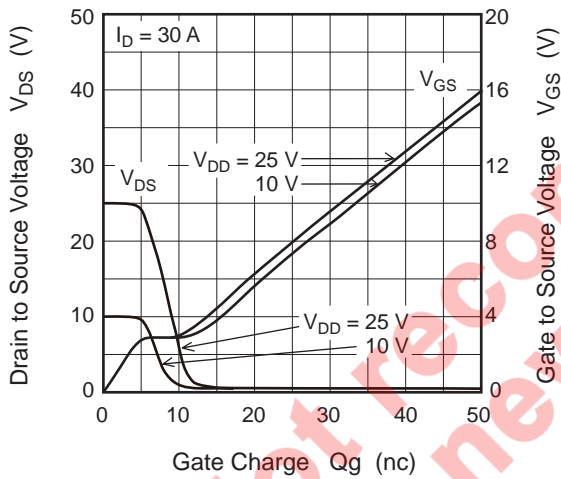
Static Drain to Source On State Resistance vs. Temperature



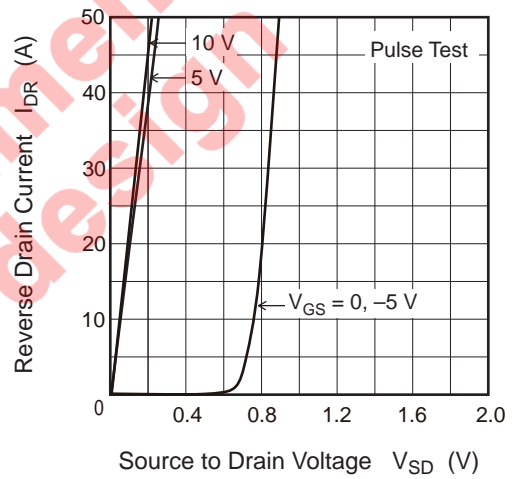
Typical Capacitance vs. Drain to Source Voltage



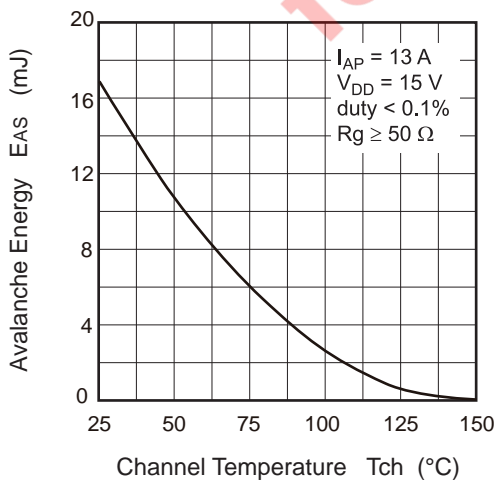
Dynamic Input Characteristics



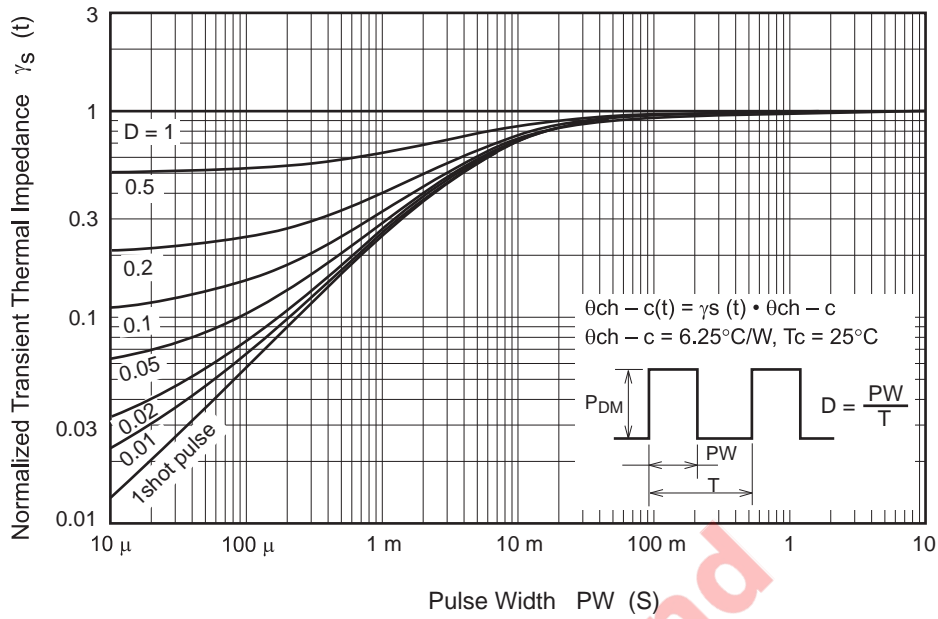
Reverse Drain Current vs. Source to Drain Voltage



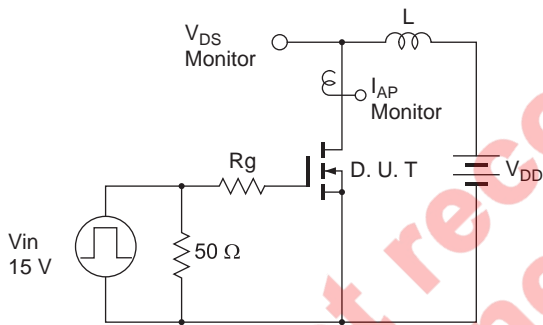
Maximum Avalanche Energy vs. Channel Temperature Derating



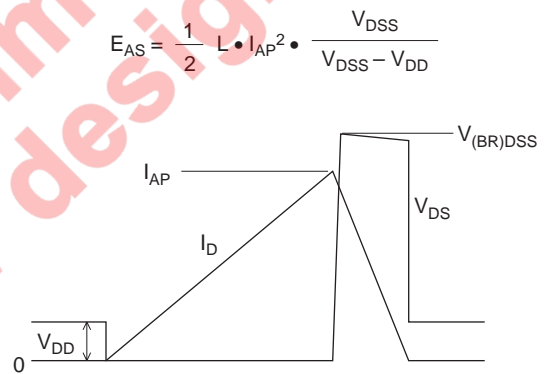
Normalized Transient Thermal Impedance vs. Pulse Width



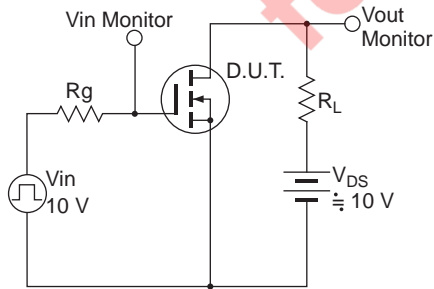
Avalanche Test Circuit



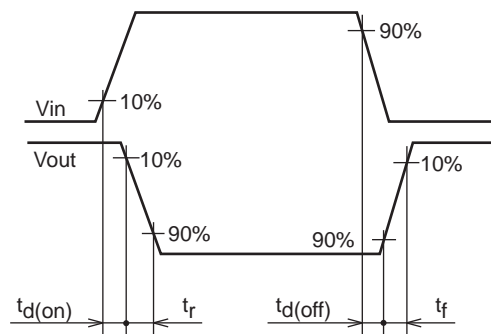
Avalanche Waveform



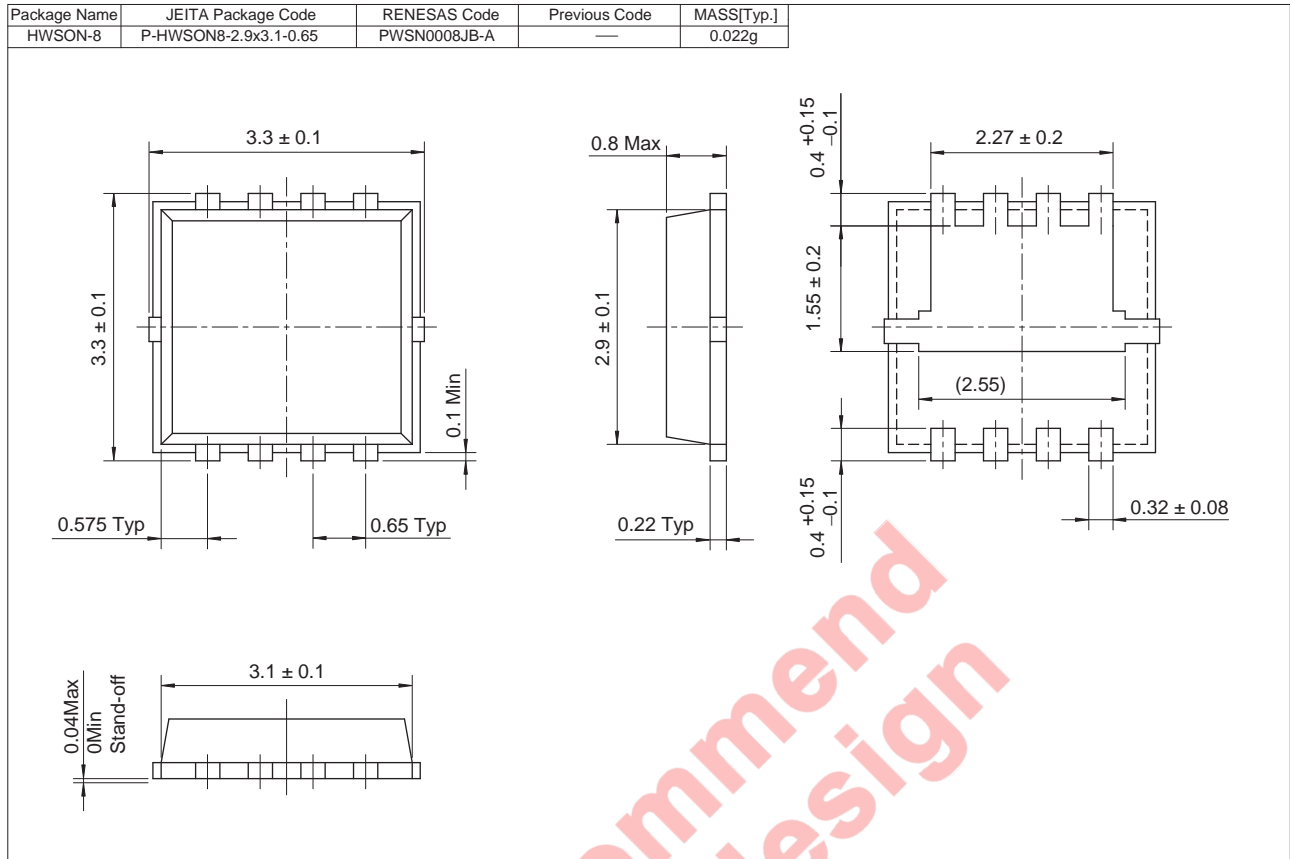
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03M8DNS-00-J5	5000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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