NP29N04QUK

40 V – 30 A – Dual N-channel Power MOS FET Application: Automotive

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Rev. 2.00
May 24, 2018

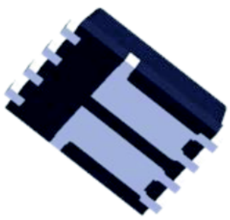
Description

NP29N04QUK is a dual N-channel MOS Field Effect Transistor designed for high current switching applications.

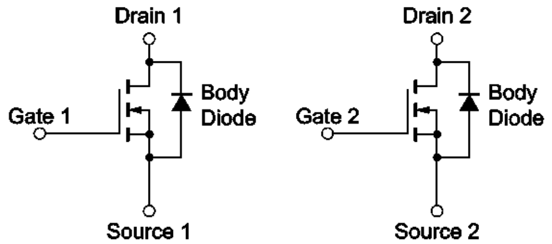
Features

- Super low on-state resistance
  — $R_{DS(on)}$ = 10.1 mΩ MAX. (V_{GS} = 10 V, I_D = 15 A)
- Low C_{iss}: C_{iss} = 1000 pF TYP. (V_{DS} = 25 V)
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON dual

Outline



8-pin HSON dual



Equivalent circuit

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Packing		Package
NP29N04QUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON dual
NP29N04QUK -E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C) *4	$I_{D(DC)}$	±30	A
Drain Current (pulse) *1, 4, 5	$I_{D(pulse)}$	±60	A
Total Power Dissipation (T_C = 25°C) *4	P_{T1}	44	W
Total Power Dissipation (T_A = 25°C) *2, 4	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	−55 to +175	°C
Repetitive Avalanche Current *3, 5	I_{AR}	17	A
Repetitive Avalanche Energy *3, 5	E_{AR}	30	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *5	3.37	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$ *5	150	°C/W

Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on glass epoxy substrate of 40 mm × 40 mm × 1.6 mmt with 4% copper area (35 μm)
*3. R_G = 25 Ω, V_{GS} = 20 V → 0 V
*4. One channel operation
*5. Not subject of production test. Verified by design/characterization.

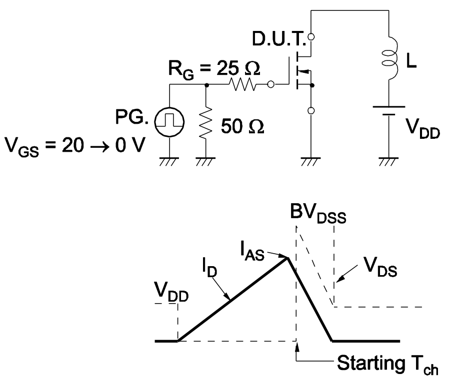
Electrical Characteristics (T_A = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	| y_{fs} |	10	17		S	V_{DS} = 5 V, I_D = 15 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		8.5	10.1	mΩ	V_{GS} = 10 V, I_D = 15 A
Input Capacitance *2	C_{iss}		1000	1500	pF	V_{DS} = 25 V,
Output Capacitance *2	C_{oss}		150	230	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance *2	C_{rss}		70	130	pF	f = 1 MHz
Turn-on Delay Time *2	$t_{d(on)}$		14	28	ns	V_{DD} = 20 V, I_D = 15 A,
Rise Time *2	t_r		4	10	ns	V_{GS} = 10 V,
Turn-off Delay Time *2	$t_{d(off)}$		30	60	ns	R_G = 0 Ω
Fall Time *2	t_f		6	15	ns	
Total Gate Charge *2	Q_G		19	29	nC	V_{DD} = 32 V,
Gate to Source Charge	Q_{GS}		6		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		5		nC	I_D = 30 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I_F = 30 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		30		ns	I_F = 30 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		31		nC	di/dt = 100 A/μs

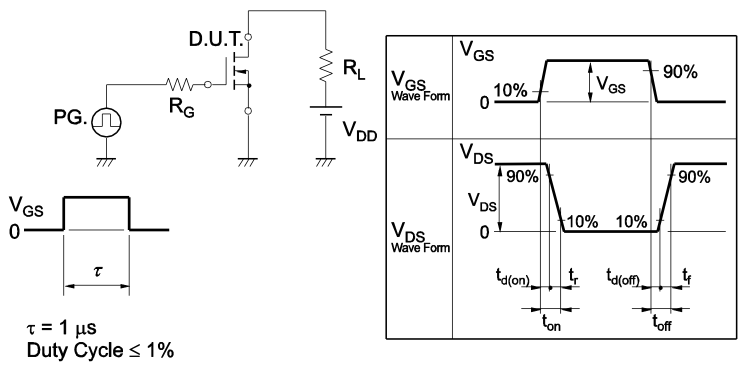
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

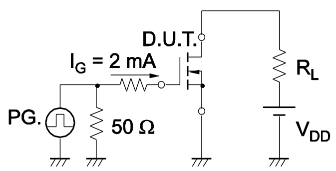
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

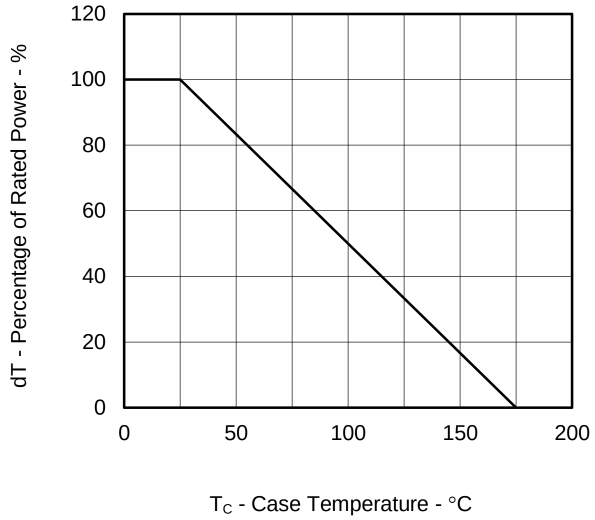


TEST CIRCUIT 3 GATE CHARGE

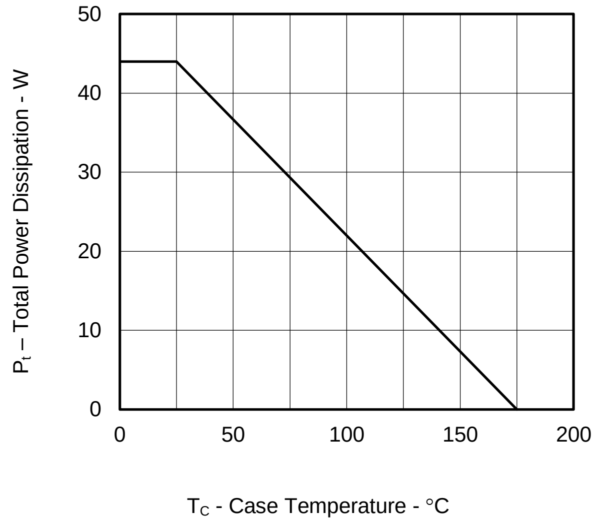


Typical Characteristics (T_A = 25°C)

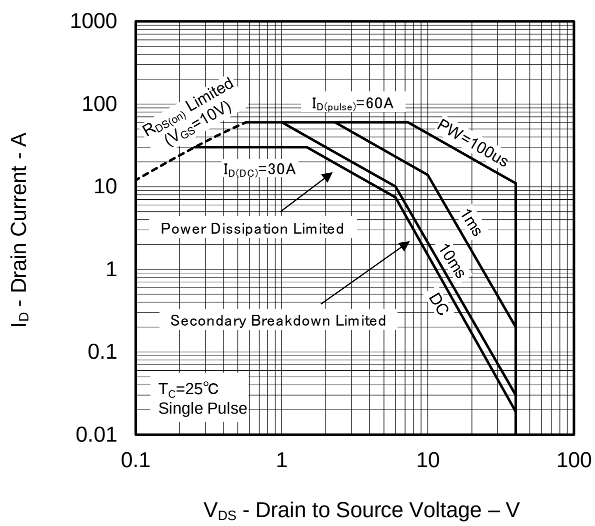
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



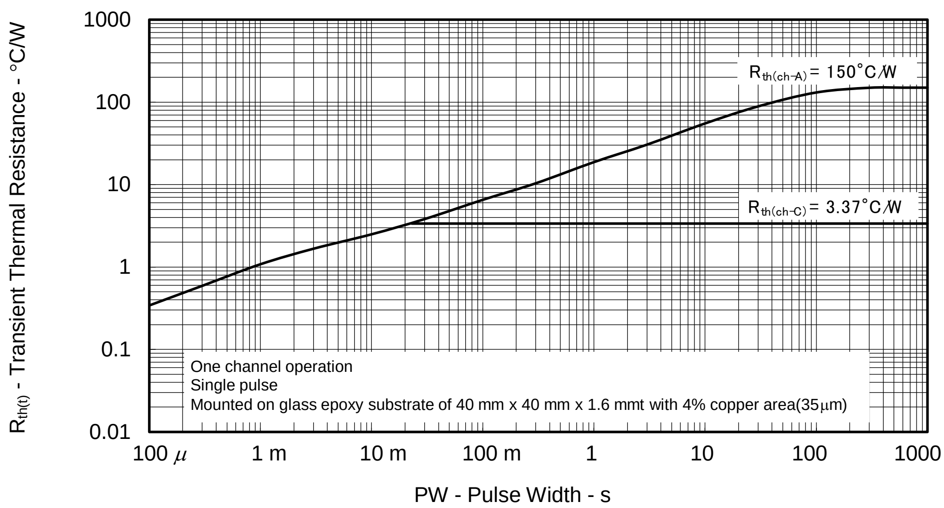
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



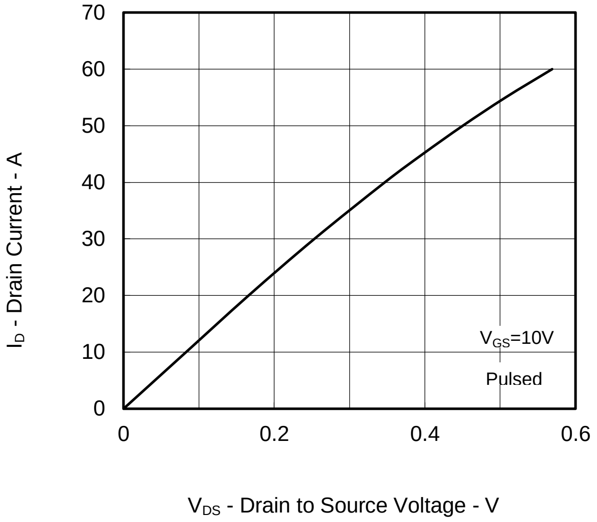
FORWARD BIAS SAFE OPERATING AREA



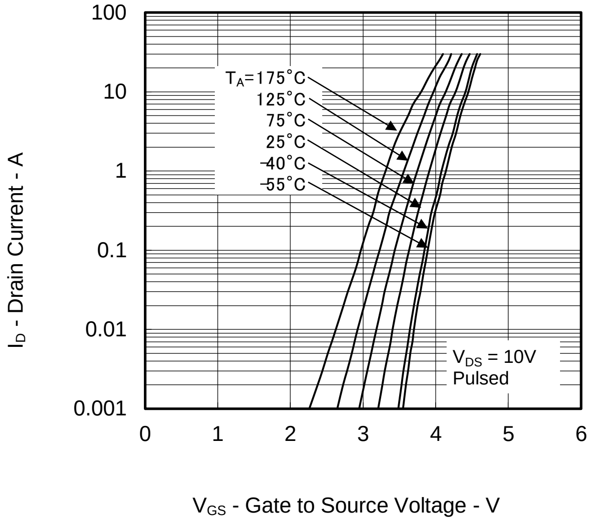
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



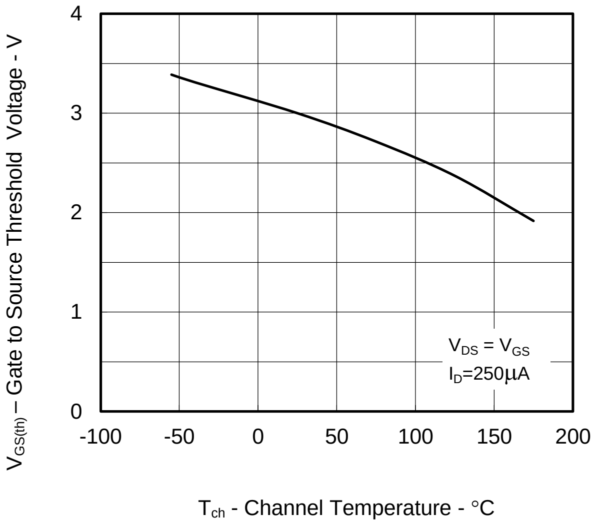
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



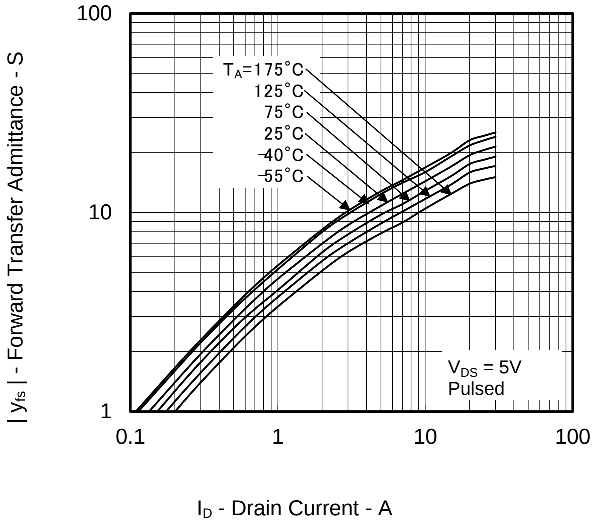
FORWARD TRANSFER CHARACTERISTICS



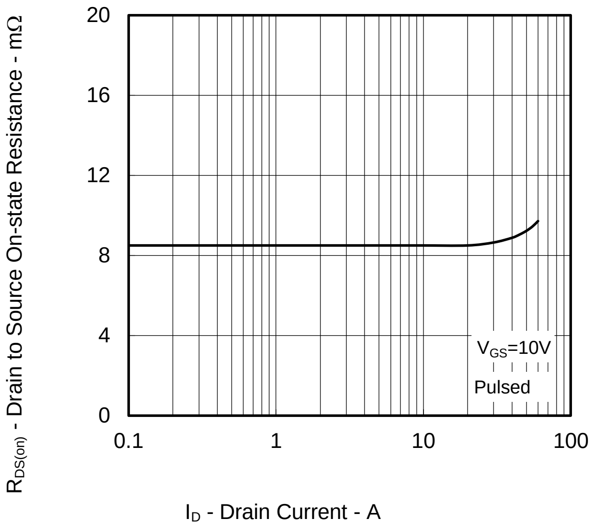
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



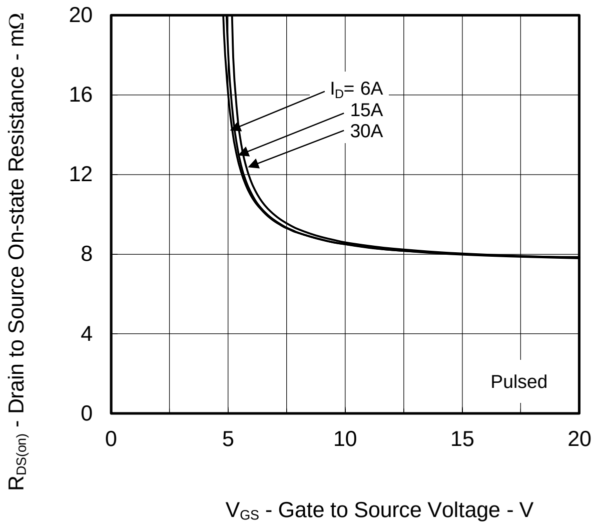
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



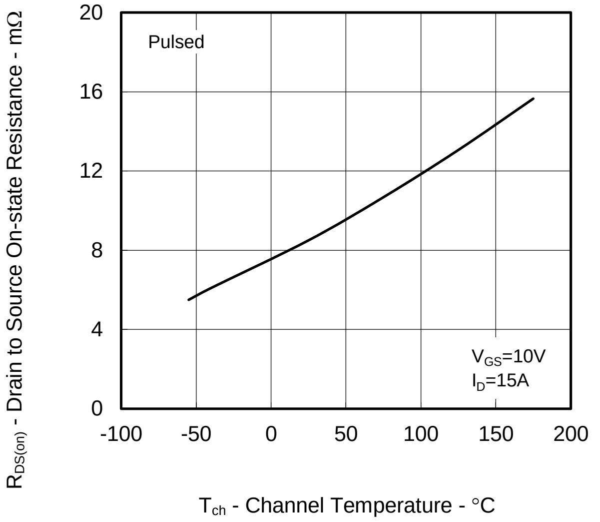
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



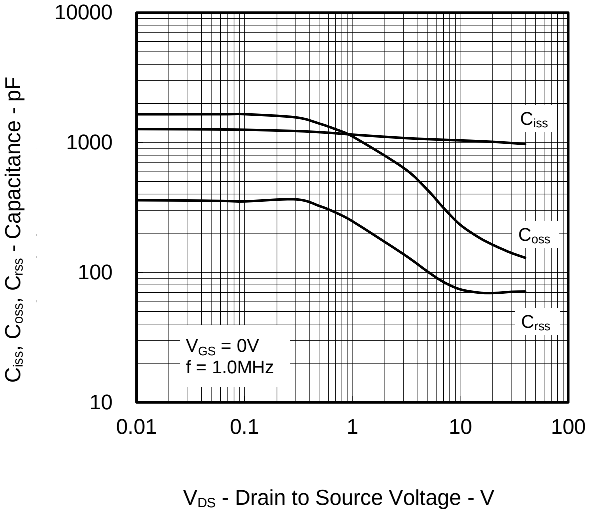
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



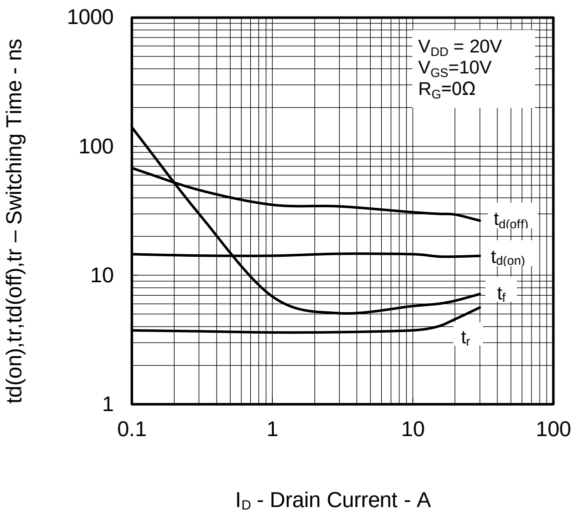
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



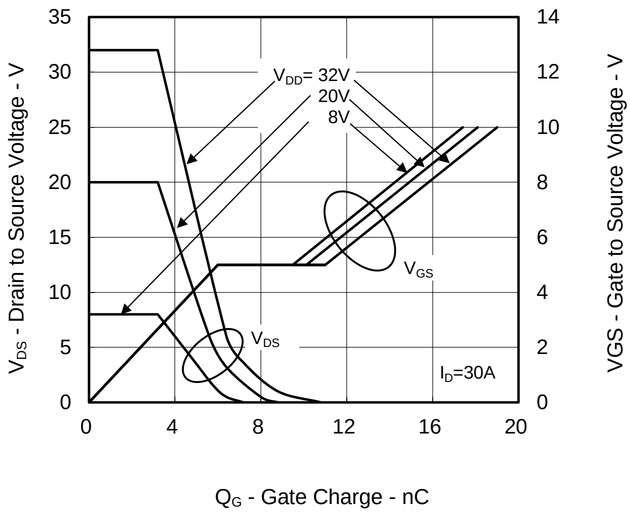
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



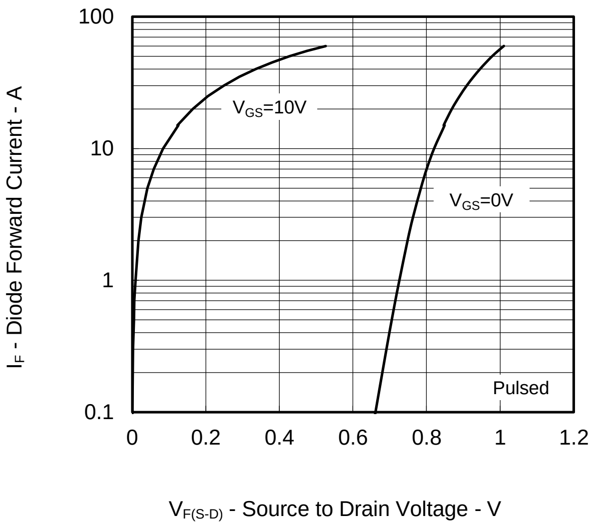
SWITCHING CHARACTERISTICS



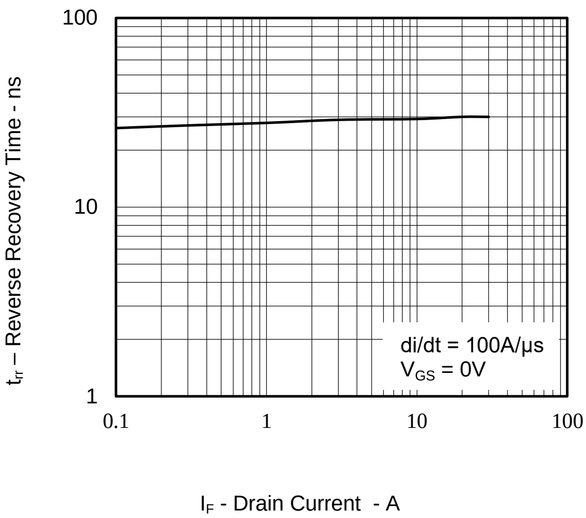
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



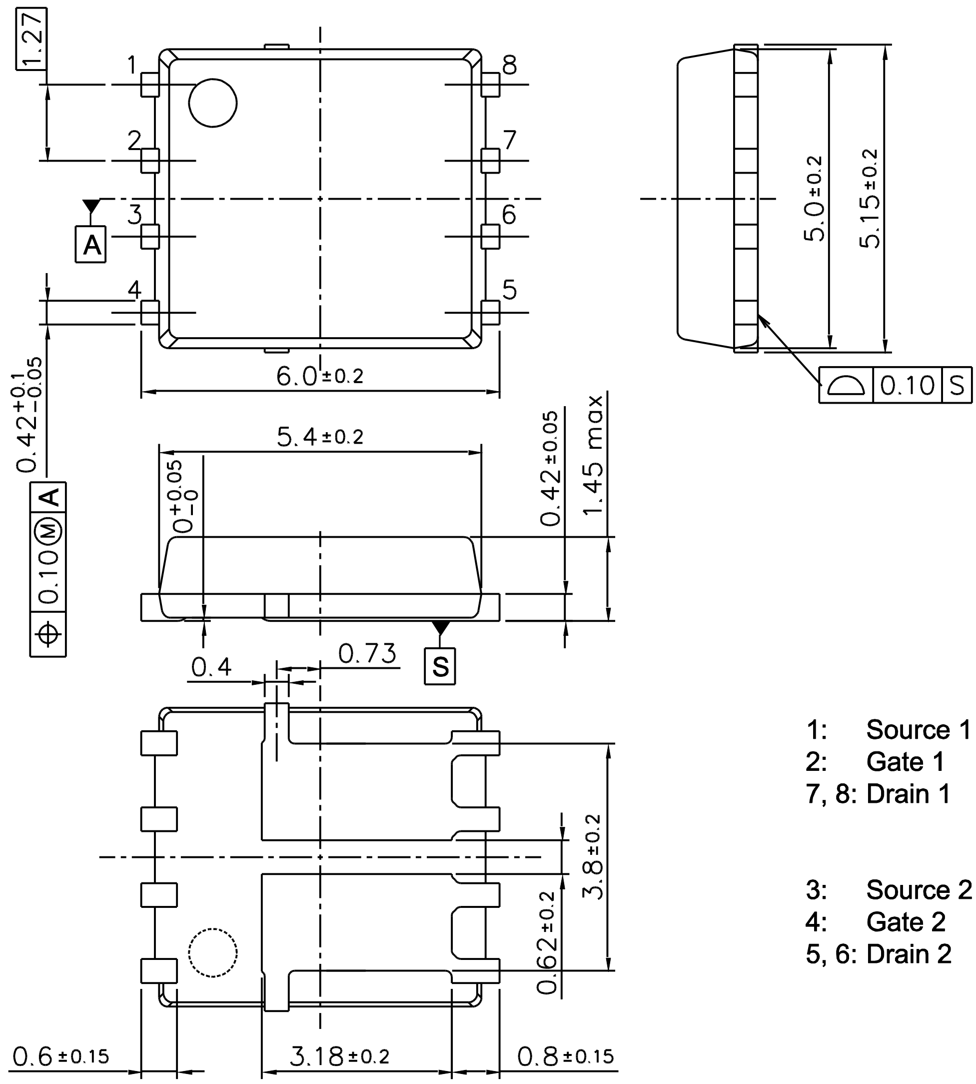
REVERSE RECOVERY TIME vs. DRAIN CURRENT



Package Drawings (Unit: mm)

8-pin HSON Dual (Mass: 0.12 g TYP.)

Renesas package code: PLSN0008DA-A



1: Source 1
2: Gate 1
7, 8: Drain 1

3: Source 2
4: Gate 2
5, 6: Drain 2

Revision History	NP29N04QUK Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar 28, 2016	—	First Edition Issued
2.00	May 24,2018	2	Note 5 was added
		3	Note 2 was added

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