HARRIS

IRFD9120
IRFD9123

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -1.0A and -0.8A, -80V and -100V
- $r_{DS(ON)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

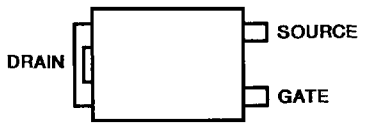
Description

The IRFD9120 and IRFD9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

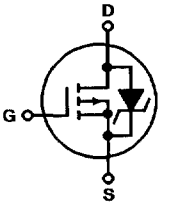
Package

4-PIN DUAL-IN-LINE
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9120	IRFD9123	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-80	V
Continuous Drain Current T_C = 25°C	I_D	-1.0	-0.8	A
Pulsed Drain Current (3)	I_{DM}	-8.0	-6.4	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	370	370	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

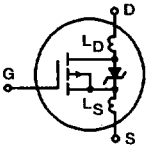
NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 555mH, R_G = 25Ω, Peak I_L = 1.0A (See Figures 14 and 15)

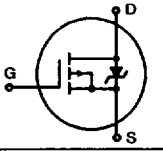
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2285.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9120	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFD9123			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9120	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-1.0	-	-	A
IRFD9123			-0.8	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9120	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.8A	-	0.5	0.6	Ω
IRFD9123			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} < 50V, I_D = -0.8A	0.8	1.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 1.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -1.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	20	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-1.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -1.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	150	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	0.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 555mH, R_G = 25Ω, Peak I_L = 1.0A (See Figures 14 and 15)

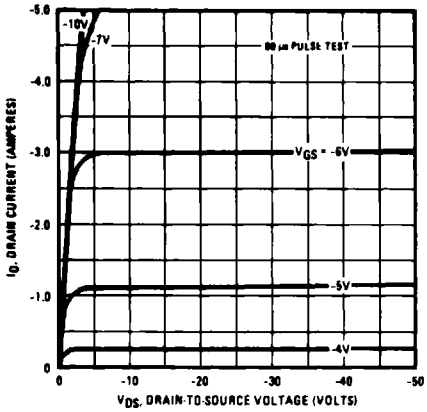


Fig. 1 - Typical output characteristics.

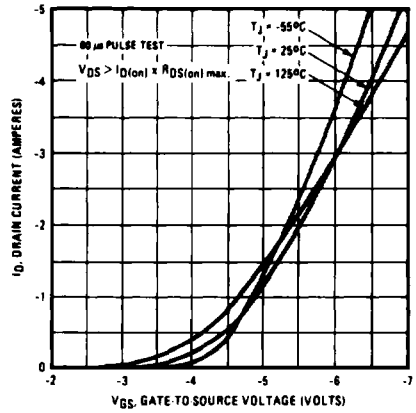


Fig. 2 - Typical transfer characteristics.

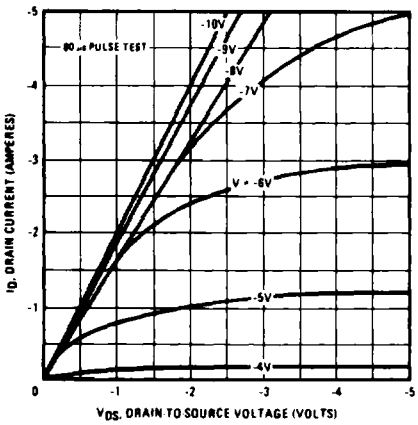


Fig. 3 - Typical saturation characteristics.

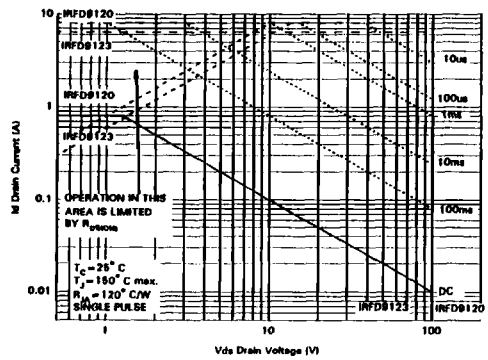


Fig. 4 - Maximum safe operating area.

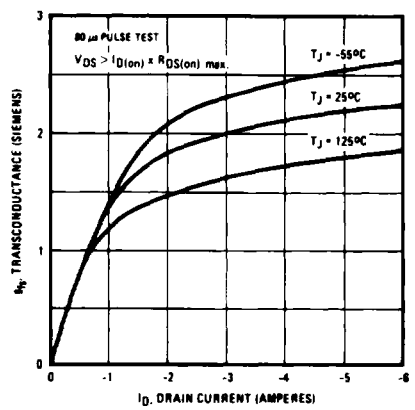


Fig. 5 - Typical transconductance vs. drain current.

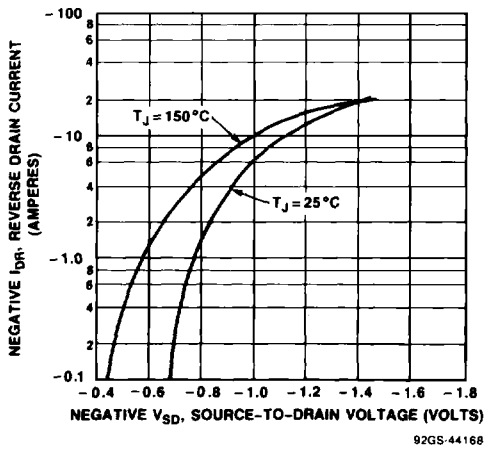


Fig. 6 - Typical source-drain diode forward voltage.

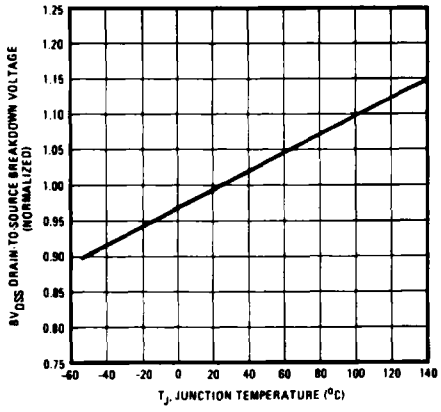


Fig. 7 - Breakdown voltage vs. temperature.

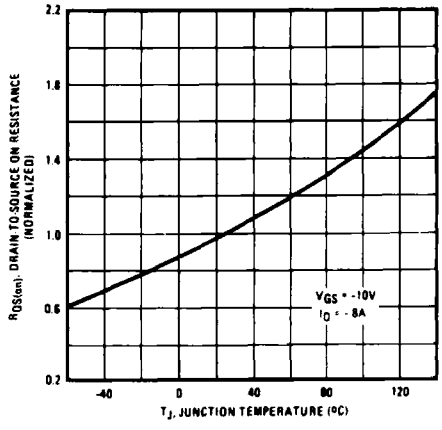


Fig. 8 - Normalized on-resistance vs. temperature.

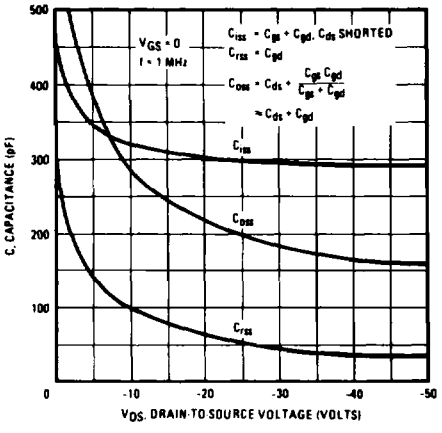


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

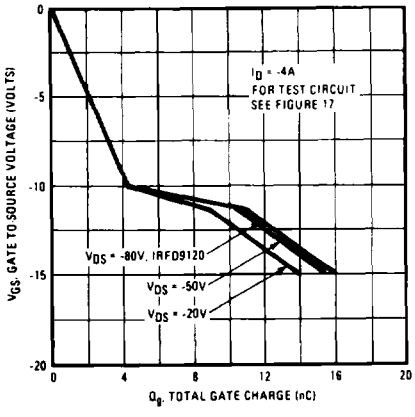


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

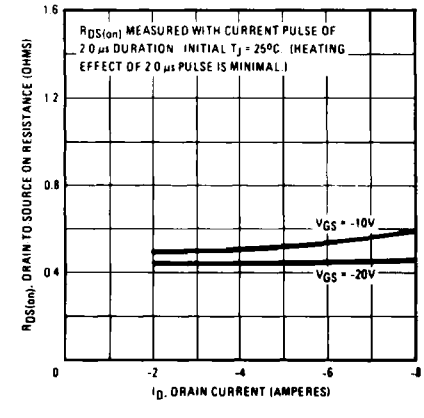


Fig. 11 - Typical on-resistance vs. drain current.

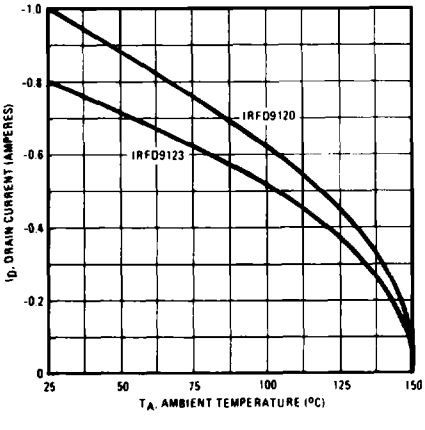


Fig. 12 - Maximum drain current vs. case temperature.

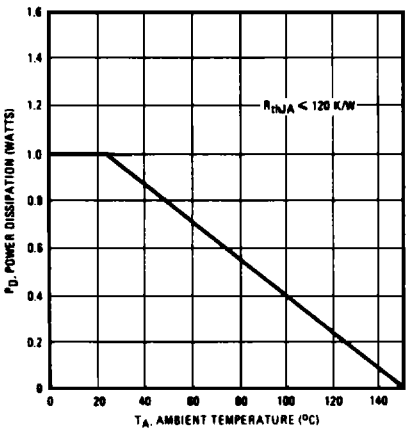


Fig. 13 - Power vs. temperature derating curve.

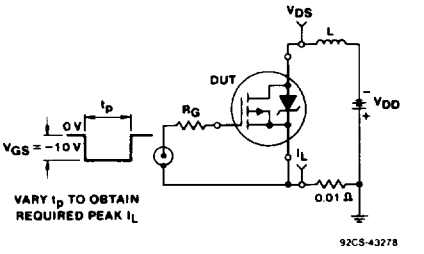


Fig. 14 - Unclamped inductive test circuit.

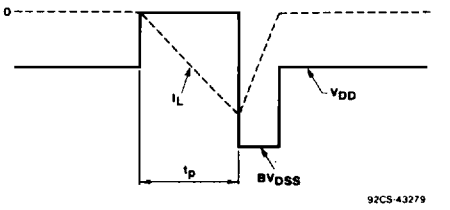


Fig. 15 - Unclamped inductive waveforms.

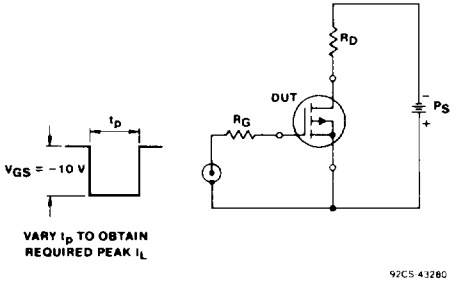


Fig. 16 - Switching time test circuit.

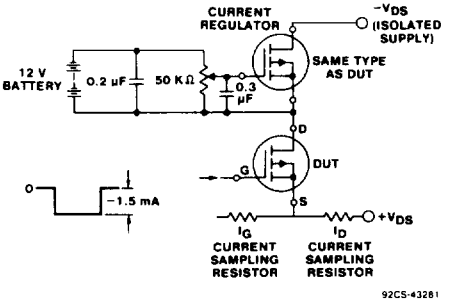


Fig. 17 - Gate charge test circuit.