FINAL | COM'L: -12/15/20 | MIL: -20

MACH110-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 12 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 66.7 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 38 Inputs
- 32 Outputs
- 32 Flip-flops; 2 clock choices
- 2 "PAL22V16" Blocks
- Pin-compatible with MACH210, MACH215

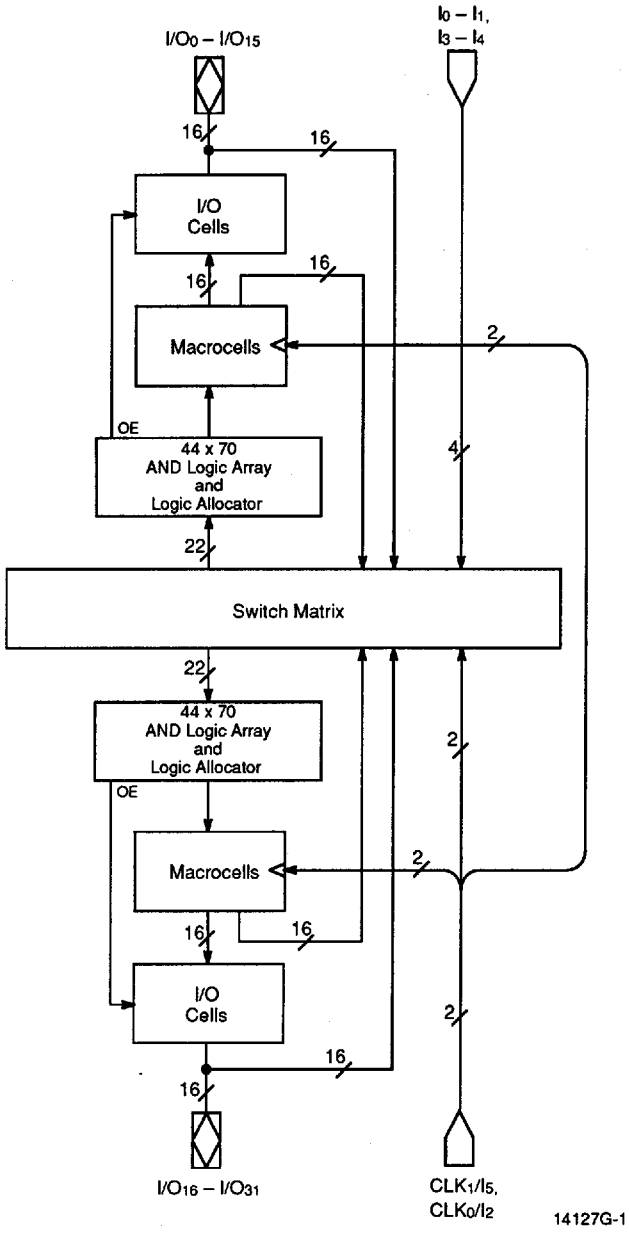
GENERAL DESCRIPTION

The MACH110 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 with no loss of speed.

The MACH110 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

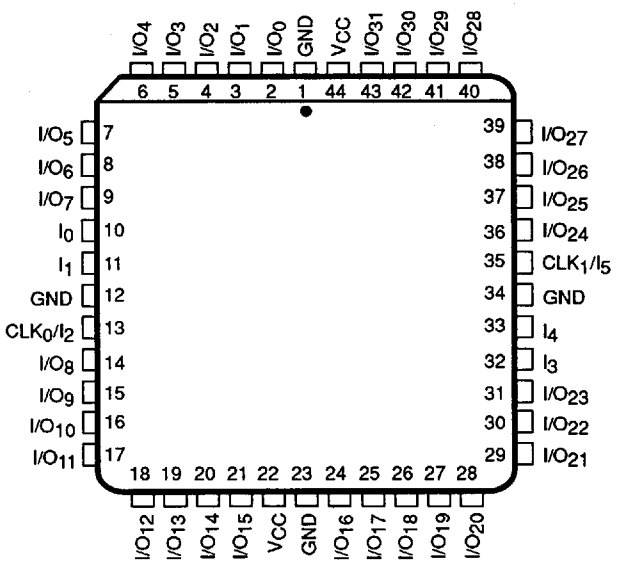
The MACH110 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View

PLCC/CQFP



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Note:
Pin-compatible with MACH210, MACH215.

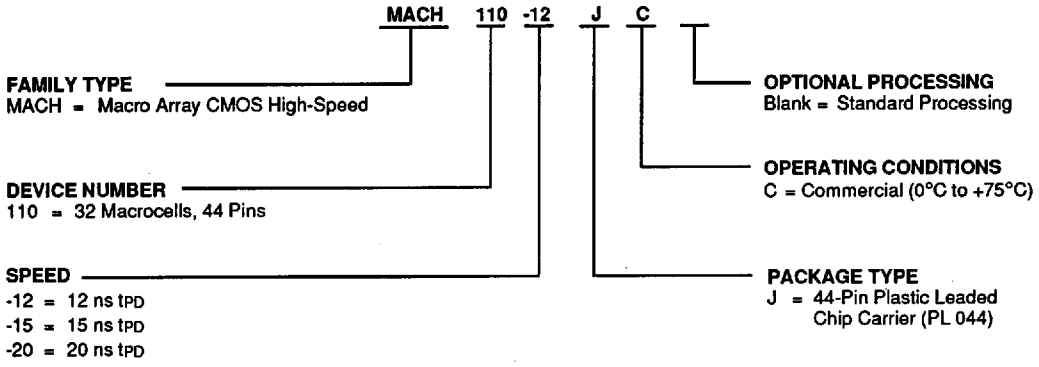
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH110-12 MACH110-15 MACH110-20	JC

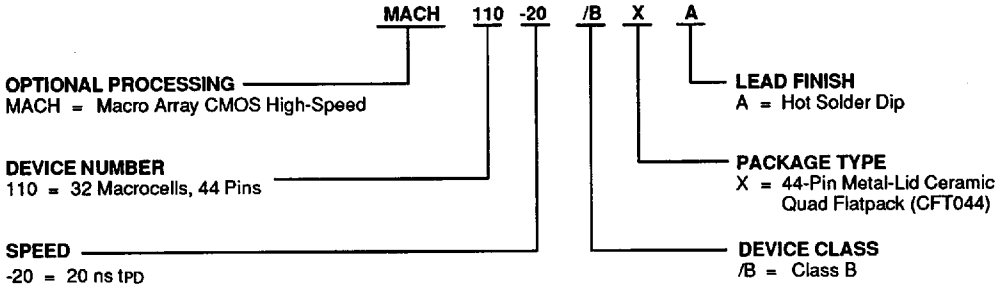
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations
MACH110-20/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH110 consists of two PAL blocks connected by a switch matrix. There are 32 I/O pins and 6 dedicated input pins feeding the switch matrix. These signals are distributed to the two PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH110 (Figure 8) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH110 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH110 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH110 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 5 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 8 for cluster and macrocell numbers.

Table 5. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7
M_8	C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

The MACH110 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH110 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

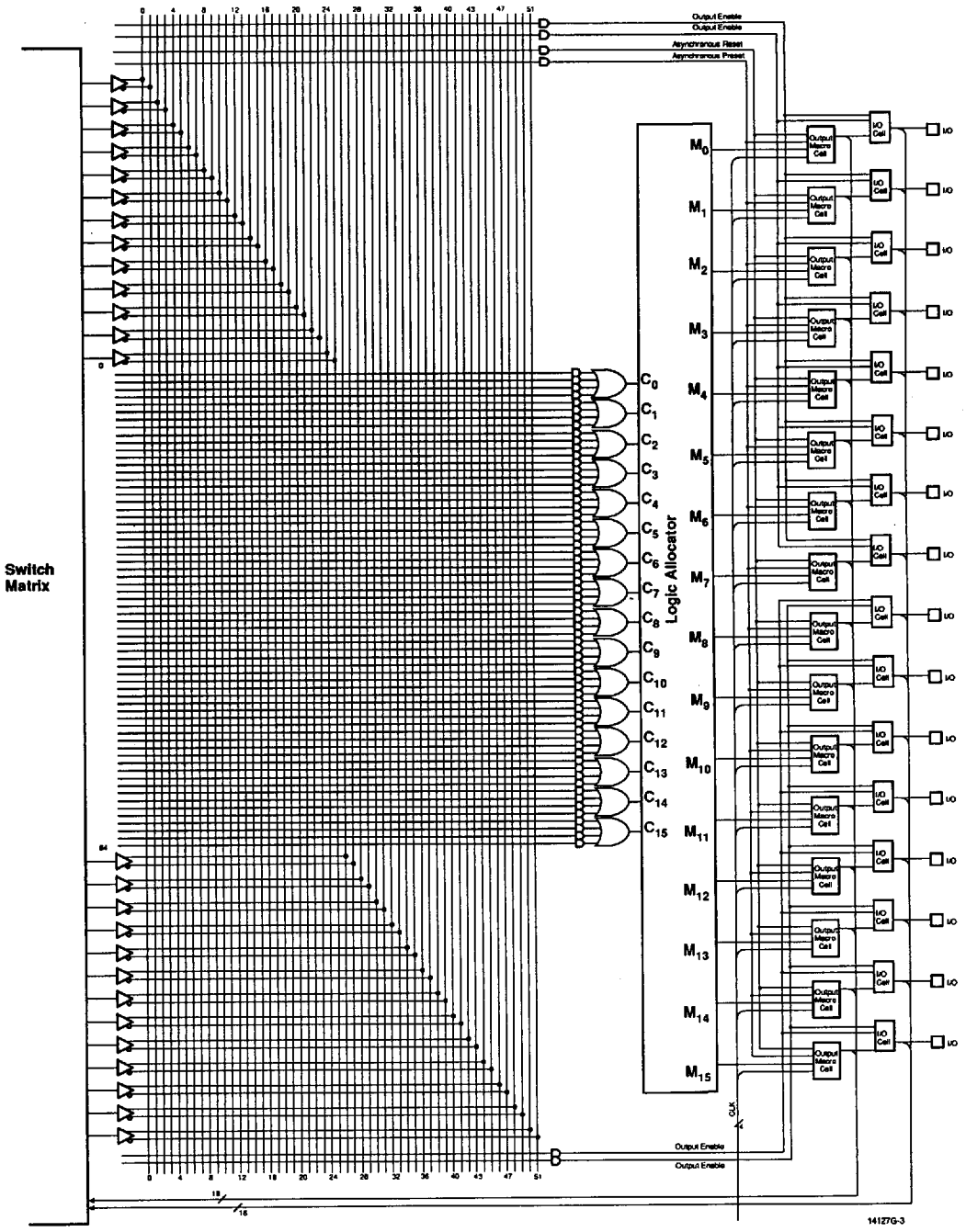


Figure 8. MACH110 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 75°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 0 MHz (Note 4)		150	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.9		66.6		47.6		MHz
				T-type	71.4		55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				8		10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					12		15		20	ns

Notes:

2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature
With Power Applied ..... −55°C to +125°C

Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = −55°C to 125°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A)
Operating in Free Air ..... −55°C to +125°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.5 V to +5.5 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		−40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	−30	−200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 0 MHz (Note 6)		170	mA

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.*
6. *This parameter is guaranteed worst case. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

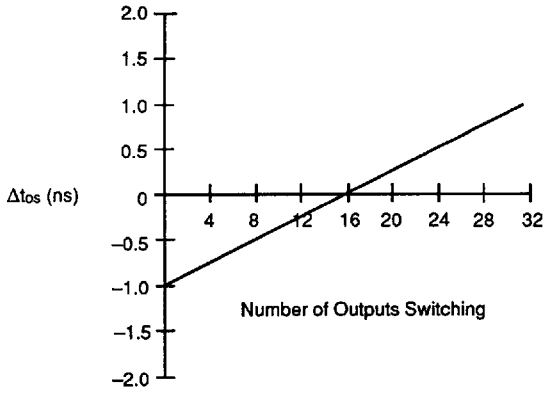
Parameter Symbol	Parameter Description				-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback (f_{CNT})		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{AP}	Asynchronous Preset to Registered Output					25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				20		ns
t_{APR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					20	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *Parameters measured with 16 outputs switching.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



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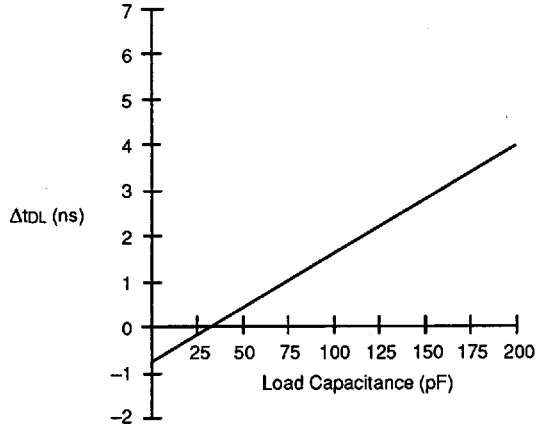
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{16\ O/P} + \Delta t_{os}$

Datasheet numbers ($t_{16\ O/P}$) are specified at 16 outputs switching



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Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

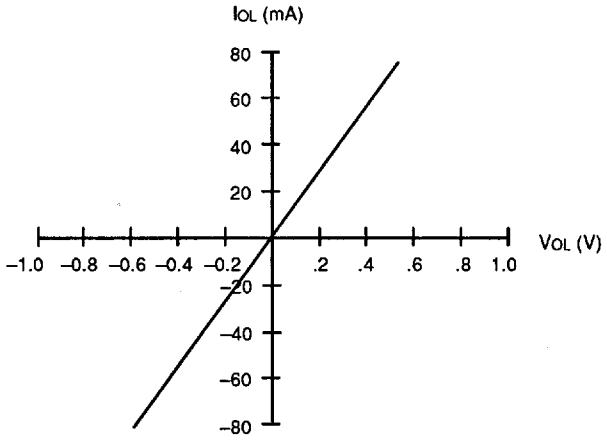
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

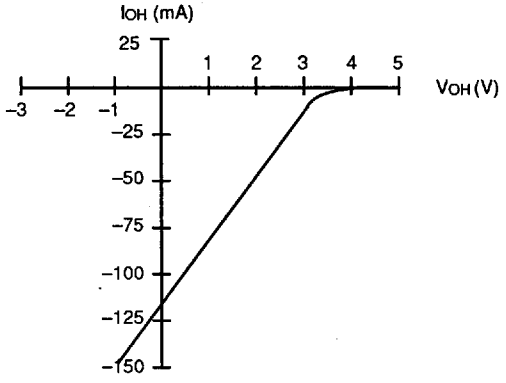
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



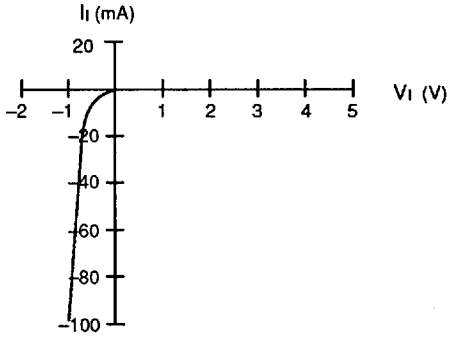
Output, LOW

14127G-7



Output, HIGH

14127G-8



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Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to the General Information section for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ	Unit
I_{CCO}	Base static I_{CC}	90	mA
i_I	Incremental input current	15	µA/MHz
i_B	Incremental current per PAL block	13	µA/MHz
i_O	Incremental output current	90	µA/MHz
i_V	Voltage dependence	40	%/V
i_T	Temperature dependence	–0.17	%/°C

TYPICAL DATA DESIGN GUIDELINES

The following parameters are provided in response to questions from designers. They are intended only as design guidelines, and should be used with care. They are not guaranteed or tested.

Parameter Description	Typ	Unit
Delay Minimums (Note 1)		
Combinatorial propagation delay minimum	3	ns
Clock-to-output delay minimum	2	ns
Edge Rates (Note 2)		
Rise rate	1	V/ns
Fall rate	1	V/ns
Skew (Note 3)		
Clock-to-output skew, same clock polarity and same output polarity	1	ns
Clock-to-output skew, same clock polarity only	2	ns
Clock-to-output skew, same output polarity only	2	ns
Clock-to-output skew, different clock polarity and different output polarity	2	ns
Internal Delay Savings (Note 4)		
Propagation delay savings	2	ns
Clock-to-output delay savings	3	ns
Ground Bounce (Note 5)		
Ground bounce noise level on low output	0.5	V

Notes:

1. *Minimum delays shown anticipate some future technology improvements, but it cannot be guaranteed that process and design changes will not increase the best-case performance beyond the values below.*
2. *Rise and fall rates are for unloaded outputs.*
3. *Skew values assume equal output loading.*
4. *Internal delay savings gives the typical amount of delay saved by not going through an output buffer.*
5. *The ground bounce noise level should be added to the static V_{OL} under normal load conditions as applied to a silent low output when all other I/O pins are switching from high to low.*

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			PLCC	CQFP	
θ_{jc}	Thermal impedance, junction to case		14	13	°C/W
θ_{ja}	Thermal impedance, junction to ambient		39	44	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	33	38	°C/W
		400 lfpm air	30	35	°C/W
		600 lfpm air	27	33	°C/W
		800 lfpm air	25	31	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.