NEC ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTORS

2SK1060, 2SK1060-Z

DESCRIPTION The 2SK1060, 2SK1060-Z are N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Second Breakdown
- Designed for Hybrid Integrated Circuits

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation*		2.0	W
Total Power Dissipation (T_c ** = 25 °C) . .		20	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±5	A
$I_{D(pulse)}$	Drain Current (pulse)***	±20	A

* Mounted on ceramic substrate of 7.5 cm² x 0.7 mm

** T_c = 25 °C

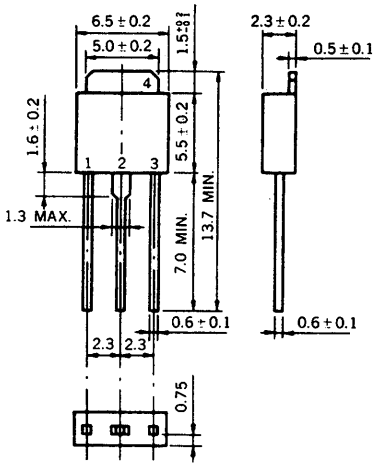
*** PW ≦ 10 μs, Duty Cycle ≦ 1 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.18	0.27	Ω	V_{GS} = 10 V, I_D = 3 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.22	0.38	Ω	V_{GS} = 4 V, I_D = 3 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	4.0			S	V_{DS} = 10 V, I_D = 3 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		900		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		250		pF	
C_{rss}	Reverse Transfer Capacitance		50		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	I_D = 3 A, V_{DD} ≒ 50 V R_L = 17 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		110		ns	
t_f	Fall Time		30		ns	

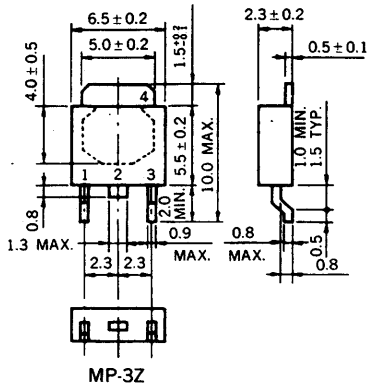
PACKAGE DIMENSIONS (Unit : mm)

2SK1060



MP-3

2SK1060-Z

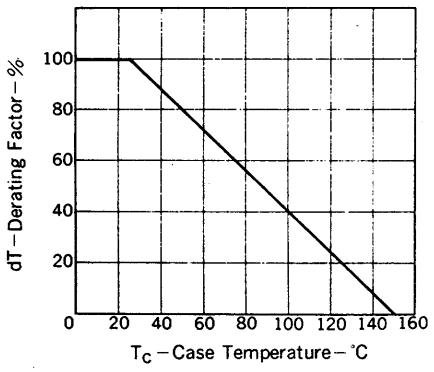


MP-3Z

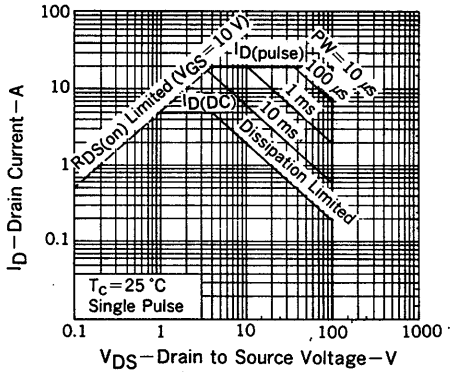
1. Gate
2. Drain
3. Source
4. Drain (Fin)

TYPICAL CHARACTERISTICS (T_a = 25 °C)

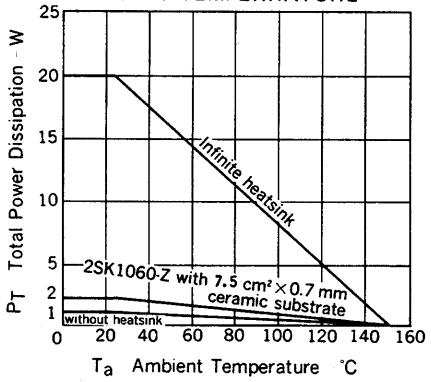
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



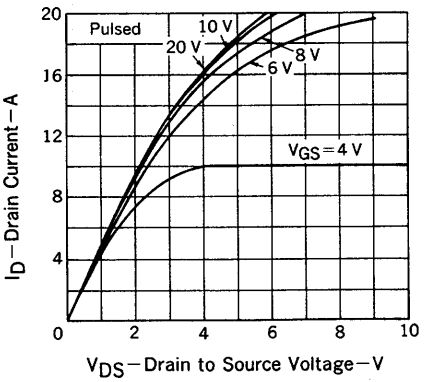
FORWARD BIAS SAFE OPERATING AREA



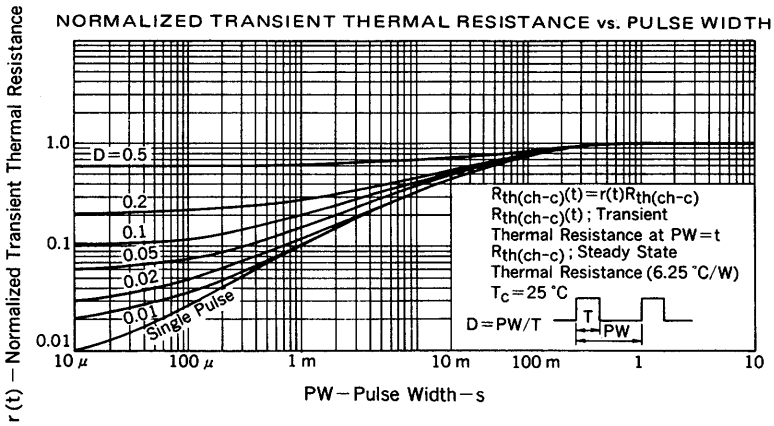
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERRATURE



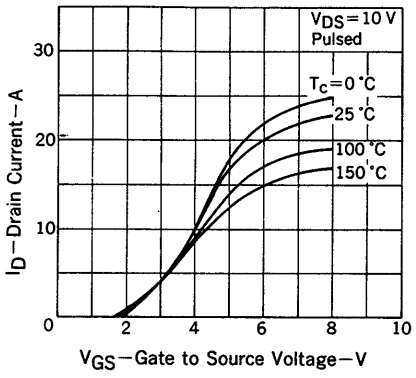
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



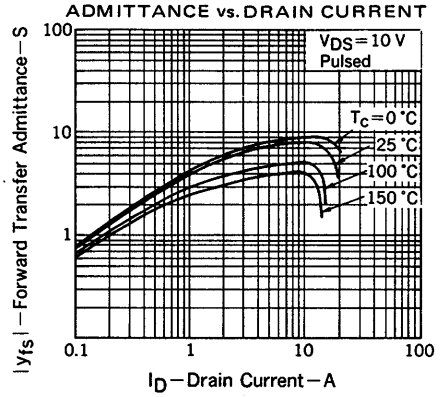
NORMALIZED TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



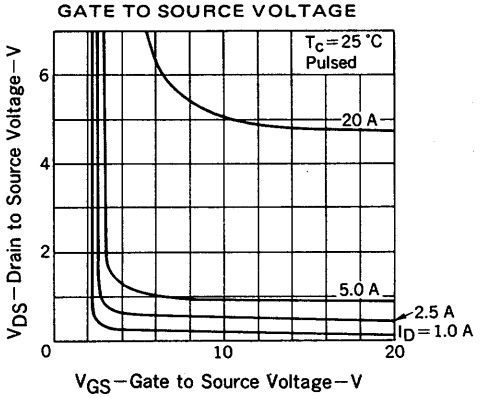
TRANSFER CHARACTERISTICS



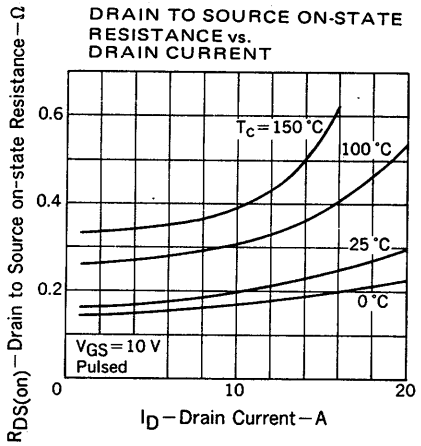
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



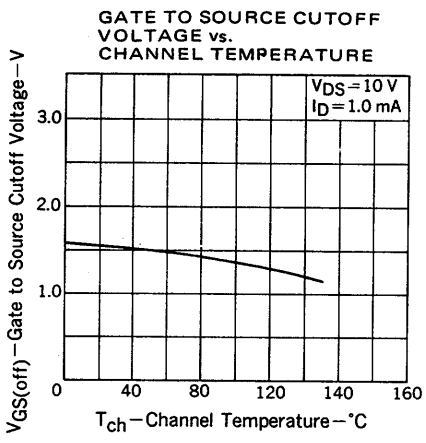
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE



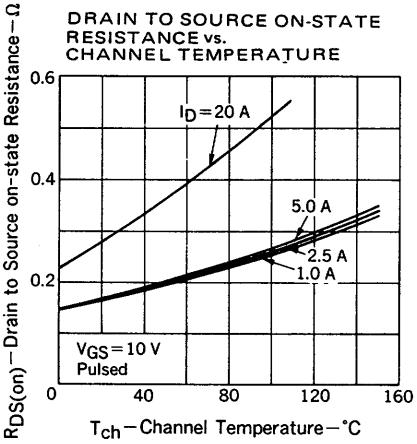
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



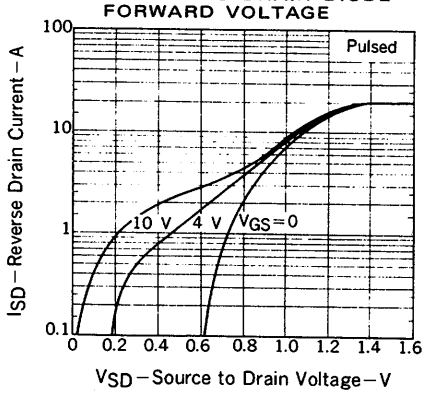
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



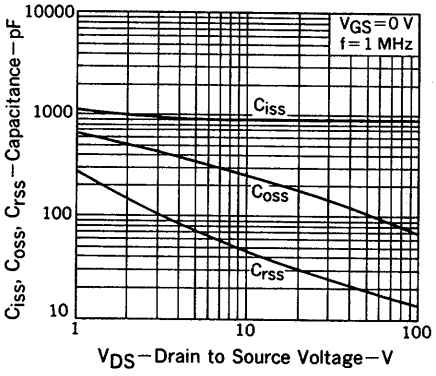
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



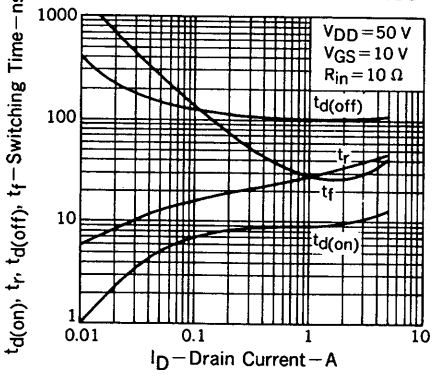
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



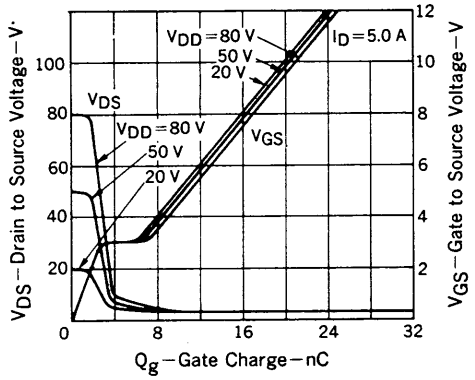
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



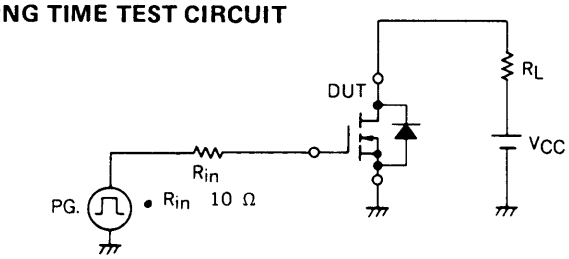
SWITCHING CHARACTERISTICS

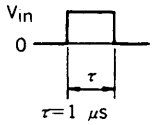


DYNAMIC INPUT/OUTPUT CHARACTERISTICS



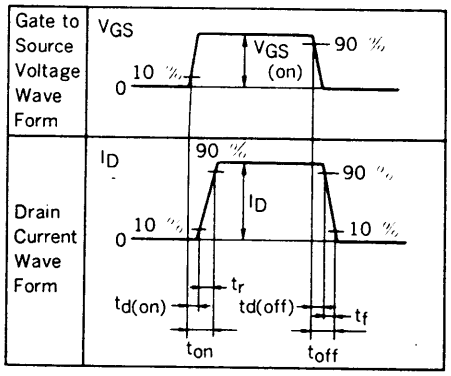
SWITCHING TIME TEST CIRCUIT





τ=1 μs
Duty Cycle≦1 %

(The diode in this figure is the parasitic diode.)



GATE CHARGE TEST CIRCUIT