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April 1st, 2010 Renesas Electronics Corporation

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SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3221 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3211	Isolated TO-220

FEATURES

- · Low gate charge
 - $Q_G = 9 \text{ nC TYP.}$ (VDD = 450 V, VGS = 10 V, ID = 2.0 A)
- Gate voltage rating ±30 V
- · Low on-state resistance

RDS(on) = 4.4 Ω MAX. (VGS = 10 V, ID = 1.0 A)

- · Avalanche capability ratings
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	600	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±30	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±2.0	Α
Drain Current (pulse) Note1	ID(pulse)	±8.0	Α
Total Power Dissipation (T _A = 25°C)	P _{T1}	2.0	W
Total Power Dissipation (Tc = 25°C)	P _{T2}	25	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	2.0	Α
Single Avalanche Energy Note2	Eas	2.7	mJ
Diode Recovery dv/dt Note3	dv/dt	3.5	V/ns

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- 2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V
- **3.** If ≤ 1.0 A, $V_{clamp} = 600$ V, $di/dt \leq 100$ A/ μ s, $T_A = 25$ °C

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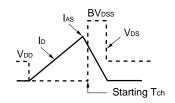


ELECTRICAL CHARACTERISTICS (TA = 25°C)

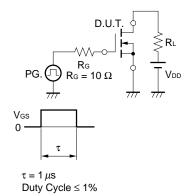
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	Vps = 600 V, Vgs = 0 V			100	μΑ
Gate Leakage Current	Igss	Vgs = ±30 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	y fs	V _{DS} = 10 V, I _D = 1.0 A	0.5			S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, ID = 1.0 A		3.3	4.4	Ω
Input Capacitance	Ciss	Vps = 10 V		290		pF
Output Capacitance	Coss	V _G s = 0 V		60		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		5		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 1.0 A		7		ns
Rise Time	tr	Vgs = 10 V		2		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 10 \Omega$		20		ns
Fall Time	t _f			10		ns
Total Gate Charge	QG	V _{DD} = 450 V		9		nC
Gate to Source Charge	Qgs	Vgs = 10 V		2.4		nC
Gate to Drain Charge	Q _{GD}	ID = 2.0 A		2		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 2.0 A, VGS = 0 V		0.9		V
Reverse Recovery Time	trr	IF = 2.0 A, VGS = 0 V		0.9		μs
Reverse Recovery Charge	Qrr	$di/dt = 50 \text{ A/ } \mu\text{s}$		2.0		μC

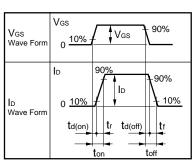
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{RG} = 25 \ \Omega \\ \text{PG.} \\ \text{Vgs} = 20 \rightarrow 0 \ V \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{PG.} \\ \text{VpD} \end{array}$

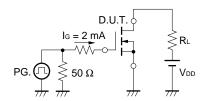


TEST CIRCUIT 2 SWITCHING TIME

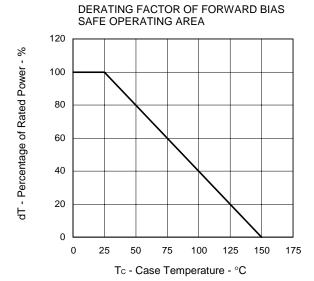




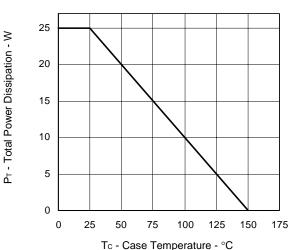
TEST CIRCUIT 3 GATE CHARGE



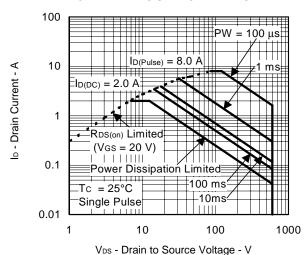
TYPICAL CHARACTERISTICS (TA = 25°C)

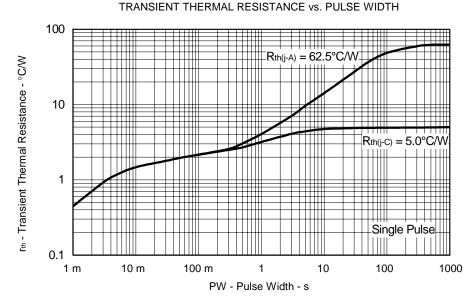


TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

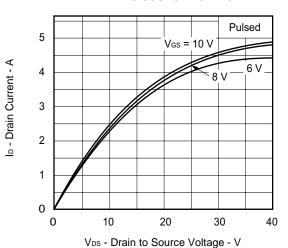




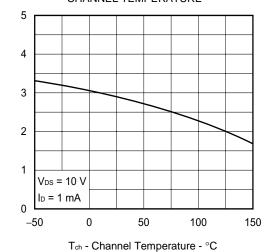
3

Phase-out/Discontinued

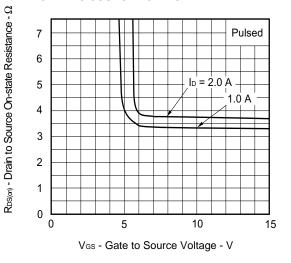
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



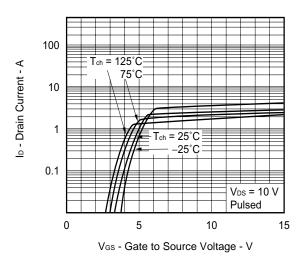
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



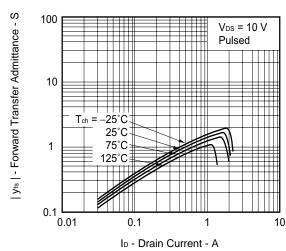
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



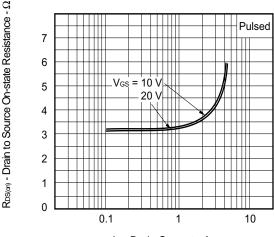
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

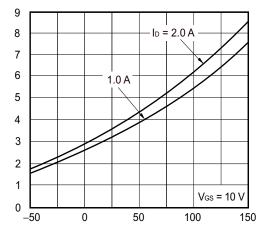


I_D - Drain Current - A

Ves(off) - Gate Cut-off Voltage - V

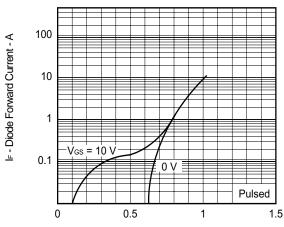
 $\mathsf{R}_{\mathsf{DS}(on)}$ - Drain to Source On-state Resistance - Ω

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



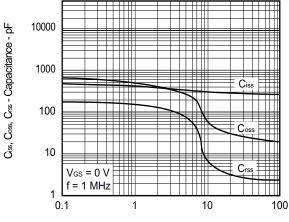
Tch - Channel Temperature - °C

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



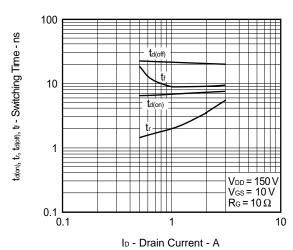
V_{F(S-D)} - Source to Drain Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

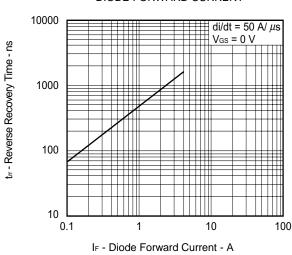


V_{DS} - Drain to Source Voltage - V

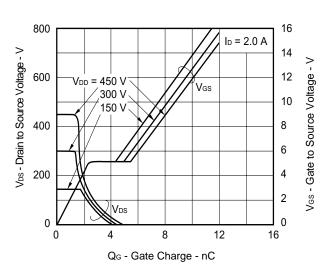
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



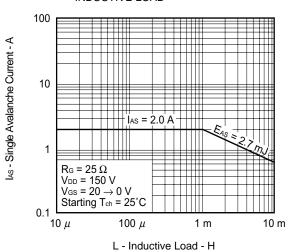
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



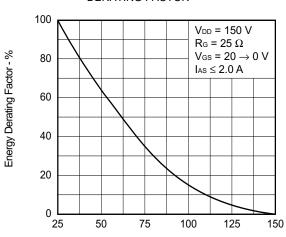
5



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



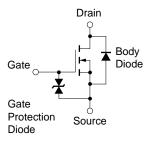
Starting T_{ch} - Starting Channel Temperature - $^{\circ}C$



PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F) 4.5±0.2 10.0±0.3 3.2±0.2 2.7±0.2 15.0 ± 0.3 3±0.1 12.0±0.2 <u>0.7±</u>0.1 2.5±0.1 1.5±0.2 0.65±0.1 2.54 TYP 2.54 TYP. 1. Gate 2. Drain 3. Source

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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