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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR **2SK3058**

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION	ORD	ORDERING INFORMATION			
This product is N-Channel MOS Field Effect Transistor			PART NUMBER	PACKAGE	
designed for high current switching app		2SK3058	TO-220AB		
FEATURES		2SK3058-S	TO-262		
Super Low On-State Resistance		2SK3058-ZJ	TO-263		
$R_{DS(on)1} = 17 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ I})$	*	2SK3058-Z	TO-220SMD ^{Note}		
RDS(on)2 = 27 mΩ MAX. (VGS = 4.0 V, ID = 28 A) • Low Ciss : Ciss = 2100 pF (TYP.)				ckage is produced only	
		Note	Japan.		
Built-in Gate Protection Diode			Japan.		
			0		
ABSOLUTE MAXIMUM RATINGS	. ,			(TO-220AB)	
Drain to Source Voltage (Vcs = 0)	VDSS	60		\sim	
Gate to Source Voltage (VDS = 0)	VGSS(AC)	±20	V		
Gate to Source Voltage (VDS = 0)	VGSS(DC)	+20, –10	V		
Drain Current (DC)	D(DC)	±55	A		
Drain Current (Pulse) ^{Note1}	D(pulse)	± 165	А		
Total Power Dissipation (Tc = 25°C)	P	58	W		
Total Power Dissipation ($T_A = 25^{\circ}C$)	Рт	1.5	W		
Channel Temperature	Tch	150	°C	(TO-262)	
Storage Temperature	Tstg	-55 to + 150	°C		
Single Avalanche Current Note2	las	27.5	А		
Single Avalanche Energy	Eas	75.6	mJ		
\sim					
Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %	6				
2. Starting Tch = $25 \degree C$, VDD = 3	80 V, Rg = 25 Ω	, Vgs = 20 V \rightarrow	• 0	(TO 262 TO 2200MD)	
				(TO-263, TO-220SMD)	

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ELECTRICAL CHARACTERISTICS (TA = 25 °C)

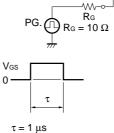
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Id = 28 A		12	17	mΩ
	RDS(on)2	Vgs = 4.0 V, Id = 28 A		19	27	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 28 A	13	42		S
Drain Leakage Current	IDSS	Vds = 60 V, Vgs = 0 V			10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Input Capacitance	Ciss	V _{DS} = 10 V		2100		pF
Output Capacitance	Coss	V _G s = 0 V		550		pF
Reverse Transfer Capacitance	Crss	F = 1 MHz		220		pF
Turn-on Delay Time	td(on)	ID = 28 A		36		ns
Rise Time	tr	V _{GS} = 10 V	Ċ	410		ns
Turn-off Delay Time	td(off)	Vdd = 30 V	5	130		ns
Fall Time	tr	R _G = 10 Ω		260		ns
Total Gate Charge	Q _G	Ib = 55 A		45		nC
Gate to Source Charge	Q _{GS}	Vdd = 48 V		7		nC
Gate to Drain Charge	Qgd	V _{GS} = 10 V		13		nC
Body Diode Forward Voltage	VF(S-D)	IF = 55 A, Vgs = 0 V		1.0		V
Reverse Recovery Time	trr	I⊧ = 55 A, V₀s = 0 V		60		ns
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s$		100		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$PG. \bigoplus_{m} \underbrace{FG} = 25 \Omega$ $V_{GS} = 20 \rightarrow 0 V \bigoplus_{m} \underbrace{FG} = 50 \Omega$ $V_{DD} \underbrace{V_{DD}}$ $V_{DD} \underbrace{V_{DD}}$

TEST CIRCUIT 3 GATE CHARGE

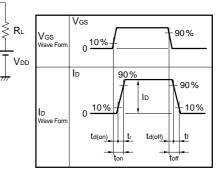
 $PG. \bigoplus_{m=1}^{D.U.T.} \underbrace{Solution}_{m=1}^{LU.T.} V_{DD}$



D.U.T.

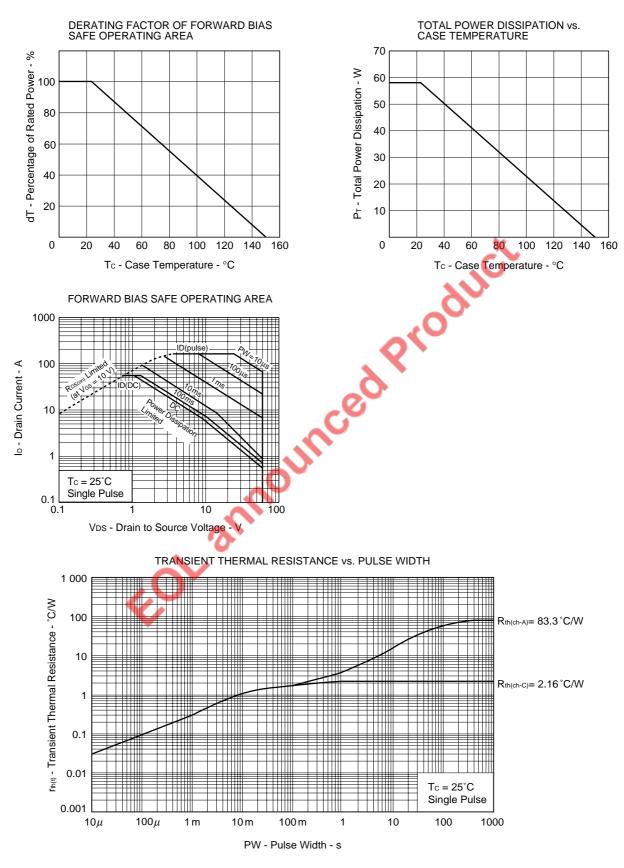
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 $\label{eq:tau} \begin{array}{l} \tau = 1 \ \mu s \\ \text{Duty Cycle} \leq 1 \ \% \end{array}$

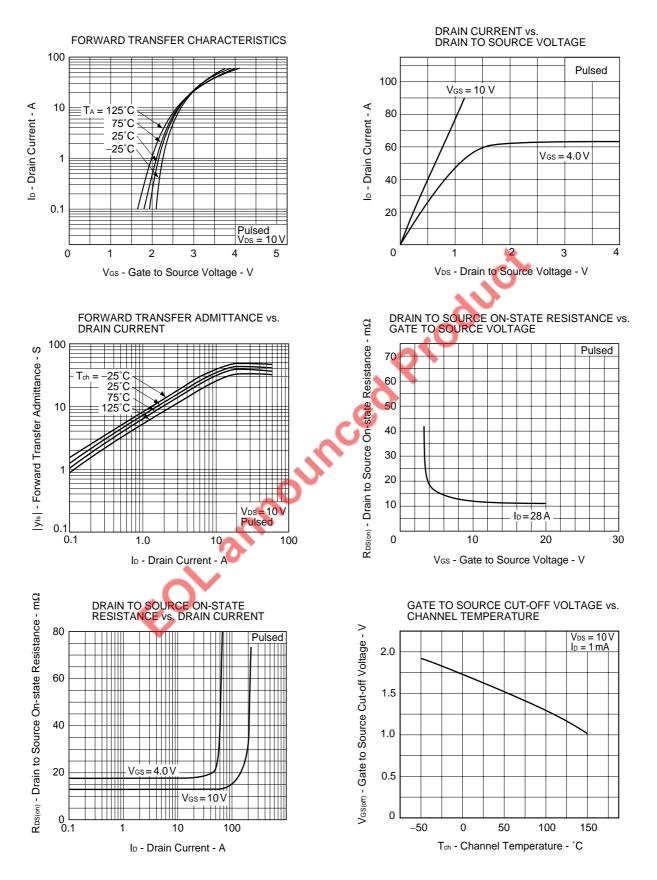


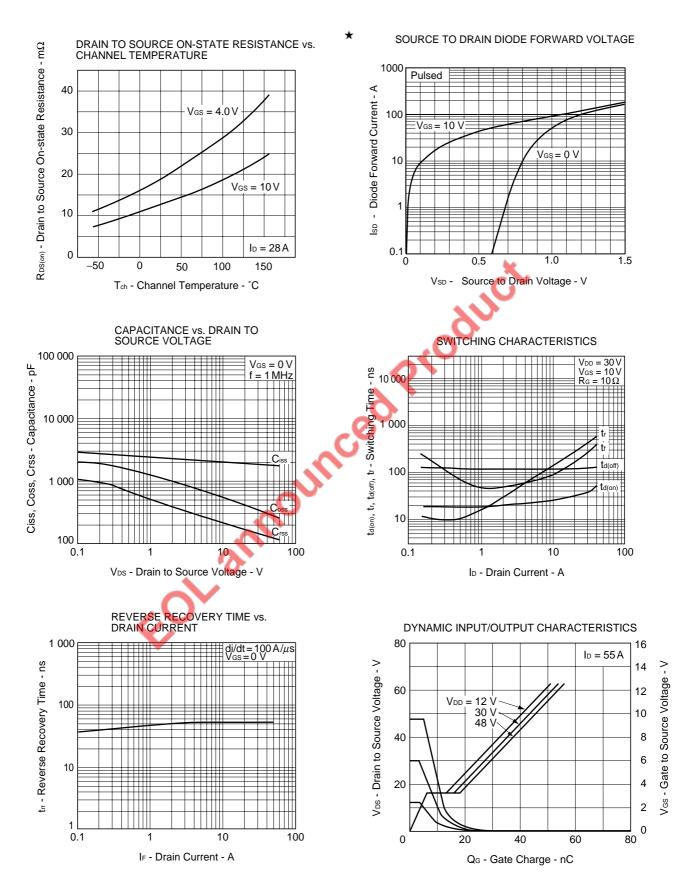
TEST CIRCUIT 2 SWITCHING TIME



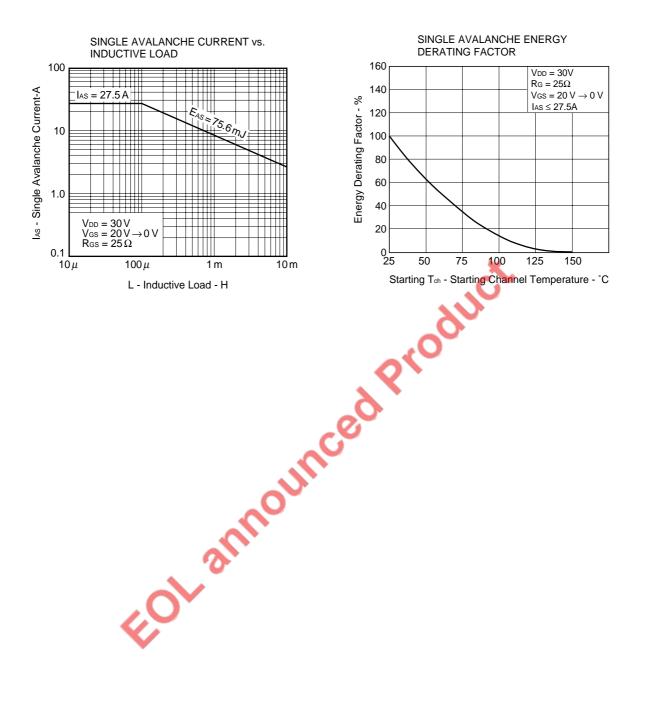


Data Sheet D13097EJ2V0DS



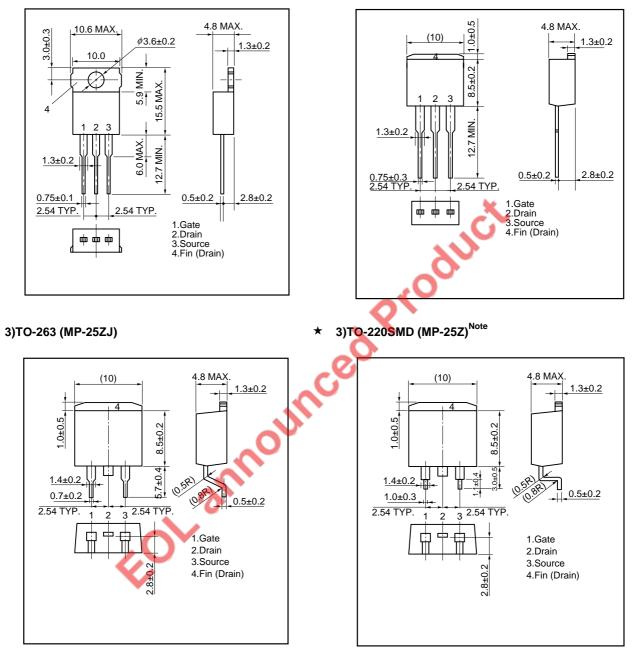


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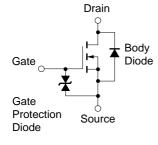
PACKAGE DRAWINGS (Unit : mm)

1)TO-220AB (MP-25)



2)TO-262 (MP-25 Fin Cut)

EQUIVALENT CIRCUIT



Note This package is produced only in Jaman.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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