HPL-16RC8
HPL-16RC6
HPL-16RC4

CMOS HPL™ Harris Programmable Logic

Features

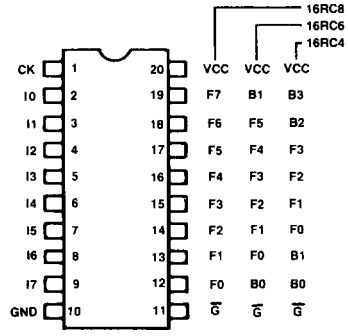
- Pin & Function Compatible with the Bipolar 16R8, 16R6 and 16R4
- Scaled SAJI IV CMOS Process
- Fast Access ..... Input to Output 125ns Max.
  ..... Clock to Output 60ns Max.
- Low Standby and Operating Power
  - ICCSB = 150μA
  - ICCOP = 7mA/MHz
- Wide Operating Temperature Ranges:
  - HPL-16RC8-5, HPL-16RC6-5, HPL-16RC4-5.....0°C to +75°C
  - HPL-16RC8-9, HPL-16RC6-9, HPL-16RC4-9..... -40°C to +85°C
  - HPL-16RC8-8, HPL-16RC6-8, HPL-16RC4-8 ..... -55°C to +125°C
- 20 Pin Dual-In-Line Package
- Security Fuse for Pattern Protection
- TTL/CMOS Compatible Inputs/Outputs for Mixed System Compatibility
- Logic Paths Tested to Insure Functionality
- Programmable Output Polarity

Applications

- Random Logic Replacement
- Code Converters
- Address Decoding
- Custom Shift Registers
- Boolean Function Generators
- Digital Multiplexers
- Parity Generators
- Pattern Recognition
- State Machine Design

Pinouts

TOP VIEW



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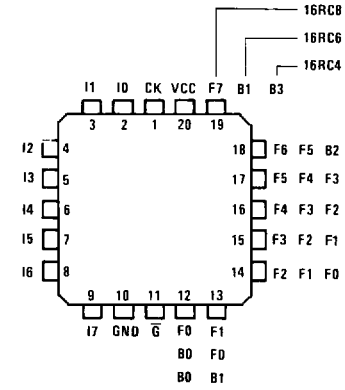
TOP VIEW



Description

The HPL-16RC8, HPL-16RC6, and HPL-16RC4 are CMOS Programmable Logic Devices designed to provide high performance, low power alternatives to the industry standard 16RC8, 16RC6, and 16RC4 bipolar programmable logic devices.

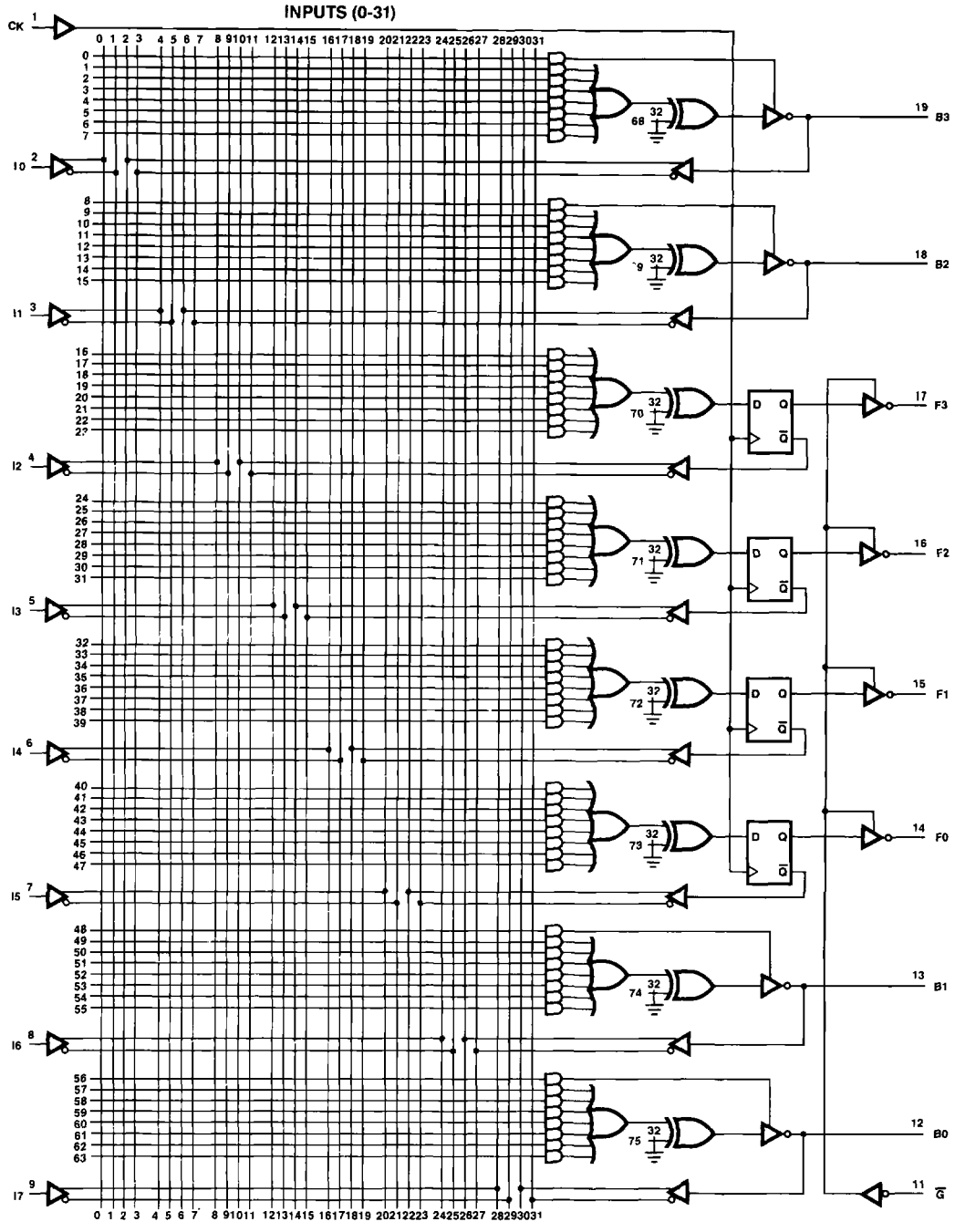
In addition to the low power advantage of these devices over their bipolar counterparts, the HPL-16RC8, HPL-16RC6, and HPL-16RC4 contain programmable output polarity, allowing the user to individually select each output as either active-high or active-low. When all output polarity fuses are left intact, all active outputs are active-low.

These three devices provide a choice of either eight (16RC8), six (16RC6), or four (16RC4) registered outputs with feedback, each output consisting of eight product terms. The HPL-16RC6 and the HPL-16RC4 also contain two and four bi-directional pins, respectively.

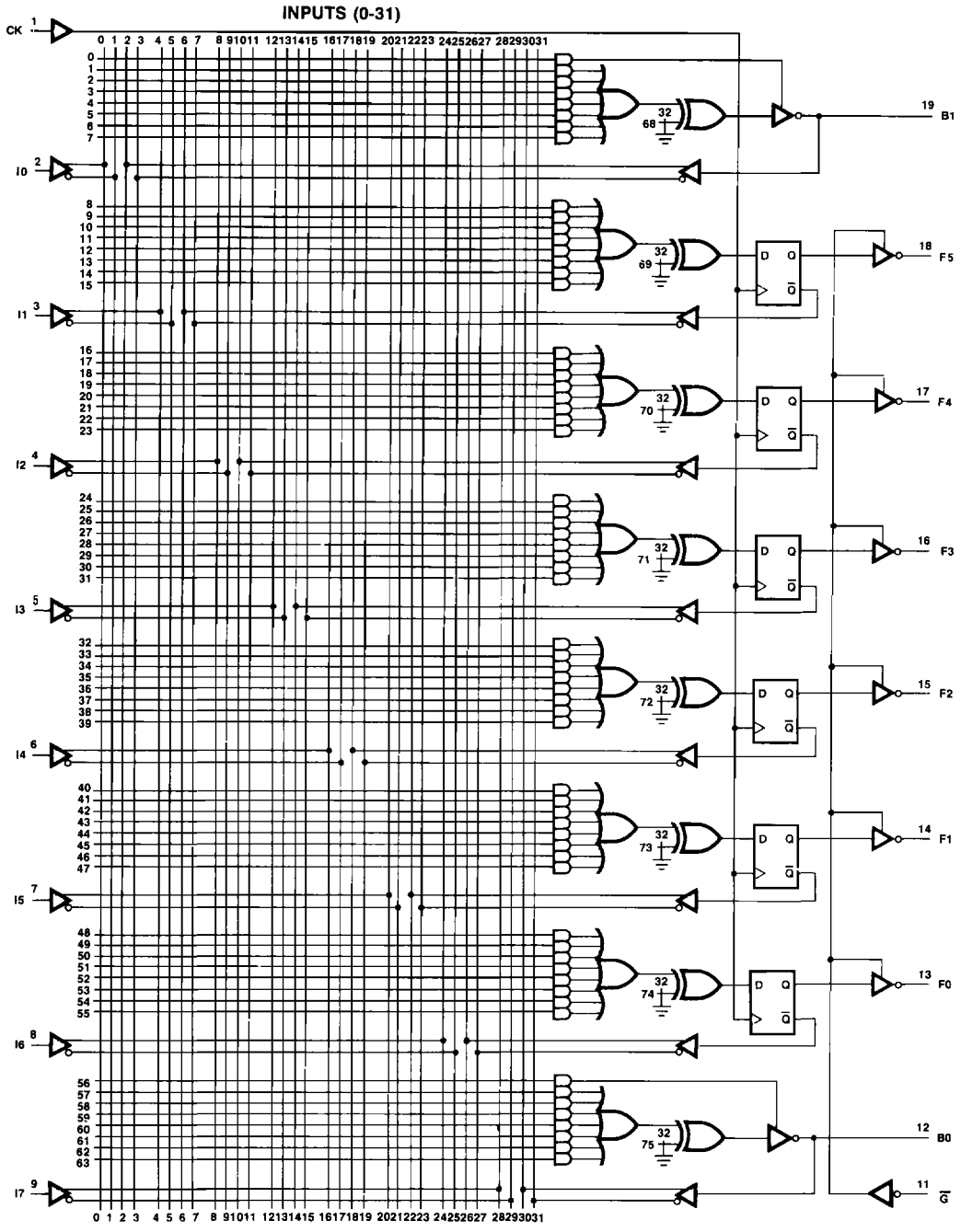
The Harris fuse link technology provides a permanent fuse with stable storage characteristics of the full temperature ranges of 0°C to +75°C, -40°C to +85°C and -55°C to +125°C. Like all Harris Programmable Logic (HPL), these devices contain unique test circuitry developed by Harris which allows AC, DC and functional testing before programming.

On-chip automatic power-down circuitry places internal circuitry into an ultra-low ICCSB power mode after output data becomes valid.

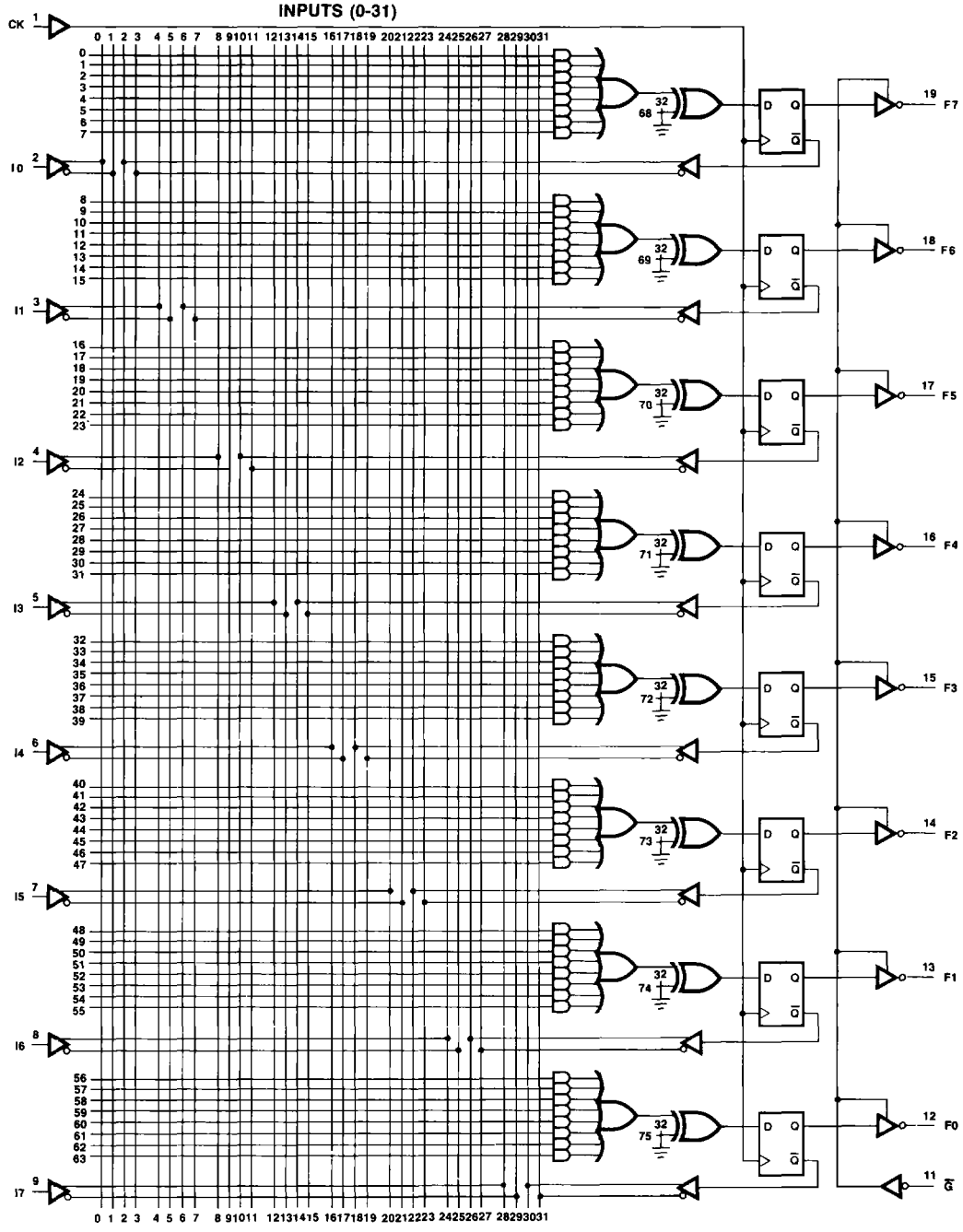
Functional Diagram



Functional Diagram



Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 16°C/W (CERDIP Package), 19°C/W (LCC Package)
θ_{ja} ..... 70°C/W (CERDIP Package), 76°C/W (LCC Package)
Gate Count ..... 1500 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HPL-16RC8,6,4-5 ..... 0°C to +70°C
HPL-16RC8,6,4-9 ..... -40°C to +85°C
HPL-16RC8,6,4-8 ..... -55°C to +125°C

D.C. Electrical Specifications (Operating)

HPL-16RC8,6,4-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-16RC8,6,4-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-16RC8,6,4-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS ③
IIH IIL	Dedicated Input Current	"1" "0"		+1 -1	μA μA	VIH = VCC MAX VIL = 0V VCC = VCC MAX
IFZH IFZL	Output Current Hi-Z State	"1" "0"		+10 -10	μA μA	VFH = VCC MAX VFL = 0V VCC = VCC MAX
IBZH IBZL	Bidirectional Hi-Z Current	"1" "0"		+10 -10	μA μA	VBH = VCC MAX VBL = 0V VCC =VCC MAX
VIH VIL	Input Threshold Voltage ①	"1" "0"	2.0	 0.8	V V	VCC = VCC MAX VCC = VCC MIN
VOH1 VOH2 VOL	Output Voltage ② Output Voltage	"1" "1" "0"	3.0 VCC-0.4	 0.4	V V V	IOH1 = -5.0 mA IOH2 = -1.0 mA VCC MIN, VIL MAX, VIH MIN IOL = +5.0 mA
ICCSB	Standby Power Supply Current			150	μA	VI = VCC or GND IF = 0μA, VCC = VCC MAX
ICCOP	Operating Power Supply Current			7	mA/MHz	VI = VCC or GND IF = 0μA, VCC = VCC MAX

① These specifications apply to both Input (I) and Bidirectional (B) Pins.
② These specifications apply to both Output (F) and Bidirectional (B) Pins.
③ All DC parameters tested under worst case conditions.

Capacitance TA = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CF	Output Capacitance	10	pF	VF = VCC or GND, f = 1MHz
CB	Bidirectional Capacitance	12	pF	VB = VCC or GND, f = 1 MHz

*NOTE: Sampled and guaranteed — but not 100% tested

A.C. Switching Specifications ⓘ
(Operating)

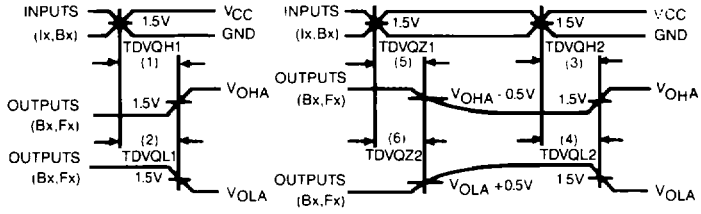
HPL-16RC8,6,4-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-16RC8,6,4-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-16RC8,6,4-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

	SYMBOL			HPL-16RC8,6,4-5		HPL-16RC8,6,4-9		HPL-16RC8,6,4-8		
	JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
(1)	TDVQH1	TPD	Propagation delay Input or I/O to Active High Output	-	125	-	125	-	125	ns
(2)	TDVQL1	TPD	Propagation delay Input or I/O to Active Low Output	-	125	-	125	-	125	ns
(3)	TDVQH2 ⓘ	TPZX	Enable Access Time to Active High Output - Product Term Controlled	TDVQZ1	125	TDVQZ1	125	TDVQZ1	125	ns
(4)	TDVQL2 ⓘ	TPZX	Enable Access Time to Active Low Output-Product Term Controlled	TDVQZ2	125	TDVQZ2	125	TDVQZ2	125	ns
(5)	TDVQZ1	TPXZ	Disable Access Time from Active High Output-Product Term Controlled	-	125	-	125	-	125	ns
(6)	TDVQZ2	TPXZ	Disable Access Time from Active Low Output-Product Term Controlled	-	125	-	125	-	125	ns
(7)	TCHQH	TCLK	Propagation delay Clock to Active High	-	60	-	60	-	60	ns
(8)	TCHQL	TCLK	Propagation delay Clock to Active Low	-	60		60	-	60	ns
(9)	TGLQH ⓘ	TPZX	Enable Access Time to Active High Output - Enable Pin Controlled	TGHQZ1	60	TGHQZ1	60	TGHQZ1	60	ns
(10)	TGLQL ⓘ	TPZX	Enable Access Time to Active Low Output - Enable Pin Controlled	TGHQZ2	60	TGHQZ2	60	TGHQZ2	60	ns
(11)	TGHQZ1	TPXZ	Disable Access Time from Active High Output - Enable Pin Controlled	-	60	-	60	-	60	ns
(12)	TGHQZ2	TPXZ	Disable Access Time from Active Low Output - Enable Pin Controlled	-	60	-	60	-	60	ns
(13)	TDVCH	TSU	Data Setup Time	125	-	125	-	125	-	ns
(14)	TCHDX	TH	Data Hold Time	0	-	0	-	0	-	ns
(15)	TCHCL	TW	Clock Pulse Width (High)	25	-	25	-	25	-	ns
(16)	TCLCH	TW	Clock Pulse Width (Low)	25	-	25	-	25	-	ns
(17)	fMAX	fMAX	Maximum Frequency	-	5	-	5	-	5	MHz

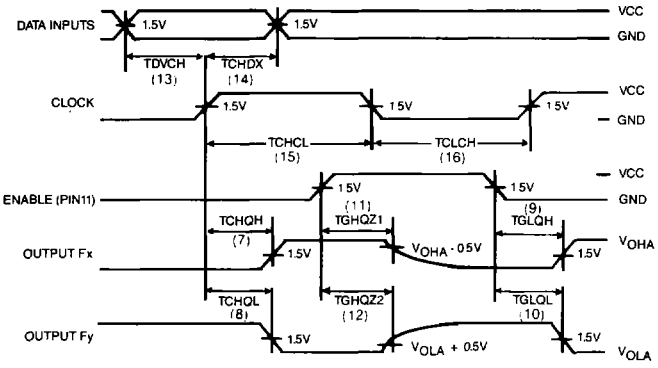
ⓘ Enable access time is guaranteed to be greater than disable access time to avoid device contention.

Switching Time Definitions

Asynchronous Outputs



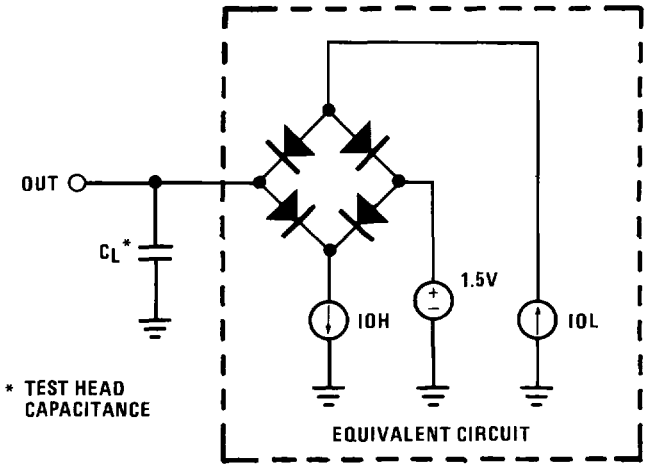
Synchronous Outputs



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the three-state product term or the output enable pin drives the output inactive The high impedance state is defined as a point on the output waveform equal to a Δ V of 0.5V from VOHA or VOLA, the active output level

A.C. Test Load



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CMOS HPL

Programming

Following is the programming procedure used for the HPL-16RC8,6,4 programmable logic devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

TABLE 1
PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	IC Limit During Programming			100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-5.00	-5.00	-7.00	V
INEG	Edit Enable & Mode Select Current				-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	Verify	⑤ VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	Programming	⑤ VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V		0	1	μA
IIHV	Input Current High	Verify		0	1	μA
IIHP	Input Current High	Programming		0	1	μA
VSI	Verify voltage	Intact Fuse	3.00	3.30		V
VSP	Verify voltage	Programmed Fuse		0.00	0.50	V
TV	Verify Pulse Delay		500	750	1000	μsec
PWP	Programming Width		4.5	5.0	5.5	msec
td	Pulse Seq. Delay		1	1	10	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1		μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
tNEG	Mode Select Width		1	1	5	μsec
TPP	Programming Period			5.1		msec
FL	Fuse Attempts/Link		1	1	2	cycles

⑤ Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC PIN.

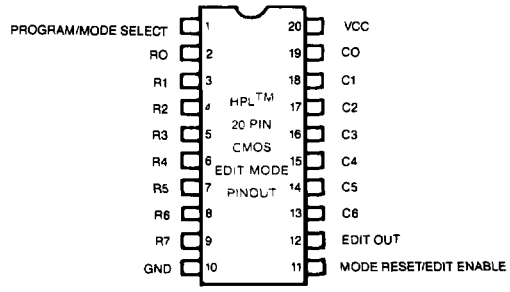

FIGURE 1
EDIT MODE PINOUT
HPL-16RC8, 6, 4

NOTES:
- While programming the CMOS HPL™ device, no pins should be left floating. EDIT OUT appears as an open drain output during programming. It should be tied to GND through a 1M-ohm resistor.
- CMOS HPL outputs are not put into a high impedance state (suitable for row and column address application) until the device is reset and put into the edit mode. For this reason it is recommended that the outputs be left floating until the edit mode is enabled or that the outputs be driven thru a 2k-ohm resistor.
- It is suggested that a 0.01μF capacitor be put between VCC and GND to minimize VCC voltage spikes. Also, particular care should be exercised in regard to transients on the MODE SELECT and MODE RESET pins, which could place the device in the incorrect mode.

Programming Procedure

① Set-Up:

NOTE: Refer to the Figure 1 for the pin definitions, Table 1 for the timing and level definitions, Table 2 for the mode decode, and Tables 3 & 4 for the address decoding.

a. During programming, no pins should be left floating.
b. EDIT OUT(Pin 12) should be terminated with a 1 M-ohm (± 1%) resistor to GND and stray capacitances on this pin should be ≤ 50 pF.
c. Set GND to 0.00 volts.
d. Outputs are only in a high impedance state (and available for addressing of edit mode rows and columns) while in Edit Modes 1 thru 4. Do not apply signals to these pins until a valid Edit Mode is entered.
e. All input and bi-directional pins should be at zero volts nominal with a maximum of 0.3 volts applied.
f. Apply VCCV to the part. No input should ever exceed the level on the VCC PIN.

② Mode Reset/Edit Enable:

a. Wait td and reset the edit control logic by pulsing the MODE RESET PIN to VNEG for tNEG.
b. Wait td and enable Edit mode by applying VNEG to the EDIT ENABLE PIN.

③ Mode Select:

a. Wait td and select EDIT MODE 1 by pulsing the MODE SELECT PIN to VNEG for tNEG. Subsequent pulses will increment the mode to 2, 3 and 4 sequentially (sequencing the device beyond mode 4 will result in unpredictable results — if in doubt, return to STEP 2).
b. Verify entry into the proper mode by addressing column 64 and the row indicated in Table 2, waiting TV and monitoring the EDIT OUT PIN for the proper data.
c. Address column 65 and the row indicated in Table 2, wait TV and monitor the EDIT OUT PIN for the proper data. If both steps 3b and 3c are correct, then the proper mode has been selected.
d. To re-enter a mode lower than the current mode, return to step 2. Mode 1 can only be (re-)entered from step 2.

④ Fuse select:

NOTE: The voltage for a logical "1" (VIHP) must not exceed VCCP and must track VCCP as it rises from VCCV in step 5.

a. wait td and select a row by applying the appropriate address from Table 3.
b. Select a column by applying the appropriate address from Table 4.

⑤ Verify Intact Fuse:

NOTE: Skip this step for post-programming verify.

a. Wait TV and monitor EDIT OUT (Pin 12) for VSI.
b. If EDIT OUT has indicated less than VSI, the fuse is not intact. Reject this device for a non-blank matrix.

⑥ Program the Fuse:

NOTE: The PROTECT and POLARITY fuses can be accessed from either mode 1 or mode 3 by applying the addresses indicated in Tables 3 & 4.
THE 'PROTECT' FUSE SHOULD NOT BE PROGRAMMED UNTIL ALL OTHER FUSES HAVE BEEN PROGRAMMED AND VERIFIED AS PROGRAMMING THIS FUSE DEFEATS ALL FURTHER VERIFICATION!!

a. Wait td and raise the VCC PIN to VCCP (allow VIHP to track this rise).
b. Wait td and pulse the PROGRAM PIN(Pin 1) to VIHP for a duration of PWP.
c. Wait td and lower the VCC PIN to VCCV (allow VIHP to track this fall)

⑦ Verify Fuse:

a. Wait TV and monitor EDIT OUT for VSP (or VSI if verifying an intact fuse).
b. If EDIT OUT has indicated greater than VSP for an attempted programmed fuse, repeat step 6 so that the fuse receives a maximum of FL fusing attempts.

⑧ Repeat steps 4 through 7 for all addresses in a given mode.....

⑨ Repeat steps 3 through 8 for all modes.

Programming Waveforms

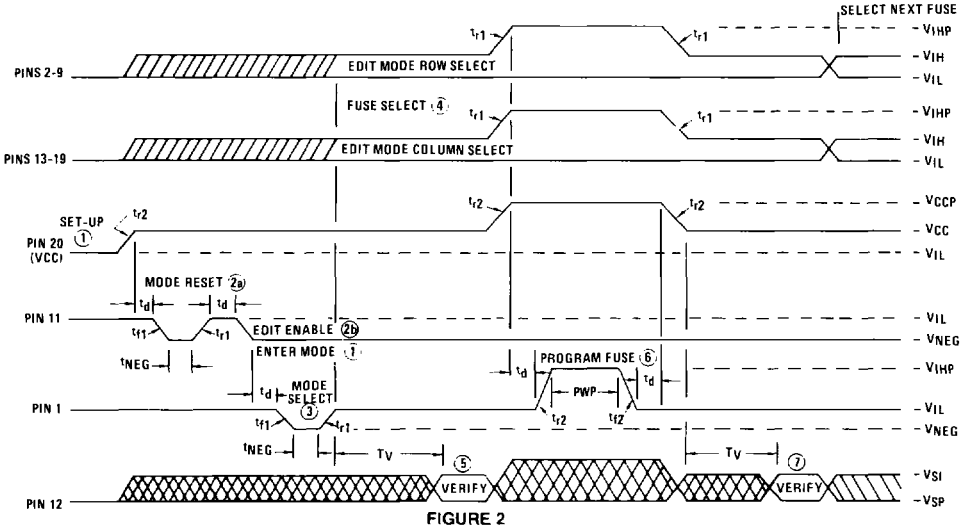

FIGURE 2

NOTE: Pins 13-19 are not necessarily three-stated and available for application of column address input signals until a valid edit mode is entered. Refer to the edit mode pinout (Figure 1) for further details.

MODE VERIFICATION TABLE 2

MODE	COLUMN NUMBER	ROW NUMBER	EDIT OUT(PIN 12) LOGICAL LEVEL
1	64	0	0
	65	0	0
2	64	1	0
	65	1	1
3	64	2	1
	65	2	0
4	64	3	1
	65	3	1

NOTE: *At least two addresses must be checked to verify the proper edit mode.
*The conversion from the decimal column and row addresses in the table above to the actual pin levels can be made in Tables 3 and 4.

EDIT MODE ROW SELECT TABLE 3 HPL-16RC8,6,4

PROG. MODE	ROW NUMBER	R7 Pin 9	R6 Pin 8	R5 Pin 7	R4 Pin 6	R3 Pin 5	R2 Pin 4	R1 Pin 3	R0 Pin 2	VARIABLE 16RC8	16RC6	16RC4
1	0	H	H	H	H	H	H	H	L	I0	I0	I0
	4	H	H	H	H	H	H	L	H	I1	I1	I1
	8	H	H	H	H	H	L	H	H	I2	I2	I2
	12	H	H	H	H	L	H	H	H	I3	I3	I3
	16	H	H	H	L	H	H	H	H	I4	I4	I4
	20	H	H	L	H	H	H	H	H	I5	I5	I5
	24	H	L	H	H	H	H	H	H	I6	I6	I6
	28	L	H	H	H	H	H	H	H	I7	I7	I7
2	1	L	L	L	L	L	L	L	H	/I0	/I0	/I0
	5	L	L	L	L	L	L	H	L	/I1	/I1	/I1
	9	L	L	L	L	L	H	L	L	/I2	/I2	/I2
	13	L	L	L	L	H	L	L	L	/I3	/I3	/I3
	17	L	L	L	H	L	L	L	L	/I4	/I4	/I4
	21	L	L	H	L	L	L	L	L	/I5	/I5	/I5
	25	L	H	L	L	L	L	L	L	/I6	/I6	/I6
	29	H	L	L	L	L	L	L	L	/I7	/I7	/I7
3	2	H	H	H	H	H	H	H	L	F7	B1	B3
	6	H	H	H	H	H	H	L	H	F6	F5	B2
	10	H	H	H	H	H	L	H	H	F5	F4	F3
	14	H	H	H	H	L	H	H	H	F4	F3	F2
	18	H	H	H	L	H	H	H	H	F3	F2	F1
	22	H	H	L	H	H	H	H	H	F2	F1	F0
	26	H	L	H	H	H	H	H	H	F1	F0	B1
	30	L	H	H	H	H	H	H	H	F0	B0	B0
4	3	L	L	L	L	L	L	L	H	/F7	/B1	/B3
	7	L	L	L	L	L	L	H	L	/F6	/F5	/B2
	11	L	L	L	L	L	H	L	L	/F5	/F4	/F3
	15	L	L	L	L	H	L	L	L	/F4	/F3	/F2
	19	L	L	L	H	L	L	L	L	/F3	/F2	/F1
	23	L	L	H	L	L	L	L	L	/F2	/F1	/F0
	27	L	H	L	L	L	L	L	L	/F1	/F0	/B1
	31	H	L	L	L	L	L	L	L	/F0	/B0	/B0
1 or 3	32	H	H	H	H	H	H	H	H	CONFIGURE		

LEGEND: L = Logic Low H = Logic high

NOTE: The configure row can be selected while in either mode 1 or mode 3.

EDIT MODE COLUMN SELECT TABLE 4

COLUMN NUMBER	C6 Pin 13	C5 Pin 14	C4 Pin 15	C3 Pin 16	C2 Pin 17	C1 Pin 18	C0 Pin 19	
0	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	H	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	P
5	L	L	L	L	H	L	H	
6	L	L	L	L	H	H	L	
7	L	L	L	L	H	H	H	
8	L	L	L	H	L	L	L	R
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	O
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	D
18	L	L	H	L	L	H	L	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	L	
21	L	L	H	L	H	L	H	U
22	L	L	H	L	H	H	L	
23	L	L	H	L	H	H	H	
24	L	L	H	H	L	L	L	
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	C
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	T
31	L	L	H	H	H	H	H	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	H	L	
35	L	H	L	L	L	H	H	
36	L	H	L	L	H	L	L	
37	L	H	L	L	H	L	H	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	
40	L	H	L	H	L	L	L	T
41	L	H	L	H	L	L	H	
42	L	H	L	H	L	H	L	
43	L	H	L	H	L	H	H	
44	L	H	L	H	H	L	L	E
45	L	H	L	H	H	L	H	
46	L	H	L	H	H	H	L	
47	L	H	L	H	H	H	H	
48	L	H	H	L	L	L	L	
49	L	H	H	L	L	L	H	R
50	L	H	H	L	L	H	L	
51	L	H	H	L	L	H	H	
52	L	H	H	L	H	L	L	
53	L	H	H	L	H	L	H	M
54	L	H	H	L	H	H	L	
55	L	H	H	L	H	H	H	
56	L	H	H	H	L	L	L	
57	L	H	H	H	L	L	H	S
58	L	H	H	H	L	H	L	
59	L	H	H	H	L	H	H	
60	L	H	H	H	H	L	L	
61	L	H	H	H	H	L	H	
62	L	H	H	H	H	H	L	
63	L	H	H	H	H	H	H	
64	H	L	L	L	L	L	H	MODE VERIFY
65	H	L	L	L	L	L	H	
68	H	L	L	L	H	L	L	Pin 19 P
69	H	L	L	L	H	L	H	Pin 18 C O
70	H	L	L	L	H	H	L	Pin 17 U L
71	H	L	L	L	H	H	H	Pin 16 T A
72	H	L	L	H	L	L	L	Pin 15 P R
73	H	L	L	H	L	L	H	Pin 14 U I
74	H	L	L	H	L	H	L	Pin 13 T T
75	H	L	L	H	L	H	H	Pin 12 Y
76	H	L	L	H	H	L	L	PROTECT

LEGEND: L = Logic Low H = Logic High.