



PAL22V10 Family, AmPAL22V10/A

24-Pin TTL Versatile PAL Device

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns propagation delay and 91 MHz f_{MAX} (external)
- 10 Macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-Pin SKINNYDIP, 24-pin Flatpack and 28-pin PLCC and LCC packages save space

GENERAL DESCRIPTION

The PAL22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

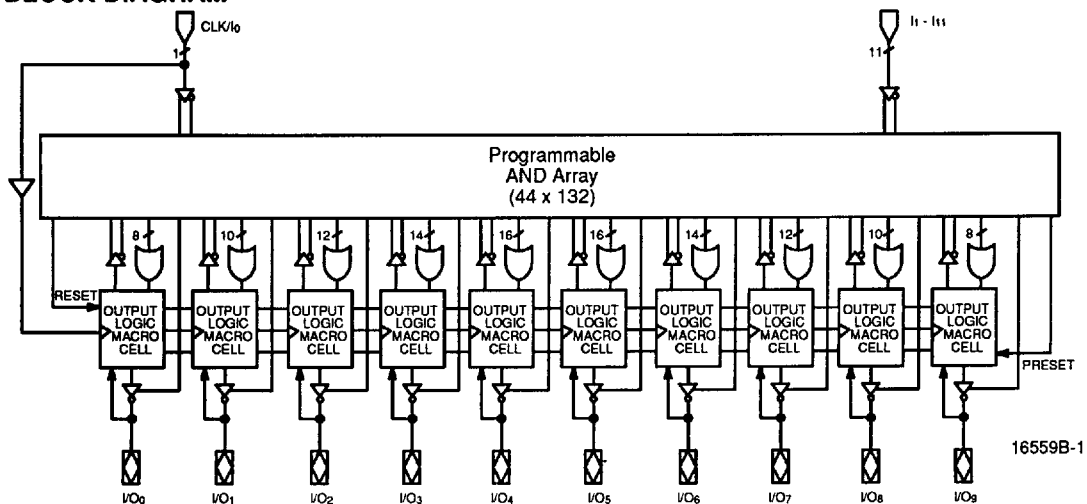
The PAL22V10 device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is

determined by two fuses controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PAL22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

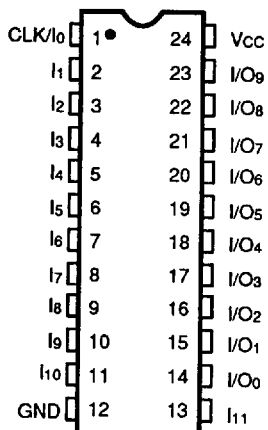
BLOCK DIAGRAM



CONNECTION DIAGRAMS

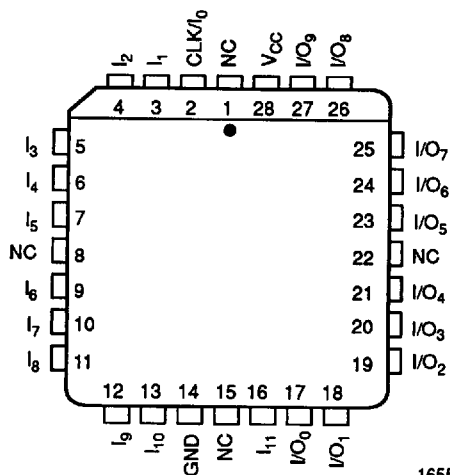
Top View

SKINNYDIP/FLATPACK



16559B-2

PLCC/LCC



16559B-3

Note:

Pin 1 is marked for orientation.

PIN DESIGNATIONS

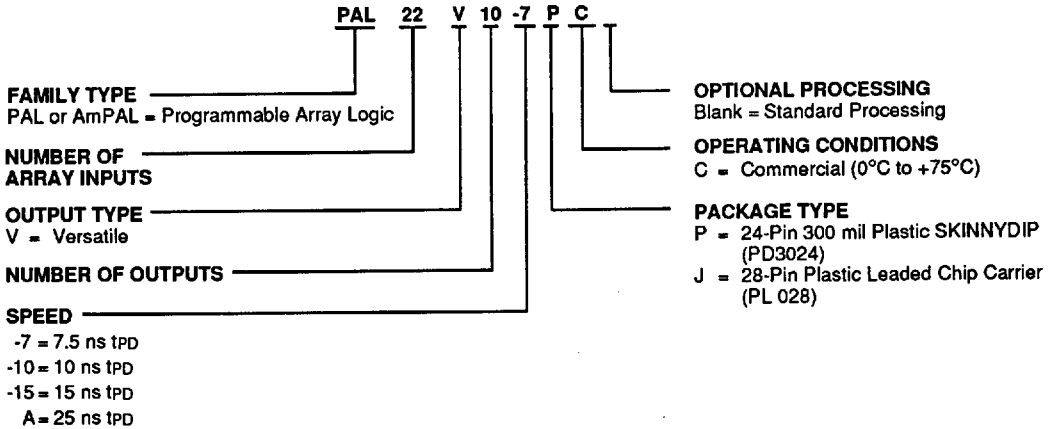
- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V_{cc} = Supply Voltage



ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-7	PC, JC
PAL22V10-10	
PAL22V10-15	
AmPAL22V10A	

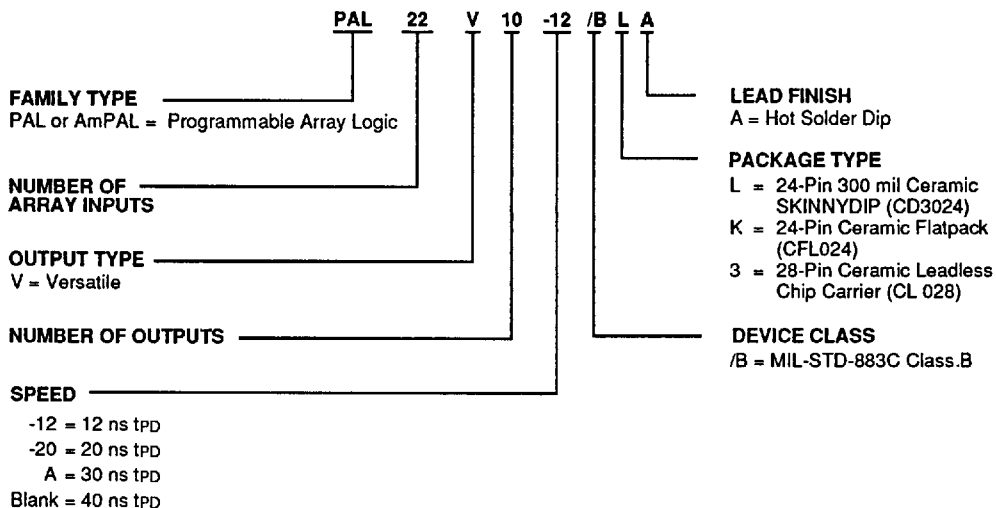
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-12	/BLA, /BKA, /B3A
PAL22V10-20	
AmPAL22V10A	
AmPAL22V10	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PAL22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

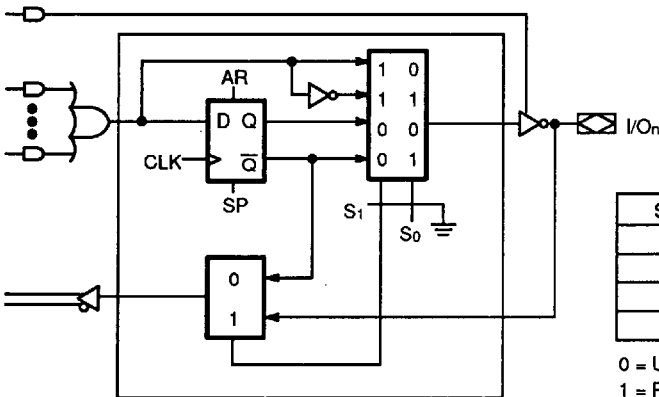
The PAL22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design

specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls initially are connected to ground (0) through a programmable fuse, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Variable Input/Output Pin Ratio

The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{cc} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Unprogrammed fuse
1 = Programmed fuse

16659B-4

Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from \bar{Q} of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

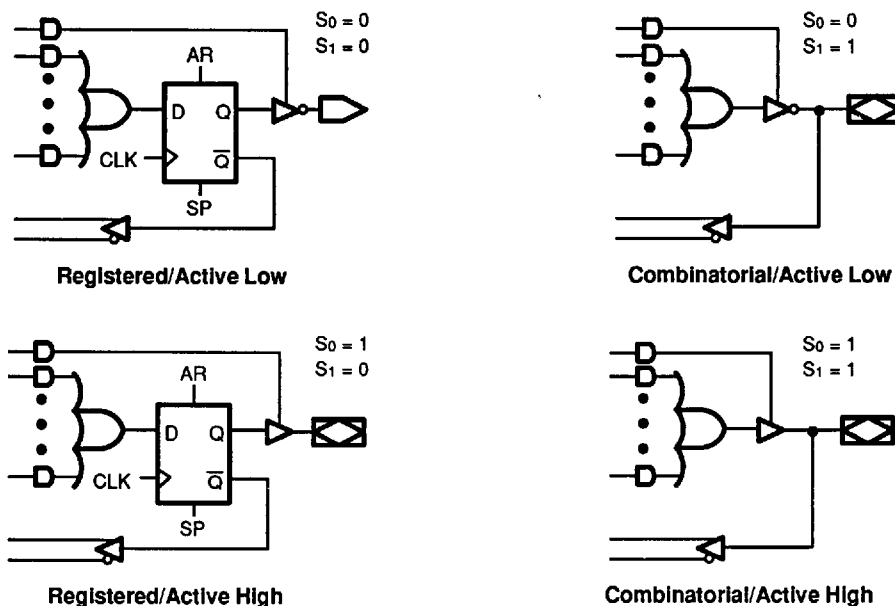


Figure 2. Macrocell Configuration Options

16559B-5

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions.

Preset/Reset

For initialization, the PAL22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

Programming

The PAL22V10 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

Quality and Testability

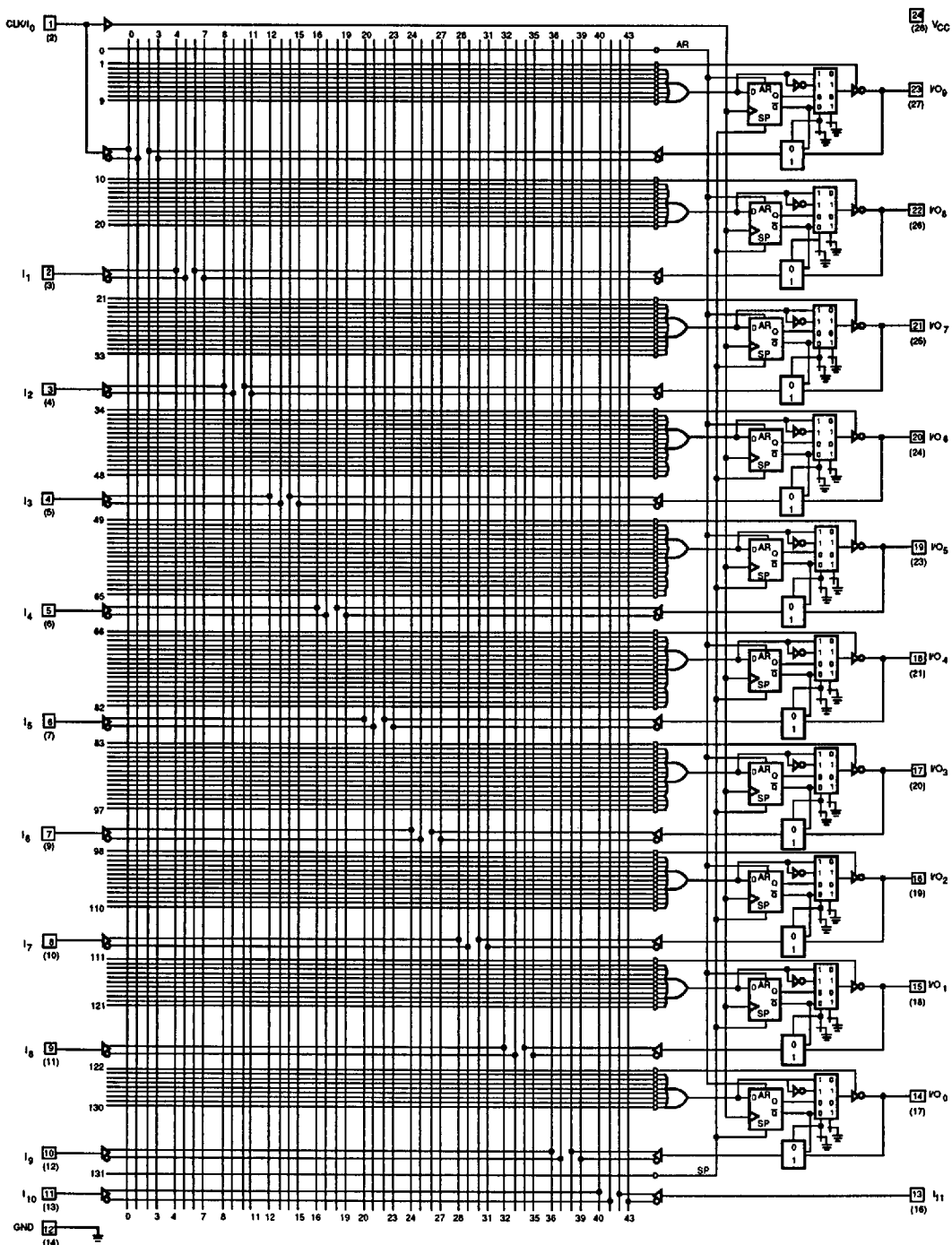
The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses, test words and test columns provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL22V10A is fabricated with AMD's diffusion-isolated bipolar process. The array connections are formed with highly reliable PtSi fuse.

The PAL22V10-15, -10 and -7 are fabricated with AMD's diffusion-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with PtSi fuses on the -15, and TiW fuses on the -7 and -10 for reliable operation.

LOGIC DIAGRAM SKINNYDIP (PLCC/LCC) Pinouts



16559B-6



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (TA)	
Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 16$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)	Input	-100	μ A
			CLK	-150	
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max}$		220	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	Min (Note 3)	Max	Unit	
t _{PD}	Input or Feedback to Combinatorial Output	1	7.5	ns	
t _S	Setup Time from Input, Feedback or SP to Clock	5		ns	
t _H	Hold Time	0		ns	
t _{CO}	Clock to Output	1	6	ns	
t _{SKWR}	Skew Between Registered Outputs (Note 5)		1	ns	
t _{AR}	Asynchronous Reset to Registered Output		12	ns	
t _{ARW}	Asynchronous Reset Width	8		ns	
t _{ARR}	Asynchronous Reset Recovery Time	8		ns	
t _{SPR}	Synchronous Preset Recovery Time	5		ns	
t _{WL}	Clock Width	LOW	4	ns	
t _{WH}		HIGH	4	ns	
f _{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t _S + t _{CO})	91	MHz
		Internal Feedback (f _{CNT})		100	MHz
		No Feedback	1/(t _{WH} + t _{WL})	125	MHz
t _{EA}	Input to Output Enable Using Product Term Control		8	ns	
t _{ER}	Input to Output Disable Using Product Term Control		7.5	ns	

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. Skew is measured with all outputs switching in the same direction.



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC})	with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 16$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_i	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)		25	μ A
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)	Input	-100	μ A
			CLK	-150	
I_i	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μ A
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μ A
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max}$		180	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min (Note 3)	Max	Unit
t _{PD}	Input or Feedback to Combinatorial Output		1	10	ns
t _S	Setup Time from Input, Feedback or SP to Clock		7		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output		1	7	ns
t _{AR}	Asynchronous Reset to Registered Output			15	ns
t _{ARW}	Asynchronous Reset Width		10		ns
t _{ARR}	Asynchronous Reset Recovery Time		8		ns
t _{SPR}	Synchronous Preset Recovery Time		8		ns
t _{WL}	Clock Width	LOW	5		ns
t _{WH}		HIGH	5		ns
f _{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t _S + t _{CO})	71	MHz
		Internal Feedback (f _{CNT})		80	MHz
		No Feedback	1/(t _{WH} + t _{WL})	100	MHz
t _{EA}	Input to Output Enable Using Product Term Control			11	ns
t _{ER}	Input to Output Disable Using Product Term Control			9	ns

Notes:

2. See *Switching Test Circuit* for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Input Current	-30 mA to +5 mA
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground		+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 16$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)		25	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)		-100	μA
I_I	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-100	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)	-30	-130	mA
I_{CC}	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max}$		180	mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
CIN	Input Capacitance	VIN = 2.0 V	VCC = 5.0 V TA = 25°C f = 1 MHz	9	pF
COUT	Output Capacitance	VOUT = 2.0 V		6	
			5		

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min (Note 3)	Max	Unit
tpd	Input or Feedback to Combinatorial Output			15	ns
ts	Setup Time from Input, Feedback or SP to Clock		10		ns
th	Hold Time		0		ns
tco	Clock to Output			10	ns
tar	Asynchronous Reset to Registered Output			20	ns
tarw	Asynchronous Reset Width		15		ns
tarr	Asynchronous Reset Recovery Time		10		ns
tsprr	Synchronous Preset Recovery Time		10		ns
twl	Clock Width	LOW	6		ns
		HIGH	6		ns
fmax	Maximum Frequency (Note 4)	External Feedback	1/(ts + tco)	50	MHz
		Internal Feedback (fcnt)		80	MHz
		No Feedback	1/(twh + twl)	83	MHz
tea	Input to Output Enable Using Product Term Control			15	ns
ter	Input to Output Disable Using Product Term Control			15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to +5.5 V
DC Input Current	-30 mA to +5 mA
DC Output or I/O Pin Voltage	-0.5 V to V _{CC} Max

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T _A)	Operating in Free Air	0°C to +75°C
Supply Voltage (V _{CC})	with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -3.2 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min		-1.2	V
I _{IH}	Input HIGH Current	V _{IN} = 2.7 V, V _{CC} = Max (Note 2)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max (Note 2)		-100	μA
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max		1	mA
I _{OZH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.7 V, V _{CC} = Max V _{IN} = V _{IH} or V _{IL} (Note 2)		100	μA
I _{OZL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
I _{SC}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max (Note 3)	-30	-90	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
CIN	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	11	pF
				6	
COUT	Output Capacitance	V _{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min	Max	Unit
t _{PD}	Input or Feedback to Combinatorial Output			25	ns
t _S	Setup Time from Input, Feedback or SP to Clock		20		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			15	ns
t _{AR}	Asynchronous Reset to Registered Output			30	ns
t _{ARW}	Asynchronous Reset Width		25		ns
t _{ARR}	Asynchronous Reset Recovery Time		35		ns
t _{SPR}	Synchronous Preset Recovery Time		20		ns
t _{WL}	Clock Width	LOW	15		ns
t _{WH}		HIGH	15		ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(t _S + t _{CO})	28.5	MHz
t _{EA}	Input to Output Enable Using Product Term Control			25	ns
t _{ER}	Input to Output Disable Using Product Term Control			25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to +7.0 V
DC Output or I/O Pin Voltage	-0.5 V to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T _A)	Operating in Free Air	-55°C Min
Operating Case (T _C)	Temperature	125°C Max
Supply Voltage (V _{CC})	with Respect to Ground	+4.50 V to +5.50 V

Note:

- Military products are tested at T_C = +25°C, +125°C, and -55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -2 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 12 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V _I	Input Clamp Voltage	I _{IN} = -18 mA, V _{CC} = Min		-1.2	V
I _{IH}	Input HIGH Current	V _{IN} = 2.7 V, V _{CC} = Max (Note 4)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max (Note 4)		-100	μA
		Input CLK		-150	
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max		1	mA
I _{OZH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.7 V, V _{CC} = Max V _{IN} = V _{IH} or V _{IL} (Note 4)		100	μA
I _{OZL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max V _{IN} = V _{IH} or V _{IL} (Note 4)		-100	μA
I _{sc}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max (Note 5)	-30	-130	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max		200	mA

Notes:

- For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min	Max	Unit
t _{PD}	Input or Feedback to Combinatorial Output			12	ns
t _S	Setup Time from Input or Feedback to Clock		10		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			10	ns
t _{AR}	Asynchronous Reset to Registered Output			20	ns
t _{ARW}	Asynchronous Reset Width (Note 3)		15		ns
t _{ARR}	Asynchronous Reset Recovery Time (Note 3)		10		ns
t _{SPR}	Synchronous Preset Recovery Time (Note 4)		10		ns
t _{WL}	Clock Width	LOW	6		ns
t _{WH}		HIGH	6		ns
f _{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t _S + t _{CO})	50	MHz
		Internal Feedback (fc _{NT})		58.8	MHz
		No Feedback	1/(t _{WH} + t _{WL})	83.3	MHz
t _{EA}	Input to Output Enable Using Product Term Control (Note 4)			15	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 4)			12.5	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to +5.5 V
DC Output or I/O Pin Voltage	-0.5 V to +7.0 V
DC Input Current	-30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	-55°C Min
Operating Case (T_C) Temperature	125°C Max
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Note:

1. Military products are tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C , per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -2\text{ mA}$ $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12\text{ mA}$ $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	$I_{IN} = -18\text{ mA}$, $V_{CC} = \text{Min}$		-1.2	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7\text{ V}$, $V_{CC} = \text{Max}$ (Note 4)		25	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.4\text{ V}$, $V_{CC} = \text{Max}$ (Note 4)		-100	μA
I_I	Maximum Input Current	$V_{IN} = 5.5\text{ V}$, $V_{CC} = \text{Max}$		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7\text{ V}$, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4\text{ V}$, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		-100	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5\text{ V}$, $V_{CC} = \text{Max}$ (Note 5)	-30	-90	mA
I_{CC}	Supply Current	$V_{IN} = 0\text{ V}$, Outputs Open ($I_{OUT} = 0\text{ mA}$) $V_{CC} = \text{Max}$		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5\text{ V}$ has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	9	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		6	
			9		

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min	Max	Unit
t _{PD}	Input or Feedback to Combinatorial Output			20	ns
t _s	Setup Time from Input or Feedback to Clock		17		ns
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			15	ns
t _{AR}	Asynchronous Reset to Registered Output			25	ns
t _{ARW}	Asynchronous Reset Width (Note 3)		20		ns
t _{ARR}	Asynchronous Reset Recovery Time (Note 3)		20		ns
t _{SPR}	Synchronous Preset Recovery Time (Note 4)		20		ns
t _{WL}	Clock Width	LOW	15		ns
t _{WH}		HIGH	15		ns
f _{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t _s + t _{CO})	31.2	MHz
		Internal Feedback (f _{CNT})		33.3	MHz
t _{EA}	Input to Output Enable Using Product Term Control (Note 4)			20	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 4)			20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_s and t_{AR}.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to +5.5 V
DC Output or I/O Pin Voltage ...	-0.5 V to V _{CC} Max
DC Input Current	-30 mA to +5 mA
Output Sink Current	100 mA (Note 6)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T _A) Operating in Free Air	-55°C Min
Operating Case Temperature (T _C)	125°C Max
Supply Voltage (V _{CC}) with Respect to Ground	+4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and -55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -2 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min	2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 12 mA V _{IN} = V _{IH} or V _{IL} V _{CC} = Min		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V _I	Input Clamp Voltage	I _{IIN} = -18 mA, V _{CC} = Min		-1.2	V
I _{IH}	Input HIGH Current	V _{IN} = 2.7 V, V _{CC} = Max (Note 4)		25	μA
I _{IL}	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max (Note 4)		-100	μA
I _I	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max		1	mA
I _{OZH}	Off-State Output Leakage Current HIGH	V _{OUT} = 2.7 V, V _{CC} = Max V _{IN} = V _{IH} or V _{IL} (Note 4)		100	μA
I _{OZL}	Off-State Output Leakage Current LOW	V _{OUT} = 0.4 V, V _{CC} = Max V _{IN} = V _{IH} or V _{IL} (Note 4)		-100	μA
I _{SC}	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max (Note 5)	-30	-90	mA
I _{CC}	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C _{IN}	Input Capacitance	Pins 1, 13	V _{IN} = 2.0 V	V _{CC} = 5.0 V T _A = 25°C f = 1 MHz	11	pF
		Others			6	
C _{OUT}	Output Capacitance		V _{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

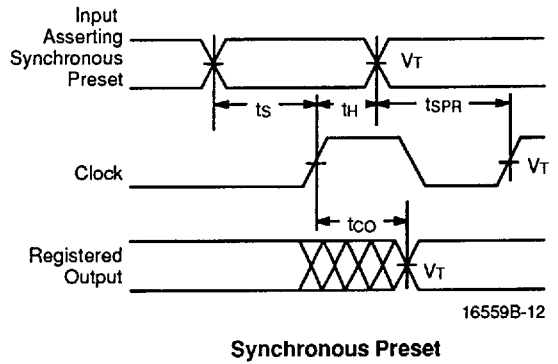
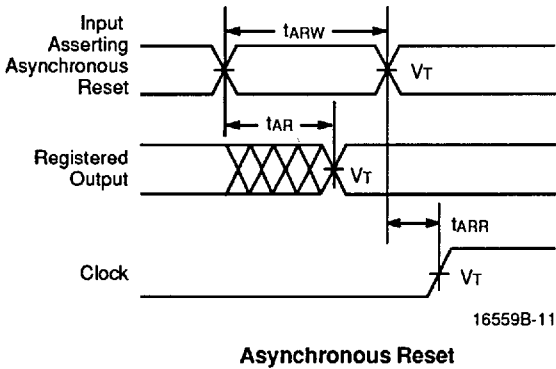
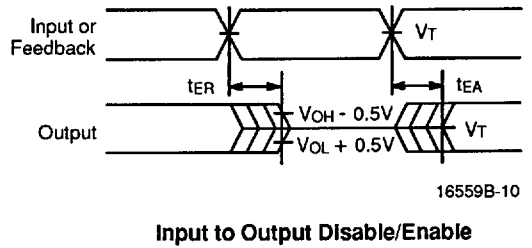
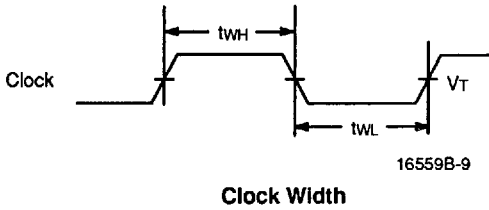
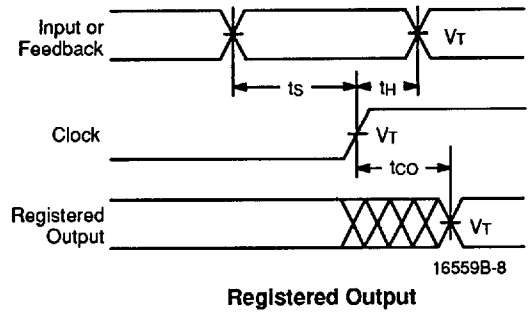
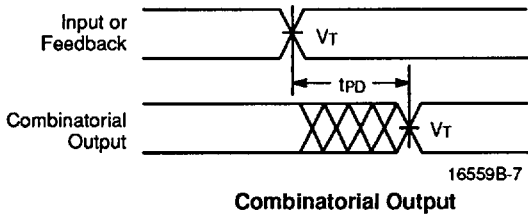
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		A		Std		Unit
			Min	Max	Min	Max	
t _{PD}	Input or Feedback to Combinatorial Output			30		40	ns
t _s	Setup Time from Input or Feedback to Clock		25			35	ns
t _H	Hold Time		0		0		ns
t _{CO}	Clock to Output			20		25	ns
t _{AR}	Asynchronous Reset to Registered Output			35		45	ns
t _{ARW}	Asynchronous Reset Width (Note 3)		30		40		ns
t _{ARR}	Asynchronous Reset Recovery Time (Note 3)		30		40		ns
t _{WL}	Clock Width	LOW	20		30		ns
		HIGH	20		30		ns
f _{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t _s + t _{CO})	22		16.5	MHz
t _{EA}	Input to Output Enable Using Product Term Control (Note 5)			30		40	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 5)			30		40	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_s and t_{AR}.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

SWITCHING WAVEFORMS



Notes:

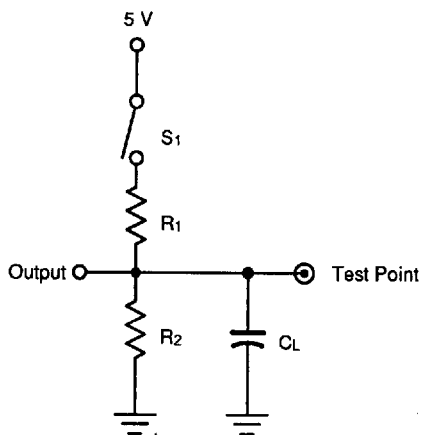
1. $V_T = 1.5\text{ V}$.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns – 4 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



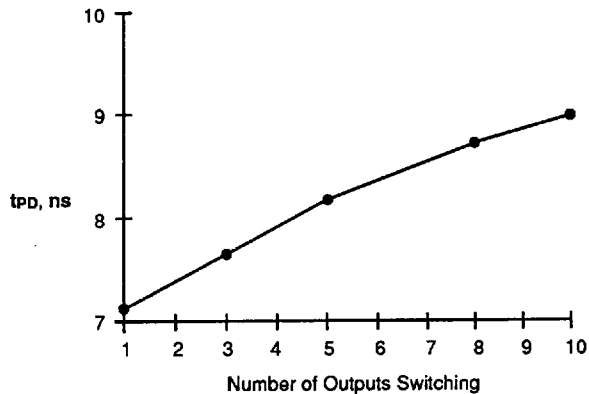
16559B-13

Specification	S ₁	C _L	Commercial		Military		Measured Output Value
			R ₁	R ₂	R ₁	R ₂	
t _{PD} , t _{CO}	Closed	50 pF	300 Ω	All except -7: 390 Ω	390 Ω	750 Ω	1.5 V
t _{EA}	Z → H: Open Z → L: Closed						1.5 V
t _{ER}	H → Z: Open L → Z: Closed	5 pF		-7: 300 Ω			H → Z: V _{OH} - 0.5 V L → Z: V _{OL} + 0.5 V



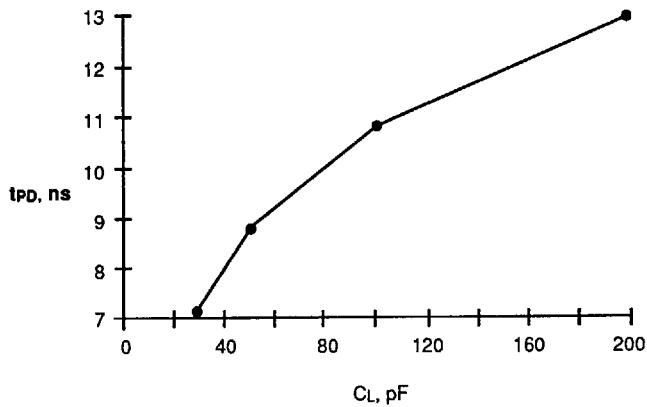
MEASURED SWITCHING CHARACTERISTICS for the PAL22V10-10

$V_{CC} = 4.75 \text{ V}$, $T_A = 75^\circ\text{C}$ (Note 1)



t_{PD} vs. Number of Outputs Switching

16559B-14



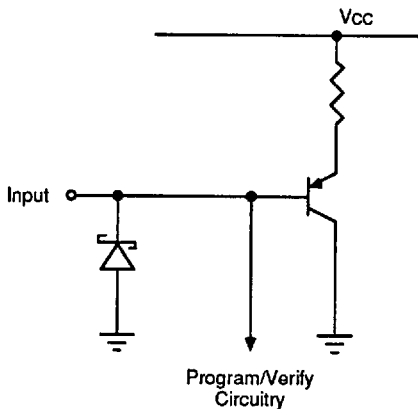
t_{PD} vs. Load Capacitance

16559B-15

Note:

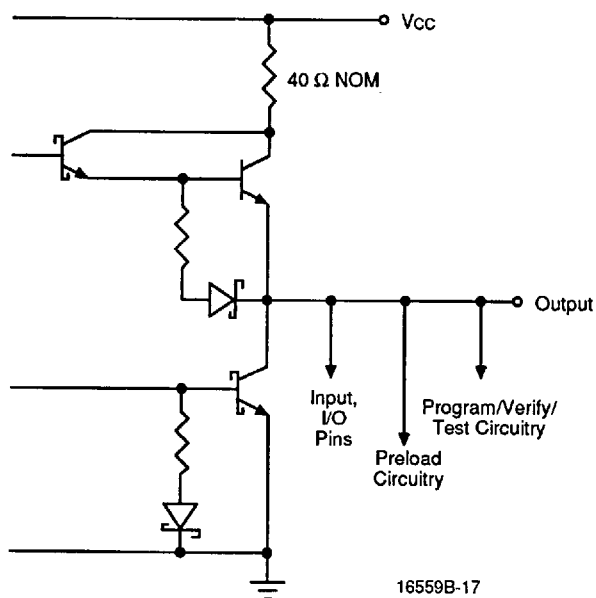
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



16559B-16

Typical Input



16559B-17

Typical Output

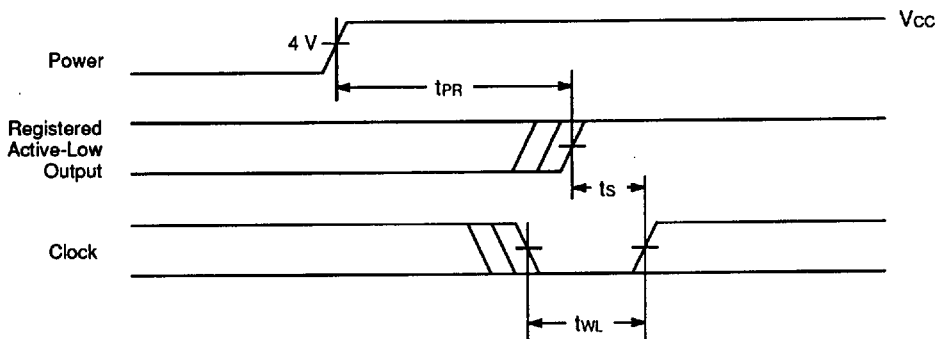
POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC}

can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_s	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



16559B-18

Power-Up Reset Waveform