Rochester Electronics®

Datasheet

XC3100, XC3100A

Logic Cell Array Families

XC3100 and XC3100A are performance-optimized relatives of the XC3000 and XC3000A families. While all families are footprint compatible, the XC3100 and XC3100A families extend the system performance beyond 80 MHz.

The XC3100 and XC3100A families follow the XC4000 speed-grade nomenclature, indicating device performance with a number that is based on the internal logic-block delay, in ns.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

XC3100, XC3100A Logic Cell Array Families

Product Specifications

Features

- Two ultra-high-speed FPGA families with six members each
  - 50-80 MHz system clock rates
  - 190 to 270 MHz guaranteed flip-flop toggle rates
  - 2.7 to 4.1 ns logic delays
- High-end additional family members in the 22 X 22 CLB array-size XC3195 and XC3195A devices
- 8 mA output sink current and 8 mA source current
- Maximum power-down and quiescent current is 5 mA
- Both families are 100% architecture and pin-out compatible with other XC3000 families
- Beyond this, XC3100 is also software and bitstream compatible with the XC3000 family, while XC3100A is software and bitstream compatible with the XC3000A and XC3000L families

The XC3100A family is recommended for all new designs, since it offers improved functionality and enhanced development system support

XC3100A combines the features of the XC3000A and XC3100 families.

- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

Description

XC3100 and XC3100A are performance-optimized relatives of the XC3000 and XC3000A families. While all families are footprint compatible, the XC3100 and XC3100A families extend the system performance beyond 80 MHz.

The XC3100 and XC3100A families follow the XC4000 speed-grade nomenclature, indicating device performance with a number that is based on the internal logic-block delay, in ns.

The XC3100A family offers the following enhancements over the popular XC3100 family.

The XC3100A family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3100A devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in all XC3000 families, determined by the individual configuration option.

The XC3100A family is a superset of the XC3000 families. Any bitstream used to configure an XC3000, XC3000A, XC3000L or XC3100 device, will configure the same-size XC3100A device exactly the same way.

Device	CLBs	Array	User I/O Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3120 / XC3120A	64	8 x 8	64	256	16	14,779
XC3130 / XC3130A	100	10 x 10	80	360	20	22,176
XC3142 / XC3142A	144	12 x 12	96	480	24	30,784
XC3164 / XC3164A	224	16 x 14	120	688	28	46,064
XC3190 / XC3190A	320	16 x 20	144	928	40	64,160
XC3195 / XC3195A	484	22 x 22	176	1,320	44	94,944

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial –40°C to +85°C	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

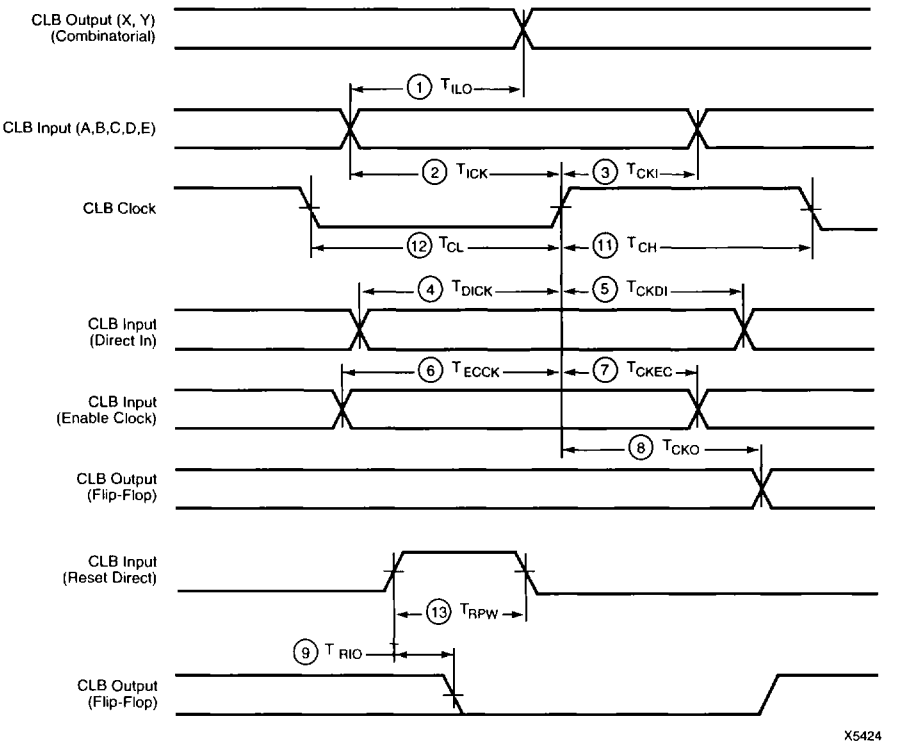
DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} max)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} max)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCO}	Quiescent LCA supply current Chip thresholds programmed as CMOS levels[1]			8	mA
	Chip thresholds programmed as TTL levels			14	mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low		0.20	2.80	mA

Note: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120 in the PC84 package, to eight for the XC3195 in the PQ208 or PG223 package.

CLB Switching Characteristic Guidelines



Buffer (Internal) Switching Characteristic Guidelines

Speed Grade		-5	-4	-3	-2	
Description	**Symbol**	**Max**	**Max**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution*						
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	6.8	6.5	5.6	5.2	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	5.4	5.1	4.3	4.0	ns
TBUF driving a Horizontal Long line (L.L.)*						
I to L.L. while T is Low (buffer active) (XC3100)	T_{IO}	4.1	3.7	3.1		ns
(XC3100A)	T_{IO}	3.6	3.6	3.1	3.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	5.6	5.0	4.2	4.2	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	7.1	6.5	5.7	5.7	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	15.6	13.5	11.4	11.4	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	12.0	10.5	8.8	8.1	ns
BIDI						
Bidirectional buffer delay	T_{BIDI}	1.4	1.2	1.0	0.9	ns

* Timing is based on the XC3142, for other devices see XACT timing calculator.

CLB Switching Characteristic Guidelines (continued)

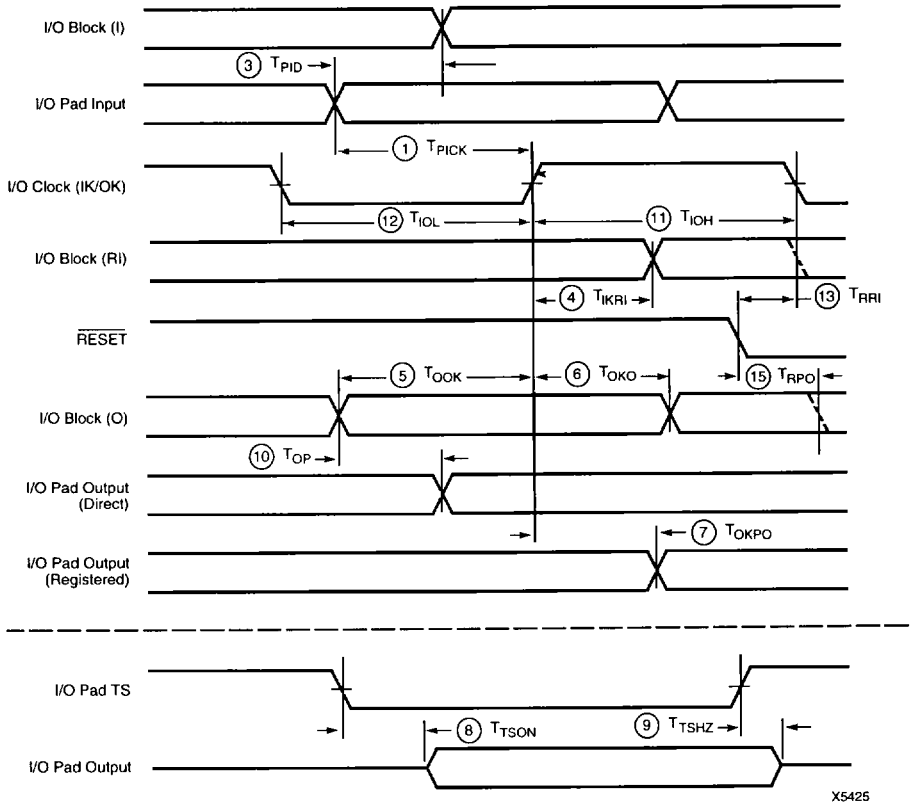
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

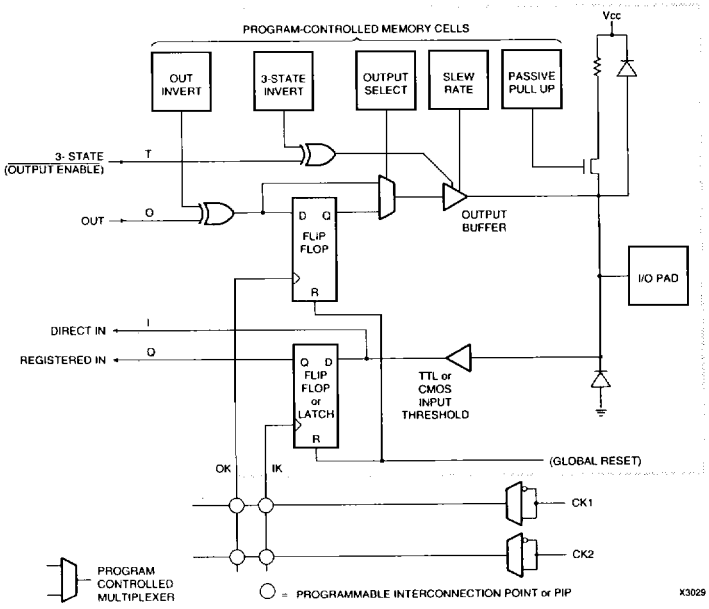
Speed Grade			-5		-4		-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay											
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		4.1		3.3		2.7		2.2	ns
Sequential delay											
Clock K to outputs X or Y	8	T_{CKO}		3.1		2.5		2.1		1.7	ns
Clock K to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		6.3		5.2		4.3		3.5	ns
Set-up time before clock K											
Logic Variables A, B, C, D, E	2	T_{ICK}	3.1		2.5		2.1		1.8		ns
Data In DI	4	T_{DICK}	2.0		1.6		1.4		1.3		ns
Enable Clock EC	6	T_{ECCK}	3.8		3.2		2.7		2.5		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		ns
Hold Time after clock k											
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		1.0		0.9		0.9		ns
Enable Clock EC	7	T_{CKEC}	1.0		0.8		0.7		0.7		ns
Clock											
Clock High time	11	T_{CH}	2.4		2.0		1.6		1.3		ns
Clock Low time	12	T_{CL}	2.4		2.0		1.6		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	190		230		270		325		MHz
Reset Direct (RD)											
RD width	13	T_{RPW}	3.8		3.2		2.7		2.3		ns
delay from RD to outputs X or Y	9	T_{RIO}		4.4		3.7		3.1		2.7	ns
Global Reset, from $\overline{\text{RESET}}$ Pad, based on XC3142 and XC3142A											
$\overline{\text{RESET}}$ width (Low) (XC3142)		T_{MRW}	18.0		15.0		13.0				ns
(XC3142A)		T_{MRW}	14.0		14.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		17.0		14.0		12.0		12.0	ns

Notes: The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100 family increases by 0.60 ns (-5), 0.6 ns (-4) and 0.5 ns (-3) and each of these specifications for the XC3100A family increses by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3).

IOB Switching Characteristic Guidelines





IOB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-5		-4		-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)											
Pad to Direct In (I)	3	T_{PID}		2.8		2.5		2.2		2.0	ns
Pad to Registered In (q) with											
latch transparent (XC3100A)		T_{PTG}		14.0		12.0		11.0		11.0	ns
(XC3100)		T_{PTG}		16.0		15.0		13.0			ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		2.8		2.5		2.2		1.9	ns
Set-up Time (Input)											
Pad to Clock (IK) set-up time											
XC3100 Family	1	T_{PICK}	15.0		14.0		12.0				ns
XC3120A,XC3130A			10.9		10.6		9.4		8.9		ns
XC3142A			11.0		10.7		9.5		9.0		ns
XC3164A			11.2		11.0		9.7		9.2		ns
XC3190A			11.5		11.2		9.9		9.4		ns
XC3195A			12.0		11.6		10.3		9.8		ns
Propagation Delays (Output)											
Clock (OK) to Pad (fast)	7	T_{OKPO}		5.5		5.0		4.4		4.0	ns
same (slew-rate limited)	7	T_{OKPO}		14.0		12.0		10.0		9.7	ns
Output (O) to Pad (fast)	10	T_{OPF}		4.1		3.7		3.3		3.0	ns
same (slew-rate limited) (XC3100A)	10	T_{OPS}		12.1		11.0		9.0		8.7	ns
(XC3100)	10	T_{OPF}		13.0		11.0		9.0			ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		6.9		6.2		5.5		5.0	ns
same (slew-rate limited)	9	T_{TSHZ}		6.9		6.2		5.5		5.0	ns
3-state to Pad active and valid (fast) (XC3100A)	8	T_{TSON}		10.0		10.0		9.0		8.5	ns
same (slew-rate limited)	8	T_{TSON}		18.0		17.0		15.0		14.2	ns
3-state to Pad active and valid (fast) (XC3100)	8	T_{TSON}		12.0		10.0		9.0			ns
same (slew-rate limited)	8	T_{TSON}		20.0		17.0		15.0			ns
Set-up and Hold Times (Output)											
Output (O) to clock (OK) set-up time,(XC3100A)	5	T_{OOK}	5.0		4.5		4.0		3.6		ns
(XC3100)	5	T_{OOK}	6.2		5.6		5.0				ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		0		0		ns
Clock											
Clock High time	11	T_{IOH}	2.4		2.0		1.6		1.3		ns
Clock Low time	12	T_{IOL}	2.4		2.0		1.6		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	190.0		230.0		270.0		325.0		MHz
Global Reset Delays											
$\overline{\text{RESET}}$ Pad to Registered In (Q),											
(XC3120/XC3120A)	13	T_{RRI}		18.0		15.0		13.0		13.0	ns
(XC3195/XC3195A)				29.5		25.0		21.0		21.0	ns
$\overline{\text{RESET}}$ Pad to output pad (fast)	15	T_{RPO}		24.0		20.0		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		32.0		27.0		23.0		23.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see XAPP 024. Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTAL2 when the pin is configured as a user input.

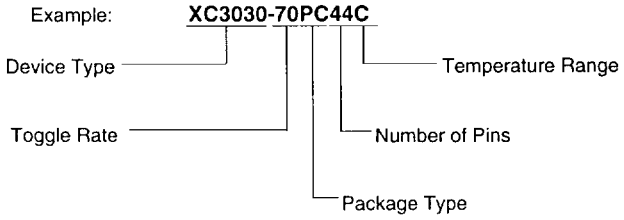
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3120	-5			C I	C I	C I	C I (M B)			(M B)										
	-4			C I	C I	C I	C I													
	-3			C	C	C	C													
XC3130	-5	C I		C I	C I	C I	C I	C												
	-4	C I		C I	C I	C I	C I	C												
	-3	C		C	C	C	C	C												
XC3142	-5				C I	C I	C I (M B)	C		(M B)	C	C I (M B)	C I							
	-4				C I	C I	C I	C			C	C I	C I							
	-3				C	C	C	C			C	C	C							
XC3164	-5				C I						C I	C I		C I						
	-4				C I						C I	C I		C I						
	-3				C						C	C		C						
XC3190	-5				C I									C I	(M B)	C I	C I (M B)		C I	
	-4				C I									C I		C I	C I		C I	
	-3				C									C		C	C		C	
XC3195	-5				C I									C I		C I	C I (M B)		C I	C I (M B)
	-4				C I									C I		C I	C I		C I	C I
	-3				C									C		C	C		C	C
XC3120A	-5			C I	C I	C I	C I (M B)			(M B)										
	-4			C I	C I	C I	C I													
	-3			C	C	C	C													
	-2			C	C	C	C													
XC3130A	-5	C I		C I	C I	C I	C I		C											
	-4	C I		C I	C I	C I	C I		C											
	-3	C		C	C	C	C		C											
	-2	C		C	C	C	C		C											
XC3142A	-5				C I	C I	C I (M B)		C	(M B)	C	C I (M B)	C I							
	-4				C I	C I	C I		C		C	C I	C I							
	-3				C	C	C		C		C	C	C							
	-2				C	C	C		C		C	C	C							
XC3164A	-5				C I						C I	C I	C I	C I						
	-4				C I						C I	C I	C I	C I						
	-3				C						C	C	C	C						
	-2				C						C	C	C	C						
XC3190A	-5				C I									C I	(M B)	C I	C I (M B)	C I	C I	
	-4				C I									C I		C I	C I	C I	C I	
	-3				C									C		C	C	C	C	
	-2				C									C		C	C	C	C	
XC3195A	-5				C I									C I		C I	C I (M B)		C I	C I (M B)
	-4				C I									C I		C I	C I		C I	C I
	-3				C									C		C	C		C	C
	-2				C									C		C	C		C	C

C = Commercial = 0° to +70° C I = Industrial = -40° to +85° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

Parentheses indicate future product plans