

## Description

The TSV639x series of dual and quad operational amplifiers (op amps) offers low voltage operation and rail-to-rail input and output.

For applications configured with gain, the TSV639x series offers an excellent speed/power consumption ratio, 2.4 MHz gain bandwidth product while consuming only 60  $\mu$ A at 5 V. The devices also feature an ultra-low input bias current and have a shutdown mode (TSV6393, TSV6395).

These features make the TSV639x family ideal for sensor interfaces, battery supplied and portable applications, as well as active filtering.

## Features

- Rail-to-rail input and output
- Low-power consumption: 60  $\mu$ A typ at 5 V
- Low supply voltage: 1.5 V - 5.5 V
- Gain bandwidth product: 2.4 MHz typ, stable for gain equal or above -3 or 4
- Low-power shutdown mode: 5 nA typ
- Low offset voltage: 800  $\mu$ V max (A version)
- Low input bias current: 1 pA typ
- EMI hardened operational amplifiers
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40  $^{\circ}$ C to 125  $^{\circ}$ C

## Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

## Package pin connections

Figure 1: Pin connections for each package (top view)



## Absolute maximum ratings and operating conditions

**Table 2: Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V	
$V_{id}$	Differential input voltage <sup>(2)</sup>	$\pm V_{CC}$		
$V_{in}$	Input voltage <sup>(3)</sup>	$(V_{CC}^-) - 0.2$ to $(V_{CC}^+) + 0.2$		
$I_{in}$	Input current <sup>(4)</sup>	10	mA	
$\overline{SHDN}$	Shutdown voltage <sup>(3)</sup>	$(V_{CC}^-) - 0.2$ to $(V_{CC}^+) + 0.2$	V	
$T_{stg}$	Storage temperature	-65 to 150	°C	
$T_j$	Maximum junction temperature	150		
$R_{thja}$	Thermal resistance junction to ambient <sup>(5)/(6)</sup>	SOP-8	125	°C/W
		TSSOP14	100	
ESD	HBM: human body model <sup>(7)</sup>	4	kV	
	MM: machine model <sup>(8)</sup>	300	V	
	CDM: charged device model <sup>(9)</sup>	1.5	kV	
	Latch-up immunity	200	mA	

**Notes:**

- <sup>(1)</sup>All voltage values, except the differential voltage are with respect to the network ground terminal.
- <sup>(2)</sup>Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- <sup>(3)</sup> $V_{CC} - V_{in}$  must not exceed 6 V,  $V_{in}$  must not exceed 6 V.
- <sup>(4)</sup>The input current must be limited by a resistor in-series with the inputs.
- <sup>(5)</sup> $R_{th}$  are typical values.
- <sup>(6)</sup>Short-circuits can cause excessive heating and destructive dissipation.
- <sup>(7)</sup>Human body model: 100 pF discharged through a 1.5 k $\Omega$  resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- <sup>(8)</sup>Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5  $\Omega$ ), done for all couples of pin combinations with other pins floating.
- <sup>(9)</sup>Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

**Table 3: Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	1.5 to 5.5	V
$V_{icm}$	Common-mode input voltage range	$(V_{CC}^-) - 0.1$ to $(V_{CC}^+) + 0.1$	
$T_{oper}$	Operating free-air temperature range	-40 to 125	°C

## Electrical characteristics

Table 4: Electrical characteristics at  $V_{CC+} = 1.8$  V with  $V_{CC-} = 0$  V,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25$  °C, and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV639x			3	mV
		TSV639xA			0.8	
		$T_{min} < T_{op} < T_{max}$ , TSV639x			4.5	
		$T_{min} < T_{op} < T_{max}$ , TSV639xA			2	
$DV_{io}$	Input offset voltage drift			2		$\mu$ V/°C
$I_{io}$	Input offset current, $V_{out} = V_{CC}/2$			1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current, $V_{out} = V_{CC}/2$			1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 1.8 V, $V_{out} = 0.9$ V	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			
$A_{vd}$	Large signal voltage gain	$R_L = 10$ k $\Omega$ , $V_{out} = 0.5$ V to 1.3 V	85	95		dB
		$T_{min} < T_{op} < T_{max}$	80			
$V_{OH}$	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	$R_L = 10$ k $\Omega$		5	35	mV
		$R_L = 10$ k $\Omega$ , $T_{min} < T_{op} < T_{max}$			50	
$V_{OL}$	Low-level output voltage	$R_L = 10$ k $\Omega$		4	35	mV
		$R_L = 10$ k $\Omega$ , $T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	$I_{sink}$	$V_o = 1.8$ V	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	$I_{source}$	$V_o = 0$ V	6	10		
		$T_{min} < T_{op} < T_{max}$	4			
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	40	50	60	$\mu$ A
		$T_{min} < T_{op} < T_{max}$			62	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10$ k $\Omega$ , $C_L = 100$ pF		2		MHz
Gain	Minimum gain for stability	Phase margin = 60 °, $R_f = 10$ k $\Omega$ , $R_L = 10$ k $\Omega$ , $C_L = 20$ pF		4		V/V
				-3		
SR	Slew rate	$R_L = 10$ k $\Omega$ , $C_L = 100$ pF, $V_{out} = 0.5$ V to 1.3 V		0.7		V/ $\mu$ s
$e_n$	Equivalent input noise voltage	$f = 1$ kHz		60		nV/ $\sqrt$ Hz
		$f = 10$ kHz		33		

Micropower (60  $\mu$ A), wide bandwidth (2.4 MHz) CMOS op amps

**Table 5: Shutdown characteristics VCC = 1.8 V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
I <sub>CC</sub>	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{CC^-}$		2.5	50	nA
		T <sub>min</sub> < T <sub>op</sub> < 85 °C			200	
		T <sub>min</sub> < T <sub>op</sub> < 125 °C			1.5	$\mu$ A
t <sub>on</sub>	Amplifier turn-on time	R <sub>L</sub> = 2 k $\Omega$ , V <sub>out</sub> = (V <sub>CC^-</sub> ) to (V <sub>CC^-</sub> ) + 0.2 V		200		ns
t <sub>off</sub>	Amplifier turn-off time	R <sub>L</sub> = 2 k $\Omega$ , V <sub>out</sub> = (V <sub>CC^+</sub> ) - 0.5 V to (V <sub>CC^+</sub> ) - 0.7 V		20		
V <sub>IH</sub>	$\overline{\text{SHDN}}$ logic high		1.35			V
V <sub>IL</sub>	$\overline{\text{SHDN}}$ logic low				0.6	
I <sub>IH</sub>	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC^+}$		10		pA
I <sub>IL</sub>	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC^-}$		10		
I <sub>OLeak</sub>	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC^-}$		50		
		T <sub>min</sub> < T <sub>op</sub> < 125 °C		1		nA

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**Table 6: Electrical characteristics at VCC+ = 3.3 V, VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, RL connected to VCC/2 (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV639x			3	mV
		TSV639xA			0.8	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV639x			4.5	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV639xA			2	
DV <sub>io</sub>	Input offset voltage drift			2		$\mu$ V/°C
I <sub>io</sub>	Input offset current			1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			1	
I <sub>ib</sub>	Input bias current			1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			1	
CMR	Common mode rejection ratio 20 log ( $\Delta V_{ic}/\Delta V_{io}$ )	0 V to 3.3 V, V <sub>out</sub> = 1.65 V	57	79		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	53			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 k $\Omega$ , V <sub>out</sub> = 0.5 V to 2.8 V	88	98		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	83			
V <sub>OH</sub>	High-level output voltage, V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub>	R <sub>L</sub> = 10 k $\Omega$		6	35	mV
		R <sub>L</sub> = 10 k $\Omega$ , T <sub>mi.</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 k $\Omega$		7	35	mV
		R <sub>L</sub> = 10 k $\Omega$ , T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>o</sub> = 3.3 V	23	45		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	20			
	I <sub>source</sub>	V <sub>o</sub> = 0 V	23	38		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	20			
I <sub>CC</sub>	Supply current (per operator)	No load, V <sub>out</sub> = 1.75 V	43	55	64	$\mu$ A
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			66	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 10 k $\Omega$ , C <sub>L</sub> = 100 pF		2.2		MHz
Gain	Minimum gain for stability	Phase margin = 60°, R <sub>f</sub> = 10 k $\Omega$ , R <sub>L</sub> = 10 k $\Omega$ , C <sub>L</sub> = 20 pF		4		V/V
				-3		
SR	Slew rate	R <sub>L</sub> = 10 k $\Omega$ , C <sub>L</sub> = 100 pF, V <sub>out</sub> = 0.5 V to 2.8 V		0.9		V/ $\mu$ s

Micropower (60  $\mu$ A), wide bandwidth (2.4 MHz) CMOS op amps

**Table 7: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL connected to VCC/2 (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltages	TSV639x			3	mV
		TSV639xA			0.8	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV639x			4.5	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV639xA			2	
DV <sub>io</sub>	Input offset voltage drift		2			$\mu$ V/°C
I <sub>io</sub>	Input offset current, V <sub>out</sub> = V <sub>CC</sub> /2			1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current, V <sub>out</sub> = V <sub>CC</sub> /2			1	10 <sup>(1)</sup>	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio 20 log ( $\Delta$ V <sub>ic</sub> / $\Delta$ V <sub>io</sub> )	0 V to 5 V, V <sub>out</sub> = 2.5 V	60	80		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	55			
SVR	Supply voltage rejection ratio 20 log ( $\Delta$ V <sub>CC</sub> / $\Delta$ V <sub>io</sub> )	V <sub>CC</sub> = 1.8 to 5 V	75	93		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	73			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 k $\Omega$ , V <sub>out</sub> = 0.5 V to 4.5 V	89	98		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	84			
EMIRR	EMI rejection ratio, EMIRR = -20 log (V <sub>RFpeak</sub> / $\Delta$ V <sub>io</sub> )	V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 400 MHz		61		dB
		V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 900 MHz		85		
		V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 1800 MHz		92		
		V <sub>RF</sub> = 100 mV <sub>rms</sub> , f = 2400 MHz		83		
V <sub>OH</sub>	High-level output voltage, V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub>	R <sub>L</sub> = 10 k $\Omega$		7	35	mV
		R <sub>L</sub> = 10 k $\Omega$ , T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 k $\Omega$		6	35	mV
		R <sub>L</sub> = 10 k $\Omega$ , T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>o</sub> = 5 V	40	65		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	35			
	I <sub>source</sub>	V <sub>o</sub> = 0 V	40	72		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	35			
I <sub>CC</sub>	Supply current (per operator)	No load, V <sub>out</sub> = V <sub>CC</sub> /2	50	60	69	$\mu$ A
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			72	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 10 k $\Omega$ , C <sub>L</sub> = 100 pF		2.4		MHz
Gain	Minimum gain for stability	Phase margin = 60°, R <sub>f</sub> = 10 k $\Omega$ , R <sub>L</sub> = 10 k $\Omega$ , C <sub>L</sub> = 20 pF,		4		V/V
				-3		
SR	Slew rate	R <sub>L</sub> = 10 k $\Omega$ , C <sub>L</sub> = 100 pF		1.1		V/ $\mu$ s

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$e_n$	Equivalent input noise voltage	$f = 1 \text{ kHz}$		60		nV/ $\sqrt{\text{Hz}}$
		$f = 10 \text{ kHz}$		33		
THD+N	Total harmonic distortion + noise	$V_{CC} = 5 \text{ V}$ , $f_{in} = 1 \text{ kHz}$ , $A_{CL} = -10$ , $R_L = 100 \text{ k}\Omega$ , $V_{icm} = V_{CC}/2$ , $BW = 22 \text{ kHz}$ , $V_{out} = 1 \text{ V}_{rms}$		0.015		%

**Table 8: Shutdown characteristics at  $V_{CC} = 5 \text{ V}$**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{CC}^-$		5	50	nA
		$T_{min} < T_{op} < 85 \text{ }^\circ\text{C}$			200	
		$T_{min} < T_{op} < 125 \text{ }^\circ\text{C}$				1.5
$t_{on}$	Amplifier turn-on time	$R_L = 2 \text{ k}\Omega$ , $V_{out} = (V_{CC}^-) \text{ V to } (V_{CC}^-) + 0.2 \text{ V}$		200		ns
$t_{off}$	Amplifier turn-off time	$R_L = 2 \text{ k}\Omega$ , $V_{out} = (V_{CC}^+) - 0.5 \text{ V to } (V_{CC}^+) - 0.7 \text{ V}$		20		
$V_{IH}$	$\overline{\text{SHDN}}$ logic high		2			V
$V_{IL}$	$\overline{\text{SHDN}}$ logic low				0.8	V
$I_{IH}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC}^+$		10		pA
$I_{IL}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC}^-$		10		
$I_{OLeak}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC}^-$		50		nA
		$T_{min} < T_{op} < 125 \text{ }^\circ\text{C}$		1		

**Electrical characteristic curves**

Figure 2: Supply current vs. supply voltage at  $V_{icm} = V_{CC}/2$

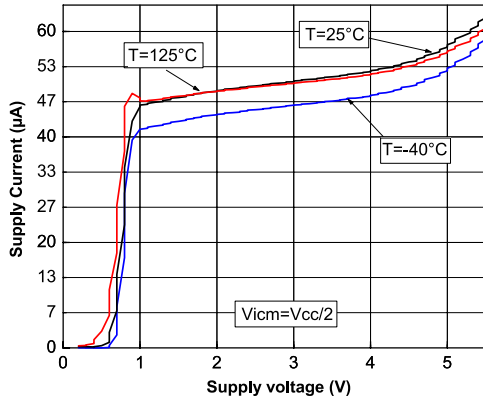


Figure 3: Output current vs. output voltage at  $V_{CC} = 1.5$  V

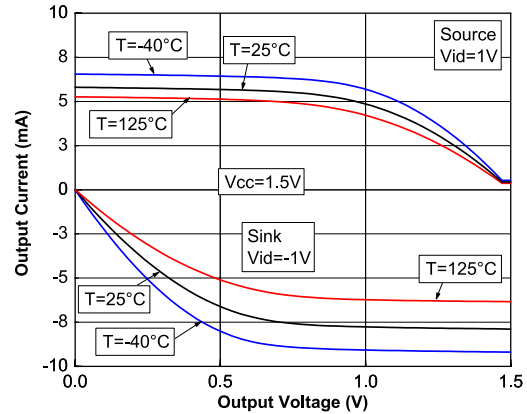


Figure 4: Output current vs. output voltage at  $V_{CC} = 5$  V

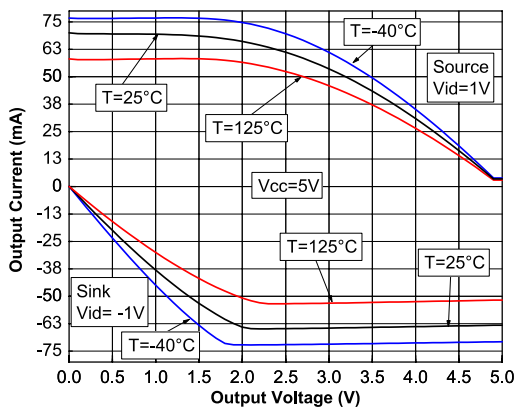


Figure 5: Closed loop response for gain = -10, at  $V_{CC} = 1.5$  V and  $V_{CC} = 5$  V

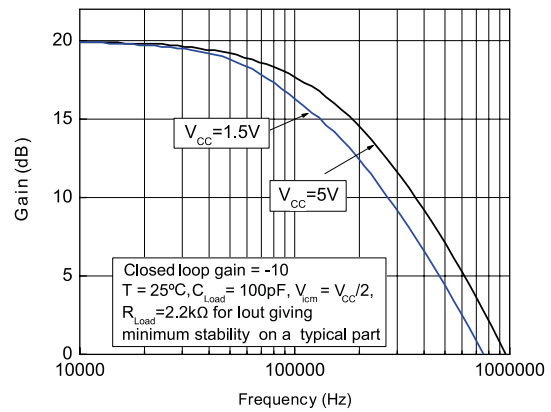


Figure 6: Closed loop response for gain = -3 at  $V_{CC} = 1.5$  V

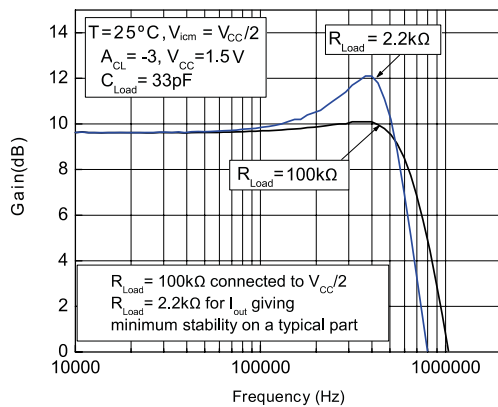


Figure 7: Closed loop response for gain = -3 at  $V_{CC} = 5$  V

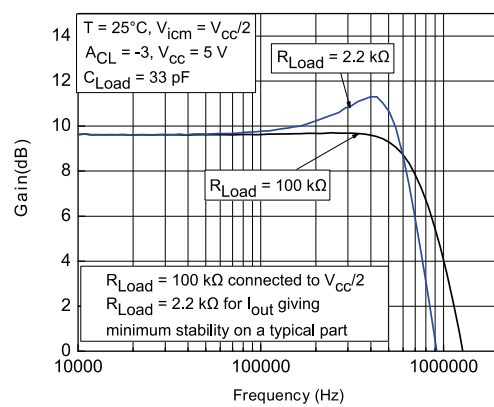




Figure 8: Positive slew rate vs. supply voltage in closed loop

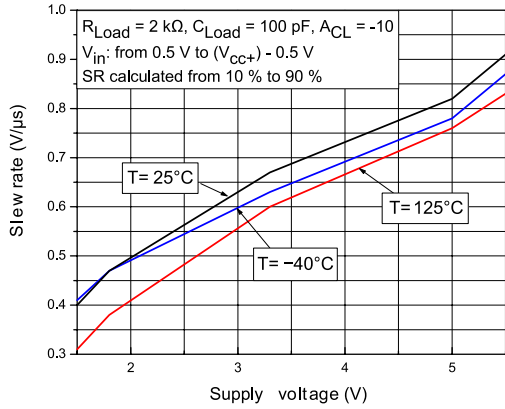


Figure 9: Negative slew rate vs. supply voltage in closed loop

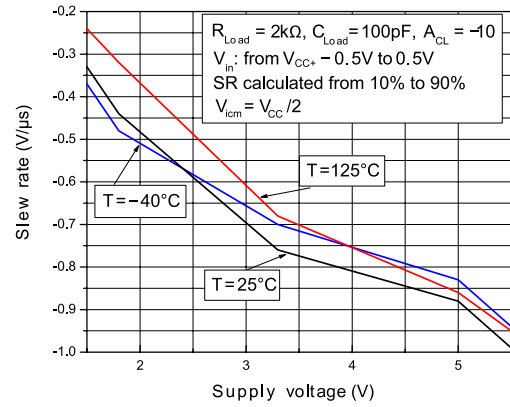


Figure 10: Slew rate vs. supply voltage in open loop

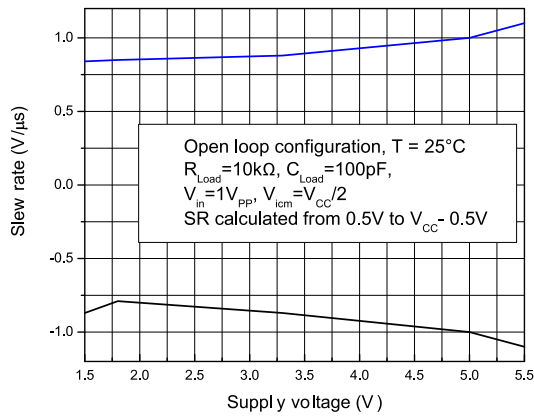


Figure 11: Slew rate timing in open loop

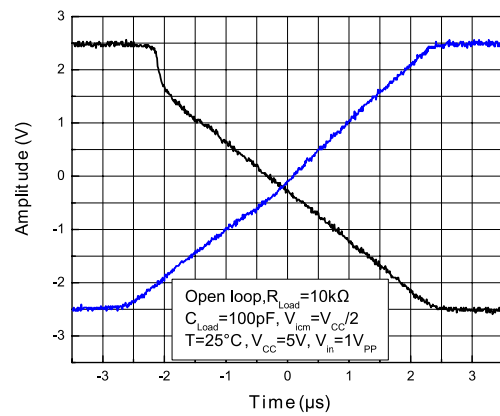


Figure 12: Slew rate timing in closed loop

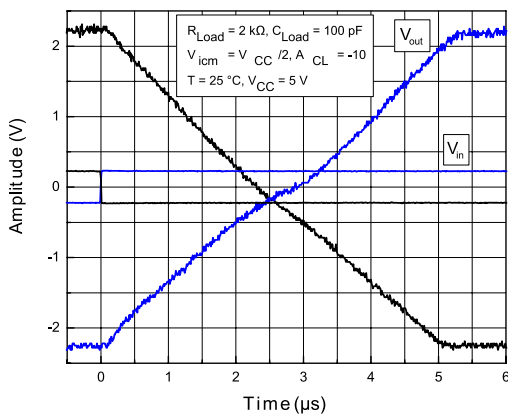


Figure 13: Noise vs. frequency

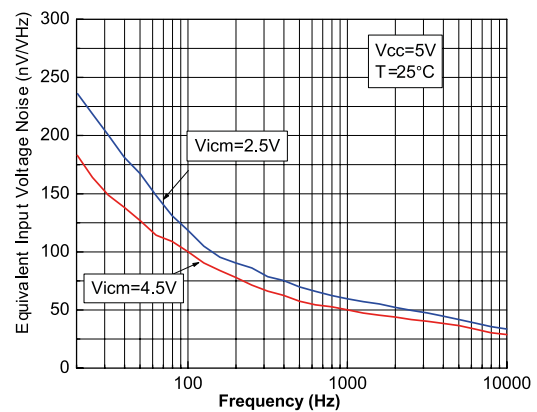


Figure 14: Distortion and noise vs. output voltage at VCC = 1.8 V

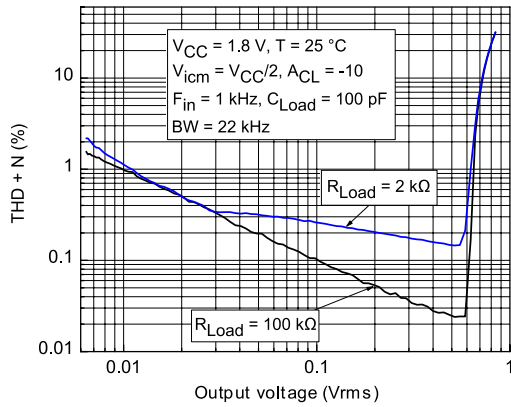


Figure 15: Distortion and noise vs. frequency at VCC = 1.8 V

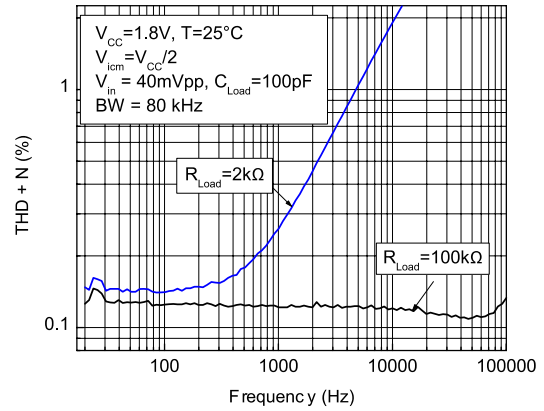


Figure 16: Distortion and noise vs. output voltage at VCC = 5 V

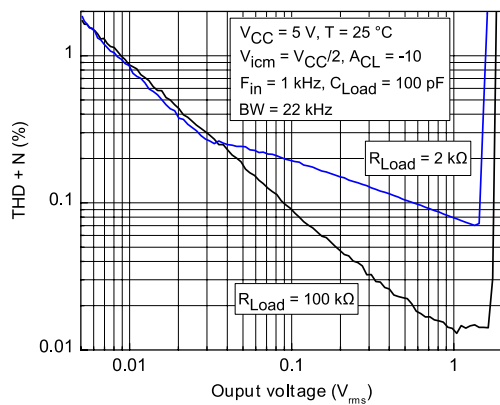


Figure 17: Distortion and noise vs. frequency at VCC = 5 V

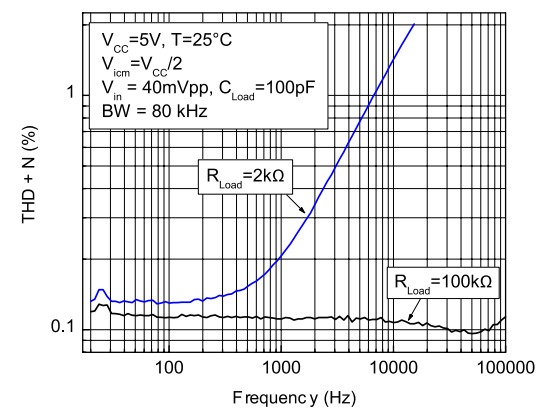


Figure 18: EMIRR vs. frequency at VCC = 5 V, T = 25 °C

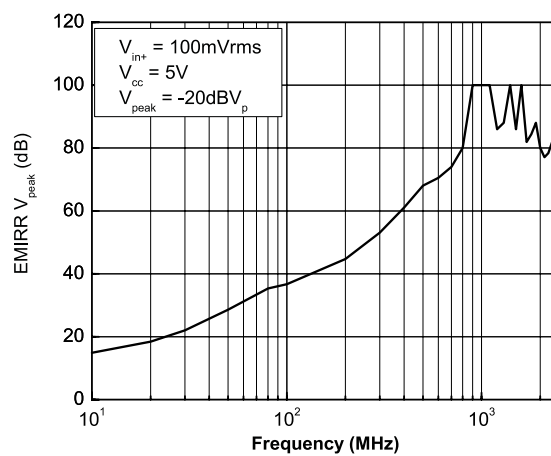


Figure 19: Input offset voltage vs input common-mode at VCC = 1.5 V

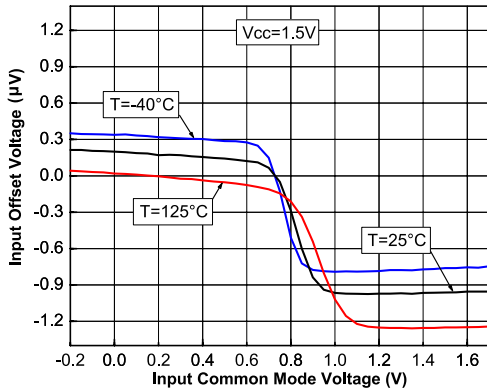


Figure 20: Input offset voltage vs input common-mode at VCC = 5 V

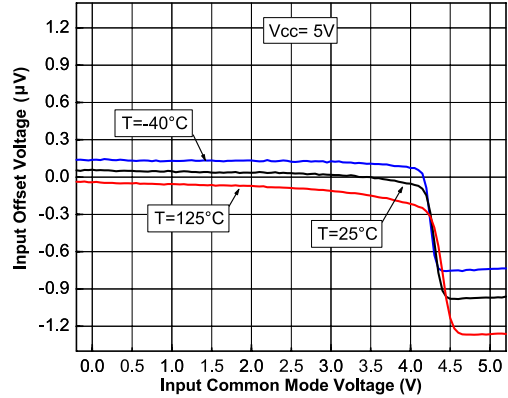


Figure 21: Test configuration for turn-on time (Vout pulled down)

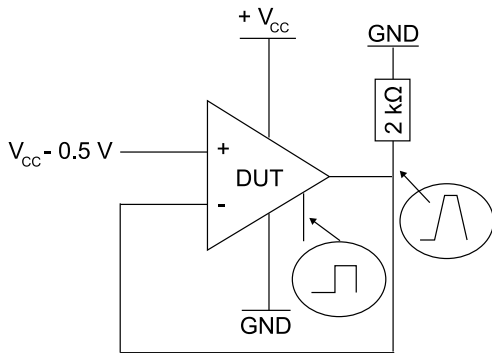


Figure 22: Test configuration for turn-off time (Vout pulled down)

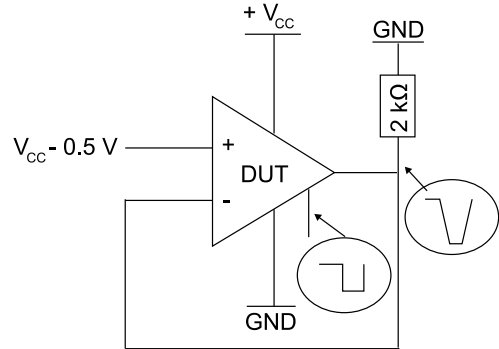


Figure 23: Turn-on time, VCC = 5 V, Vout pulled down, T = 25 °C

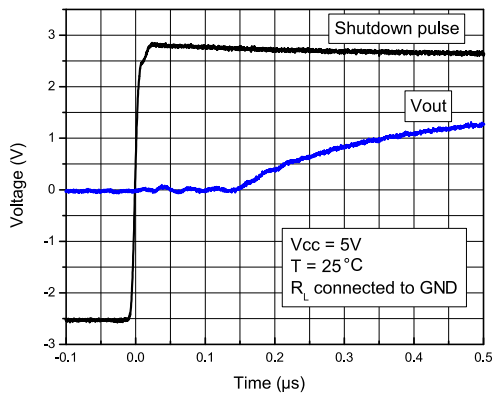
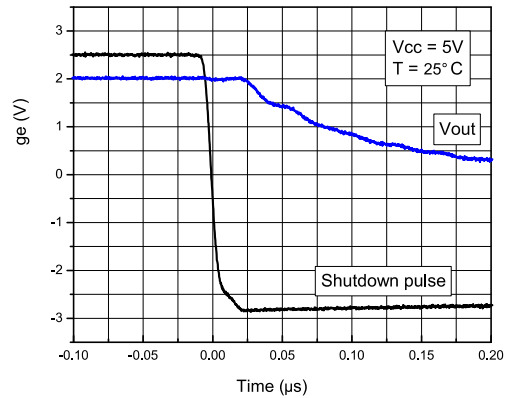
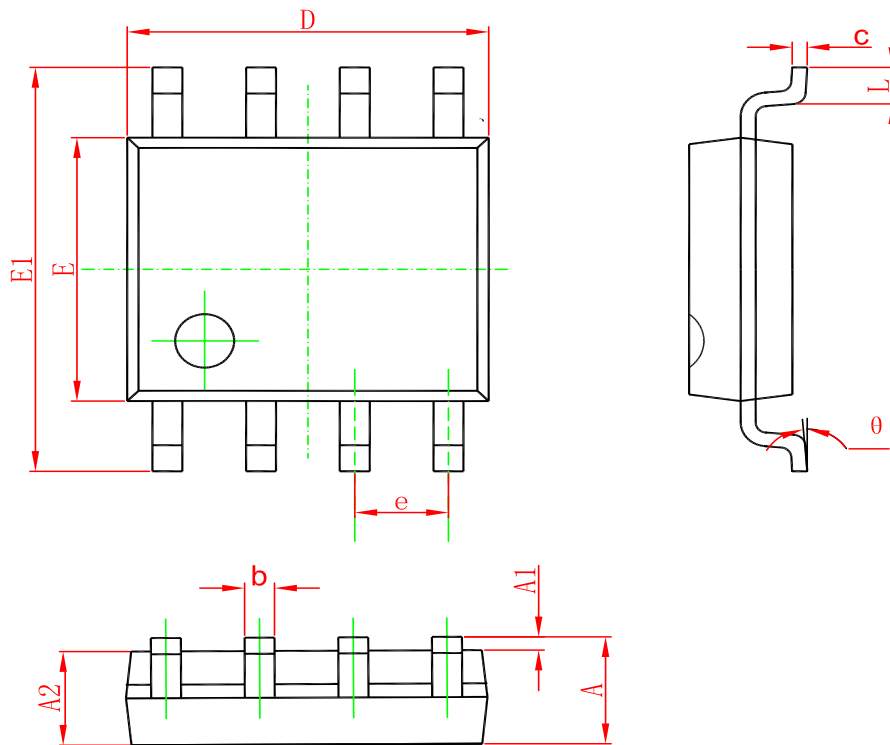


Figure 24: Turn-off time, VCC = 5 V, Vout pulled down, T = 25 °C

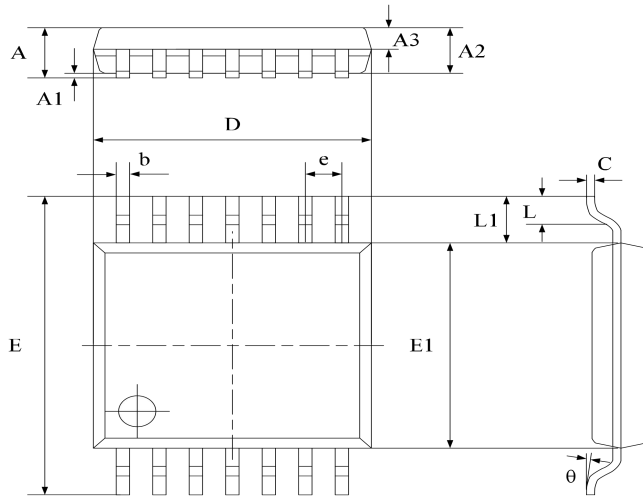


**SOP-8**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

## TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
$\theta$	0°	8°	0°	8°

## Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW TSV6392AIDT	SOP-8	2500	Tape and reel	V632AI
UMW TSV6392IDT	SOP-8	2500	Tape and reel	V6392I
UMW TSV6394IPT	TSSOP-14	4000	Tape and reel	TSV6394
UMW TSV6394AIPT	TSSOP-14	4000	Tape and reel	TSV6394