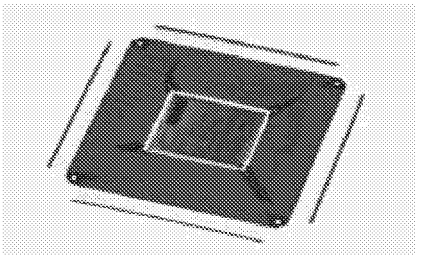
MOBILE PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY ON 0.25 MICRON

Operating Frequency	166 MHz	200 MHz	233 MHz	266 MHz

- **Support for MMX™ Technology**
- **Compatible with Large Software Base**
  - **MS-DOS*, Windows*, OS/2*, UNIX***
- **32-Bit CPU with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **Enhanced pipelines**
  - **Two Pipelined Integer Units Capable of 2 Instructions/Clock**
  - **Pipelined MMX Technology**
  - **Pipelined Floating-Point Unit**
- **Separate Code and Data Caches**
  - **16-Kbyte Code, 16-Kbyte Write Back Data**
  - **MESI Cache Protocol**
- **4-Mbyte Pages for Increased TLB Hit Rate**
- **320-pin TCP or Mobile Module**
- **IEEE 1149.1 Boundary Scan**
- **Advanced Design Features**
  - **Deeper Write Buffers**
  - **Enhanced Branch Prediction Feature**
  - **Virtual Mode Extensions**
- **0.25 Micron Process Technology**
  - **1.8 V core supply (166/200/233 MHz)**
  - **2.0 V core supply (266 MHz)**
  - **2.5 V I/O Interface (166/200/233/266 MHz)**
- **Internal Error Detection Features**
- **On-Chip Local APIC Controller**
- **Power Management Features**
  - **System Management Mode**
  - **Clock Control**
- **Fractional Bus Operation**
  - **166-MHz Core/66-MHz Bus**
  - **200-MHz Core/66-MHz Bus**
  - **233-MHz Core/66-MHz Bus**
  - **266-MHz Core/66-MHz Bus**

The mobile Pentium® processor with MMX™ technology on 0.25 micron extends the mobile Pentium processor family, providing additional performance for notebook applications. The mobile Pentium processor with MMX technology on 0.25 micron is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2*, and UNIX* and is one of the major microprocessors to support Intel MMX technology. Furthermore, the mobile Pentium processor with MMX technology on 0.25 micron has superscalar architecture which can execute two instructions per clock cycle, and enhanced branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The mobile Pentium processor with MMX technology on 0.25 micron has 4.5 million transistors, is built on Intel's 0.25 micron manufacturing process technology and has full SL Enhanced power management features including System Management Mode (SMM) and clock control. The additional SL Enhanced features, 1.8/2.0V core operation along with 2.5V I/O buffer operation, a 320-pin Tape Carrier Package (TCP), and the Intel mobile module, make the mobile Pentium processor with MMX technology on 0.25 micron ideal for enabling mobile MMX technology designs. The mobile Pentium processor with MMX technology on 0.25 micron may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available upon request.



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1.0. INTRODUCTION

The mobile Pentium® processors with MMX™ technology on 0.25 micron are fully compatible with the existing mobile Pentium processors with MMX technology (120, 133, 150, & 166 MHz) with the following differences: voltage supplies, power consumption, and performance. These processors, when used in a TCP package, are socket compatible with the mobile Pentium processor (75, 90, 100, 120, 133, 150 MHz) making it possible to design a flexible motherboard that supports both the mobile Pentium processor (75 MHz - 150 MHz) and the mobile Pentium processor with MMX technology (120 MHz - 266 MHz). It has all the advanced features of the desktop version of the Pentium processor with MMX technology except for the differences listed in Section 3.1.

The mobile Pentium processor with MMX technology on 0.25 micron has several features which allow high-performance notebooks to be designed, including the following:

- TCP dimensions are ideal for small form-factor designs.
- TCP has superior thermal resistance characteristics.
- 1.8V (166/200/233 MHz)/2.0V (266 MHz) core and 2.5V I/O buffer V_{CC} inputs reduce power consumption significantly.
- The SL Enhanced feature set.

The architecture and internal features of the mobile Pentium processor with MMX technology on 0.25 micron are identical to the desktop version specifications provided in the *Pentium® Processor Family Developer's Manual* (Order Number 241428), except several features not used in mobile applications which have been eliminated to streamline it for mobile applications.

This document should be used in conjunction with *Pentium® Processor Family Developer's Manual* (Order Number: 241428)

2.0. MICROPROCESSOR ARCHITECTURE OVERVIEW

The mobile Pentium processor with MMX technology on 0.25 micron extends the mobile Pentium processor with MMX technology family. It is binary compatible with the 8086/88™, 80286™, Intel386™ DX, Intel386 SX, Intel486™ DX, Intel486 SX, Intel486 DX2, and mobile Pentium processors with voltage reduction technology (75-150).

The mobile Pentium processor family consists of the mobile Pentium processor with MMX technology (120, 133, 150, & 166), The mobile Pentium processor with MMX technology on 0.25 micron (166, 200, 233, & 266) and the mobile Pentium processor with voltage reduction technology (75 MHz -150 MHz).

The mobile Pentium processor with MMX technology on 0.25 micron contains all of the features of previous Intel Architecture and provides significant enhancements and additions including the following:

- Support for MMX™ Technology
- Superscalar Architecture
- Enhanced Branch Prediction Algorithm
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 16K Code and 16K Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Enhanced Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- 0.25 Micron Process Technology
- SL Power Management Features
- Pool of four write buffers used by both pipes

2.1. Mobile Pentium® Processor Family Architecture

The application instruction set of the mobile Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 and Intel486 families of processors.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the Branch Target Buffer (BTB) so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 processor. Faster algorithms provide up to 10X speed-up for common operations including add, multiply and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache has a 32-byte line size and is 4-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst writeback cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' MMU contains optional extensions to the architecture which allow 4-Kbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a vir tual 8086 monitor.

Figure 1 shows a block diagram of the mobile Pentium processor with MMX technology.

The block diagram shows the two instruction pipelines, the "u" pipe and "v" pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate code and data caches are shown,. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

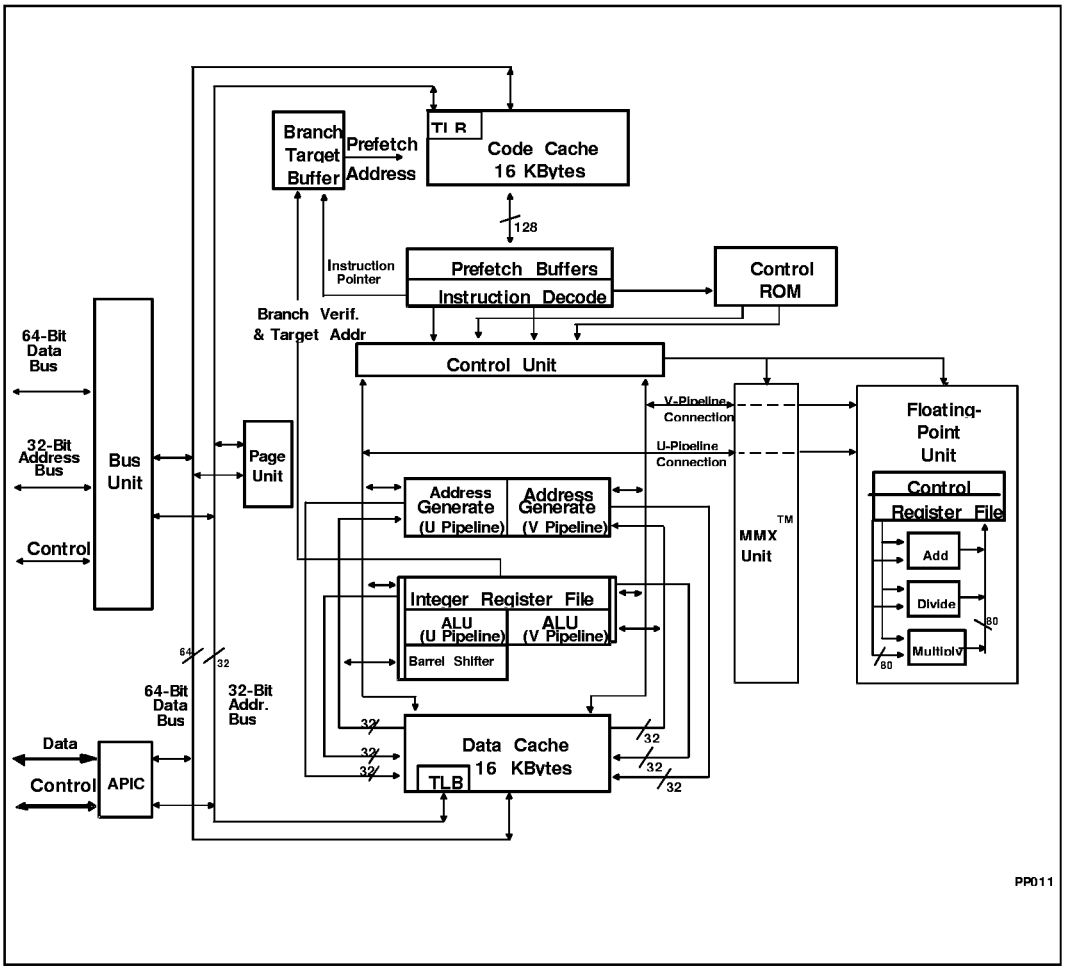


Figure 1. Mobile Pentium® Processor with MMX™ Technology Block Diagram

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the mobile Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the mobile Pentium processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the mobile Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The mobile Pentium processor contains a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

In addition to the SMM features described above, the mobile Pentium processor supports clock control. When the clock to the processor is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the mobile Pentium processor a good choice for energy-efficient notebook designs.

The mobile Pentium processor supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The mobile Pentium® processor with MMX™ technology on 0.25 micron contains an on-chip advanced programmable interrupt controller (APIC). This function is reserved for future multi-processing function.

The architectural features introduced in this section are more fully described in the *Pentium® Processor Family Developer's Manual* (Order Number: 241428).

2.2. Mobile Pentium® Processor with MMX™ Technology

The mobile Pentium processor with MMX technology is a significant addition to the mobile Pentium processor family. Available at 120, 133, 150, 166, 200, 233, and 266 MHz, it is the first microprocessor to support Intel MMX technology.

The mobile Pentium processor with MMX technology is both software and pin compatible with previous members of the mobile Pentium processor family. It contains 4.5 million transistors and is manufactured on Intel's enhanced 0.35 micron (120/133/150/166 MHz) or 0.25 micron (166/200/233/266 MHz) CMOS process which allows voltage reduction technology for low power and high density. This enables the mobile Pentium processor with MMX technology to remain within the thermal envelope while providing a significant performance increase.

In addition to the architecture described in the previous section for the mobile Pentium processor family, the mobile Pentium processor with MMX technology has several additional micro-architectural enhancements, which are described below.

2.2.1. Full support for Intel MMX ™ technology

MMX technology is based on SIMD technique (Single Instruction, Multiple Data) which enables increased performance on a wide variety of multimedia and communications applications. Fifty-seven new instructions and four new 64-bit data types are supported in the mobile Pentium processor with MMX technology. All existing operating system and application software are fully-compatible.

2.2.2. Doubled code / data caches to 16K each

On-chip level-1 data and code cache sizes have been doubled to 16KB each and are 4-way set associative on the mobile Pentium processor with MMX technology. Larger separate internal caches improve performance by reducing average memory access time and providing fast access to recently-used instructions and data. The instruction and data caches can be accessed simultaneously while the data cache supports two data references simultaneously. The data cache supports a write-back (or alternatively, write-through, on a line by line basis) policy for memory updates.

2.2.3. Improved branch prediction

Dynamic branch prediction uses the Branch Target Buffer (BTB) to boost performance by predicting the most likely set of instructions to be executed. The BTB has been improved on the mobile Pentium processor with MMX technology to increase its accuracy. Further, this processor has four prefetch

buffers that can hold up to four successive code streams.

2.2.4. Enhanced pipeline

An additional pipeline stage has been added and the pipeline has been enhanced to improve performance. The integration of the MMX technology pipeline with the integer pipeline is very similar to that of the floating-point pipeline. Under some circumstances, two MMX instructions or one integer and one MMX instruction can be paired and issued in one clock cycle to increase throughput. The enhanced pipeline is described in more detail in the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

Deeper write buffers. A pool of four write buffers is now shared between the dual pipelines to improve memory write performance.

2.3. 0.25 micron technology

The 0.25 micron technology is the latest state-of-the-art CMOS manufacturing process Intel unveiled on April 12, 1997, which enables the use of lower core supply to sub-2V. As a result, the mobile Pentium processor with MMX technology on 0.25 micron consumes significantly less power at even higher speeds. The mobile Pentium processor with MMX technology on 0.25 micron is the first Intel microprocessor utilizing 0.25 micron technology.

3.0. MOBILE PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY PINOUT

3.1. Mobile Differences from Desktop

To better streamline the part for mobile applications, the following features have been eliminated: Upgrade, Dual Processing (DP), and Master/Checker functional redundancy.

Table 1 lists the corresponding pins which exist on the desktop Pentium processor with MMX technology but have been removed on the mobile Pentium processor with MMX technology on 0.25 micron.

Table 1. Signals Removed in Mobile Pentium ® Processor with MMX™ Technology 200/233 MHz

Signal	Function
ADSC#	Additional Address Status. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	Additional Burst Ready. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	CPU Type. This signal is used for dual processing systems.
D/P#	Dual/Primary processor identification. This signal is only used for an upgrade processor.
FRCMC#	Functional Redundancy Checking. This signal is only used for error detection via processor redundancy and requires two Pentium ® processors (master/checker).
PBGNT#	Private Bus Grant. This signal is only used for dual processing systems.
PBREQ#	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	Private Hit. This signal is only used for dual processing systems.
PHITM#	Private Modified Hit. This signal is only used for dual processing systems.

3.2. TCP Pinout and Pin Descriptions

The text orientation on the top side view drawings in this section represent the orientation of the ink mark on the actual packages (Note that the text shown in this section is not the actual text which will be marked on the packages).

3.2.1. MOBILE PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY ON 0.25 MICRON TCP PINOUT

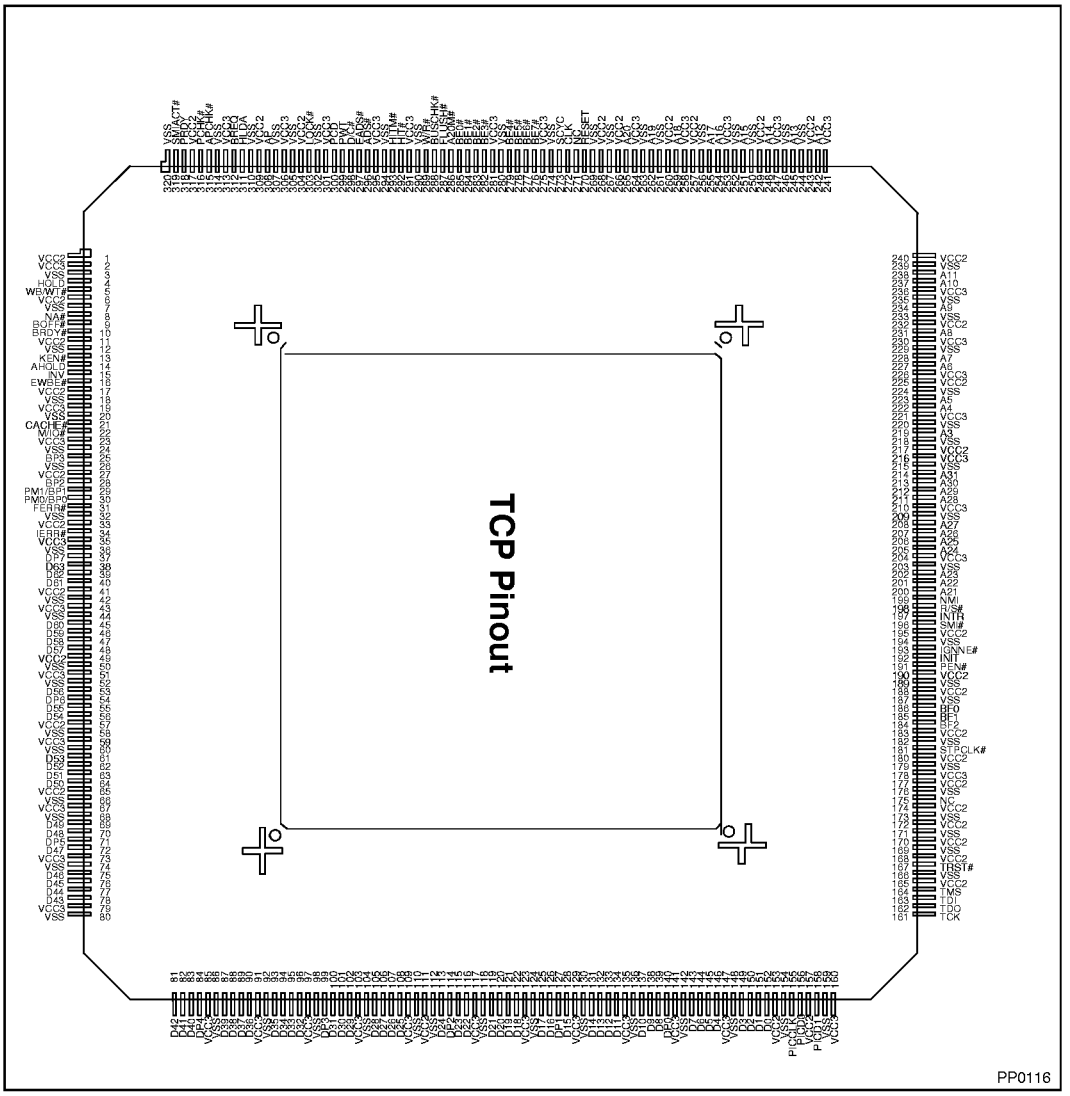


Figure 2. TCP Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron Pinout

3.2.2. TCP MOBILE PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY ON 0.25 MICRON PIN CROSS REFERENCE

Table 2. TCP Pin Cross Reference by Pin Name

Address									
A3	219	A9	234	A15	251	A21	200	A27	208
A4	222	A10	237	A16	254	A22	201	A28	211
A5	223	A11	238	A17	255	A23	202	A29	212
A6	227	A12	242	A18	259	A24	205	A30	213
A7	228	A13	245	A19	262	A25	206	A31	214
A8	231	A14	248	A20	265	A26	207		
Data									
D0	152	D13	132	D26	107	D39	87	D52	62
D1	151	D14	131	D27	106	D40	83	D53	61
D2	150	D15	128	D28	105	D41	82	D54	56
D3	149	D16	126	D29	102	D42	81	D55	55
D4	146	D17	125	D30	101	D43	78	D56	53
D5	145	D18	122	D31	100	D44	77	D57	48
D6	144	D19	121	D32	96	D45	76	D58	47
D7	143	D20	120	D33	95	D46	75	D59	46
D8	139	D21	119	D34	94	D47	72	D60	45
D9	138	D22	116	D35	93	D48	70	D61	40
D10	137	D23	115	D36	90	D49	69	D62	39
D11	134	D24	113	D37	89	D50	64	D63	38
D12	133	D25	108	D38	88	D51	63		
APIC									
PICCLK					155				
PICD0					156				
PICD1					158				

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

Control							
A20M#	286	BREQ	312	HITM#	293	PM0/BP0	30
ADS#	296	BUSCHK#	288	HLDA	311	PM1/BP1	29
AHOLD	14	CACHE#	21	HOLD	4	PRDY	318
AP	308	D/C#	298	IERR#	34	PWT	299
APCHK#	315	DP0	140	IGNNE#	193	R/S#	198
BE0#	285	DP1	127	INIT	192	RESET	270
BE1#	284	DP2	114	INTR/LINT0	197	SCYC	273
BE2#	283	DP3	99	INV	15	SMI#	196
BE3#	282	DP4	84	KEN#	13	SMIACT#	319
BE4#	279	DP5	71	LOCK#	303	TCK	161
BE5#	278	DP6	54	M/IO#	22	TDI	163
BE6#	277	DP7	37	NA#	8	TDO	162
BE7#	276	EADS#	297	NMI/LINT1	199	TMS	164
BOFF#	9	EWBE#	16	PCD	300	TRST#	167
BP2	28	FERR#	31	PCHK#	316	W/R#	289
BP3	25	FLUSH#	287	PEN#	191	WB/WT#	5
BRDY#	10	HIT#	292				

Clock Control	
BF0	186
BF1	185
BF2	184
CLK	272
PICCLK	155
STPCLK#	181

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

V_{CC2}[1]			
1	111	183	257
6	153	188	260
11	157	190	266
17	165	195	268
27	168	217	304
33	170	225	309
41	172	232	317
49	174	240	
57	177	243	
65	180	249	
V_{CC3}[2]			
2	91	178	258
19	97	204	264
23	103	210	275
35	109	216	281
43	117	221	291
51	123	226	295
59	129	230	301
67	135	236	306
73	141	241	313
79	147	247	
85	160	253	

Table 2. TCP Pin Cross Reference by Pin Name (Contd.)

V_{SS}			
3	80	173	246
7	86	176	250
12	92	179	252
18	98	182	256
20	104	187	261
24	110	189	263
26	112	194	267
32	118	203	269
36	124	209	274
42	130	215	280
44	136	218	290
50	142	220	294
52	148	224	302
58	154	229	305
60	159	233	307
66	166	235	310
68	169	239	314
74	171	244	320
NC			
175	184	271	

NOTE:

1. These V_{CC2} pins are 1.8V (166/200/233 MHz) or 2.0V (266 MHz) inputs to the core, but may change to a different voltage on future offerings of this microprocessor family.

2. All V_{CC3} pins are 2.5V I/O power inputs.

Table 3. TCP Pin Cross References by Pin Number (Pins 1-320)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	V_{CC2}	41	V_{CC2}	81	D42	121	D19
2	V_{CC3}	42	V_{SS}	82	D41	122	D18
3	V_{SS}	43	V_{CC3}	83	D40	123	V_{CC3}
4	HOLD	44	V_{SS}	84	DP4	124	V_{SS}
5	WB/WT#	45	D60	85	V_{CC3}	125	D17
6	V_{CC2}	46	D59	86	V_{SS}	126	D16
7	V_{SS}	47	D58	87	D39	127	DP1
8	NA#	48	D57	88	D38	128	D15
9	BOFF#	49	V_{CC2}	89	D37	129	V_{CC3}
10	BRDY#	50	V_{SS}	90	D36	130	V_{SS}
11	V_{CC2}	51	V_{CC3}	91	V_{CC3}	131	D14
12	V_{SS}	52	V_{SS}	92	V_{SS}	132	D13
13	KEN#	53	D56	93	D35	133	D12
14	AHOLD	54	DP6	94	D34	134	D11
15	INV	55	D55	95	D33	135	V_{CC3}
16	EWBE#	56	D54	96	D32	136	V_{SS}
17	V_{CC2}	57	V_{CC2}	97	V_{CC3}	137	D10
18	V_{SS}	58	V_{SS}	98	V_{SS}	138	D9
19	V_{CC3}	59	V_{CC3}	99	DP3	139	D8
20	V_{SS}	60	V_{SS}	100	D31	140	DP0
21	CACHE#	61	D53	101	D30	141	V_{CC3}
22	M/IO#	62	D52	102	D29	142	V_{SS}
23	V_{CC3}	63	D51	103	V_{CC3}	143	D7
24	V_{SS}	64	D50	104	V_{SS}	144	D6
25	BP3	65	V_{CC2}	105	D28	145	D5
26	VSS	66	V_{SS}	106	D27	146	D4
27	V_{CC2}	67	V_{CC3}	107	D26	147	V_{CC3}
28	BP2	68	V_{SS}	108	D25	148	V_{SS}
29	PM1/BP1	69	D49	109	V_{CC3}	149	D3

Table 3. TCP Pin Cross References by Pin Number (Pins 1-320)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
30	PM0/BP0	70	D48	110	VSS	150	D2
31	FERR#	71	DP5	111	V_{CC2}	151	D1
32	V_{SS}	72	D47	112	V_{SS}	152	D0
33	V_{CC2}	73	V_{CC3}	113	D24	153	V_{CC2}
34	IERR#	74	V_{SS}	114	DP2	154	V_{SS}
35	V_{CC3}	75	D46	115	D23	155	PICCLK
36	V_{SS}	76	D45	116	D22	156	PICD0
37	DP7	77	D44	117	V_{CC3}	157	V_{CC2}
38	D63	78	D43	118	V_{SS}	158	PICD1
39	D62	79	V_{CC3}	119	D21	159	V_{SS}
40	D61	80	V_{SS}	120	D20	160	V_{CC3}
161	TCK	201	A22	241	V_{CC3}	281	V_{CC3}
162	TDO	202	A23	242	A12	282	BE3#
163	TDI	203	V_{SS}	243	V_{CC2}	283	BE2#
164	TMS	204	V_{CC3}	244	V_{SS}	284	BE1#
165	V_{CC2}	205	A24	245	A13	285	BE0#
166	V_{SS}	206	A25	246	V_{SS}	286	A20M#
167	TRST#	207	A26	247	V_{CC3}	287	FLUSH#
168	V_{CC2}	208	A27	248	A14	288	BUSCHK#
169	V_{SS}	209	V_{SS}	249	V_{CC2}	289	W/R#
170	V_{CC2}	210	V_{CC3}	250	V_{SS}	290	V_{SS}
171	V_{SS}	211	A28	251	A15	291	V_{CC3}
172	V_{CC2}	212	A29	252	V_{SS}	292	HIT#
173	V_{SS}	213	A30	253	V_{CC3}	293	HITM#
174	V_{CC2}	214	A31	254	A16	294	V_{SS}
175	NC	215	V_{SS}	255	A17	295	V_{CC3}
176	V_{SS}	216	V_{CC3}	256	V_{SS}	296	ADS#
177	V_{CC2}	217	V_{CC2}	257	V_{CC2}	297	EADS#
178	V_{CC3}	218	V_{SS}	258	V_{CC3}	298	D/C#
179	V_{SS}	219	A3	259	A18	299	PWT

Table 3. TCP Pin Cross References by Pin Number (Pins 1-320)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
180	V_{CC2}	220	V_{SS}	260	V_{CC2}	300	PCD
181	STPCLK#	221	V_{CC3}	261	V_{SS}	301	V_{CC3}
182	V_{SS}	222	A4	262	A19	302	V_{SS}
183	V_{CC2}	223	A5	263	V_{SS}	303	LOCK#
184	BF2	224	V_{SS}	264	V_{CC3}	304	V_{CC2}
185	BF1	225	V_{CC2}	265	A20	305	V_{SS}
186	BF0	226	V_{CC3}	266	V_{CC2}	306	V_{CC3}
187	V_{SS}	227	A6	267	V_{SS}	307	V_{SS}
188	V_{CC2}	228	A7	268	V_{CC2}	308	AP
189	V_{SS}	229	V_{SS}	269	V_{SS}	309	V_{CC2}
190	V_{CC2}	230	V_{CC3}	270	RESET	310	V_{SS}
191	PEN#	231	A8	271	NC	311	HLDA
192	INIT	232	V_{CC2}	272	CLK	312	BREQ
193	IGNNE#	233	V_{SS}	273	SCYC	313	V_{CC3}
194	V_{SS}	234	A9	274	V_{SS}	314	V_{SS}
195	V_{CC2}	235	V_{SS}	275	V_{CC3}	315	APCHK#
196	SMI#	236	V_{CC3}	276	BE7#	316	PCHK#
197	INTR/LINT0	237	A10	277	BE6#	317	V_{CC2}
198	R/S#	238	A11	278	BE5#	318	PRDY
199	NMI/LINT1	239	V_{SS}	279	BE4#	319	SMIACT#
200	A21	240	V_{CC2}	280	V_{SS}	320	V_{SS}

NOTE:

1. V_{CC2} pins are 1.8V (166/200/233 MHz) or 2.0V (266 MHz) inputs to the core.
2. V_{CC3} pins are 2.5V inputs to the I/O.

3.3. Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active HIGH inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

3.4. Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the Hardware Interface chapter in the *Pentium® Processor Family Developer's Manual.*

Note

All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The pins are classified as Input or Output based on their function in Master Mode. See the Error Detection chapter of the *Pentium® Processor Family Developer's Manual,* for further information.

Table 4. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the mobile Pentium ® processor with MMX™ technology emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of **address hold**, the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31 -3).
BF[2:0]	I	The **Bus Frequency** pins determine the bus-to-core frequency ratio. BF [2:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[2:0] must not change values while RESET is active. See Table 6 for Bus Frequency Selection. In order to override the internal defaults and guarantee that the BF[2:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pullup/pulldown resistor to VCC3 or ground. Drving these pins with active logic is not recommended unless stability during RESET can be guaranteed. During power up, RESET should be asserted prior to or ramped simultaneously with the core voltage supply to the processor.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
[APICEN] PICD1	I	Advanced Programmable Interrupt Controller Enable enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception. **NOTE:** To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST# and PICD0-1 are specified with respect to the rising edge of CLK. This pin is 3.3V-tolerant-only on the Pentium® processor with MMX™ technology. **NOTE:** It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63-D56; DP0 applies to D7-D0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using MS-DOS type floating-point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. **NOTE:** If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
HOLD	I	In response to the **bus hold request**, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.

PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium® processor with MMX™ technology.
PICD0-1 [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium® processor with MMX™ technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistor. These signals are multiplexed with APICEN.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1 -0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The **page writethrough** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for more details.
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode will be entered or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2	I	These pins are the 1.8V (166/200/233 MHz) or 2.0V (266 MHz) power inputs to the core.

Table 4. Quick Pin Reference (Contd.)

Symbol	Type	Name and Function
VCC3	I	These pins are the 2.5V power inputs to the I/O.
VSS	I	These pins are the ground inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

3.5. Bus Frequency

Core and bus frequencies can be set according to Table 5 below. Each mobile Pentium processor with MMX technology is specified to operate within a single bus-to-core ratio. Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported.

Table 5. Bus Frequency Selections (1)

BF2	BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)
0	0	0	2/5	66/166
0	0	1	1/3	66/200
0	1	1	2/7	66/233
1	0	0	1/4	66/266

NOTES:

1. Each processor must be externally configured with the BF0-2 pins to operate in the specified bus fraction mode. Operation out of the specification is not supported.

3.6. Pin Reference Tables

Table 6. Output Pins[1]

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE4#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#[2]	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTE:

1. All output and input/output pins are floated during tristate test mode (except TDO).
2. HITM# pin has an internal pull-up resistor.

Table 7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal resistor	Qualified
A20M#	LOW	Asynchronous		
AHOLD	HIGH	Synchronous		
BF0	HIGH	Synchronous/RESET	Pulldown	
BF1	HIGH	Synchronous/RESET	Pullup	
BF2	HIGH	Synchronous/RESET	Pulldown	
BOFF#	LOW	Synchronous		
BRDY#	LOW	Synchronous	Pullup	Bus State T2,T12,T2P
BUSCHK#	LOW	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	LOW	Synchronous		
EWBE#	LOW	Synchronous		BRDY#
FLUSH#	LOW	Asynchronous		
HOLD	HIGH	Synchronous		
IGNNE#	LOW	Asynchronous		
INIT	HIGH	Asynchronous		
INTR	HIGH	Asynchronous		
INV	HIGH	Synchronous		EADS#
KEN#	LOW	Synchronous		First BRDY#/NA#
NA#	LOW	Synchronous		Bus State T2,TD,T2P
NMI	HIGH	Asynchronous		
PEN#	LOW	Synchronous		BRDY#
PICCLK	HIGH	Asynchronous	Pullup	
R/S#	n/a	Asynchronous	Pullup	
RESET	HIGH	Asynchronous		
SMI#	LOW	Asynchronous	Pullup	
STPCLK#	LOW	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	LOW	Asynchronous	Pullup	

WB/WT#	n/a	Synchronous		First BRDY#/NA#

Table 8. Input/Output Pins [1]

Name	Active Level	When Floated	Qualified (when an input)	Internal Resistor
A31-A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE3#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown[2]
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0	n/a			Pullup
PICD1[APICEN]	n/a			Pulldown

NOTES:

1. All output and input/output pins are floated during tristate test mode (except TDO).
2. BE3#-BE0# have pulldowns during RESET only.

3.7. Pin Grouping According to Function

Table 9 organizes the pins with respect to their function.

Table 9. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF[2:0]
Address Bus	A31-A3, BE7# - BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0-1
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Clock Control	STPCLK#
Debugging	R/S#, PRDY

4.0. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Ratings

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the mobile Pentium processor with MMX technology contains protective circuitry to resist damage from Electrostatic Discharge (ESD), always take precautions to avoid high static voltages or electric fields.

Case temperature under bias .....–65°C to 110°C

Storage temperature.....–65°C to 150°C

V_{CC3} Supply voltage with respect to V_{SS} .....–0.5V to +3.2V

V_{CC2} Supply voltage with respect to V_{SS} .....–0.5V to +2.8V

2.5V Only Buffer DC Input Voltage.....–0.5V to V_{CC3}+0.5V*

*not to exceed V_{CC3} max

WARNING

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

4.2. DC Specifications

Tables 10, 11, 12 and 13 list the DC specifications which apply to the mobile Pentium processor with MMX technology on 0.25 Micron. The processor core operates at 1.8V (166/200/233 MHz) or 2.0V (266 MHz) internally while the I/O interface operates at 2.5V.

4.2.1. POWER SEQUENCING

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, for compatibility with future mobile processors, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both ON or both OFF within one second of each other.

Table 10. V_{CC} and T_{CASE} Specifications

Package	TCASE	Supply	Min Voltage	Max Voltage	Voltage Tolerance	Frequency
TCP	0 to 95ºC	VCC2	1.665V	1.935V	1.8V +/- 0.135V	166/200/233 MHz
			1.850V	2.150V	2.0V +/- 0.150V	266 MHz
		VCC3	2.375V	2.625V	2.5V +/- 0.125V	166/200/233/266 MHz

Table 11. DC Specifications[1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	-0.3	0.5	V	
V_{IH3}	Input High Voltage	V_{CC3} - 0.7	V_{CC3} + 0.3	V	TTL Level
V_{OL3}	Output Low Voltage		0.4	V	TTL Level[1]
V_{OH3}	Output High Voltage	V_{CC3} - 0.4		V	TTL Level[2]
		V_{CC3} - 0.2		V	TTL Level[3]

NOTES:

1. Parameter measured at -4 mA..
2. Parameter measured at 3 mA.
3. Parameter measured at 1mA; not 100% tested, guaranteed by design.

Table 12. I_{CC} Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		2.35	A	166 MHz[1]
			2.70	A	200 MHz[1]
			3.10	A	233 MHz[1]
			4.00	A	266 MHz[1]
I_{CC3}	Power Supply Current		0.33	A	166 MHz[1]
			0.33	A	200 MHz[1]
			0.38	A	233 MHz[1]
			0.38	A	266 MHz[1]

NOTE:

1. This value should be used for power supply design. It was determined using a worst case instruction mix and maximum V_{CC} at Tcase = 0C. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Table 13. Power Dissipation Requirements for Thermal Design

Parameter	Typical[1]	Max[2]	Unit	Frequency	Notes
Thermal Design Power		4.1 5.0 5.5 7.6	Watts Watts Watts Watts	166 MHz 200 MHz 233 MHz 266 MHz	
Active Power[5]	2.3 2.7 3.0 4.5		Watts Watts Watts Watts	166 MHz 200 MHz 233 MHz 266 MHz	
Stop Grant / Auto Halt Powerdown Power Dissipation[3]		0.42 0.46 0.53 0.70	Watts Watts Watts Watts	166 MHz 200 MHz 233 MHz 266 MHz	
Stop Clock Power[4]	0.02 0.02 0.02	0.05 0.05 0.05 0.06	Watts Watts Watts Watts	166 MHz 200 MHz 233 MHz 266 MHz	

NOTES:

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at V_{CC2} = 1.8V (166/200/233 MHz) or 2.0V (266 MHz) running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum thermal design power unless the system uses thermal feedback to limit processor's maximum power. The maximum thermal design power is determined using a worst-case instruction mix with V_{CC2} = 1.8V (166/200/233 MHz) or 2.0V (266 MHz) and also takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction. When in this mode, the processor has a new feature which allows it to power down additional circuitry to enable lower power dissipation. This is the power without snooping at Vcc2 = 1.8V/2.0V and with TR12 bit 21 set. In order to enable this feature, TR12 bit 21 must be set to 1 (the default is 0 or disabled). Stop grant/Auto Halt Powerdown power dissipation without TR12 bit21 set may be higher. The Max rating may be changed in future spec update.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input. This is specified at a Tcase of 50 ºC.
5. Active power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal Vcc and room temperature.

Table 14. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	4
C_O	Output Capacitance		20	pF	4
$C_{I/O}$	I/O Capacitance		25	pF	4
C_{CLK}	CLK Input Capacitance		15	pF	4
C_{TIN}	Test Input Capacitance		15	pF	4
C_{TOUT}	Test Output Capacitance		20	pF	4
C_{TCK}	Test Clock Capacitance		15	pF	4
I_{LI}	Input Leakage Current		±15	µA	$0<V_{IN}<V_{IL}$, $V_{IH}<V_{IN}<V_{CC3}$(1)
I_{LO}	Output Leakage Current		±15	µA	$0<V_{IN}<V_{IL}$, $V_{IH}<V_{IN}<V_{CC3}$(1)
I_{IH}	Input High Leakage Current		200	µA	$V_{IN} = V_{CC3}$ - 0.4V (3)
I_{IL}	Input Low Leakage Current		–400	µA	V_{IN} = 0.4V (2,5)

NOTES:

1. This parameter is for inputs/outputs without an internal pull up or pull down.
2. This parameter is for inputs with an internal pull up.
3. This parameter is for inputs with an internal pull down.
4. Guaranteed by design.
5. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).

4.3. AC Specifications

The AC specifications of the mobile Pentium processor with MMX technology on 0.25 Micron consist of setup times, hold times, and valid delays at 0 pF.

4.3.1. POWER AND GROUND

For clean on-chip power distribution, the TCP has 37 V_{CC2} (core power), 42 V_{CC3} (I/O power) and 72 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC2}, V_{CC3} and V_{SS} pins. On the circuit board all V_{CC2} pins must be connected to a 1.8V (166/200/233 MHz) or 2.0V (266 MHz) V_{CC2} plane (or island) and all V_{CC3} pins must be connected to a 2.5V V_{CC3} plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 2 for the list of V_{CC2}, V_{CC3} and V_{SS} pins.

4.3.2. DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the processor. The processor's large address and data buses can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level power consumption to a high level one (or high to low power transition). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT

Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor.

Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor on both V_{CC2} plane and V_{CC3} plane to ensure that the supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please contact Intel or refer to the *Mobile Pentium Processor with MMX™ Technology: Power Supply Design Considerations* application note (Order Number 243306).

4.3.3. CONNECTION SPECIFICATIONS

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to ground.

4.3.4. AC TIMINGS FOR A 66-MHZ BUS

The AC specifications given in Table 15 consist of output delays, input setup requirements and input hold requirements for the mobile standard 66 MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to $V_{CC3}/2$ for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, asynchronous inputs must be stable for correct operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays. Do not select a bus fraction and clock speed which will cause the processor to exceed its internal maximum frequency.

Table 15. Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron AC Specifications for 66-MHz Bus Operation

See Table 10 for V_{CC} and T_{CASE} Specifications, CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	33.33	66.66	MHz		23
t_{1a}	CLK Period	15.0	30.0	nS	3	
t_{1b}	CLK Period Stability		± 250	pS		1, 19
t_2	CLK High Time	4.0		nS	3	@ V_{CC3} - 0.7V, (1)
t_3	CLK Low Time	4.0		nS	3	@ 0.5V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(V_{CC3} - 0.7V to 0.5V), (1, 5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.5V to V_{CC3} – 0.7V), (1, 5)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	nS	4	
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	
t_{6c}	LOCK# Valid Delay	0.9	7.0	nS	4	
t_{6d}	ADS# Valid Delay	1.0	6.2	nS	4	
t_{6e}	A3-A31 Valid Delay	0.8	6.4	nS	4	
t_{6f}	M/IO# Valid Delay	0.8	6.2	nS	4	
t_{6g}	BE0-7#, D/C#, W/R#, SCYC Valid Delay	0.8	7.0	nS	4	
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	4

Table 15. Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron AC Specifications for 66-MHz Bus Operation (Contd.)

See Table 10 for V_{CC} and T_{CASE} Specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	4
t_{9a}	BREQ Valid Delay	1.0	8.0	nS	4	4
t_{9b}	SMIACT# Valid Delay	1.0	7.3	nS	4	4
t_{9c}	HLDA Valid Delay	1.0	6.8	nS	4	4
t_{10a}	HIT# Valid Delay	1.0	6.8	nS	4	
t_{10b}	HITM# Valid Delay	0.9	6.0	nS	4	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.0	7.7	nS	4	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	1
t_{14}	A5-A31 Setup Time	6.0		nS	6	20
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	4.75		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		nS	6	
t_{24b}	PEN# Setup Time	4.8		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	

Table 15. Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron AC Specifications for 66-MHz Bus Operation (Contd.)

See Table 10 for V_{CC} and T_{CASE} Specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	11, 15
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	12
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	11, 15, 16
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	12
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		14, 16
t_{31}	R/S# Setup Time	5.0		nS	6	11, 15, 16
t_{32}	R/S# Hold Time	1.0		nS	6	12
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		14, 16
t_{34}	D0-D63, DP0-7 Read Data Setup Time	2.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	11, 15
t_{37}	RESET Hold Time	1.0		nS	7	12
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	7	16
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	11, 15, 16
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	12
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#) Hold Time, Async..	2.0		CLKs	7	To RESET falling edge

Table 15. Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron AC Specifications for 66-MHz Bus Operation (Contd.)

See Table 10 for V_{CC} and T_{CASE} Specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43b}	BF0-BF2 Hold Time	2.0		CLKs	7	To RESET falling edge(18)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@ Vcc3 - 0.7V (1)
t_{47}	TCK Low Time	25.0		nS	3	@ 0.5V (1)
t_{48}	TCK Fall Time		5.0	nS	3	(Vcc3-0.7V to 0.5V (1, 8, 9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.5V to Vcc3 - 0.7V) (1, 8, 9)
t_{50}	TRST# Pulse Width	40.0		CLKs	9	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	8	7
t_{52}	TDI, TMS Hold Time	13.0		nS	8	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	8
t_{54}	TDO Float Delay		25.0	nS	8	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	3, 7, 10

Table 16. Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron APIC AC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60	500	nS	3	
t_{60c}	PICCLK High Time	15		nS	3	
t_{60d}	PICCLK Low Time	15		nS	3	
t_{60e}	PICCLK Rise Time	0.15	2.5	nS	3	
t_{60f}	PICCLK Fall Time	0.15	2.5	nS	3	
t_{60g}	PICD0-1 Setup Time	3		nS	6	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	6	To PICCLK
t_{60i}	PICD0-1 Valid Delay (L to H)	4	38	nS	4	From PICCLK, 21
t_{60j}	PICD0-1 High Time (H to L)	4	22	nS	4	From PICCLK, 21
t_{61}	PICCLK Setup Time	5.0		nS	6	To CLK
t_{62}	PICCLK Hold Time	2.0		nS	6	To CLK
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				22

NOTES for TABLES 15 and 16:

Notes 2, 6, and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 2.5V transitions with 1V/nS rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.87V/ns ≤ CLK input rise/fall time ≤ 8.7V/ns.
6. 0.3V/ns ≤ input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from $V_{CC3}/2$.
14. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF[2:0] must not change values while RESET is active. In order to override the internal defaults and guarantee that the BF[2:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pullup/pulldown resistor to VCC3 or ground. Driving these pins with active logic is not recommended unless stability during RESET can be guaranteed.
19. These signals are measured on the rising edge of adjacent CLKs at $V_{CC3}/2$. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within ±250ps. Therefore, the CLK input cannot be changed dynamically.
20. Timing (t14) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
21. This assumes an external pullup resistor to VCC and a lumped capacitive load. The pullup resistor must be between 300 ohms and 1k ohms, the capacitance must be between 20pF and 120pF, and the RC product must be between 6nS and 36nS.
22. The CLK to PICCLK ratio has to be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4.
23. CLK input frequency must be either 33.33 MHz (+1 MHz) or 66.66 MHz (-1 MHz). Operations in the range between 33.33 MHz and 66.6 MHz is not supported.

* Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

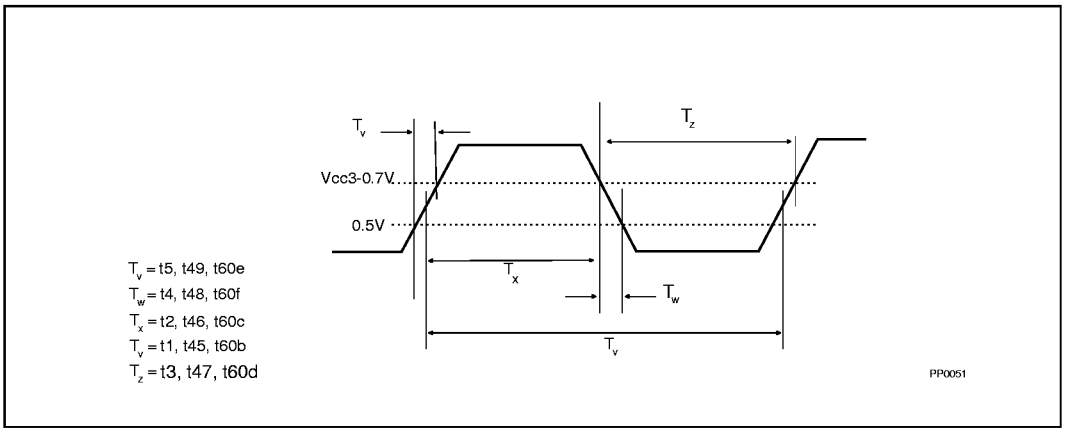


Figure 3. Clock Waveform

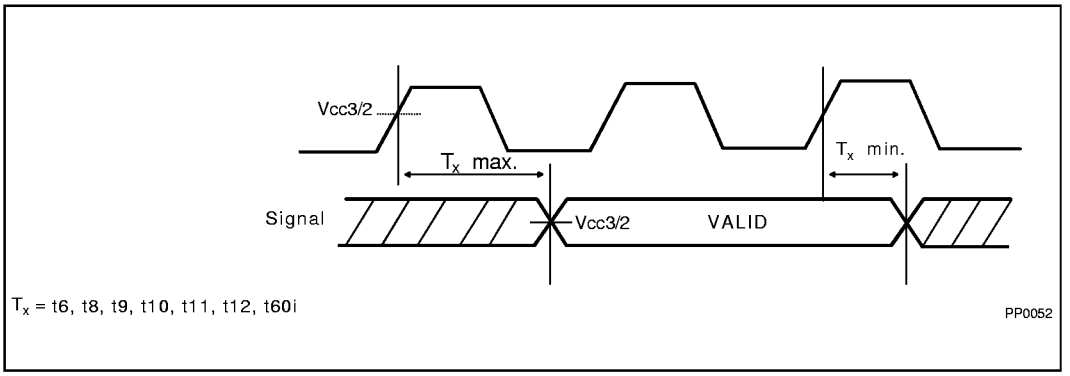


Figure 4. Valid Delay Timings

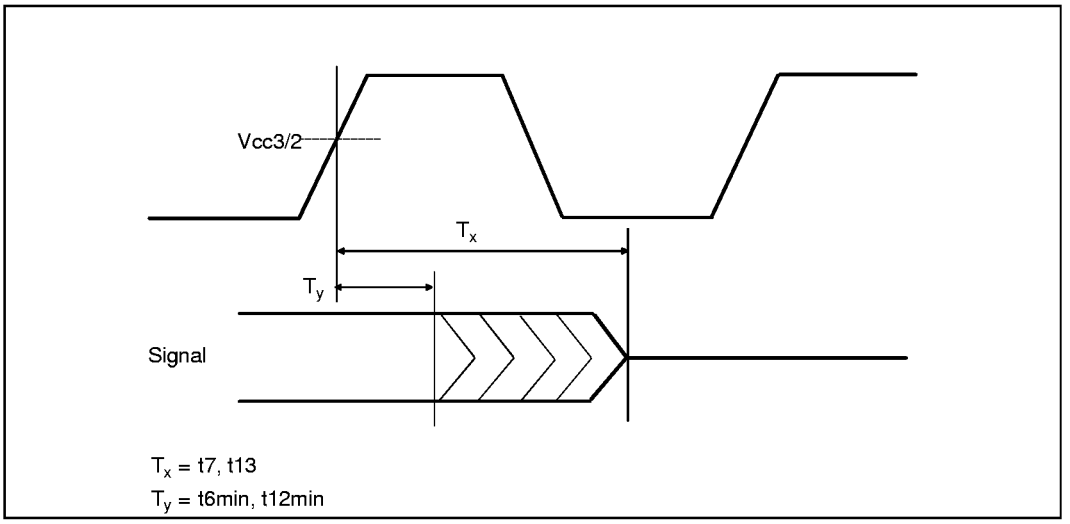


Figure 5. Float Delay Timings

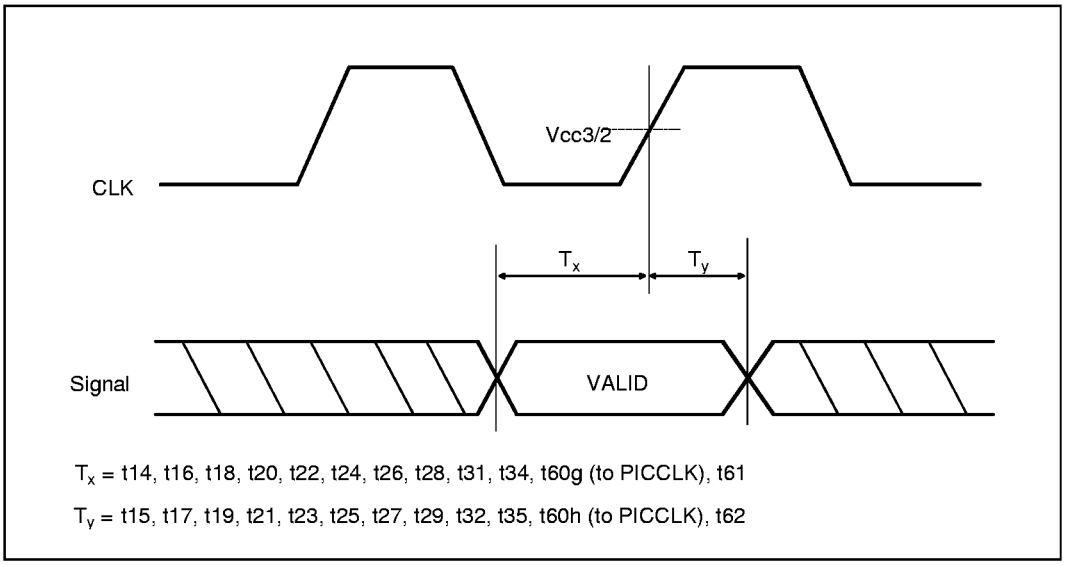
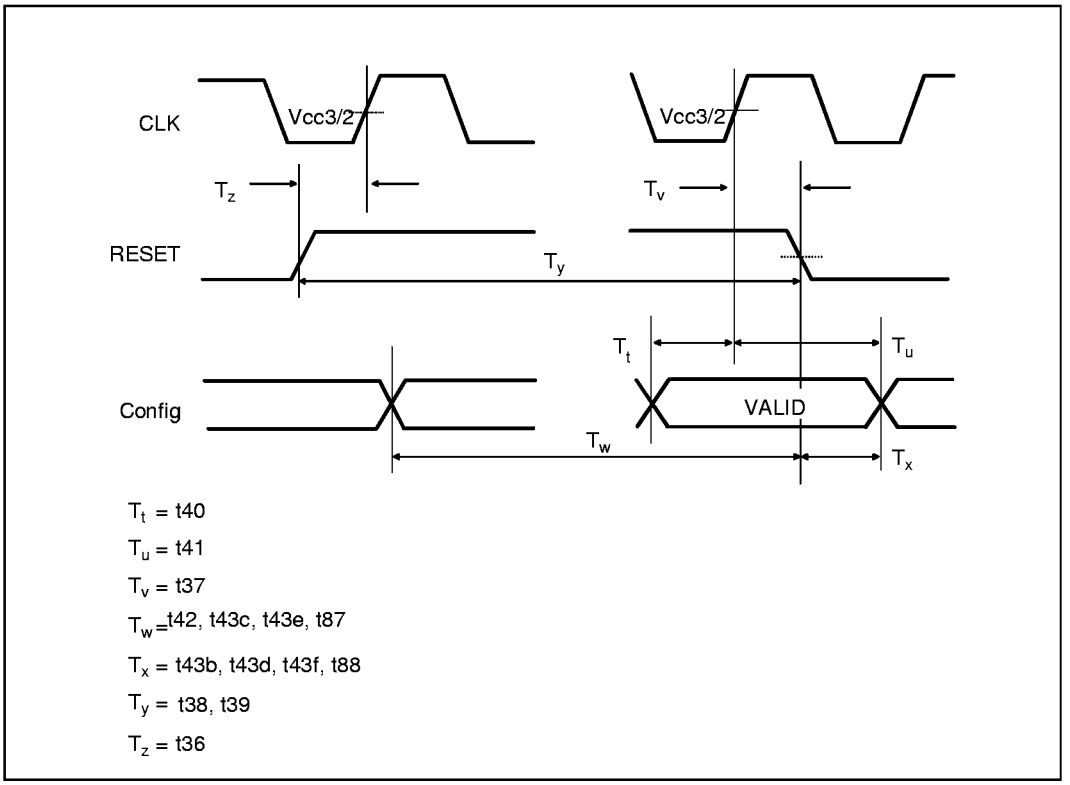


Figure 6. Setup and Hold Timings



T_t = t40

T_u = t41

T_v = t37

T_w = t42, t43c, t43e, t87

T_x = t43b, t43d, t43f, t88

T_y = t38, t39

T_z = t36

Figure 7. Reset and Configuration Timings

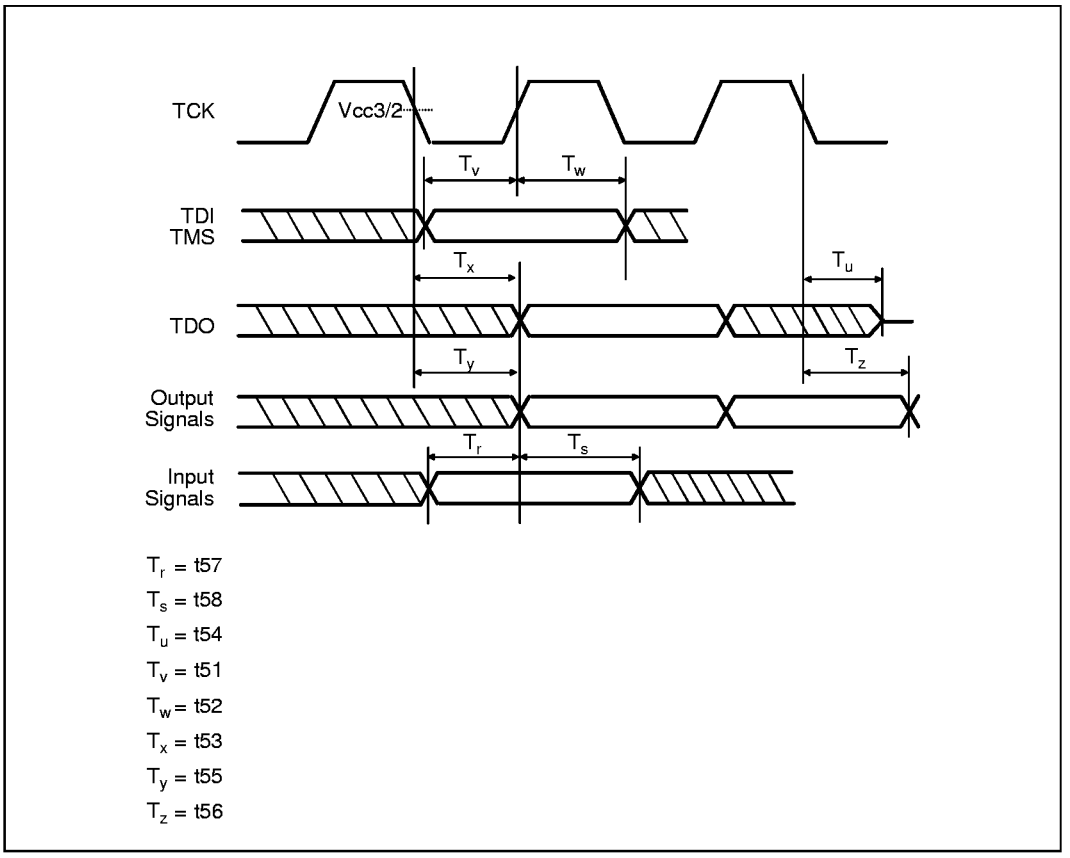


Figure 8. Test Timings

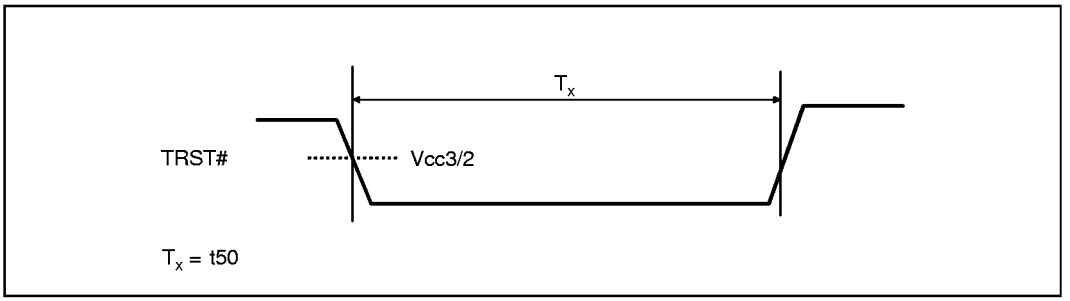


Figure 9. Test Reset Timings

4.4. I/O Buffer Models

This section describes the I/O buffer models of the mobile Pentium processor with MMX technology on 0.25 Micron.

The first order I/O buffer model is a simplified representation of the complex input and output buffers used. Figure 10 shows the structure of the input buffer model and Figure 11 shows the output buffer model. Tables 17 and 18 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors (R_S) are a part of the diode model. Remove these when removing the diodes from the input model.

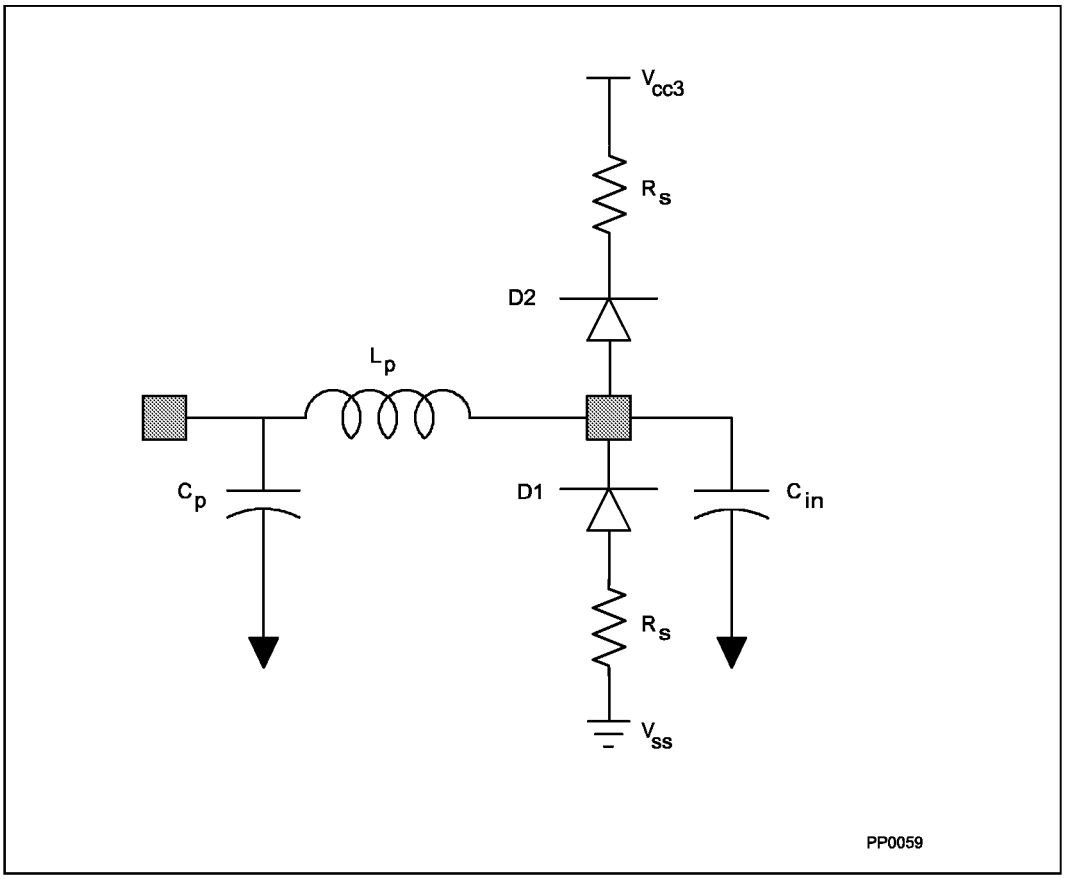


Figure 10. First Order Input Buffer Model

Table 17. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
Cin	Minimum and Maximum value of the capacitance of the input buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance
Rs	Diode Series Resistance
D1, D2	Ideal Diodes

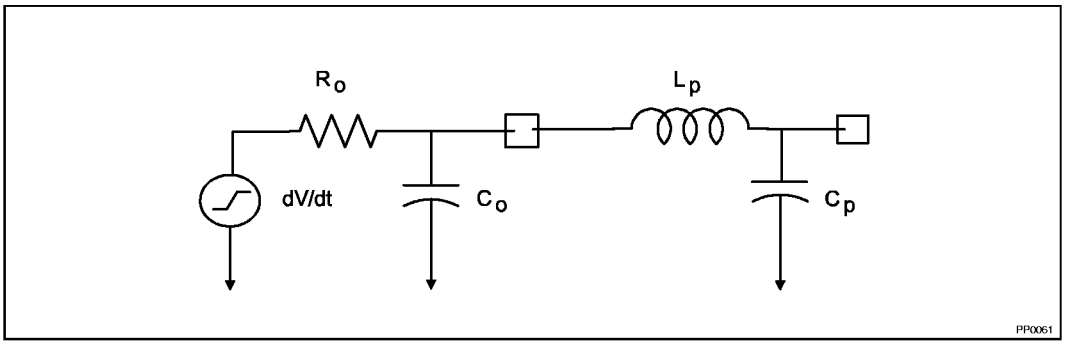


Figure 11. First Order Output Buffer Model

Table 18. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
R_O	Minimum and maximum value of the output impedance of the output buffer model
C_O	Minimum and Maximum value of the capacitance of the output buffer model
L_P	Minimum and Maximum value of the package inductance
C_P	Minimum and Maximum value of the package capacitance

4.4.1. BUFFER MODEL PARAMETERS

This section gives the parameters for each input, output and bidirectional buffers.

The input, output and bidirectional buffer values of the processor are listed in Table 20. These tables contain listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the C_{IN}, C_P and L_P values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 19 for the groupings of the buffers.

The input, output and bi-directional buffer's values are listed below. These tables contain listings for all three types. When a bi-directional pin is operating as an input, just use the C_{IN}, C_P and L_P values, if it is operating as a driver use all the data parameters.

Table 19. TCP Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, PICCLK, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE[7:5]#, BP[3:2], BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO	O	ED1	
A[31: 3], AP, BE[4:0]#, CACHE#, D/C#, D[63:0], DP[8:0], HLDA, LOCK#, M/IO#, SCYC, ADS#, HITM#, HIT#, W/R#, PICD0, PICD1	I/O	EB1	EB1

Table 20. Input, Output and Bi-directional Buffer Model Parameters for TCP

Buffer Type	Transi-tion	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					0.2	0.4	6.4	11.3	0.8	1.2
(input)	Falling					0.2	0.4	6.4	11.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	29	65	0.2	0.5	5.4	11.7	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	25	75	0.2	0.5	5.4	11.7	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	29	65	0.2	0.4	5.2	10.3	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	25	75	0.2	0.4	5.2	10.3	2.0	2.6

Table 21. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e-14A	2.78e-16A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983V	0.967V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

4.4.2. SIGNAL QUALITY SPECIFICATIONS

Signals driven by the system into the mobile Pentium processor with MMX technology on 0.25 Micron must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: Ringback and Settling Time. See Section 4.4.2.3 for CLK signal quality specification.

4.4.2.1. Ringback

Excessive ringback can contribute to long-term reliability degradation of the processor, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC3} (or above V_{SS}) relative to V_{CC3} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

Maximum Ringback on Inputs = 0.5V (falling edge)

Maximum Ringback on Inputs = 0.7V (rising edge)

(with diodes)

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (Undershoot) is the absolute value of the maximum voltage above V_{CC3} (below V_{SS}). The guideline assumes the absence of diodes on the input.

•

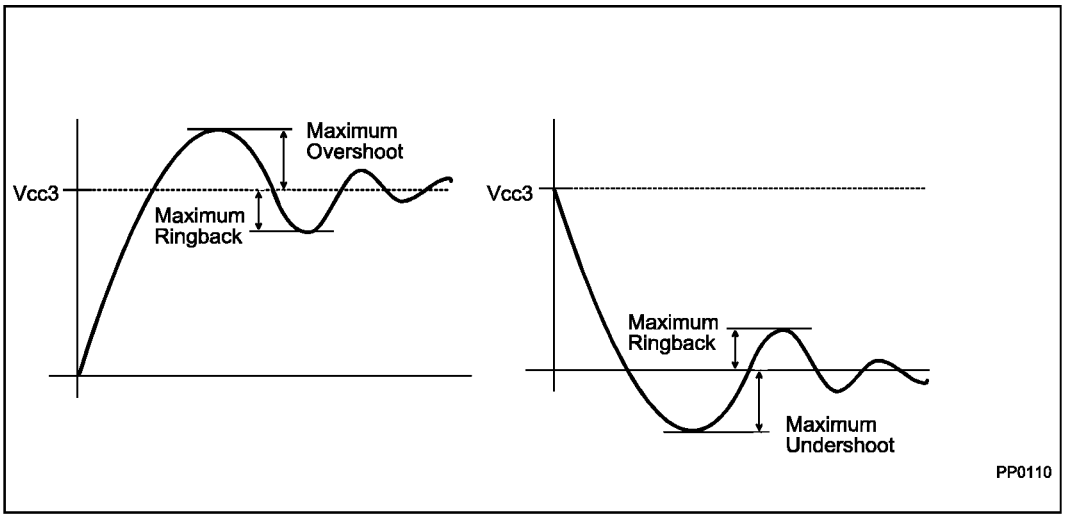


Figure 12. Overshoot/Undershoot and Ringback Guidelines

4.4.2.2. Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10 percent of V_{CC3} or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

- Simulate settling time at the slow corner for a particular signal.
- If settling time violations occur (signal requires more than 12.5 ns. to settle to ± 10 percent of its final value), simulate signal trace with D.C. diodes in place at the receiver pin. The D.C. diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
- If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
- If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.
- Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

Maximum Settling Time to within 10% of V_{IH} or V_{IL} is: 12.5 nS at 66 MHz

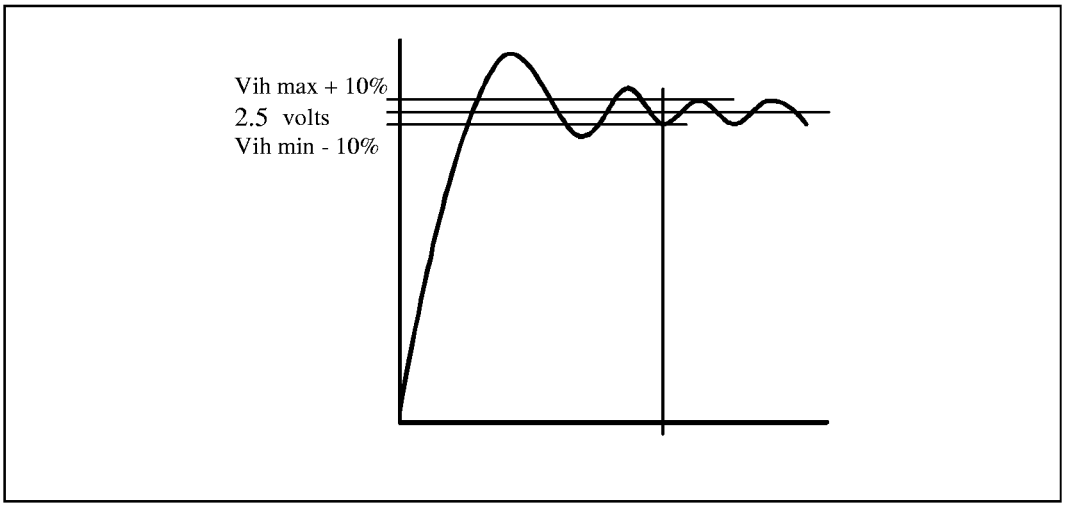


Figure 13. Settling Time

4.4.2.3. Signal Quality Specification

The maximum overshoot, maximum undershoot, overshoot threshold duration, undershoot threshold duration, and maximum ringback specifications for CLK are described below:

MAXIMUM OVERSHOOT AND MAXIMUM UNDERSHOOT SPECIFICATION: The maximum overshoot of the CLK signals should not exceed V_{CC3},nominal + 0.6V. The maximum undershoot of the CLK signals must not drop below -0.6V.

OVERSHOOT THRESHOLD DURATION SPECIFICATION: The overshoot threshold duration is defined as the sum of all time during which the CLK signal is above V_{CC3},nominal + 0.3V within a single clock period. The overshoot threshold duration must not exceed 20 percent of the period.

UNDERSHOOT THRESHOLD DURATION SPECIFICATION: The undershoot threshold duration is defined as the sum of all time during which the CLK signal is below -0.3V within a single clock period. The undershoot threshold duration must not exceed 20 percent of the period.

MAXIMUM RINGBACK SPECIFICATION: The maximum ringback of CLK associated with their high states (overshoot) must not drop below V_{CC3} - 0.7V as shown in Figure 15. Similarly, the maximum ringback of CLK associated with their low states (undershoot) must not exceed 0.5V as shown in Figure 17.

Refer to Table 22 and Table 23 for a summary of the clock overshoot and undershoot specifications for the 200- and 233 MHz Pentium processor with MMX technology.

Table 22. Overshoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	$V_{CC}3$,nominal + 0.3 (CLK & PICCLK) $V_{CC}3$,nominal + 0.5 (All other inputs)	V	1,2
Maximum Overshoot Level	$V_{CC}3$,nominal + 0.6 (CLK & PICCLK) $V_{CC}3$,nominal + 1.0 (All other inputs)	V	1,2
Maximum Threshold Duration	20% of clock period above threshold voltage	nS	2
Maximum Ringback	$V_{CC}3$,nominal - 0.7	V	1,2

NOTES:

1. V_{CC3}, nominal refers to the voltage measured at the bottom side of the $V_{CC}3$ pins. See Section 4.3.1. for details.
2. See Figures 14 and 15.

Table 23. Undershoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	- 0.3 (CLK & PICCLK) - 0.5 (All other inputs)	V	See Figures 18 & 19
Minimum Undershoot Level	- 0.6 (CLK & PICCLK) - 1.0 (All other inputs)	V	See Figures 18 & 19
Maximum Threshold Duration	20% of clock period below threshold voltage	nS	See Figures 18 & 19
Maximum Ringback	0.5	V	See Figures 18 & 19

4.4.3. CLOCK SIGNAL MEASUREMENT METHODOLOGY: The waveform of the clock signals should be measured at the bottom side of the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 MS/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board. An 1 MOhm probe with loading of less than 1 pF (e.g., Tektronics 6243 or Tektronics 6245) is recommended. The measurement should be taken at the CLK (AK18) pin and its nearest V_{SS} pin (AM18).

MAXIMUM OVERSHOOT, MAXIMUM UNDERSHOOT AND MAXIMUM RINGBACK SPECIFICATIONS: The display should show continuous sampling (e.g., infinite persistence) of the waveform at 500 mV/div and 5 nS/div for a recommended duration of approximately five seconds. Adjust the vertical position to measure the maximum overshoot and associated ringback with the largest possible granularity. Similarly, readjust the vertical position to measure the maximum undershoot and associated ringback.

There is no allowance for crossing the maximum overshoot, maximum undershoot or maximum ringback specifications.

OVERSHOOT THRESHOLD DURATION SPECIFICATION: A snapshot of the clock signal should be taken at 500 mV/div and 500 pS/div. Adjust the vertical position and horizontal offset position to view the threshold duration. The overshoot threshold duration is defined as the sum of all time during which the clock signal is above V_{CC3},nominal + 0.3V within a single clock period. The overshoot threshold duration must not exceed 20 percent of the period.

UNDERSHOOT THRESHOLD DURATION SPECIFICATION: A snapshot of the clock signal should be taken at 500 mV/div and 500 pS/div. Adjust the vertical position and horizontal offset position to view the threshold duration. The undershoot threshold duration is defined as the sum of all time during which the clock signal is below -0.3V within a single clock period. The undershoot threshold duration must not exceed 20 percent of the period.

These overshoot and undershoot specifications are illustrated graphically in Figures 14 through 17.

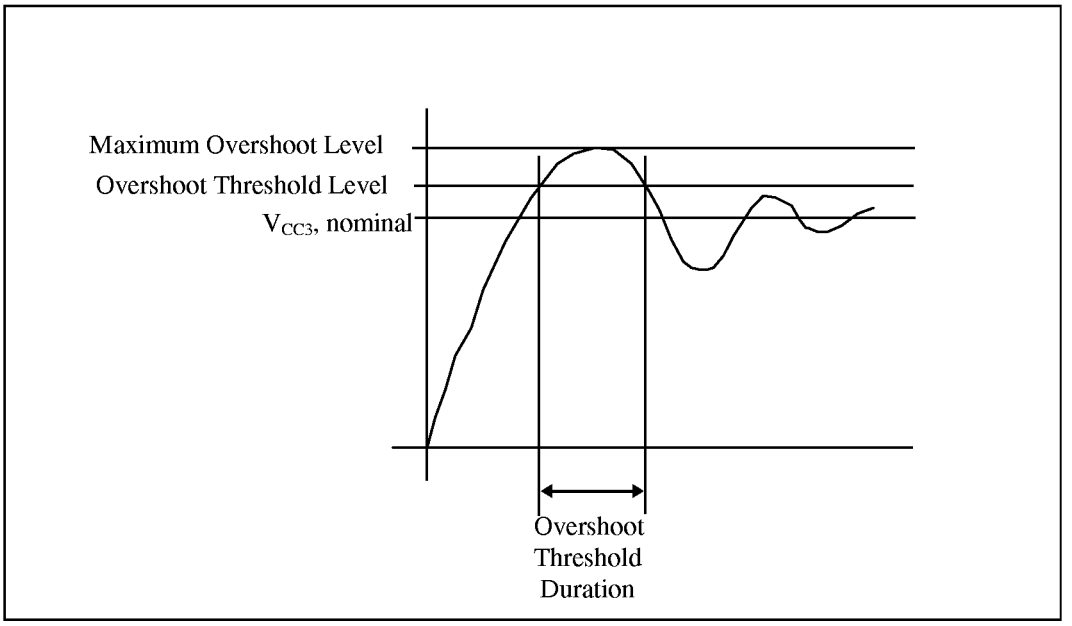


Figure 14. Maximum Overshoot Level, Overshoot Threshold Level, and Overshoot Threshold Duration

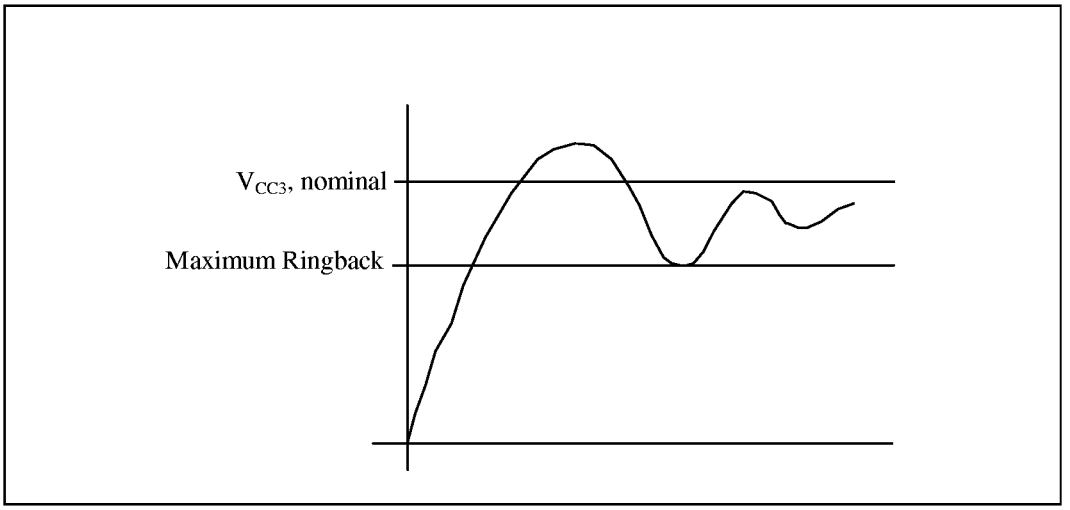


Figure 15. Maximum Ringback Associated with the Signal High State

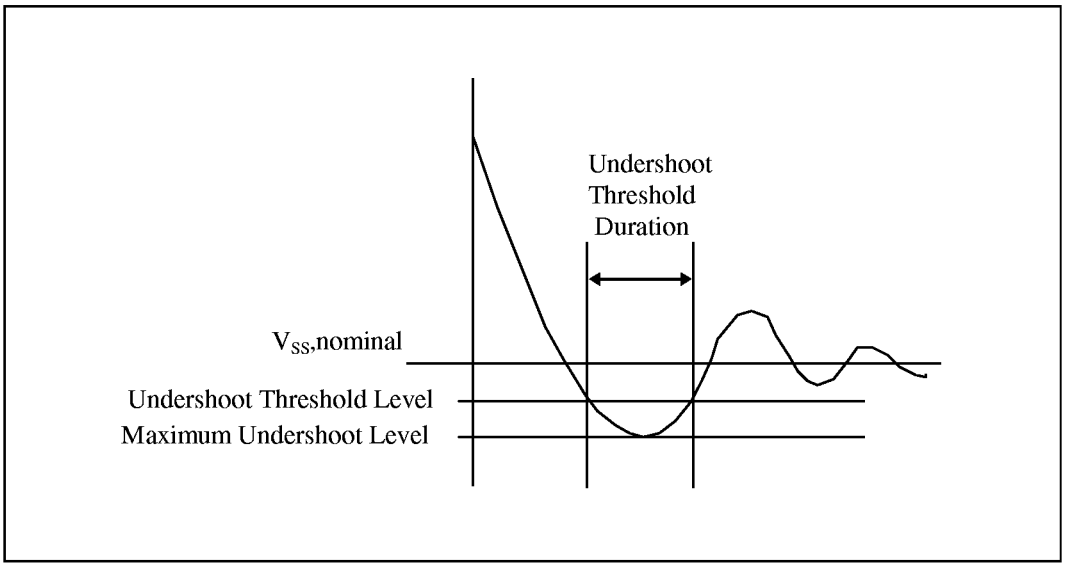


Figure 16. Maximum Undershoot Level, Undershoot Threshold Level, and Undershoot Threshold Duration

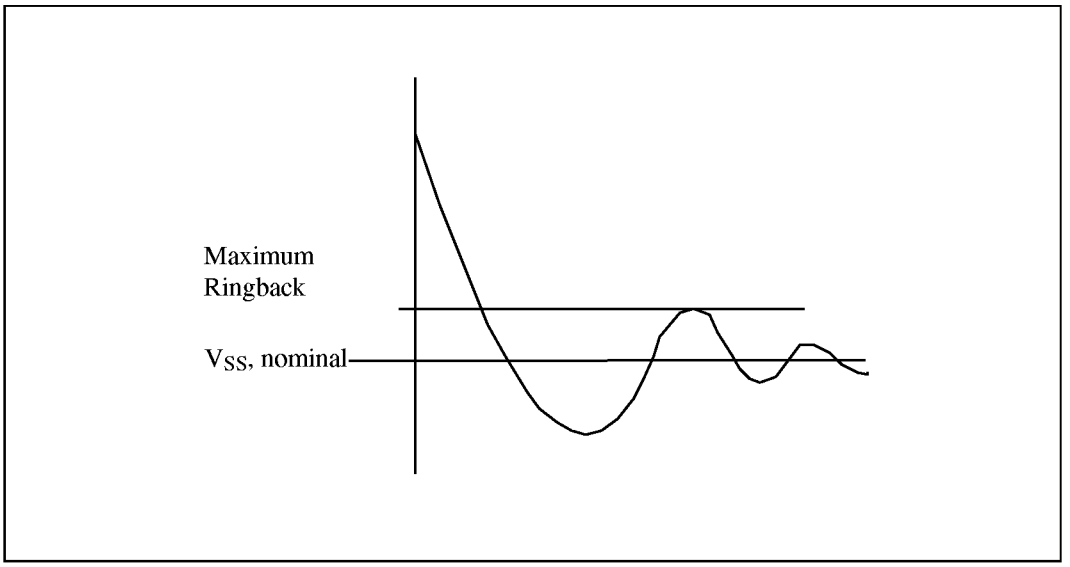


Figure 17. Maximum Ringback Associated with the Signal Low State

5.0. MECHANICAL SPECIFICATIONS

Today's portable computers face the challenge of meeting desktop performance in an environment that is constrained by thermal, mechanical and electrical design considerations. These considerations have driven the development and implementation of Intel's Tape Carrier Package (TCP). The Intel TCP has been designed to offer a high pin count, low profile, reduced footprint package with uncompromised thermal and electrical performance. Intel continues to provide packaging solutions that meet our rigorous criteria for quality and performance.

Key features of the TCP include: surface mount technology design, lead pitch of 0.25 mm, polyimide body size of 24 mm and polyimide up for pick-and-place handling. TCP components are shipped with the leads flat in slide carriers, and are designed to be excised and lead formed at the customer manufacturing site. Recommendations for the manufacture of this package are included in the *1996 Packaging Databook* (Order Number 240800) or at www.intel.lv/design/packtech/chap12.pdf.

Figure 18 shows a cross-section view of the TCP as mounted on the Printed Circuit Board. Figures 19 and 20 show the TCP as shipped in its slide carrier, and key dimensions of the carrier and package. Figure 21 shows a cross-section detail of the package. Figure 22 shows an enlarged view of the outer lead bond area of the package.

5.1. TCP Mechanical Diagrams

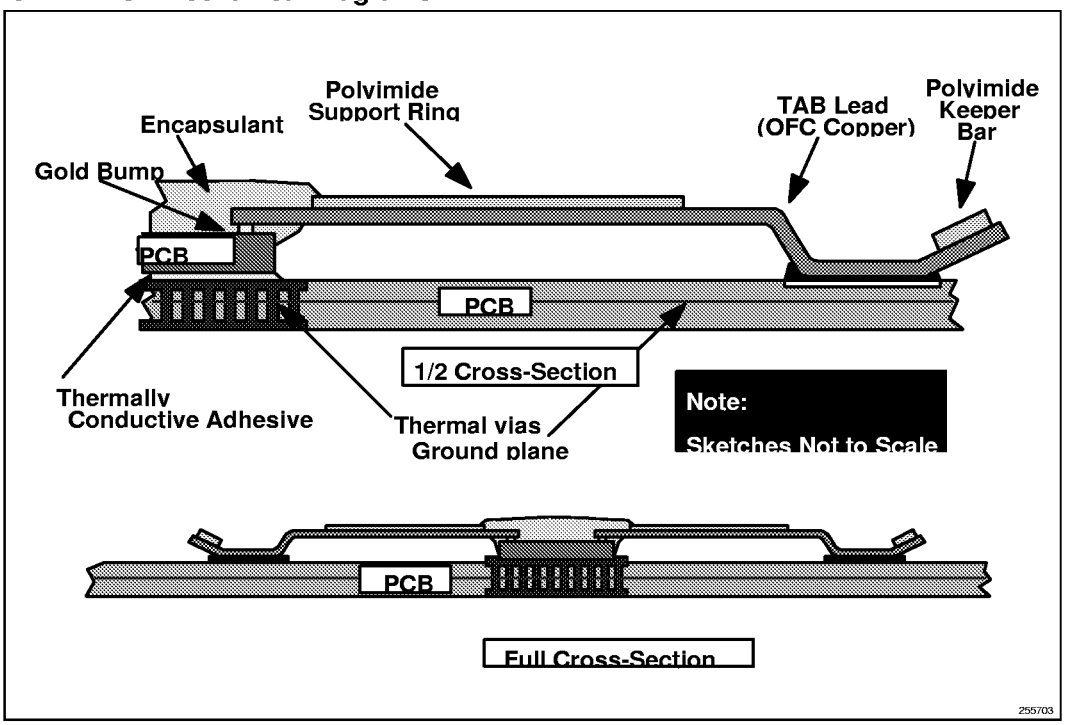


Figure 18. Cross-Sectional View of the Mounted TCP

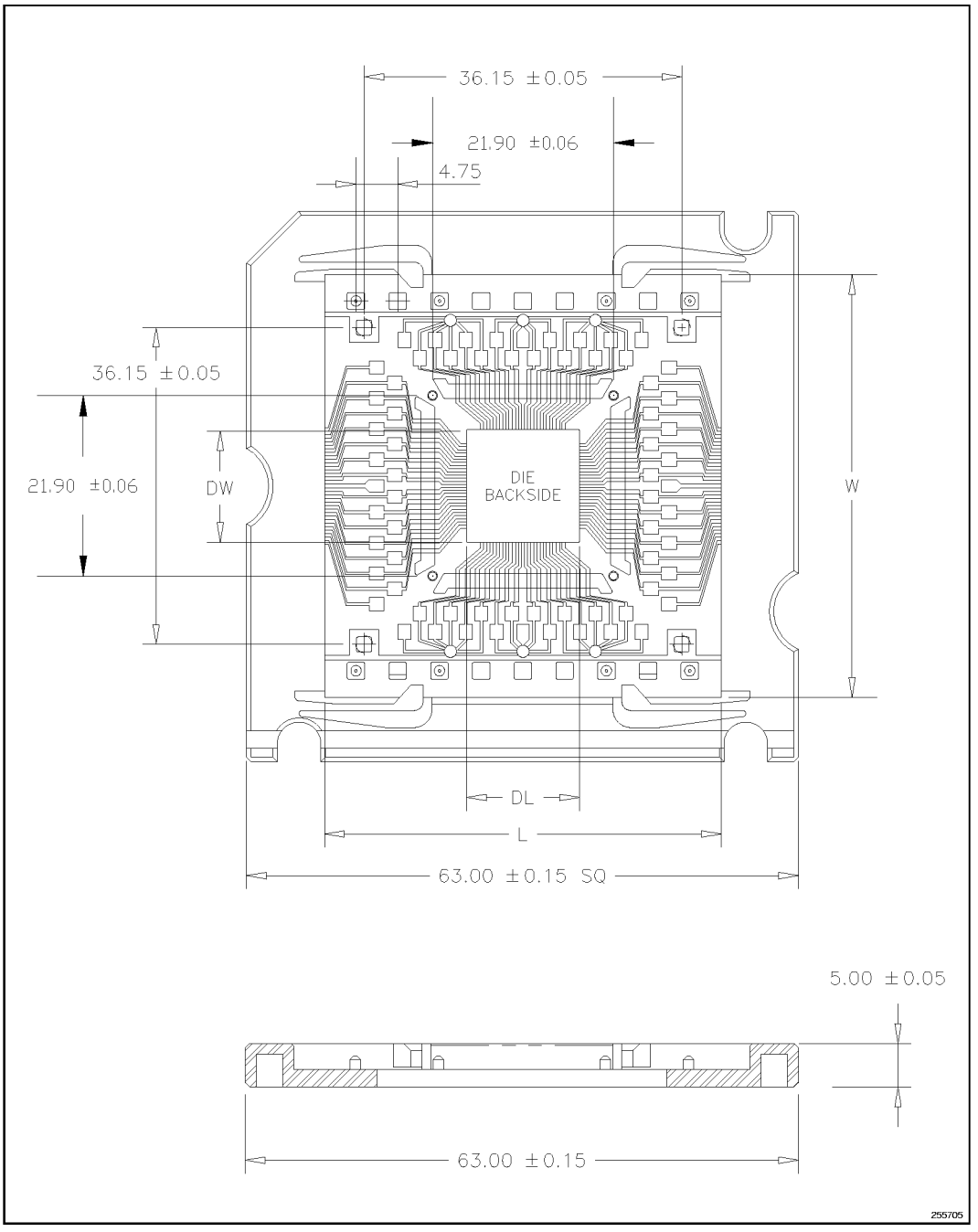


Figure 19. One TCP Site in Carrier (Bottom View of Die)

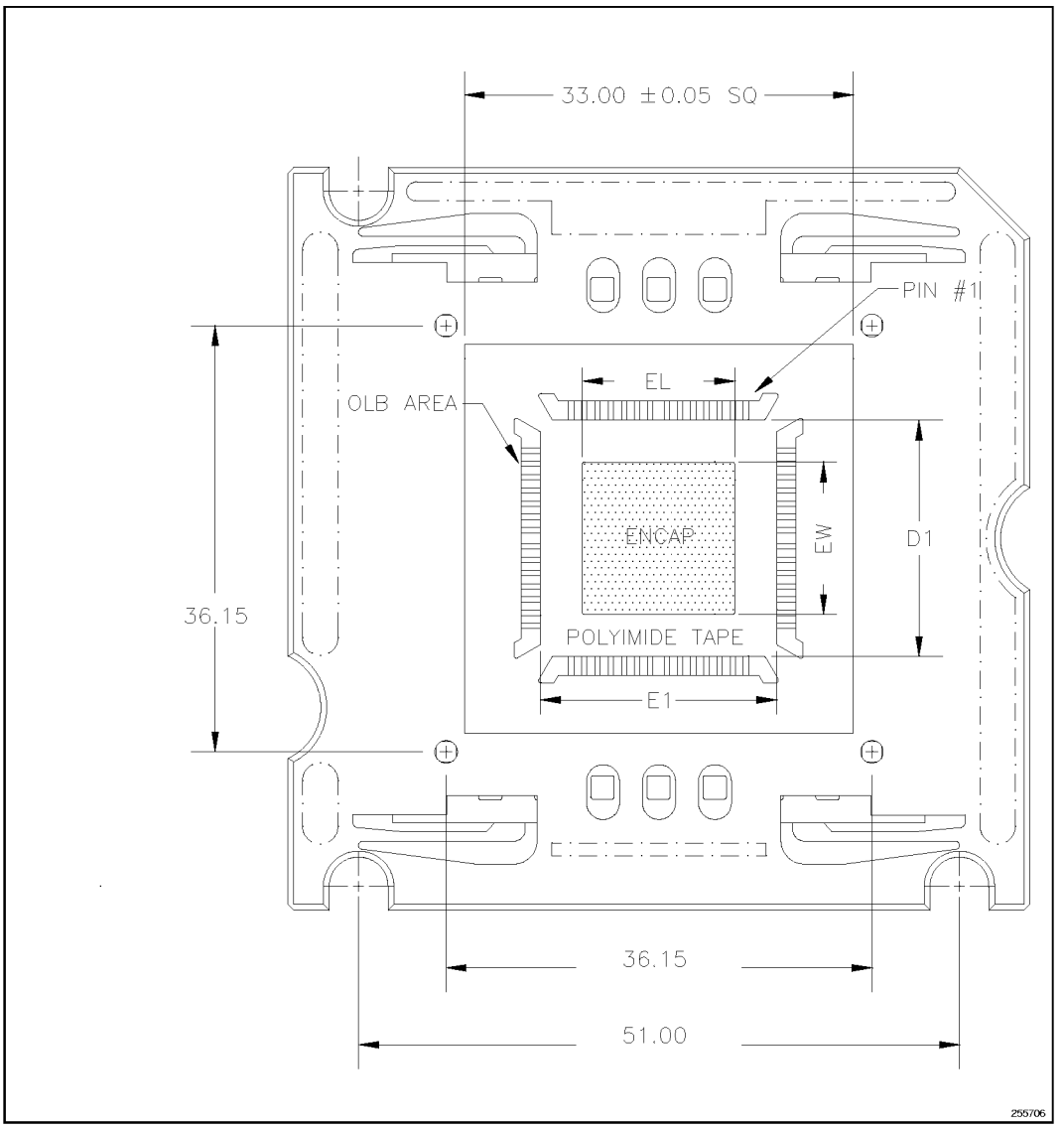


Figure 20. One TCP Site in Carrier (Top View of Die)

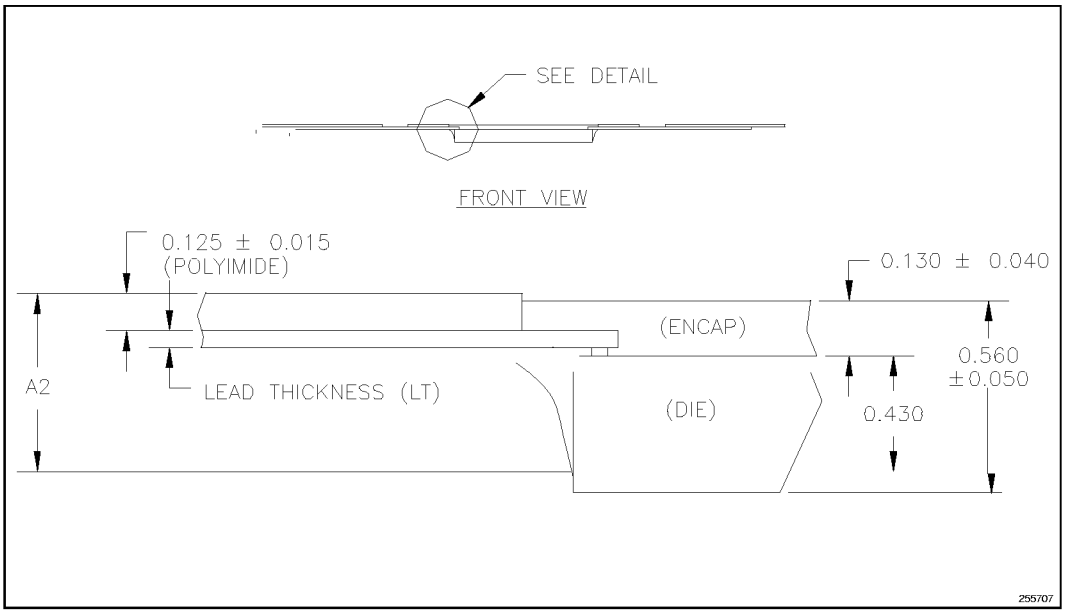


Figure 21. One TCP Site (Cross-Sectional Detail)

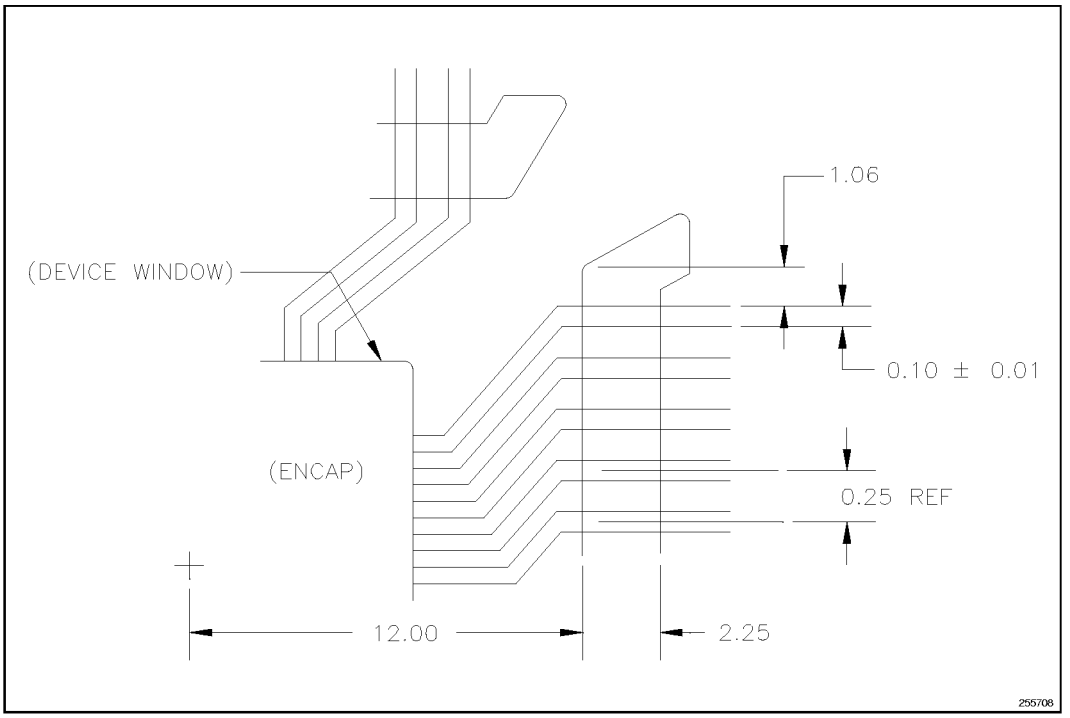


Figure 22. Outer Lead Bond (OLB) Window Detail

Table 24. TCP Key Dimensions

Symbol	Description	Dimension
N	Leadcount	320 leads
W	Tape Width	48.18 ±0.12
L	Site Length	(43.94) reference only
T	Test Pad Pitch	0.40 nominal
e1	Outer Lead Pitch	0.25 nominal
b	Outer Lead Width	0.10 ±0.01
D1,E1	Package Body Size	24.0 ±0.1
A2	Package Height	0.597 ±0.030
DL	Die Length	10.450 +/- 0.015
DW	Die Width	9.088 +/- 0.015
LT	Lead Thickness	0.025 mm
EL	Encap Length	11.053 +/- 0.015
EW	Encap Width	9.691 +/- 0.015

NOTES:
- Dimensions are in millimeters unless otherwise noted.
- Dimensions in parentheses are for reference only.

Table 25. Mounted TCP Dimensions

Symbol	Description	Dimension
A	Package Height	0.75 maximum
D, E	Terminal Dimension	29.5 nominal
WT	Package Weight	0.5 g maximum

NOTE:
- Dimensions are in millimeters unless otherwise noted.
- Package terminal dimension (lead tip-to-lead tip) assumes the use of a keeper bar.

6.0. THERMAL SPECIFICATIONS

The mobile Pentium processor with MMX technology on 0.25 Micron is specified for proper operation when the case temperature, T_{CASE} (T_C), for TCP is within the specified range of 0 °C to 95 °C.

6.1. Measuring Thermal Values for TCP

To verify that the proper T_C (case temperature) is maintained, it should be measured at the center of the package top surface (encapsulant). To minimize any measurement errors, the following techniques are recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using highly thermally conductive cements. Intel's laboratory testing was done by using Omega Bond* (part number: OB-100).
- The thermocouple should be attached at a 90° angle as shown in Figure 23.

6.1.1. TCP Thermal Equations

For the TCP mobile Pentium processor with MMX technology, an ambient temperature (T_A) is not specified directly. The only requirement is that the case temperature (T_C) is met. The ambient temperature can be calculated from the following equations:

$$T_J = T_C + P \times \theta_{JC}$$
$$T_A = T_J - P \times \theta_{JA}$$
$$T_A = T_C - (P \times \theta_{CA})$$
$$T_C = T_A + P \times [\theta_{JA} - \theta_{JC}]$$
$$\theta_{CA} = \theta_{JA} - \theta_{JC}$$

where,

T_A and T_C are ambient and case temperatures (°C)

θ_{CA} = Case-to-Ambient thermal resistance (°C/W)

θ_{JA} = Junction-to-Ambient thermal resistance (°C/W)

θ_{JC} = Junction-to-Case thermal resistance (°C/W)

P = maximum power consumption (Watts)

P (maximum power consumption) is specified in Section 3.1.

6.1.2. TCP Thermal Characteristics

The primary heat transfer path from the die of the TCP is through the back side of the die and into the PC board. There are two thermal paths traveling from the PC board to the ambient air. One is the spread of heat within the board and the dissipation of heat by the board to the ambient air. The other is the transfer of heat through the board and to the opposite side where thermal enhancements (e.g., heat sinks, pipes) are attached. Solder-side heat sinking, compared to TCP component-side heat sinking, is the preferred method due to reduced risk of die damage, easier mechanical implementation and larger surface area for attachment. However, component-side heat sinking is possible. The design requirements in a component-side thermal solution are: no direct loading of inner lead bonds on the TCP, a maximum force of 4.5 kgf on the center of a clean TCP, no direct loading of the TAB tape or outer lead bonds and controlled board deflection.

6.1.3. TCP PC Board Enhancements

Copper planes, thermal pads, and vias are design options that can be used to improve heat transfer from the PC board to the ambient air. Tables 26 and 27 present thermal resistance data for copper plane thickness and via effects. It should be noted that although thicker copper planes will reduce the θ_{ca} of a system without any thermal enhancements, they have less effect on the θ_{ca} of a system with thermal enhancements. However, placing vias under the die will reduce the θ_{ca} of a system with and without thermal enhancements.

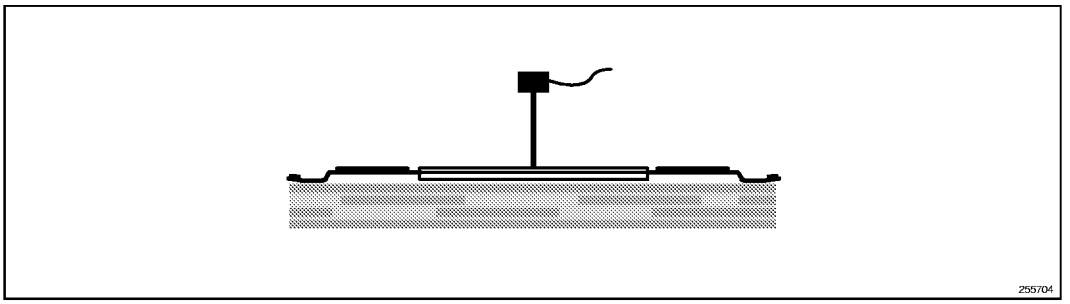


Figure 23. Technique for Measuring Case Temperature (T_C) on TCP

Table 26. TCP Thermal Resistance vs. Copper Plane Thickness With and Without Enhancements

Copper Plane Thickness*	q_{CA} (°C/Watt) No Enhancements	q_{CA} (°C/Watt) With Heat Pipe and Al Plates
1 oz. Cu	18	7.8
3 oz. Cu	14	7.8

NOTE:
*225 vias underneath the die

Table 27. TCP Thermal Resistance vs. Thermal Vias Underneath the Die

Number of Vias Under the Die*	q_{CA} (°C/Watt) No Enhancements
0	15
144	13

NOTE:
*3 oz. copper planes in tet boards

6.1.3.1. TCP STANDARD TEST BOARD CONFIGURATION

All Tape Carrier Package (TCP) thermal measurements familiarity provided in the following tables were taken with the component soldered to a 2" x 2" test board outline. This six-layer board contains 225 vias in the die attach pad which are connected to two 3 oz. copper planes located at layers two and five. For the TCP, the vias in the die attach pad should be connected without thermal reliefs to the ground plane(s). The die is attached to the die attach pad using a thermally conductive adhesive. This test board was designed to optimize the heat spreading into the board and the heat transfer through to the opposite side of the board.

NOTE

Thermal resistance values should be used as guidelines only, and are highly system dependent. Final system verification should always refer to the case temperature specification.

Table 28. TCP Thermal Resistance without Enhancements

	q_{JC} (°C/Watt)	q_{CA} (°C/Watt)
Thermal Resistance without Enhancements	0.8	14

Table 29. TCP Thermal Resistance with Enhancements (Without Airflow)

Thermal Enhancements	q_{CA} (°C/W)	Notes
Heat sink	11.7	1.2"×1.2"×.35"
Al Plate	8.7	4"×4"×.030"
Al Plate with Heat Pipe	7.8	0.3”×1"×4" Heat pipe 4”x4”x0.3” Al plate

Table 30. TCP Thermal Resistance with Enhancements (With Airflow)

Thermal Enhancements	q_{CA} (°C/W)	Notes
Heat sink with Fan @ 1.7 CFM	5.0	1.2"×1.2"×.35" HS 1"×1"×.4" Fan
Heat sink with Airflow @ 400 LFM	5.1	1.2”x1.2”x.35” HS
Heat sink with Airflow @ 600 LFM	4.3	1.2"×1.2"×.35" HS

NOTES:
HS = heat sink
LFM = Linear Feet/Minute
CFM = Cubic Feet/Minute