809XJC/839XJC/879XJC
ADVANCED 16-BIT MICROCONTROLLER WITH 8- OR 16-BIT EXTERNAL BUS

Automotive

- (−40°C to +125°C Case)
- 232 Bytes of On-Chip Register RAM
- 128 Byte External RAM On-Chip
- 12 Kbytes of On-Chip ROM/EPROM
- High Performance HMOS Process
- Register-to-Register Architecture
- 10-Bit A/D Converter with S/H
- Five 8-Bit I/O Ports
- 20 Interrupt Sources
- 8-Bit Pulse Width Modulated Output
- Dedicated Baud Rate Generator
- High Speed I/O Subsystem
- Full Duplex Serial Port
- 6.25 μs 16 x 16 Multiply
- 6.25 μs 32/16 Divide
- 16-Bit On-Chip Watchdog Timer
- Four 16-Bit Software Timers
- Two 16-Bit Counter/Timers
- 52-Pin PLCC Package
- 68-Pin PLCC and PFP Packages

The 8096 family of 16-bit microcontrollers consist of many members, all of which are designed for high speed control functions. The 8X9XJC members, produced for the automotive environment, use Intel's HMOS-III process, with 12 Kbytes of EPROM/ROM or ROMless and 360 total bytes of on-chip RAM. 232 bytes are register RAM and 128 bytes are additional RAM (addressed as external memory) located on-chip.

The CPU supports bit, byte, and word operations. Thirty-two bit double words are supported for a subset of the instruction set. With a 12 MHz input frequency, the 8X9XJC can do a 16-bit addition in 1.0 μs and a 16 x 16 multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1.0 μs to 2.0 μs in typical applications.

Four high-speed capture inputs are provided to record the times at which external events occur, stored in an eight level FIFO. Rising, falling, rising and falling, or every eight rising edges can be recorded every 2.25 μs using a 12 MHz input clock. Interrupts can be programmed for every FIFO entry, or every 4th FIFO entry, which makes the JC different than other 8096 devices.

Up to 6 high speed pulse generator outputs are provided to trigger external events at preset times. The high speed output unit can simultaneously perform software timer functions, start A/D conversions, or pulse one or more outputs. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold (S/H), and converts up to 8 multiplexed analog input channels to a 10-bit digital result. With 12 MHz input frequency, each conversion takes as little as 22 μs. A/D conversions can be performed at predetermined times or asynchronously.

Also provided on-chip are: a full duplex, double buffered receive serial port with 3 asynchronous and 1 synchronous modes; a 16-bit watchdog timer, and 1 256-state pulse width modulated output signal.

For further 8096 device information refer to the *1995 Embedded Microcontrollers Databook,* (Order Number 270646).

NOTICE:

This datasheet contains information on products in full production. Specifications within this datasheet are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

January 1995
Order Number: 270836-004

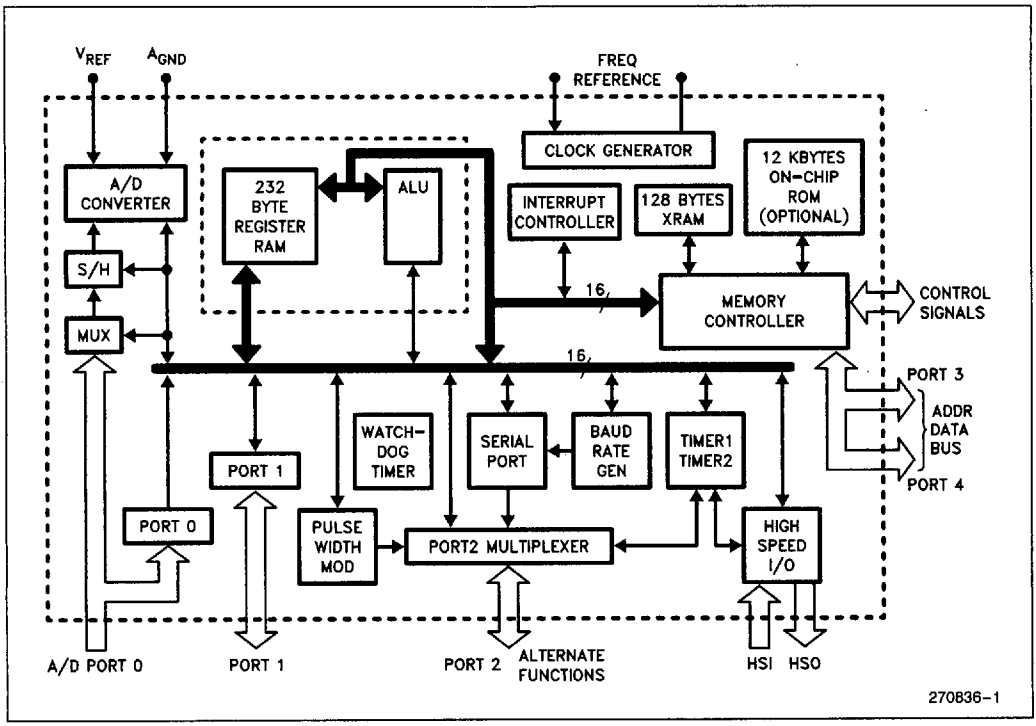
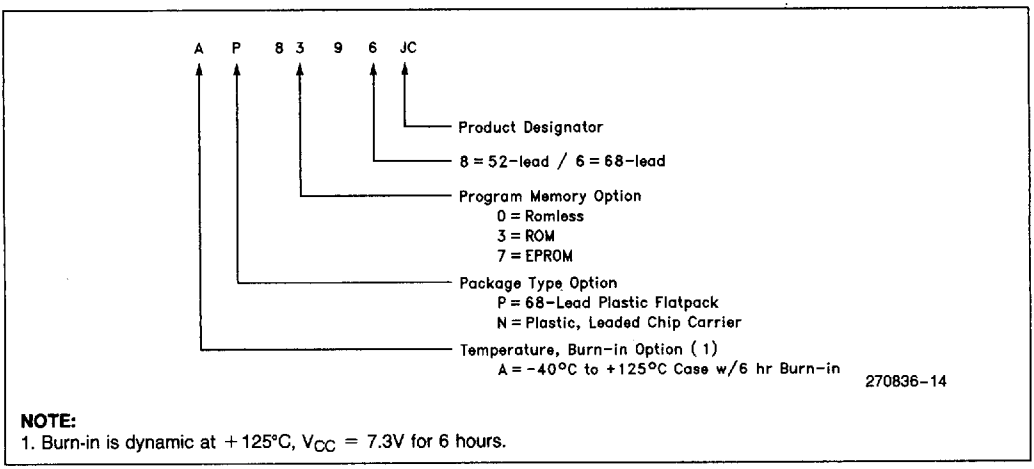


Figure 1. 8X9XJC Block Diagram



NOTE:
1. Burn-in is dynamic at +125°C, V_{CC} = 7.3V for 6 hours.

Figure 2. The 8X9XJC Family Nomenclature

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PFP	52-pin PLCC	68-pin PLCC	Description
1	7	9	ACH7/P0.7
2	6	8	ACH6/P0.6
3	—	7	ACH2/P0.2
4	5	6	ACH0/P0.0
5	4	5	ACH1/P0.1
6	—	4	ACH3/P0.3
7	—	3	NMI
8	3	2	$\overline{EA}$
9	2	1	V_{CC}
10	1	68	V_{SS}
11	52	67	XTAL1
12	51	66	XTAL2
13	—	65	CLKOUT
14	—	64	BUSWIDTH
15	—	63	INST
16	50	62	ALE/$\overline{ADV}$
17	49	61	$\overline{RD}$
18	48	60	AD0/P3.0
19	47	59	AD1/P3.1
20	46	58	AD2/P3.2
21	45	57	AD3/P3.3
22	44	56	AD4/P3.4
23	43	55	AD5/P3.5
24	42	54	AD6/P3.6
25	41	53	AD7/P3.7
26	40	52	AD8/P4.0
27	39	51	AD9/P4.1
28	38	50	AD10/P4.2
29	37	49	AD11/P4.3
30	36	48	AD12/P4.4
31	35	47	AD13/P4.5
32	34	46	AD14/P4.6
33	33	45	AD15/P4.7
34	—	44	T2CLK/P2.3

PFP	52-pin PLCC	68-pin PLCC	Description
35	32	43	READY
36	31	42	T2RST/P2.4
37	—	41	BHE/$\overline{WRH}$
38	30	40	$\overline{WR}$/$\overline{WRL}$
39	29	39	PWM/P2.5
40	28	38	P2.7/
41	27	37	V_{PP}
42	26	36	V_{SS}
43	25	35	HSO.3
44	—	34	HSO.2
45	24	33	P2.6
46	—	32	P1.7
47	23	31	P1.6
48	22	30	P1.5
49	—	29	HSO.1
50	—	28	HSO.0
51	21	27	HSO.5/HSI.3
52	20	26	HSO.4/HSI.2
53	19	25	HSI.1
54	18	24	HSI.0
55	—	23	P1.4
56	17	22	P1.3
57	—	21	P1.2
58	—	20	P1.1
59	—	19	P1.0
60	16	18	TXD/P2.0
61	15	17	RXD/P2.1
62	14	16	$\overline{RESET}$
63	13	15	EXTINT/P2.2
64	12	14	V_{PD}
65	11	13	V_{REF}
66	10	12	ANGND
67	9	11	ACH4/P0.4
68	8	10	ACH5/P0.5

Figure 3. PLCC and PFP Functional Pinouts

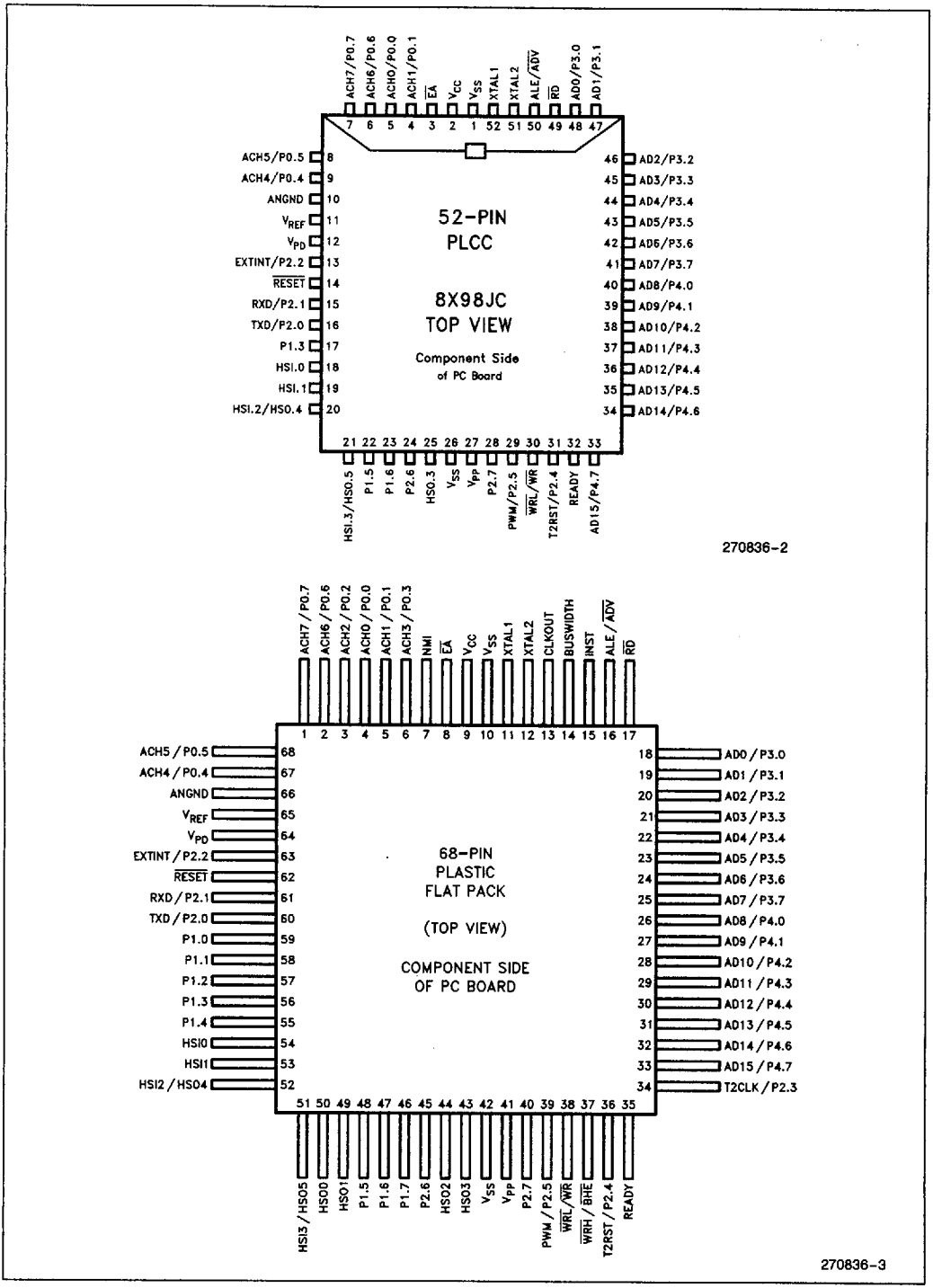

Figure 4. Package Diagrams

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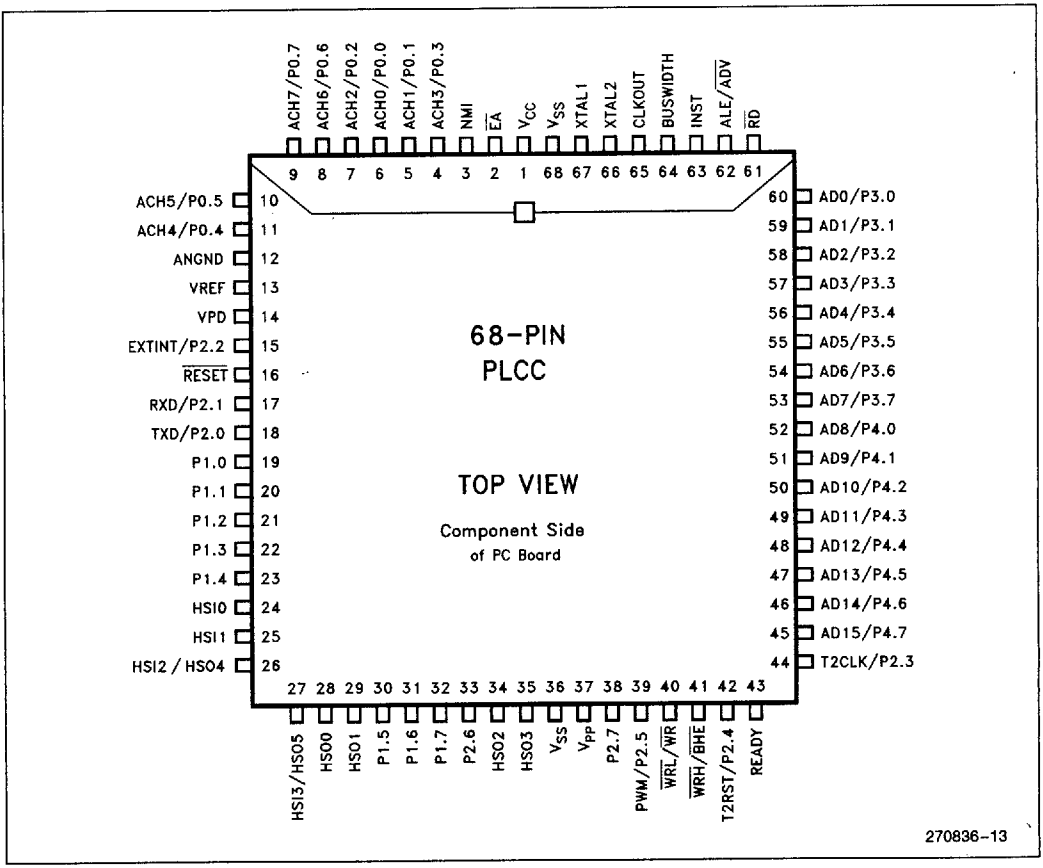

Figure 5. 68-Pin PLCC Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V)
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which MUST be connected.
V_{PD}	RAM standby supply voltage (+5V). This voltage must be present during normal operation. In a Power Down condition (i.e., V_{CC} drops to zero volts), if $\overline{RESET}$ is activated before V_{CC} drops below specification and V_{PD} continues to be held within specification, the upper 16 bytes in the Register File will be retained. $\overline{RESET}$ must be held low during the Power Down and should not be brought high until V_{CC} is within specification and the oscillator has stabilized.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.75V for programming. This pin is V_{BB} on 8X9X-90 parts. Systems that have this pin connected to ANGND through a capacitor (required on 8X9X-90 parts) do not need to change.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle.
$\overline{RESET}$	Reset input to the chip. Input low for at least 2 state times will reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, a byte is read from 2018H loading the CCB, and a jump to location 2080H is executed. Input high for normal operation. $\overline{RESET}$ has an internal pullup.
BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one, this pin selects the buswidth for the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. This pin is the $\overline{TEST}$ pin on the 8X9X-90 parts. Systems with $\overline{TEST}$ tied to V_{CC} need NOT change. Internal Pullup.
NMI	A positive transition causes a vector to external memory location 0000H. External memory from 00H through 0FFH is reserved for Intel development systems.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory fetches, during internal EPROM/ROM fetches INST is held low.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 4FFFH to be directed to on-chip EPROM/ROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ = +12.75V causes an execution to begin in the Programming Mode. $\overline{EA}$ has an internal pulldown, so it defaults to execute from external memory, unless otherwise driven. $\overline{EA}$ is latched at reset.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. $\overline{ADV}$ can be used as a chip select for a single external RAM memory. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR, $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is only for external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Byte High Enable or Write High output to external memory only, is selected by the CCR. $\overline{BHE}$ low selects the bank of memory that is connected to the high byte of the data bus. A0 low selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 low, $\overline{BHE}$ high), to the high byte only (A0 high, $\overline{BHE}$ low) or both bytes (A0 low, $\overline{BHE}$ low). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location.
READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high. CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. The bus cycle can be lengthened up to 1 μs. When the external memory is not used, READY has no effect. Internal control of the number of wait states inserted into the bus cycle held not ready is available through the CCR. READY has a weak pullup.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of which are shared with the HSO Unit (HSI.2 and HSI.3). The HSI pins are also used as inputs by EPROM parts in Programming Mode.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available (HSO.0 through HSO.5). HSO.4 and HSO.5 are shared with HSI.
PORT 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts in the Programming Mode.
PORT 1	8-bit quasi-bidirectional port.
PORT 2	8-bit multi-functional port. Six of its pins are shared with other functions. The two remaining are quasi-bidirectional. These pins are also used to input and output control signals on EPROM parts in Programming Mode.
PORTS 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Ports 3 and 4 are also used as a command, address and data path by EPROM parts operating in the Programming Mode.

ELECTRICAL CHARACTERISTICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias . . . −40°C to +125°C

Storage Temperature . . . . . −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND . . . . . −0.3V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND . . . . . −0.3V to +7.0V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_C	Case Temperature under Bias	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	6.0	12.0	MHz
V_{PD}	Power Down Supply Voltage	4.50	5.50	V

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS Under Listed Operating Conditions

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current (−40°C to +125°C Case)		260	mA	All Outputs Disconnected
I_{CC1}	V_{CC} Supply Current (T_C = 125°C)		170	mA	All Outputs Disconnected
I_{PD}	V_{PD} Supply Current		1	mA	Normal Oper. & PD
I_{REF}	V_{REF} Supply Current		10	mA	
V_{IL}	Input Low Voltage (except $\overline{RST}$)	−0.3	+0.8	V	
V_{IL1}	Input Low Voltage ($\overline{RST}$)	−0.3	+0.8	V	
V_{IH}	Input High Voltage (except $\overline{RST}$, NMI, XTAL1)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage $\overline{RST}$ Rising Hysteresis	2.4	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage $\overline{RST}$ Falling Hysteresis	2.1	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage NMI, XTAL1	2.3	V_{CC} + 0.5	V	
I_{LI}	Input Leakage Current, All HSI, P3, P4 and P2.1		±10	µA	V_{IN} = 0 to V_{CC}

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DC CHARACTERISTICS Under Listed Operating Conditions (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{LI1}	D.C. Input Leakage Current, All P0		+3	μA	V_{IN} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH} = 2.4V
I_{IL}	Input Low Current, All P1, P2.6, and P2.7		−150	μA	V_{IL} = 0.45V
I_{IL1}	Input Low Current to $\overline{RST}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current P2.2, P2.3, P2.4, RDY, Buswidth		−50	μA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage, All Quasi I/O, P3, P4		0.45	V	I_{OL} = 0.8 mA(1)
V_{OL1}(4)	Output Low Voltage, All Quasi I/O, P3, P4		0.75	V	I_{OL} = 2.0 mA(1, 2, 3)
V_{OL2}	Output Low Voltage, Standard I/O, Bus, Control Pins		0.45	V	I_{OL} = 2.0 mA(1, 2, 3)
V_{OH}	Output High Voltage on Quasi-I/O Pins	2.4		V	I_{OH} = −20 μA(1)
V_{OH1}	Output High Voltage, Standard I/O, Bus, Control Pins	2.4		V	I_{OH} = −200 μA(1)
I_{OH3}	Output High Current on $\overline{RST}$	−50		μA	V_{OH} = 2.4V(4)
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Quasi-bidirectional pins include those on P1, P2.6 and P2.7. Standard Output Pins include RXD (mode 0), TXD, PWM and HSO pins. Note 4 applies to RXD in mode 0. Bus/Cntl pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, INST and AD0–15.
2. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V.
   I_{OL} on quasi-bidirectional pins: 4.0 mA
   I_{OL} on standard output pins and $\overline{RST}$: 8.0 mA
   I_{OL} on Bus/Cntl pins: 2.0 mA
3. During normal (non-transient) operation the following limits apply:
   Total I_{OL} on P1 must not exceed 4.0 mA
   Total I_{OL} on P2.0, P2.6, $\overline{RST}$, and all HSO pins must not exceed 17.0 mA
   Total I_{OL} on P2.5 and P2.7 must not exceed 4.0 mA
4. These values are not tested in production, and are based on theoretical estimates and/or laboratory tests.
5. I_{OL} is typically greater than 4.0 mA, but is tested to 0.36 mA.

AC CHARACTERISTICS V_{CC}, V_{PD} = 5.0V ± 0.5V; T_C = −40°C to +125°C
F_{OSC} = 6.0 MHz to 12.0 MHz

Test Conditions: Load Capacitance on Output Pins = 80 pF; F_{OSC} = 12.0 MHz

TIMING REQUIREMENTS (Other System Components Must Meet These Specifications)

Symbol	Parameter	Min	Max	Units
T_{CLYX}	READY Hold after CLKOUT Edge	0		ns
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		2 T_{OSC} − 70	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	2 T_{OSC} + 40	4 T_{OSC} − 80	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(1)	Address Valid to Input Data Valid		5 T_{OSC} − 120	ns

NOTE:
1. Address valid applies to AD015, $\overline{BHE}$ and INST.

TIMING REQUIREMENTS (Other System Components Must Meet These Specifications)

Symbol	Parameter	Min	Max	Units
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$3T_{OSC} - 100$	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	$T_{OSC} - 25$	ns
T_{AVGV}(1)	Address Valid to Buswidth Valid		$2T_{OSC} - 125$	ns
T_{LLGX}	Buswidth Hold after ALE/$\overline{ADV}$ Low	$T_{OSC} + 40$		ns
T_{LLGV}	ALE/$\overline{ADV}$ Low to Buswidth Valid		$T_{OSC} - 95$	ns

NOTE:
1. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.

AC CHARACTERISTICS V_{CC}, V_{PD} = 5.0V ± 0.5V; T_C = −40°C to +125°C
F_{OSC} = 6.0 MHz to 12.0 MHz

Test Conditions: Load Capacitance on Output Pins = 80 pF; F_{OSC} = 12.0 MHz

TIMING REQUIREMENTS (8X9XJC Devices Meet These Specifications)

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	6.0	12.0	ns
T_{OSC}	Oscillator Period	83	166	ns
T_{OHCH}	XTAL1 Rising Edge to CLKOUT Rising Edge	0	120	ns
T_{CHCH}	CLKOUT Period(2)	$3T_{OSC}$(2)	$3T_{OSC}$(2)	ns
T_{CHCL}	CLKOUT High Time	$T_{OSC} - 35$	$T_{OSC} + 10$	ns
T_{CLLH}	CLKOUT Low to ALE High	−30	15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Low to CLKOUT High	$T_{OSC} - 25$	$T_{OSC} + 45$	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	$T_{OSC} - 30$	$T_{OSC} + 35$(3)	ns
T_{AVLL}(4)	Address Setup to End of ALE/$\overline{ADV}$	$T_{OSC} - 50$		ns
T_{RLAZ}(5)	$\overline{RD}$ or $\overline{WR}$ Low Address Float		25(6)	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ Active	$T_{OSC} - 40$		ns
T_{LLAX}	Address Hold after End of ALE/$\overline{ADV}$	$T_{OSC} - 40$		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$3T_{OSC} - 35$		ns
T_{QVWH}	Output Data Valid to End of $\overline{W_R}$/$\overline{W_{RL}}$/$\overline{W_{RH}}$	$3T_{OSC} - 60$		ns
T_{WHQX}	Output Data Hold after $\overline{W_R}$/$\overline{W_{RL}}$/$\overline{W_{RH}}$	$T_{OSC} - 50$		ns
T_{WHLH}	End of $\overline{W_R}$/$\overline{W_{RL}}$/$\overline{W_{RH}}$ to ALE/$\overline{ADV}$ High	$T_{OSC} - 75$		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$3T_{OSC} - 30$		ns
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ Low	$T_{OSC} - 45$		ns
T_{CLLL}	CLOCKOUT Low to ALE/$\overline{ADV}$ Low	$T_{OSC} - 40$(6)	$T_{OSC} + 35$(6)	ns
T_{RHBX}	$\overline{RD}$ High to INST, $\overline{BHE}$, AD0–15 Inactive	$T_{OSC} - 25$	$T_{OSC} + 30$	ns

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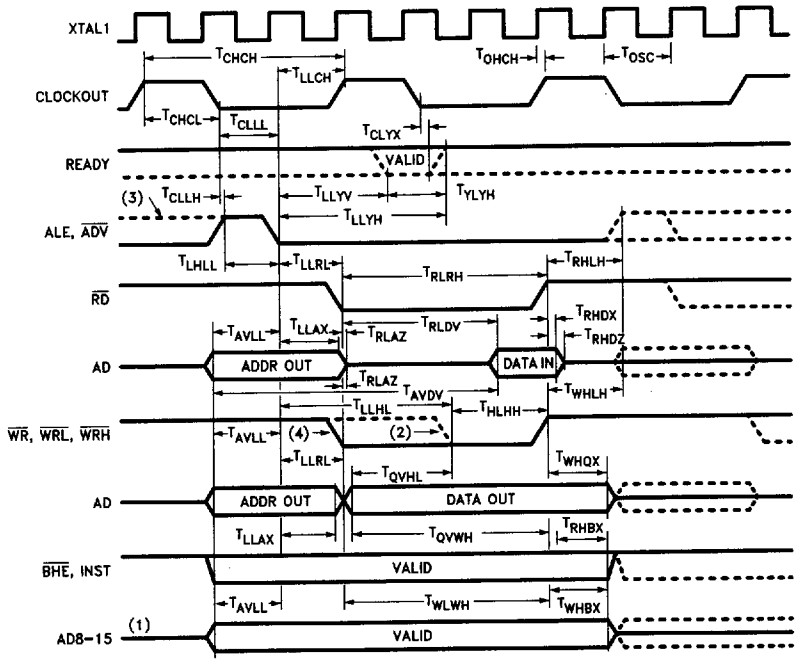
TIMING REQUIREMENTS (8X97JC Devices Meet These Specifications)

Symbol	Parameter	Min	Max	Units
T_{WHBX}	$\overline{WR}$ High to INST, $\overline{BHE}$, AD0–15 Inactive	$T_{OSC} - 50$	$T_{OSC} + 100$	ns
T_{HLHH}	$\overline{W_{RL}}$, $\overline{W_{RH}}$ Low to $\overline{W_{RL}}$, $\overline{W_{RH}}$ High	$2T_{OSC} - 35$	$2T_{OSC} + 40$	ns
T_{LLHL}	ALE/$\overline{ADV}$ Low to $\overline{W_{RL}}$, $\overline{W_{RH}}$ Low	$2T_{OSC} - 30$	$2T_{OSC} + 55$	ns
T_{QVHL}	Output Data Valid to $\overline{W_{RL}}$, $\overline{W_{RH}}$ Low	$T_{OSC} - 60$		ns

NOTES:
1. If more than one wait state is desired, add 3 T_{OSC} for each additional wait state.
2. CLKOUT is directly generated as a divide by 3 of the oscillator. The period will be 3 T_{OSC} ± 10 ns if T_{OSC} is constant and the rise and fall times on XTAL1 are less than 10 ns.
3. Max spec applies only to ALE. Min spec applied to both ALE and $\overline{ADV}$.
4. The term "Address Valid" applies to AD0–15, $\overline{BHE}$, and INST.
5. The term "Address" in this definition applies to AD0–7 for 8-bit cycles, and AD0–15 for 16-bit cycles.
6. Typical values.

WAVEFORM



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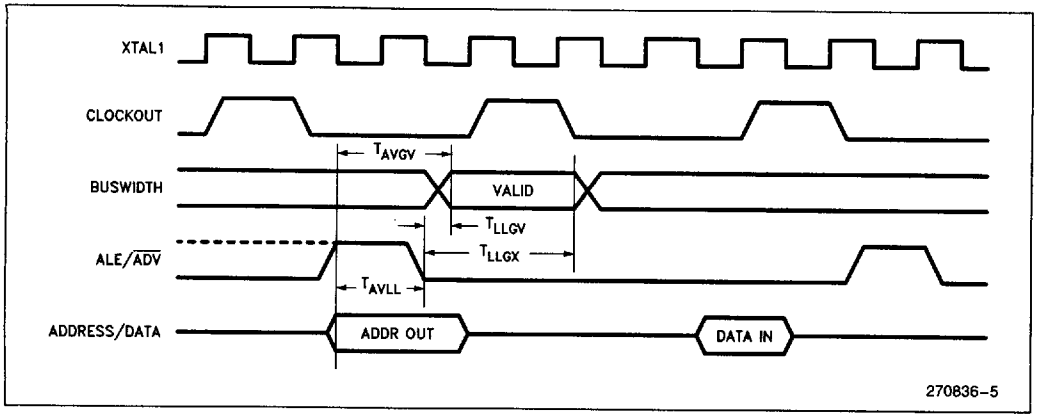
NOTES:
1. 8-bit only
2. 8-bit bus or when write strobe mode selected.
3. When $\overline{ADV}$ selected.

WAVEFORM—BUSWIDTH PIN



AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

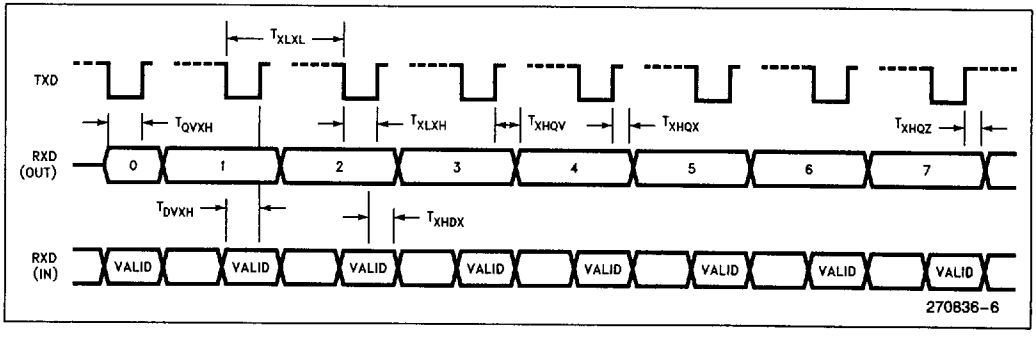
Test Conditions: $T_C = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(1)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(1)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTE:
1. Parameter not tested.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

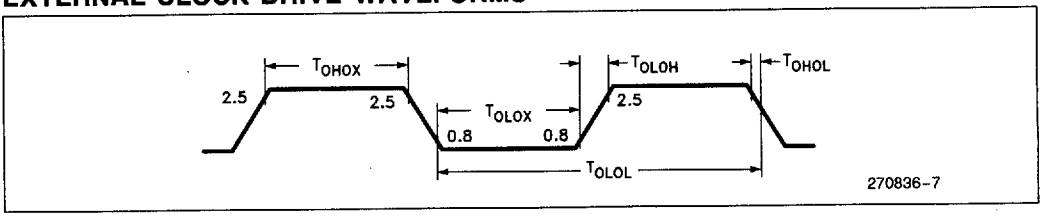
SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



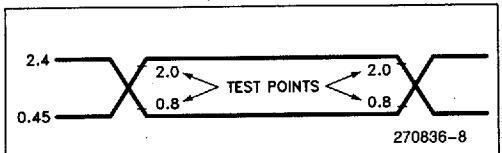
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{OLOL}$	Oscillator Frequency	6.0	12.0	MHz
T_{OHOX}	High Time	30		ns
T_{OLOX}	Low Time	30		ns
T_{OLOH}	Rise Time		15	ns
T_{OHOL}	Fall Time		15	ns

EXTERNAL CLOCK DRIVE WAVEFORMS

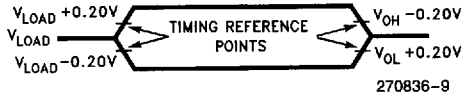


AC TESTING INPUT, OUTPUT WAVEFORMS



AC Testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS



For timing purposes a port pin is no longer floating when a 200 mV change from Load Voltage occurs, and begins to float when a 200 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq \pm 8$ mA.

A/D CONVERTER SPECIFICATIONS

The absolute conversion accuracy is dependent on the accuracy of V_{REF}. The specifications given below assume adherence to the Operating Conditions section of this datasheet. Testing is done at V_{REF} = 5.12V.

OPERATING CONDITIONS

V_{CC}, V_{PD}, V_{REF} ..... 5.0V ± 0.25V
V_{SS}, ANGND 0.0V
T_C ..... −40°C to +125°C
F_{OSC} ..... 6.0 MHz to 12.0 MHz
Test Conditions:
V_{REF} 5.120V
V_{CC} 5.0V

Parameter	Typical*(1)	Min	Max	Units**
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±4	LSBs
Full Scale Error	−0.5 ± 0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity			±4	LSBs
Differential Non-Linearity		0	±2	LSBs
Channel-to-Channel Matching		0	±1	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1, 2, 4)
Feedthrough	−60			dB(1, 2)
V_{CC} Power Supply Rejection	−60			dB(1, 2)
Input Resistance		1K	5K	Ω(1)
DC Input Leakage		0	3	µA
Sample Delay		3 T_{OSC} − 50	3 T_{OSC} + 50	ns(1, 3)
Sample Time		12 T_{OSC} − 50	12 T_{OSC} + 50	ns
Sample Capacitance			2	pF

NOTES:
*These values are expected for most parts at 25°C.
**An "LSB", as used here, has a value of approximately 5 mV.
1. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
2. DC to 100 KHz.
3. For starting the A/D with an HSO Command.
4. Multiplexer Break-Before-Make Guaranteed.

6

EPROM SPECIFICATIONS

Operating Conditions: Load Capacitance = 150 pF; T_C = 25°C ±5°C, V_{CC}, V_{PD}, V_{REF} = 5.0V ±0.5V, V_{SS}, ANGND = 0V.
V_{PP} = 12.75V ±0.25V; $\overline{EA}$ = 11V ±2.0V; F_{OSC} = 6.0 MHz

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{AVLL}	ADDRESS/COMMAND Valid to PALE Low	0		T_{OSC}
T_{LLAX}	ADDRESS/COMMAND Hold after PALE Low	80		T_{OSC}
T_{DVPL}	Output Data Setup before $\overline{PROG}$ Low	0		T_{OSC}
T_{PLDX}	Data Hold after $\overline{PROG}$ Falling	80		T_{OSC}
T_{LLLH}	PALE Pulse Width	180		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	250 T_{OSC}	100 μs + 144 T_{OSC}	
T_{LHPL}	PALE High to $\overline{PROG}$ Low	250		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next PALE Low	600		T_{OSC}
T_{PHDX}	Data Hold after $\overline{PROG}$ High	30		T_{OSC}
T_{PHVV}	$\overline{PROG}$ High to PVER/$\overline{PDO}$ High	500		T_{OSC}
T_{LLVH}	PALE Low to PVER/$\overline{PDO}$ High	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to VER/DUMP Data Valid	100		T_{OSC}
T_{SHLL}	RESET High to First PALE Low (not shown)	2000		T_{OSC}

NOTE:
Run-time programming is done with F_{OSC} = 6.0 MHz to 12.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.75V ±0.25V. For run-time programming over a full operating range, contact factory.

DC EPROM PROGRAMMING CHARACTERISTICS

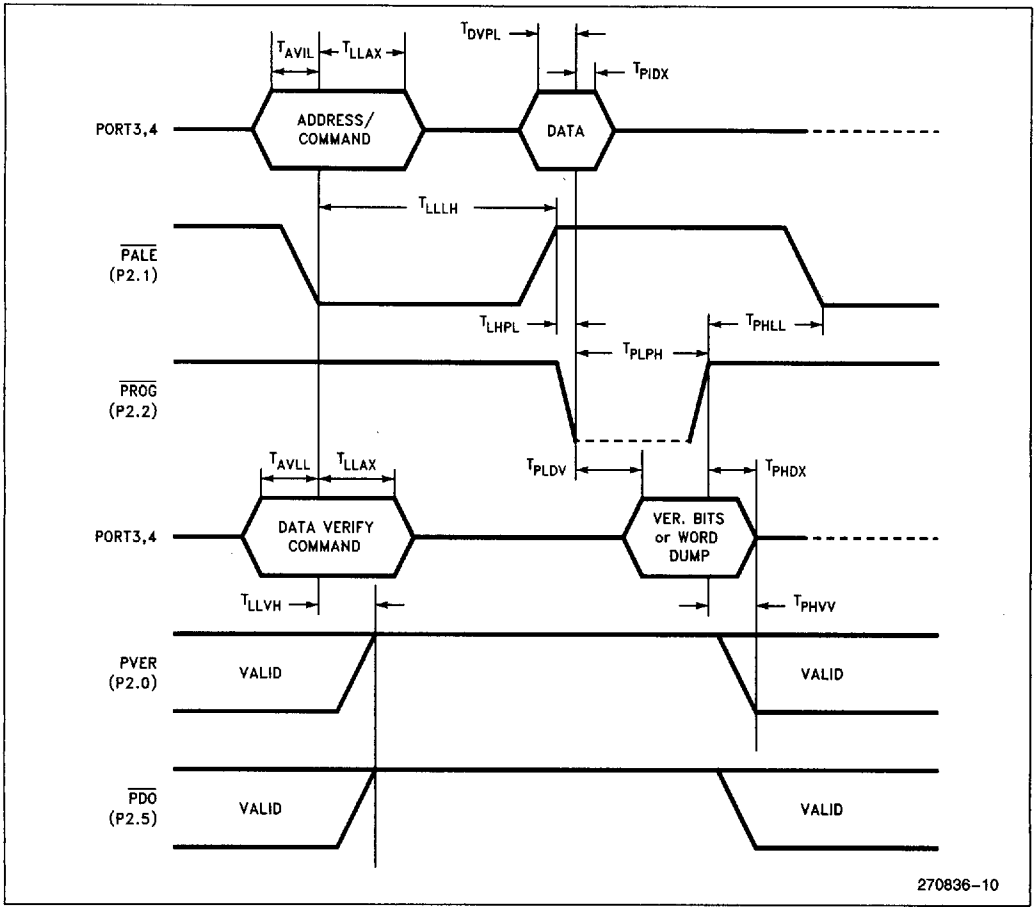
Symbol	Parameter	Min	Max	Units
I_{pp}	V_{pp} Programming Supply Current		100	mA

NOTE:
V_{pp} must be within 1V of V_{CC} while V_{CC} < 4.5V V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} > 4.5V.
See *1992 Embedded Microcontrollers and Processors Handbook,* Volume I, Chapter 15 (Order Number 270645-004) for programming information.

Slave Programming Mode Commands

P4.7	P4.6	Action
0	0	Word Dump
0	1	Data Verify
1	0	Data Program 2000H–3FFFH
1	1	Data Program 4000H–4FFFH

WAVEFORM—EPROM SLAVE PROGRAMMING MODE



6

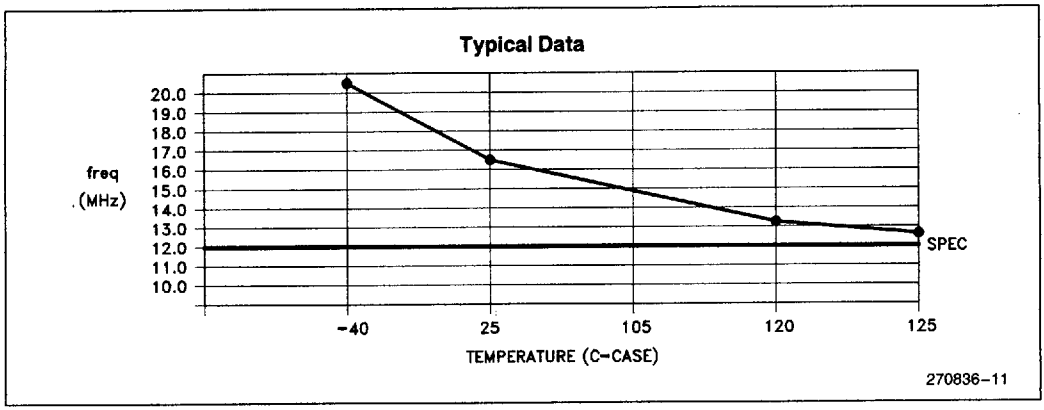


Figure 6. Frequency vs Temperature @all V_{CC}s

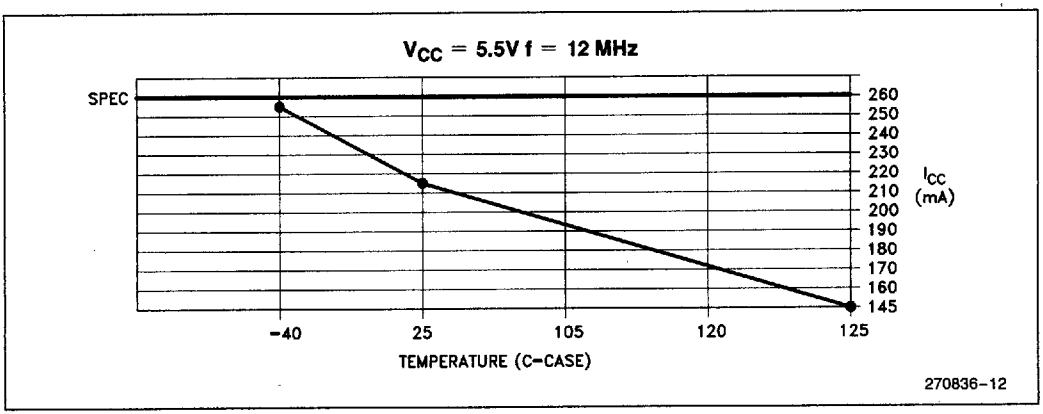


Figure 7. Max Temperature vs I_{CC}

FUNCTIONAL DEVIATIONS

The following is a list of all known functional deviations for 8X9XJC devices.

1. **Indexed, 3 Operand Multiply (Note A, B)**

   In a three word multiply (MUL, MULB, MULU, MULUB) using indexed addressing mode, the displacement portion may not be in the range of 200H through 17FFH, inclusive. If the displacements in this range are necessary, the use of a two operand indexed multiply can be used with a move.

2. **Reads of EPROM/ROM from upper 4K of internal EPROM/ROM with security bits set (Note A)**

   When reads are performed from the upper 4K (4000–4FFFH) of program memory to anywhere in EPROM/ROM space (2000–3FFFH) with the CCB security bits cleared, the memory reads are not valid. The address read will echo back rather than the data. There is no problem with memory reads when the security bits in the CCB (bits 6/7) are set to "11".

3. **BUSWIDTH and 8-bit Bus (Note A) (ROM/ROMless only)**

   If the BUSWIDTH pin is pulled high externally, or left to float, the internal pullup will pull this pin high. A high condition on this input equates to a 16-bit bus mode externally. During the CHIP CONFIGURATION BYTE fetch cycle, the port circuitry changes the CCB address about 25 ns after $\overline{RD}$ goes low. If the CCB being read is trying to configure an 8-bit bus, the upper address lines (AD8–AD15) will NOT be latched, during the CCB read. Therefore, if the read from the CCR (2018H) is in a by x8 address space, the BUSWIDTH pin MUST be held low for this read, or the address lines AD8–AD15 must be latched (via a latched external EPROM or TTL latch).

4. **FIFO/HSI Status Cleared (Note A)**

   It is possible to have a time value in the FIFO with no status bits set in the HSI_STATUS register. When events are logged, the first event is loaded into the Holding Register, the next is loaded into slot #1 of the FIFO, the next in slot #2, etc. If the Holding Register is read after the #2 slot is loaded, the #1 slot will be moved into the Holding register to be read next. If another event is logged, it will be placed in slot #3, not #1 (the one just vacated). There are 7 slots in the FIFO. If the FIFO is allowed to "roll over", that is a 9th event stored in the #1 slot again, before a cleared FIFO happens, the 9th event will have a valid time with a cleared status bits in the HSI_STATUS register (Bits 0, 2, 4 and 6 = 0). If the HSI_STATUS register status bits are cleared, there is no way of matching this time with an HSI input pin. It is important to note that in order to avoid this problem both interrupt routines and polling procedures which allow seven entries in the FIFO MUST clear all event from the FIFO before the next event is logged. If this is not possible, events will have cleared status bits and these routines should also handle that case.

   To ensure proper operation of the High Speed Input FIFO, it is imperative that no more than seven FIFO entries be placed into an empty FIFO. This includes conditions that enter and clear multiple events but leave one or more entries in the FIFO (i.e., add three entries, read one out, add four more, read one out, is seven entries). All seven must be emptied before allowing further events to occur at the pins. The FIFO is empty even if there is an entry in the Holding Register. (An "event" is defined as a pin transition. An "entry" is defined as one or more pin events loaded into a single FIFO array location.)

   Allowing more than seven FIFO entries to occur between cleared conditions will result in incorrect status information for either the eighth or ninth entry. This effectively limits the total number of entries to seven.

   There is one exception that will allow the FIFO to correctly record eight entries. If the first two entries of a cleared FIFO and Holding Register are separated by greater than 16 state times, the ninth entry (rather than the eighth entry) will be recorded with incorrect status information. This is true even if the events followed the first two entries were only separated by eight states.

5. **RESET (Note A)**

   If the XTAL inputs are driven BEFORE V_{CC} is stable (between 4.5 V_{DC}–5.5 V_{DC}), the state machine locks the device into a condition which floats the node in control of the pulldown gate on the RESET pin. The pulldown node will remain on until the floating node loses the stored charge and releases the pulldown. All subsequent RESET's after the Power-on-Reset will operate correctly. Make sure that V_{CC} is stable before XTAL is driven.

   Since RESET is asynchronous, it is possible to apply RESET during writes to quasi-bidirectional port pins. If this occurs, the QBD port pins may not RESET immediately to a logical one. Instead

of the low impedance pullup being turned on, only the high impedance device is on, causing the signals on the QBD pins to rise more slowly than usual.

6. **TIMER2 (T2CLK/HSI.1 and IOC0) (Note A)**

   On a RESET, the source for TIMER2 clocking is undefined. The user MUST write to IOC0 bit 7 to initialize which source (HSI.1 or T2CLK). By the act of for writing IOC0 register, the timer2 counter could increment by one count if the state of the HSI.1 and T2CLK pins are of the opposite state and RESET initialized IOC0 bit 7 to the opposite state that the programmer is initializing it to.

   Because of the above functionality, and the fact that IOC0 also clears timer2, it is recommended that following the initial write to the IOC0 register a reset of timer2 be performed. Reset of timer2 should NOT be another write to the IOC0 register, this could increment timer2 to 0001H. It is recommended that the reset of timer2 be performed through the HSO unit using a 0EH command.

   In common programming practices, Intel recommends writing to IOC0 register once during the initialization. After this command, a reset of timer2 should be performed through the HSO unit. If this is not possible because of other bits in IOC0, the programmer is advised to initialize timer2 after the IOC0 writes, or be aware of the possible increment of timer2 due to the write to IOC0.

7. **HSI Resolution (Note B)**

   The HSI resolution has changed from 8 state times on the JC A-step to 9 state times on the JC B-step. This decreases the maximum HSI input speed from once every 8 state times to once every 9 state times.

8. **Serial Port Flags (Note B)**

   Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set.

9. **Checksum on Reserved Locations (Note B)**

   This is a design consideration, not an errata. A test register was added to location 201Ch on the 8X9XJC B-step that controls the readability and writability of certain SFR's during testing. The addition of these bits affects the readability and writability of this reserved location when it is read. If this location is included in a checksum (which it should not), a checksum difference could occur between the B-step and previous steppings. The User Guide states that reserved locations should not be read or written, this statement includes checksum reads also.

***NOTE:**

A = present on A step devices
B = present on B step devices

The B-step and later devices can be identified by a special mark following the eight digit FPO number on the top of the package. For B-step devices, this mark is a "B".

DIFFERENCES BETWEEN THE 8X9XJC AND THE 8X9XBH

EPROM/ROM Size— The 8X9XJC devices have 4 Kbytes more of internal program memory. The address space of internal memory went from 8 Kbytes to 12 Kbytes. Starting at address 2000H and running continously to 4FFFH. No external bus signals (ALE, $\overline{RD}$, $\overline{WR}$ P3, P4, etc.) are generated when addressing within this 12 Kbyte region.

Internal RAM— On the 8X9XBH device the internal RAM space goes from physical address location 00H to 00FFH. This is considered register RAM and is accessible through ALL addressing modes (Direct, immediate, indexed, and indirect). This address space also includes Special Function Registers. This space has NOT changed on the 8X9XJC. 128 bytes of RAM was added from memory location 0100H to 017FH to the 8X9XJC device. Since this address range requires 16 bits of address, only 16-bit addressing modes can be used to access this memory (Indexed and Indirect). No eight bit addressing modes (Direct and immediate). This additional memory is as if it were external RAM, but placed internal. NO bus signals will be generated external when addressing this space. The accesses will be transparent to the user.

HSI and FIFO— The High Speed Input Unit, including the FIFO has been optimized for automotive applications. The FIFO full bit (IOS1.6) has been changed in meaning. Instead of being set when the FIFO is almost full (6th FIFO entry), the bit is set when the 4th FIFO entry has occurred. Bit 7 of ISO1 has not changed. There is no longer a FIFO full bit since the 4th entry bit replaced it. This also means that when interrupts are used with the FIFO (IOC1.7), there is a holding register loaded interrupt (when IOC1 bit 7 = "0") and a 4th entry interrupt (when IOC1 bit 7 = "1"). Nothing else in the HSI/FIFO has changed.

Function Description	8X9XJC	8X9XBH(c-2)
Hot ICC_1 Max	170 mA*	155 mA
ICC Max	260 mA	240 mA
θ_{JA}	36.6 °C/W	36.1 °C/W
θ_{JC}	13.1 °C/W	13.4 °C/W

*Proposed Specification

DATASHEET REVISION HISTORY

The following are the key differences between this datasheet and the -003 version.

1. The "preliminary" status was dropped and replaced with production status (no label).
2. Trademarks were updated.