intel

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Intel486™ SL Microprocessor SuperSet Data Book

Order Number: 241325-001

Intel486™ SL Microprocessor SuperSet

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Intel486™ SL MICROPROCESSOR SUPERSET HIGHLY-INTEGRATED STATIC Intel486™ SL MICROPROCESSOR COMPLETE ISA PERIPHERAL SUBSYSTEM SYSTEM-WIDE POWER MANAGEMENT

- **Static Intel486™ SL CPU**
  - **Runs MS-DOS*, WINDOWS*, OS/2** and UNIX*****
  - **Object Code Compatible with Intel 8086, 80286, Intel386™ and Intel486™ Microprocessors**
- **Architecture Extension for Power Management**
- **Transparent to Operating Systems and Applications**
- **Programmable Memory Control**
  - **No-Glue DRAM Interface**
  - **256K to 64 Mbytes**
- **Complete ISA System, with Extended Support**
  - **Full ISA Bus Control, Status and Address and Data Interface Logic**
  - **Compatible ISA Bus Peripherals**
  - **System I/O Decoding, Programmable Chip Selects and Support Interfaces**
  - **High-Speed Peripheral Bus (PI-Bus Support)**
  - **IdeaPort Interface for Hardware Expansion**

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The Intel486 SL Microprocessor SuperSet combines an ISA compatible personal computer's microprocessor, memory controller and peripheral subsystems into just two Very Large Scale Integration (VLSI) devices. The product's true Intel486 DX core, high-integration and power conservation features reduce the size and power consumption typically associated with fully Industry Standard Architecture (ISA) bus compatible systems without compromising performance. In addition, new expandability and flexibility features offer the capability for continued innovation in battery-operated, space-constrained systems. The SL SuperSet brings 100% ISA-Bus compatibility to system designs ranging from a new generation of notebook computers to pen-based computers.

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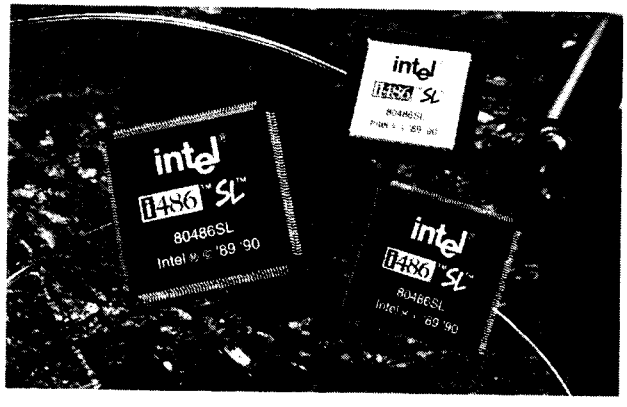
***UNIX is a trademark of UNIX System Laboratories, Inc.

Intel486™ SL MICROPROCESSOR Intel486 MICROPROCESSOR CORE, WITH INTEGRATED MEMORY CONTROLLER AND SYSTEM POWER MANAGEMENT FULLY-STATIC CHMOS™ V TECHNOLOGY

- Static 3.3V Intel486™ CPU Core
  - Optimized and Compatible with Standard Operating System Software such as MS-DOS, WINDOWS, OS/2 and UNIX
  - Object Code Compatible with Intel 8086, 80286, Intel386™ and Intel486 Microprocessors
  - Runs All Desk-Top Applications, 16-or 32-bit
  - D.C. to 33 MHz Operation
  - 64 Mbytes Physical Memory/64 Terabytes Virtual Memory
  - 4 Gigabyte Maximum Segment Size
  - High Integration, Low Power CHMOS™ V Technology
- High Integration Enables On-Chip
  - 4-Way Set Associative 8 Kbyte Cache and Cache Controller
  - Floating Point Unit
  - Paged, Virtual Memory Management
- 32-Bit Architecture
  - Data Buses
  - Registers
  - 8-, 16-, 32-Bit Data Types
- Transparent Power Management System Architecture
  - System Management Mode Architecture
  - Extension for Truly Compatible Systems
  - Programmable Hardware Supports Custom Power-Control Methods
- Direct Drive Bus Interface
  - Full ISA Bus Interface
  - High Speed Peripheral Interface (PI) Bus
- High Performance and Flexible Memory Interface
  - 32-Bit DRAM Data Bus
  - No-Glue DRAM Interface
  - Selectable 3.3V/5V DRAM Interface
  - Up to 5 Banks of DRAM, Size of Each and/or Total up to 64 Mbyte
  - Each Bank Programmable for Size, Organization, Speed, and Output Buffer Strength
  - Burst Mode Supported

Available in PQFP, LGA and SQFP Packages



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82360SL I/O SUBSYSTEM
COMPLETE ISA PERIPHERAL SUBSYSTEM
INTEGRATED SYSTEM POWER MANAGEMENT
FULLY-STATIC CHMOS™ V TECHNOLOGY

- — Complete ISA System, with Extended Support
- — Full ISA Bus Control, Status and Address and Data Interface Logic
- — Compatible ISA Bus Peripherals:
- — Two 8237 Direct Memory Access Controllers
- — Two 8254 Programmable Timer Counters (6 Timer/Counter Channels)
- — Two 8259A Programmable
- — Interrupt Controllers (15 Channels)
- — Enhanced LS612 Page Memory Mapper
- — One 146818 Compatible Real Time Clock w/256-byte CMOS RAM
- — Two 16450 Compatible Serial Port Controllers
- — One 8-Bit Parallel I/O Port with High Speed Protocol
- — (Centronics or Bi-Directional)

■ **Additional System I/O Decoding, Programmable Chip Selects and Support Interfaces:**
- — Full Integrated Drive Electronics (I.D.E.) Hard Disk Interface
- — Floppy Disk Controller
- — Keyboard Controller Chip Selects and Support Logic

■ **External Real Time Clock Support**

■ **PS/2 and EISA Control/Status Ports**

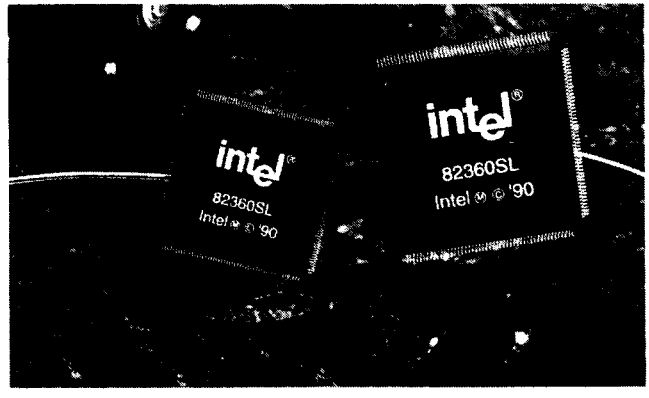
■ **Local Memory and ISA-Bus Memory Refresh Control**

■ **New IdeaPort Interface for Hardware Expansion**

■ **Transparent Power Management System Architecture**
- — Architecture Extension for Truly Compatible Systems
- — Transparent to Operating Systems and Applications Programs
- — Programmable Hardware Supports Custom Power-Control Methods
- — Integrated Power Management Unit Manages Power-Events Safety

■ **Selectable 3.3V/5V Operating Voltage**

Available in SQFP and PQFP Packages



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1.0 INTRODUCTION

This document provides the pinouts, signal descriptions, and D.C./A.C. electrical characteristics of the Intel486 SL microprocessor and 82360SL I/O peripheral device. Consult Intel for the most recent design-in information. For a thorough description of any functional topic, other than the parametric specifications, please refer to the latest Intel486 SL Microprocessor System Design Guide and the Intel486 SL Microprocessor Programmer's Reference Manual.

In recent years, users have shown an increasing tendency to insist on the most powerful processors available, and to quickly upgrade to systems based on those processors. This trend has been accelerated by the advent of 32-bit operating systems, advanced graphical user interfaces (GUIs), and computationally intensive applications (i.e., computer-aided design and multimedia), all of which place great demands on system resources. At the same time, users are demanding the ability to take their work home, on the road, and in the field. The Intel486 SL microprocessor will allow users to obtain the benefits of longer battery-life for portable computing without sacrificing the performance they require. This market for portables is expanding at a rapid pace; it is the fastest growing segment of the PC-compatible market.

1.1 Challenges Faced by the Portable PC Designer

Designing new products for the fast-paced portable computer market presents a unique set of challenges. System performance is key; GUIs, operating systems and both desktop and pen-based application programs are becoming increasingly complex while users have come to expect workstation-like performance in the palm of their hand. Form factors are shrinking so rapidly that highly integrated system logic is a must. Compatibility with existing machines, operating systems and applications software must also be maintained.

In addition, portable computers are battery-powered so power consumption must be strictly limited whenever possible. This requires the presence of power management circuitry and software that is tightly coupled to both the microprocessor and the remainder of system logic. Implementation of power management in a fashion transparent to the operating system and applications programs is essential.

Furthermore, the pressure to shorten time-to-market cycles is always increasing. The highiy competitive nature of this market means that development dollars must be spent wisely. The result is a need for a consistent and flexible architecture across an entire product line. Such an approach ensures that compatibility requirements are met and that investments in BIOS and power management firmware are amortized across multiple products.

1.2 The Intel486™ SL Microprocessor Superset

Building on the Intel386™ SL microprocessor standard for mobile computers, Intel developed the Intel486 SL microprocessor family to support the next generation of notebook and pen-based computers. The SL SuperSet consists of both the highly integrated CPU and I/O companion chip, the 82360SL. The high performance. low voltage, sophisticated power management, and design flexibility makes the Intel486 SL microprocessor SuperSet ideal for ISA-compatible portable system designs. As a member of the Intel486 processor family, it provides 100% binary compatibility with all Intelx86 software.

At the heart of the Intel486 SL CPU is a true 32-bit Intel486 DX microprocessor. The 8 Kbyte on-chip cache, RISC integer core, and full 32-bit data bus give the Intel486 SL CPU twice the performance of the Intel386 SL CPU. The on-chip math coprocessor is an enhanced version of the Intel387™ math coprocessor which further increases performance on scientific applications (floating point based).

With a full-featured on-chip memory controller and a 26-bit address bus, it directly supports up to 64 Mbytes of physical memory. The memory controller permits each memory bank to use a different DRAM size (from 256K to 4 Mbytes) and provides automatic refresh capability during suspend mode. It also automatically routes each access cycle to its appropriate destination, which could be the internal cache, ISA bus or Peripheral Interface (PI) bus.

The performance of the Intel486 SL CPU is further enhanced by a high-speed PI expansion bus, a 16-bit bus that supports high-speed graphics displays (increasingly important for ruuning state-of-the-art operating systems and applications software) and solid-state memory devices such as Flash memory disk drives.

Designed from the ground up with power savings in mind, the Intel486 SL CPU contains a fully static processor core operating at 3.3V which significantly reduces full-on power consumption. Its memory bus, PI bus, and ISA bus all feature "flexible voltage" support for either 3.3V or 5V components. Thus, the DRAM subsystem may run at either 3.3V or 5V. The Intel486 SL CPU may be used in conjunction with current 5V peripherals or—as they become available—future 3.3V peripherals. This flexible voltage feature will allow system designers to maintain compatibility with current hardware while paving the way for future designs that are fully low-voltage in design.

Equally important is the capability of the processor to manage system power consumption. The Intel486 SL CPU incorporates the same System Management Mode (SMM) found in the previous Intel386 SL CPU. A non-maskable System Management Interrupt (SMI), a corresponding Resume instruction and a new memory space for system management code are the basis of SMM. SMM ensures seamless power control of the processor core, system logic, main memory and one or more peripheral devices from within any application or operating system. Since the SMM operation with the Intel486 SL CPU is fully compatible with existing SL designs, manufacturers' investments in BIOS and power management firmware are preserved and design cycles are shortened.

The 82360SL I/O chip is the companion product to the Intel486 SL CPU. Originally developed as part of the Intel386 SL microprocessor SuperSet, the 82360SL integrates dedicated system logic that provides a complete set of PC-compatible support functions. These functions include two serial ports, one parallel port, two timer/counters, two interrupt controllers, NMI logic and two DMA controllers. A real time clock/calendar, 256 bytes of CMOS RAM and the DMA page registers are also provided.

In addition, peripheral support capability is built-in to the 82360SL. This is comprised of decoder circuitry for Flash memory and for external floppy disk and keyboard controllers. An Intelligent Device Electronics (IDE) fixed disk drive interface is also provided. The 82360SL contains extensive circuitry used to control the power consumption of peripheral devices. This is based on a full complement of hardware timers, event monitors and I/O interfaces. These are controlled by BIOS firmware so that customization for a particular system configuration can be readily achieved.

1.3 Setting the Standard for a New Class of Mobile Computers

With the Intel486 SL CPU, Intel has combined the best features from the Intel486 microprocessor and SL architecture and optimized them for mobile computing. This combination of high-performance, high-integration, and power-management features makes the Intel486 SL microprocessor the ideal microprocessor for next-generation notebook and pen-based computers. Developing these new systems will be greatly facilitated by the Intel SL architecture flexibility and compatibility with future generations.

1.4 Overview of System Architecture

The Intel486 SL microprocessor, in combination with the 82360SL I/O, provides the majority of the core logic required to design a high performance ISA-Bus compatible personal computer. The 82360SL I/O is pin-to-pin compatible with its predecessor, the 5V 82360SL I/O. Other system components not integrated in the Intel486 SL CPU or 82360SL I/O include: a graphics controller and display subsystem, a keyboard controller and keyboard/mouse, removable storage (such as floppy disk controller/floppy disk drive or PCMCIA FLASH memory card), fixed storage (such as an I.D.E. hard disk drive), DRAM system memory (such as on-board DRAM or a JEIDA/JEDEC 88 pin DRAM memory card), and BIOS/user/graphics ROM, (such as EPROM or FLASH). The Intel 80C51SL Keyboard Controller, 82365SL PCMCIA I/F Controller, 82077SL Floppy Controller and a third party graphics controller may be used to create a full-function transportable personal computer. A typical Intel486 SL microprocessor based system is depicted in Figure 1-1.

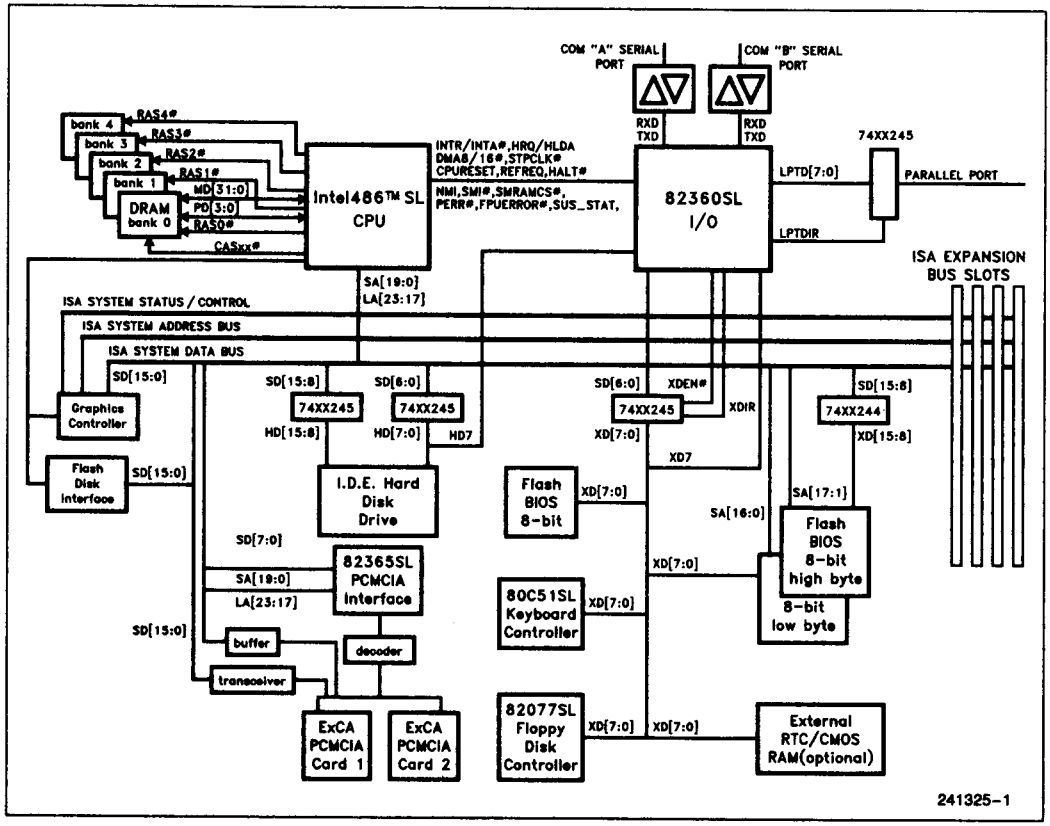

Figure 1-1. Intel486™ SL Microprocessor SuperSet System Block Diagram

1.5 Intel486™ SL Microprocessor: Central Processing Unit (CPU), On-chip Cache, On-chip Floating Point Unit (FPU) and Memory Controller Subsystem

The Intel486 SL CPU is the next generation microprocessor in the Intel SL family. Portable personal computer manufacturers may use the Intel486 SL CPU, in conjunction with the 82360SL I/O, to produce systems of higher performance, higher integration, and lower power consumption. Included in this highly integrated chip are a static Intel486 microprocessor core, an on-chip cache, an on-chip floating point unit, a 32-bit on-chip memory controller and a 16-bit external bus controller. High performance is a direct result of the reduced clocks per instruction associated with the Intel486 CPU. Intel486 SL CPU offers low power consumption by supporting reduced supply voltage operation of the core logic, by instituting a fully static design, and by using the low power Intel CHMOS V process technology. The on-board/local DRAM buffers may be selectively powered to support 3.3V or 5V DRAMs. The powering of ISA bus interface and I/O interface is at 3.3V or 5V. This ensures the usability of the Intel486 SL CPU, the existing ISA bus peripherals, and future 3.3V peripherals. Table 1-1 describes the options available with the Intel486 SL CPU. Figure 1-2 shows the internal modules of the Intel486 SL CPU.

Table 1-1. Intel486™ SL Microprocessor Options

Product	FPU	Frequency (MHz)	ISA/PI Interface Voltage	Package
Intel486 SL CPU	Internal	25, 33(1)	3.3V(1) or 5V	SQFP(1), PQFP, LGA

NOTES:
1. Currently, this document does not describe 33 MHz, SQFP and 3.3V interface to ISA/PI bus. For more updated information on the CPU options, please contact your Intel sales office.

The Intel486 SL CPU is a high performance solution that offers fast time-to-market for personal computer manufacturers. It reduces system development time by retaining the same interfaces to the 82360SL I/O, ISA expansion bus, and high speed peripheral interface bus (PI-bus). A system designer may create a personal computer which has all of the same components as the Intel386™ SL CPU system with the exception of the Intel486 SL CPU and the on-board DRAM subsystem. The new printed circuit board assembly could be smaller since the Intel486 SL CPU eliminates the need for external cache data SRAM and external math co-processor. Although the Intel486 SL CPU is not a drop in replacement for the Intel386 SL CPU, 75% of the signals share the same functionality. The Intel486 SL CPU maintains software compatibility with the Intel386 SL CPU System Management Mode (SMM). BIOS and System Setup software may be easily modified to support the new DRAM memory configurations without impacting applications software drivers.

The Intel486 CPU, with on-chip cache, yields an average of 1.8–2.4 clocks per instruction as compared to 12 clocks for the 8086/8088 and 4.5 clocks for the 80286 or 80386 CPUs. In a true zero wait state, uniprocessor environment, the Intel486 SL CPU system performance could be as much as 2.5 times that of an Intel386 CPU. Intel486 SL CPU with FPU provides both integer and floating point performance improvements when compared with the Intel386 and Intel387™ Math Co-processor combination. Figure 1-3 shows the functional modules of the Intel486 SL CPU.

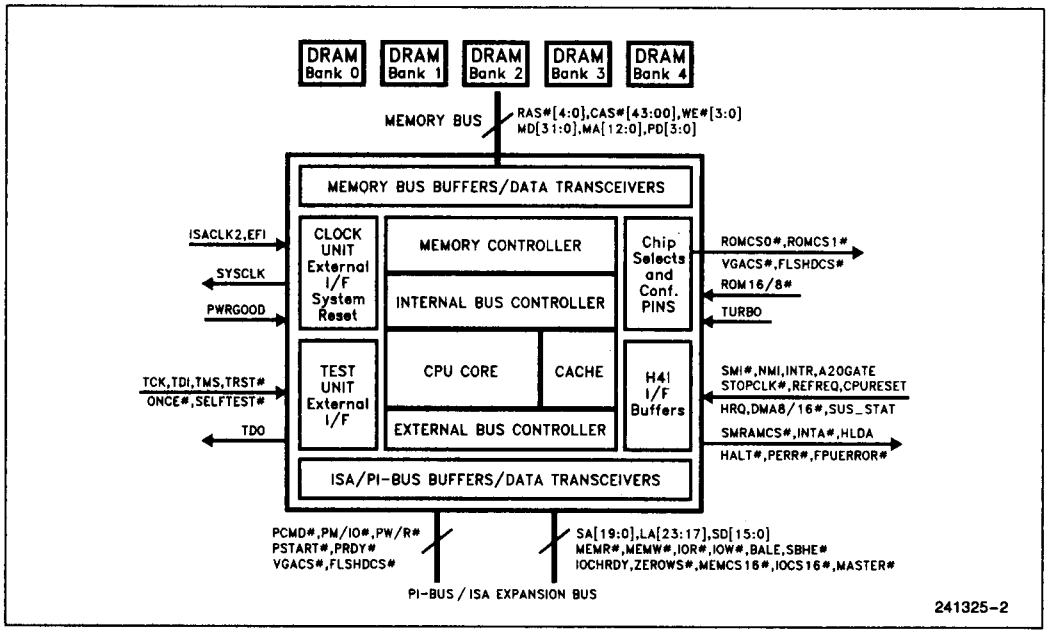

Figure 1-2. Internal Modules of Intel486™ SL Microprocessor

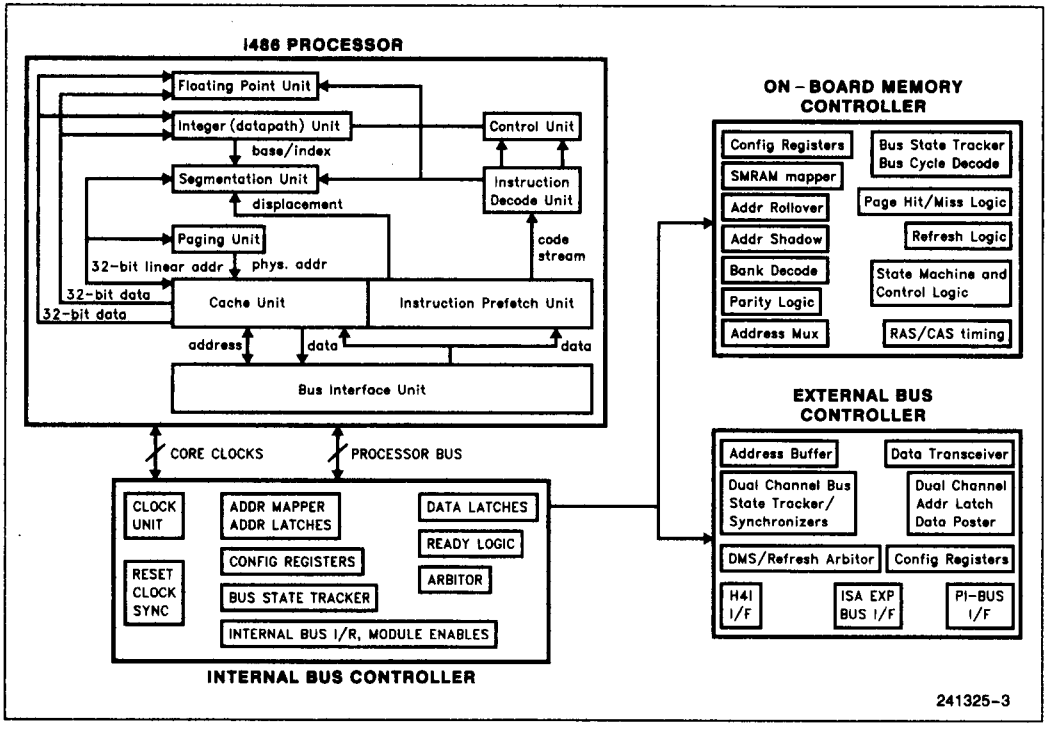

Figure 1-3. Intel486™ SL Microprocessor Internal Functional Block Diagram

1.6 82360SL I/O: Integrated ISA Peripheral and Power Management Device

The new low-voltage 82360SL Peripheral I/O is pin-for-pin compatible with the existing 5V 82360SL I/O. It can operate both at 5V and 3.3V. It is available both in 208-lead SQFP and 196-lead PQFP. The 82360SL I/O contains dedicated logic to perform a number of CPU, memory, and peripheral support functions. It also contains an extensive set of programmable power management facilities that minimize system power requirements for battery-powered portable computers.

The 82360SL I/O includes a complete set of on-chip peripheral device functions including two 16450 compatible serial ports, one 8-bit Centronics interface or bi-directional parallel port, two 8254 compatible timer counters, two 8259 compatible interrupt controllers, two 8237 compatible DMA controllers, one 74LS612 compatible DMA page register, one 14618 compatible real-time clock/calendar with an additional 128 bytes of battery backed CMOS RAM and an integrated drive electronics (IDE) hard disk interface. The Intel 82360SL I/O also contains highly programmable chip selects and complete peripheral interface logic for direct keyboard and floppy disk controller support. The peripheral registers and functions behave exactly the same as the discrete components commonly found in industry standard personal computers. The peripheral logic is enhanced for static operation by supporting write only registers as read/write.

The processor and the memory support functions contained in the 82360SL I/O eliminate most of the external random-logic "glue" that might otherwise be required. The 82360SL I/O provides internal programmable- frequency clock generators for the ISA backplane and video subsystems. A programmable, low power DRAM refresh timer is also provided to maintain system memory integrity during the power saving Suspend state.

The 82360SL I/O contains a flexible set of hardware functions to support the growing sophistication in power management schemes required by portable systems. Numerous hardware timers, event monitors, and I/O interfaces can programmably monitor and control system activity. Firmware developed by the system designer allocates and directs the hardware to fulfill the unique power management needs of a given system configuration.

All of the standard peripheral registers, clock-generation logic, and power-management facilities have been designed to ensure complete compatibility with the existing operating systems and applications software.

Figures 1-4 and 1-5 show the functional blocks and micro-architecture of the 82360SL I/O.

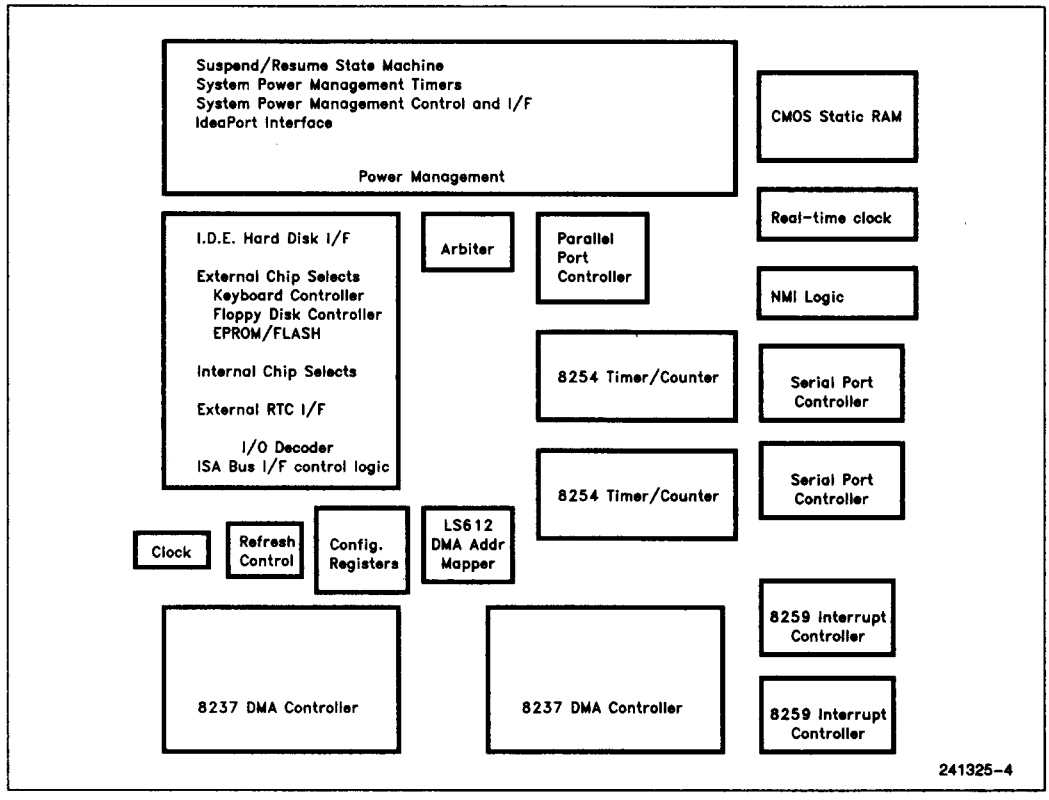

Figure 1-4. Intel 82360SL ISA Peripheral I/O Internal Functional Modules

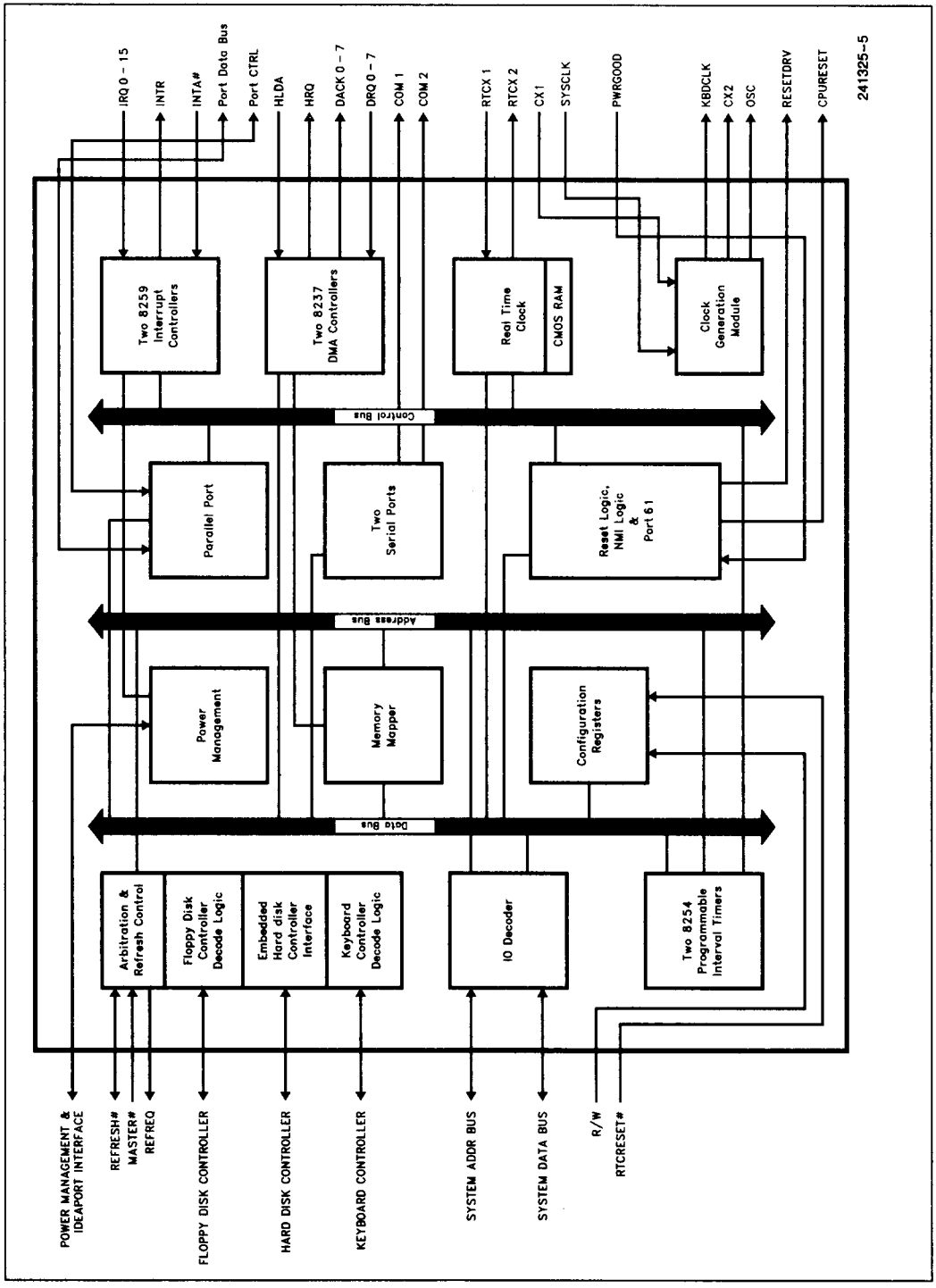

Figure 1-5. 82360SL Functional Block Diagram

2.0 Intel486™ SL MICROPROCESSOR SPECIFICATIONS

2.1 Intel486 SL Microprocessor Pin Assignment and Signal Characteristics

Section 2 provides information for the Intel486 SL CPU pin assignments and signal mnemonics. In addition to the package pin out diagrams, a table is provided for easy location of signals. The table lists the Intel486 SL CPU package device pinouts in the 196-lead JEDEC Plastic Quad Flat Package (PQFP) and the 227 lead LGA package. The table includes additional information on the signals and the associated pin. A brief explanation of each column is given in Table 2-1.

Table 2-1. Description of the Columns of Table 2-2

Mnemonic	Signal Name Associated with the Package Pinouts and Signal Descriptions
PQFP	196-lead JEDEC Plastic Quad Flatpack (MM-PQFP), approximately 0.635mm lead spacing (25 mil). The PQFP is a surface mount OEM package used for all production speed grades of the Intel486 SL CPU. There are 171 active signals. There are 13 V_{CC} pins and 12 V_{SS} pins available in the 196 PQFP. Currently 4 V_{CC}'s are always connected to 3.3V and power the plane for all internal logic and input buffers, 5 V_{CC}'s are associated with the memory bus which may be connected to either 3.3V or 5V and 4 V_{CC}'s are associated with the ISA bus which are connected to 5.0V. All grounds (V_{SS}) are common to a single ground plane. This column lists the pin number that is associated with the corresponding signal.
LGA	This column lists the pin names of the Intel486 SL CPU in a 227-lead LGA package.
Type	Input—Input pins are unidirectional signals which are driven by external devices or logic into the Intel486 SL CPU buffers. Inputs are selectively biased to either 3.3V or 5.0V when connected to the associated V_{CC}'s for each buffer group. Output—Output pins are unidirectioral signals which are driven out by the Intel486 SL CPU buffers. Outputs are selectively biased to either 3.3V or 5.0V when connected to the associated V_{CC}'s for each buffer group. I/O—Input/Output pins are bi-directional signals to/from the Intel486 SL CPU buffers. I/O pins when enabled as outputs are selectively biased to either 3.3V or 5.0V when connected to the associated V_{CC}'s for each buffer group.
Term	Indicates the internal pull-up or pull-down resistor value associated with this signal. Signals which are either pulled-up or pulled-down may be determined by referencing the Stop Clock description. In general open drain signals which are a "wire-OR" on the ISA bus use a "hard pull-up/pull-down" (typically 600Ω–1000Ω). The open drain Intel486 SL CPU ISA bus signals include: IOCHRDY, IOCS16#, MASTER#, MEMCS16# and 0WS#. Asynchronous inputs such as NMI, INTR, HRQ have "soft" pulldowns in the range of 20K. The ISA bus Command, Data and Miscellaneous Chip Selects have "soft" pull-ups or pull-downs in the range of 60 KΩ.
3.3V or 5V	This column specifies whether the named pin is powered by 3.3V or 5V and also the V_{CC} pin number associated with the supply voltage.
ONCE	On-Chip Emulation Mode (ONCE). This indicates the signal state of this pin when Intel486 SL CPU ONCE# pin is LOW. Signals when the Intel486 SL CPU is in on-chip emulation mode may be in one of five states: Tri—Tri-state logic level Drv—Active and driven, (the signal continues to operate and may change logic states) En—The input buffer is enabled, allowing signals to be recognized. Dis—The input buffer is disabled, prohibiting signals from being recognized. Hold—Held in the last logic state prior to entering ONCE mode.

Table 2-1. Description of the Columns of Table 2-2 (Continued)

Mnemonic	Signal Name Associated with the Package Pinouts and Signal Descriptions
Drive	I/O and output buffers for the memory bus and ISA bus have programmable output strengths. In general a three legged binary configuration is supported by the output buffers which have 1x, 2x and 4x "legs" corresponding to lumped capacitive load of 34 pF, 68 pF and 136 pF. The 7 strengths or loads which are supported by the programmable output buffers include: 34 pF, 68 pF, 102 pF, 136 pF, 170 pF, 204 pF and 238 pF. The V_{OH} and V_{OL} of 3.3V output and I/O buffers matches the V_{OH} and V_{OL} of 5.0V buffers. The associated I_{OL} (current into an output which will establish a logic low) and I_{OH} (current into an output which will establish a logic high) are specific to the buffer type and programming of the output buffer. The memory bus buffers are controlled by the Memory Controller Unit 32-bit MCBUFF configuration register. The memory bus buffers are divided into the following five groups: Column Address Strobe for each bank Memory Address for all DRAM banks and Write Enable per Byte Common Write Enable (for all bytes in a DRAM banks) Row Address Strobe for each bank Memory Data and Parity for all DRAM banks The ISA bus buffers are controlled by the External Bus Controller 16-bit EBCBUFF configuration register. The ISA bus buffers are divided into the following six groups: Lower System Data Byte (SD7:0) Upper System Data Byte (SD15:8) Lower System Addresses (SA16:0) Upper System Addresses (SA19:17 and LA23:17) Memory Command Signals (MEMR#, MEMW#) I/O Command Signals (IOR# IOW#)
PWR RST	Power On-Reset (PWRGOOD De-Asserted with EFI active). This indicates the signal state of this pin when the Intel486 SL CPU is in Global Reset. In general, inputs have the designation TRI for tri-state. Internal logic connected to the input buffers is electrically isolated when the Intel486 SL CPU is in suspend and the input termination (pull-up or pull-down) is disabled. Outputs and I/O buffers may be in one of five states: Tri—Tri-state logic level Drv—Active and driven, (the signal continues to operate and may change logic states) En—The input buffer is enabled, allowing signals to be recognized. Dis—The input buffer is disabled, prohibiting signals from being recognized.
SUSP	Suspend Mode (SUSP). This indicates the signal state of this pin when Intel486 SL CPU is in Suspend Mode. In general, inputs have the designation TRI for tri-state. Internal logic connected to the input buffers is electrically isolated when the Intel486 SL CPU is in suspend and the input termination (pull-up or pull-down) is disabled. The only inputs which are actively sampled (ACTV) in suspend are: EFI, ISACLK2, CPURESET, SUS_STAT, ONCE#, PWRGOOD and REFREQ. Outputs and I/O buffers may be in one of five states: Tri—Tri-state logic level Drv—Active and driven, (the signal continues to operate and may change logic states) En—The input buffer is enabled, allowing signals to be recognized. Dis—The input buffer is disabled, prohibiting signals from being recognized. Hold—Held in the last logic state prior to entering Suspend Mode PU—Pulled up PD—Pulled down

Table 2-1. Description of the Columns of Table 2-2 (Continued)

Mnemonic	Signal Name Associated with the Package Pinouts and Signal Descriptions
Load	This column lists the maximum and minimum capacitive loads which the buffer can directly drive in pF for each signal. This is specified for output and input-output pins only.
STOPCLK	Stop Clock Mode (STOPCLK). This indicates the signal state of this pin when the Intel486 SL CPU is in Stop Clock Mode. During Stop Clock the internal Intel486 SL CPU and FPU clock is stopped. Alternate Master or DMA may continue to operate and the Intel486 SL CPU cache will continue to snoop. The on-board memory controller may also be active to service DRAM accesses by an ISA bus master or DMA device as well as providing refresh. In general, input and output signals on the ISA bus are pulled high or low to their "inactive logic state" and have the designation PU or PD during Stop Clock. Signals in Stop Clock mode may be in one of four states: PU—Pulled up PD—Pulled down Drv—Active and driven, (the signal continues to operate and may change logic states) En—The input buffer is enabled, allowing signals to be recognized. Dis—The input buffer is disabled, prohibiting signals from being recognized.

THE Intel486™ SL CPU PINOUT DIAGRAM

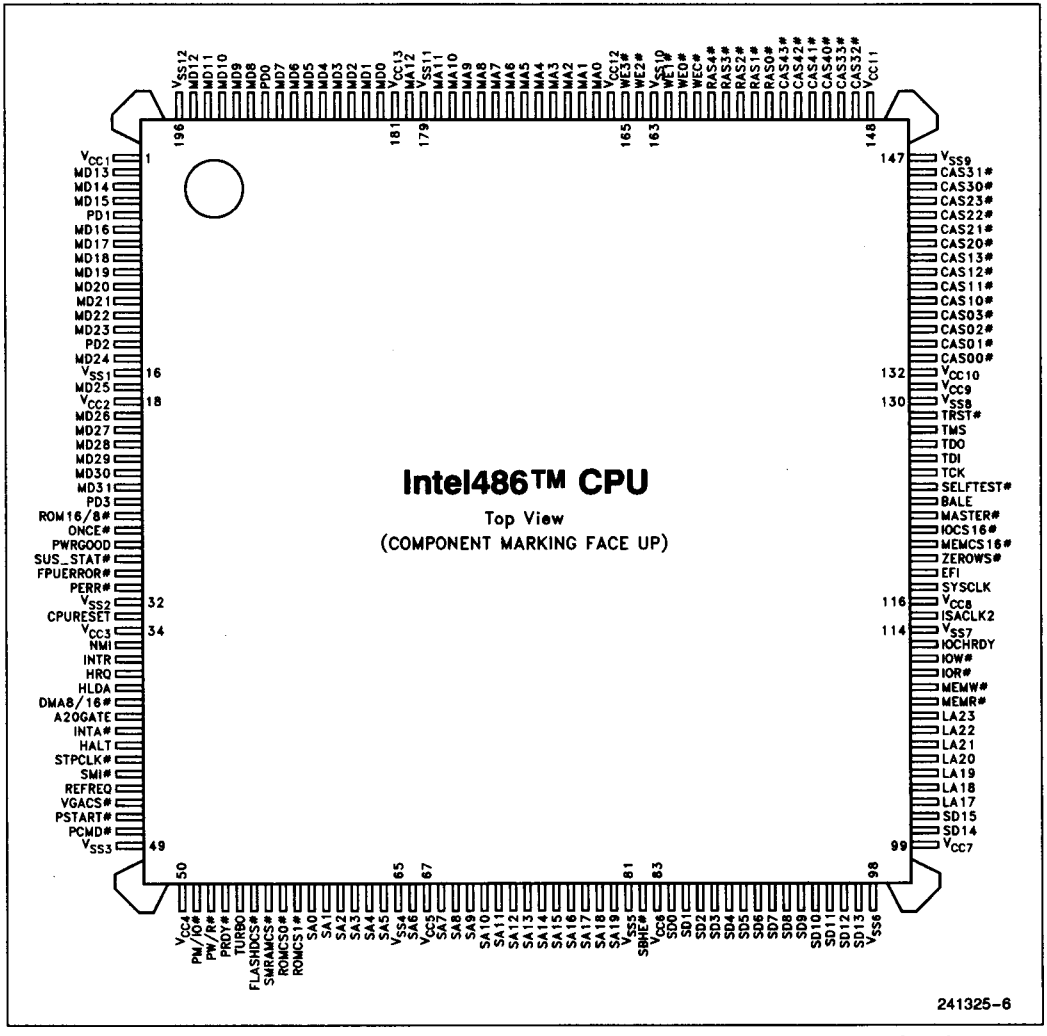

Figure 2-1. Top View of the Pinout of the Intel486™ SL Microprocessor in a 196-Lead PQFP Package

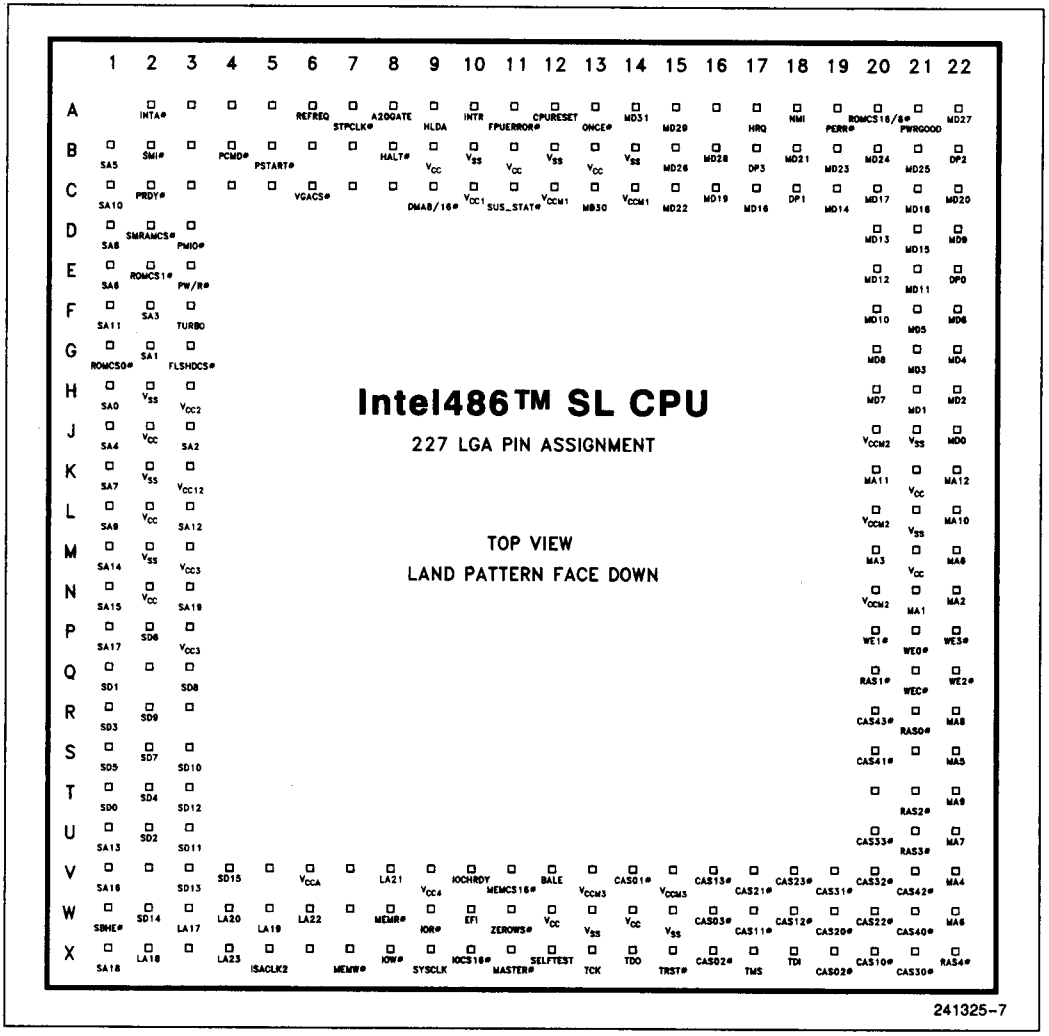

Figure 2-2. Top View of the Pinout of the Intel486™ SL Microprocessor in a 227-Lead LGA Package

Table 2-2. Intel486™ SL Microprocessor Pin Characteristics

Mnemonic	PQFP	LGA	Type	Term	Drive(1) I_{OL}/I_{OH} (Default)	Load Min, Max	PWR RST	Susp(2) (Default)	STOPCLK	ONCE	3.3V or 5V	
A20GATE	Pin 40	A08	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
BALE	Pin 123	V12	O	Hold	7/4	10, 160	Tri	Tri	Drv	Hold	5V	V_{CC8}
CAS00#	Pin 133	X16	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS01#	Pin 134	V14	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS02#	Pin 135	X19	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS03#	Pin 136	W16	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS10#	Pin 137	X20	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS11#	Pin 138	W17	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS12#	Pin 139	W18	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS13#	Pin 140	V16	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS20#	Pin 141	W19	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS21#	Pin 142	V17	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS22#	Pin 143	W20	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS23#	Pin 144	V18	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS30#	Pin 145	X21	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS31#	Pin 146	V19	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS32#	Pin 149	V20	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS33#	Pin 150	U20	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS40#	Pin 151	W21	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS41#	Pin 152	S20	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS42#	Pin 153	V21	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CAS43#	Pin 154	R20	O	Hold	17/10	15, 72	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC10}
CPURESET	Pin 33	A12	I	20K			En	En	PD	Dis	5V	V_{CC3}
DMA8/16#	Pin 39	C09	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
EFI	Pin 118	W10	I				En	Dis	En	Tri	5V	V_{CC8}
FLSHDCS#	Pin 55	G03	O	Hold	7/4	10, 50	Tri	Tri	Drv	Tri	5V	V_{CC3}
FPUERROR#	Pin 30	A11	O		7/4		Tri	Tri	Drv	Tri	5V	V_{CC3}
HALT#	Pin 42	B08	O	Hold	13/8	10, 50	Tri	Tri	Drv	Tri	5V	V_{CC3}
HLDA	Pin 38	A09	O	Hold	7/4	10, 50	Tri	Tri	Drv	Tri	5V	V_{CC3}
HRQ	Pin 37	All	I	20K			Dis	Dis	PD	Dis	5V	V_{CC3}
INTA#	Pin 41	A02	O	Hold	12/6	10, 50	Tri	Tri	Drv	Tri	5V	V_{CC3}
INTR	Pin 36	A10	I	20K			Dis	Dis	PD	Dis	5V	V_{CC3}
IOCHRDY	Pin 113	V10	I/O	1K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC8}
IOCS16#	Pin 121	X10	I/O	1K		10, 160	Dis	Dis	PU	Tri	5V	V_{CC8}
IOR#	Pin 111	W09	I/O	60K	7/4	10, 160	Tri	PU	PU	Tri	5V	V_{CC8}
IOW#	Pin 112	X08	I/O	60K	7/4	10, 160	Tri	PU	PU	Tri	5V	V_{CC8}
ISACLK2	Pin 115	X05	I				En	Dis	En	Tri	5V	V_{CC8}
LA17	Pin 102	W03	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}
LA18	Pin 103	X02	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}
LA19	Pin 104	W05	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}
LA20	Pin 105	W04	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}
LA21	Pin 106	V08	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}
LA22	Pin 107	W06	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}
LA23	Pin 108	X04	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC6}

NOTES:
1. Drive currents are for default buffer strengths only. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.
2. The states of ISA-bus and PI-bus pins listed in this column are programmable. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.

Table 2-2. Intel486™ SL Microprocessor Pin Characteristics (Continued)

Mnemonic	PQFP	LGA	Type	Term	Drive(1) I_{OL}/I_{OH} (Default)	Load Min, Max	PWR RST	Susp(2) (Default)	STOPCLK	ONCE	3.3V or 5V	
MA0	Pin 167	W22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA1	Pin 168	N21	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA2	Pin 169	N22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA3	Pin 170	M20	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA4	Pin 171	V22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA5	Pin 172	S22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA6	Pin 173	M22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA7	Pin 174	U22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA8	Pin 175	R22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA9	Pin 176	T22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA10	Pin 177	L22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA11	Pin 178	K20	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MA12	Pin 180	K22	O	Hold	12/6	32, 240	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC13}
MASTER#	Pin 122	X11	I	1K			Dis	Dis	PU	Tri	5V	V_{CC8}
MD0	Pin 182	J22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD1	Pin 183	H21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD2	Pin 184	H22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD3	Pin 185	G21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD4	Pin 186	G22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD5	Pin 187	F21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD6	Pin 188	F22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD7	Pin 189	H20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD8	Pin 191	G20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD9	Pin 192	D22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD10	Pin 193	F20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD11	Pin 194	E21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD12	Pin 195	E20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
MD13	Pin 2	D20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD14	Pin 3	C19	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD15	Pin 4	D21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD16	Pin 6	C17	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD17	Pin 7	C20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD18	Pin 8	C21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD19	Pin 9	C16	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD20	Pin 10	C22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD21	Pin 11	B18	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD22	Pin 12	C15	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD23	Pin 13	B19	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD24	Pin 15	B20	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD25	Pin 17	B21	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD26	Pin 19	B15	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD27	Pin 20	A22	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD28	Pin 21	B16	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD29	Pin 22	A15	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD30	Pin 23	C13	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}
MD31	Pin 24	A14	I/O	Hold	12/6	8, 32	Tri	Hold	Drv	Tri	3.3V/5V	V_{CC2}

NOTES:

1. Drive currents are for default buffer strengths only. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.
2. The states of ISA-bus and PI-bus pins listed in this column are programmable. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.

Table 2-2. Intel486™ SL Microprocessor Pin Characteristics (Continued)

Mnemonic	PQFP	LGA	Type	Term	Drive(1) I_{OL}/I_{OH} (Default)	Load Min, Max	PWR RST	Susp(2) (Default)	STOPCLK	ONCE	3.3V or 5V	
MEMCS16#	Pin 120	V11	I/O	1K		10, 160	Dis	Dis	PU	Tri	5V	V_{CC8}
MEMR#	Pin 109	W08	I/O	60K	7/4	10, 160	Tri	PU	PU	Tri	5V	V_{CC8}
MEMW#	Pin 110	X07	I/O	60K	7/4	10, 160	Tri	PU	PU	Tri	5V	V_{CC8}
NMI	Pin 35	A18	I	20K			Dis	Dis	PD	Dis	5V	V_{CC3}
ONCE#	Pin 27	A13	I	60K			En	En	PU	En	5V	V_{CC3}
PCMD#	Pin 48	B04	O	Hold	7/4	10, 50	Tri	PU	Drv	Tri	5V	V_{CC3}
PD0	Pin 190	E22	I/O	Hold	12/6		Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
PD1	Pin 5	C18	I/O	Hold	12/6		Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
PD2	Pin 14	B22	I/O	Hold	12/6		Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
PD3	Pin 25	B17	I/O	Hold	12/6		Tri	Hold	Drv	Tri	3.3V/5V	V_{CC13}
PERR#	Pin 31	A19	O	Hold		8, 32	Tri	Tri	Drv	Tri	5V	V_{CC3}
PM/IO#	Pin 51	D03	O	Hold	7/4	10, 50	Tri	PU	Drv	Tri	5V	V_{CC3}
PRDY#	Pin 53	C03	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
PSTART#	Pin 47	B05	O	Hold	7/4	10, 50	Tri	PU	Drv	Tri	5V	V_{CC3}
PW/R#	Pin 52	E03	O	Hold	7/4	10, 50	Tri	PU	Drv	Tri	5V	V_{CC3}
PWRGOOD	Pin 28	A21	I				En	En	En	Dis	5V	V_{CC3}
RAS0#	Pin 155	R21	O	Hold	17/10	32, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
RAS1#	Pin 156	Q20	O	Hold	17/10	32, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
RAS2#	Pin 157	T21	O	Hold	17/10	32, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
RAS3#	Pin 158	U21	O	Hold	17/10	32, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
RAS4#	Pin 159	X22	O	Hold	17/10	32, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
REFREQ	Pin 45	A06	I	Hold			Dis	En	En	Dis	5V	V_{CC3}
ROMCS0#	Pin 57	G01	O	Hold	7/4	10, 50	Tri	Tri	Drv	Tri	5V	V_{CC3}
ROMCS1#	Pin 58	E02	O	Hold	7/4	10, 50	Tri	Tri	Drv	Tri	5V	V_{CC3}
ROMCS16/8#	Pin 26	A20	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
SA0	Pin 59	H01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA1	Pin 60	G02	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA2	Pin 61	J03	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA3	Pin 62	F02	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA4	Pin 63	J01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA5	Pin 64	B01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA6	Pin 66	E01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA7	Pin 68	K01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA8	Pin 69	D01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA9	Pin 70	L01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA10	Pin 71	C01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA11	Pin 72	F01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA12	Pin 73	L03	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA13	Pin 74	U01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA14	Pin 75	M01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA15	Pin 76	N01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA16	Pin 77	V01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA17	Pin 78	P01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA18	Pin 79	X01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SA19	Pin 80	N03	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}
SBHE#	Pin 82	W01	I/O	Hold	7/4	10, 160	Tri	Tri	Drv	Tri	5V	V_{CC5}

NOTES:
1. Drive currents are for default buffer strengths only. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.
2. The states of ISA-bus and PI-bus pins listed in this column are programmable. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.

Table 2-2. Intel486™ SL Microprocessor Pin Characteristics (Continued)

Mnemonic	PQFP	LGA	Type	Term	Drive(1) I_{OL}/I_{OH} (Default)	Load Min, Max	PWR RST	Susp(2) (Default)	STOPCLK	ONCE	3.3V or 5V	
SD0	Pin 84	T01	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD1	Pin 85	Q01	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD2	Pin 86	U02	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD3	Pin 87	R01	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD4	Pin 88	T02	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD5	Pin 89	S01	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD6	Pin 90	P02	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD7	Pin 91	S02	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD8	Pin 92	Q03	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD9	Pin 93	R02	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD10	Pin 94	S03	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD11	Pin 95	U03	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD12	Pin 96	T03	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD13	Pin 97	V03	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD14	Pin 100	W02	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SD15	Pin 101	V04	I/O	60K	7/4	10, 160	Tri	Tri	PU	Tri	5V	V_{CC6}
SELFTEST	Pin 124	X12	I	20K			Dis	Dis	PD	Dis	5V	V_{CC8}
SMI#	Pin 44	B02	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
SMRAMCS#	Pin 56	D02	O	Hold	7/4	10, 50	Drv	Drv	Drv	Tri	5V	V_{CC3}
STPCLK#	Pin 43	A07	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
SUS_STAT#	Pin 29	C11	I				En	En	En	Dis	5V	V_{CC3}
SYSCLK	Pin 117	X09	O	Hold	7/4	10, 160	Drv	Tri	Drv	Hold	5V	V_{CC8}
TCK	Pin 125	X13	I	60K			Dis	Dis	PU	En	5V	V_{CC8}
TDI	Pin 126	X18	I	60K			Dis	Dis	PU	En	5V	V_{CC8}
TDO	Pin 127	X14	O		25/15		Drv	Drv	Drv	Drv	5V	V_{CC8}
TMS	Pin 128	X17	I	60K			Dis	Dis	PU	En	5V	V_{CC8}
TRST#	Pin 129	X15	I	60K			Dis	Dis	PU	En	5V	V_{CC8}
Turbo	Pin 54	F03	I	60K			Dis	Dis	PU	Dis	5V	V_{CC3}
VGACS#	Pin 46	C06	O	Hold	12/6	10, 50	Tri	PU	Drv	Tri	5V	V_{CC3}
WE0#	Pin 161	P21	O	Hold	13/8	15, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
WE1#	Pin 162	P20	O	Hold	13/8	15, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
WE2#	Pin 164	Q22	O	Hold	13/8	15, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
WE3#	Pin 165	P22	O	Hold	13/8	15, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
WEC#	Pin 160	Q21	O	Hold	12/6	15, 136	Tri	Drv	Drv	Tri	3.3V/5V	V_{CC12}
ZEROWS#	Pin 119	W11	I	1K			Dis	Dis	PU	Tri	5V	V_{CC8}

NOTES:
1. Drive currents are for default buffer strengths only. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.
2. The states of ISA-bus and PI-bus pins listed in this column are programmable. Refer to Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for details.

Power Pins:

1. V_{CC}:

PQFP—	3.3V:	V_{CC1}(Pin 1), V_{CC4}(Pin 50), V_{CC7}(Pin 99), V_{CC11}(Pin 148)
	3.3V/5V:	V_{CC2}(Pin 18), V_{CC9}(Pin 131, V_{CC10}(Pin 132), V_{CC12}(Pin 166), V_{CC13}(Pin 181)
	5V:	V_{CC3}(Pin 34), V_{CC5}(Pin 67), V_{CC6}(Pin 83), V_{CC8}(Pin 116)
LGA—	3.3V:	B09, B11, B13, J02, K21, L02, M21, N02, W12, W14, V06
	3.3V/5V:	V13, V15, N20, L20, J20, C14, C12
	5V:	C10, H03, K03, M03, P03, V09

2. V_{SS}:

PQFP—	V_{SS1}(Pin 16), V_{SS2}(Pin 32), V_{SS3}(Pin 49), V_{SS4}(Pin 65), V_{SS5}(Pin 81), V_{SS6}(Pin 98), V_{SS7}(Pin 114), V_{SS8}(Pin 130), V_{SS9}(Pin 147), V_{SS10}(Pin 163), V_{SS11}(Pin 179), V_{SS12}(Pin 196)
LGA—	B10, B12, B14, H02, J21, K02, L21, M02, W13, W15

No Connect:

LGA—	A03, A04, A05, A16, B03, B06, B07, C03, C04, C05, C07, C08, Q02, R03, S21, T20, V02, V05, V07, W07, X03, X06

2.2 Intel486™ SL Microprocessor Signal Descriptions

The following table provides a brief description of the signals of the Intel486 SL Microprocessor. Signal names which end with "#" indicate that the corresponding signal is low when active.

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Symbol	Name and Function
A20GATE	**A20 GATE:** This active HIGH input signal controls the A20 address line. When this signal is HIGH, the internal physical address signal A20 is available on the System Address (SA) bus. When LOW this signal forces the CPU to mask off (force LOW) the internal physical address signal A20. A20GATE asserted LOW limits the physical address range to 1 megabyte compatible with the Real-Mode 8086/8088 used in PC/XT systems. Accesses above 1 megabyte "wrap around" when A20GATE is LOW.
BALE	**Bus Address Latch Enable (ISA BUS SIGNAL):** This active HIGH output signal is used for two purposes. BALE is used to latch the LA-bus (LA17–LA23) address signals on the falling edge of BALE. BALE is also used to qualify ISA-bus cycles for signals on the Peripherial Interface (PI) bus (PM/IO# and PW/R#). On the falling edge of BALE, PM/IO# and PW/R# can be sampled to determine the type of ISA bus cycle. BALE may be used to qualify and generate buffered control and status signals to the ISA-bus. The PI bus signal decoding is as follows: Type of Bus Cycle — P/IO# — PW/R# Memory Read — 1 — 0 Memory Write — 1 — 1 I/O Read — 0 — 0 I/O Write — 0 — 1 Interrupt Acknowledge — 0 — 1 HALT (address = 2)* — 1 — 1 Shutdown (address = 0)* — 1 — 1 *Note that BALE is not generated for these cycles, however PM/IO# and PW/R# will reflect these states during HALT and Shutdown bus cycles where BALE is driven in typical ISA bus systems. Memory read/write, IO read/write and interrupt/interrupt acknowledge cycles correspond to the ISA bus cycle.
CAS00#	**Column Address Strobe Bank 0, Byte 0:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 0. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 0, byte 0, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 0–7, (MD7:0) of physical DRAM bank 0. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 0, DRAM LCAS# for read or write access to DRAM bank 0, byte 0 (MD7:0). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to bank 0, DRAM CAS# and supports word wide read or write access to the lower word of DRAM bank 0, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CAS01#	**Column Address Strobe Bank 0, Byte 1:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 0. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 0, byte 1, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 8–15, (MD15:8) of physical DRAM bank 0. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 0, DRAM UCAS# for read or write access to DRAM bank 0, byte 1 (MD15:8). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS00# is internally OR'ed to support word wide read or write access to the lower word of DRAM bank 0, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS02#	**Column Address Strobe Bank 0, Byte 2:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 0. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x 1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 0, byte 2, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 16–23, (MD23:16) of physical DRAM bank 0. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 0, DRAM LCAS# for read or write access to DRAM bank 0, byte 2 (MD23:16). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to the bank 0, DRAM CAS# and supports word wide read or write access to the upper word of DRAM bank 0, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS03#	**Column Address Strobe Bank 0, Byte 3:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 0. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 0, byte 3, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 24–31, (MD31:24) of physical DRAM bank 0. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 0, DRAM UCAS# for read or write access to DRAM bank 0, byte 3 (MD31:24). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS02# is internally OR'ed to support word wide read or write access to the upper word of DRAM bank 0, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CAS10#	**Column Address Strobe Bank 1, Byte 0:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 1. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 1, byte 0, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 0–7, (MD7:0) of physical DRAM bank 1. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 1, DRAM LCAS# for read or write access to DRAM bank 1, byte 0 (MD7:0). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to the bank 1, DRAM CAS# and supports word wide read or write access to the lower word of DRAM bank 1, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS11#	**Column Address Strobe Bank 1, Byte 1:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 1. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 1, byte 1, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 8–15, (MD15:8) of physical DRAM bank 1. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 1, DRAM UCAS# for read or write access to DRAM bank 1, byte 1 (MD15:8). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS10# is internally OR'ed to support word wide read or write access to the lower word of DRAM bank 1, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS12#	**Column Address Strobe Bank 1, Byte 2:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 1. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 1, byte 2, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 16–23, (MD23:16) of physical DRAM bank 1. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 1, DRAM LCAS# for read or write access to DRAM bank 1, byte 2 (MD23:16). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to the bank 1, DRAM CAS# and supports word wide read or write access to the upper word of DRAM bank 1, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CAS13#	**Column Address Strobe Bank 1, Byte 3:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 1. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 1, byte 3, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 24–31, (MD31:24) of physical DRAM bank 1. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 1, DRAM UCAS# for read or write access to DRAM bank 1, byte 3 (MD31:24). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS12# is internally OR'ed to support word wide read or write access to the upper word of DRAM bank 1, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS20#	**Column Address Strobe Bank 2, Byte 0:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 2. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 2, byte 0, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 0–7, (MD7:0) of physical DRAM bank 2. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 2, DRAM LCAS# for read or write access to DRAM bank 2, byte 0 (MD7:0). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to the bank 2, DRAM CAS# and supports word wide read or write access to the lower word of DRAM bank 2, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS21#	**Column Address Strobe Bank 2, Byte 1:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 2. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 2, byte 1, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 8–15, (MD15:8) of physical DRAM bank 2. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 2, DRAM UCAS# for read or write access to DRAM bank 2, byte 1 (MD15:8). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS20# is internally OR'ed to support word wide read or write access to the lower word of DRAM bank 2, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CAS33#	**Column Address Strobe Bank 3, Byte 3:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 3. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 3, byte 3, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 24–31, (MD31:24) of physical DRAM bank 3. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 3, DRAM UCAS# for read or write access to DRAM bank 3, byte 3 (MD31:24). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS32# is internally OR'ed to support word wide read or write access to the upper word of DRAM bank 3, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS40#	**Column Address Strobe Bank 4, Byte 0:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 4. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 4, byte 0, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 0–7, (MD7:0) of physical DRAM bank 4. When the memory controller is configured to support x16/18 DRAM with symmetrical addressing this signal is connected to the bank 4, DRAM LCAS# for read or write access to DRAM bank 4, byte 0 (MD7:0). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to the bank 4, DRAM CAS# and supports word wide read or write access to the lower word of DRAM bank 4, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS41#	**Column Address Strobe Bank 4, Byte 1:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 4. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 4, byte 1, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 8–15, (MD15:8) of physical DRAM bank 4. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 4, DRAM UCAS# for read or write access to DRAM bank 4, byte 1 (MD15:8). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS40# is internally OR'ed to support word wide read or write access to the lower word of DRAM bank 4, (MD15:0). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CAS42#	**Column Address Strobe Bank 4, Byte 2:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 4. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 4, byte 2, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 16–23, (MD23:16) of physical DRAM bank 4. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 4, DRAM LCAS# for read or write access to DRAM bank 4, byte 2 (MD23:16). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is connected to the bank 4, DRAM CAS# and supports word wide read or write access to the upper word of DRAM bank 4, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CAS43#	**Column Address Strobe Bank 4, Byte 3:** This LOW true output of the Memory Controller Unit is a column address strobe for physical DRAM bank 4. When this signal is low the multiplexed memory address signals (MA12:0) are clocked into the DRAM column address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 4, byte 3, CAS# signal. When low this signal is used to support byte wide read or write access to Memory Data bits 24–31, (MD31:24) of physical DRAM bank 4. When the memory controller is configured to support x16/18 DRAMs with symmetrical addressing this signal is connected to the bank 4, DRAM UCAS# for read or write access to DRAM bank 4, byte 3 (MD31:24). When the memory controller is configured to support x16/18 DRAMs with asymmetrical addressing this signal is not connected. CAS42# is internally OR'ed to support word wide read or write access to the upper word of DRAM bank 4, (MD31:16). This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CPURESET	**CPU RESET:** This active HIGH input forces the Intel486 SL CPU to execute a reset to the internal CPU core and state machines. CPU Reset is used for PC/AT compatibility with 80286 task switch from protected mode to real mode. CPU Reset always occurs during a PowerGood Reset and may also be generated from Keyboard RC# (INT 19), I/O Port 92 or other programmable reset furnished from the 82360SL I/O. The configuration registers are not reset.
DMA8/16#	**DMA 8-Bit or 16-Bit Cycle:** This input, in conjunction with HRQ, indicates to the Intel486 SL CPU if an 8-bit or 16-bit DMA access is occurring. When High this indicates an 8-bit DMA cycle. If an 8-bit DMA access is occurring, the Intel486 SL CPU will swap the upper byte of the data to the lower data byte for upper byte accesses. When Low this indicates a 16-bit DMA transfer. 16-bit DMA transfers are aligned and therefore no byte swapping is required.
EFI	**External Frequency Input:** This is the primary oscillator input. The EFI input provides all clock signals to the CPU core, memory controller, and additional internal logic. EFI is equal to twice the desired processor frequency.
FLSHDCS#	**FLaSH Disk Chip Select:** This LOW true output is used to support a Solid State Non-Volatile Memory such as a FLASH EPROM card. When this signal is LOW a FLASH device is being accessed on the PI-bus. The address range for a Solid State disk on the PI-bus is from 0–16 megabytes and is an off-board memory access. This signal is controlled by the External Bus Controller ISA-Sliding Window Configuration register. This pin is functionally equivalent to the Intel386 SL Microprocessor CMUX14 signal.

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
FPUERROR#	**Numerics Error:** This active LOW output is generated from the on-chip floating point unit (FPU). It indicates to the 82360SL I/O that an unmasked exception has occurred in the FPU. FPUERROR# is provided to allow numerics error handling compatible with the PC/AT ERROR# signal. FPUERROR# is directly connected to the 82360SL I/O which internally generates IRQ13.
HALT#	**HALT:** This active LOW output indicates to external devices that the Intel486 SL CPU has executed a HALT instruction (address = 2) or a shutdown condition (address = 0). This can be used as an indicator for devices to assert the STPCLK# signal to the Intel486 SL CPU.
HLDA	**HoLD Acknowledge:** This active HIGH output indicates to external devices that Intel486 SL CPU has relinquished control of the ISA bus. At this time Intel486 SL CPU has floated the address and control signals of the ISA bus. HLDA is asserted high in response to a Hold Request for PC/AT compatible Refresh, DMA and Master cycles.
HRQ	**Hold ReQuest:** This active HIGH input indicates to Intel486 SL CPU that an external device wishes to take control of the ISA bus.
INTA#	**INTerrupt Acknowledge:** This active LOW output indicates that Intel486 SL CPU has recognized a valid Interrupt Request cycle and will initiate an Interrupt Acknowledge Bus Cycle. An Interrupt Acknowledge bus cycle is composed of two 8-bit I/O cycles in which the interrupt vector is transferred on the second I/O write by Intel486 SL CPU.
INTR	**INTerrupt Request:** This active HIGH input indicates to Intel486 SL CPU that an external device is requesting the execution of an interrupt service routine.
IOCHRDY	**I/O CHannel ReaDY:** This active HIGH input indicates that the I/O Channel (ISA expansion bus) is ready to terminate the bus cycle. The ISA expansion bus is a normally ready bus. When an ISA bus peripheral wishes to extend the default 8- or 16-bit ISA bus cycle the ISA bus device drives IOCHRDY LOW. IOCHRDY is also automatically asserted low to extend bus cycles for I/O device trapping. The additional ISA bus wait states are used for start up by the 82360SL I/O when the Intel486 SL CPU is executing a Resume instruction or I/O instruction restart while in the System Management Mode.
IOCS16#	**I/O Chip Select 16:** This active LOW input indicates that an ISA bus peripheral wishes to execute a 16-bit I/O cycle. This signal has an active pull-up, when not driven the default I/O bus cycle is 8-bits.
IOR#	**I/O Read:** This bi-directional active LOW signal indicates that the ISA bus is executing an I/O read cycle. Any "normal" I/O read by the Intel486 SL CPU in the I/O address space from 0000–FFFF hex will result in IOR# being driven LOW by the Intel486 SL CPU. IOR# can also be driven by external Masters or DMA. When IOR is LOW it instructs an I/O device to drive its data onto the ISA data bus. ISA I/O bus cycles may be 8- or 16-bit.
IOW#	**I/O Write:** This bi-directional active LOW signal indicates that the ISA bus is executing an I/O write cycle. Any "normal" I/O write by the Intel486 SL CPU in the I/O address space from 0000–FFFF hex will result in an IOW# being driven LOW by the Intel486 SL CPU. IOW# can also be driven by external Masters or DMA. When IOW# is LOW it instructs an I/O device to read data from the ISA data bus. ISA I/O bus cycles may be 8- or 16-bit.
ISACLK2	**ISA Clock Two:** This is the ISA bus controller oscillator input. This clock controls all of the ISA bus timings and is equal to twice the SYSCLK frequency. Normally the ISA bus SYSCLK is 8 MHz and the ISACLK2 oscillator is 16 MHz.

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
LA[23:17]	**Latchable ISA Address Bus:** These eight bi-directional signals are the unlatched upper address of the ISA bus. When this bus is driven by the Intel486 SL CPU it provides CPU access to off-board memory and memory mapped I/O devices from 1 megabyte–16 megabytes. When DMA has control of the ISA bus the 74LS612 DMA page address mapper drives this bus to provide DMA access to off-board or on-board memory above 1 megabyte. Alternate Masters on the ISA bus may also drive LA23:17. LA23:17 are VALID when BALE is HIGH but are not latched and held valid throughout the entire ISA memory bus cycle. LA23:17 are also used to generate memory decodes for 16-bit memory bus cycles. The MEMCS16# decode should be latched on the falling edge of BALE by ISA devices. LA23:17 is also used by the Peripheral Interface (PI) Bus in conjunction with the ISA sliding window configuration register to provide PI-Bus access from 1 megabyte–32 megabytes.
MA[12:0]	**Memory Controller Multiplexed Address Bus:** These outputs are the memory address bus used by the Memory Controller and on-board DRAM. A 26-bit address space is supported (up to 64 Mbytes). The memory address signals are output in a row/column fashion to DRAM. The Intel486 SL CPU Memory Controller Unit places the ROW address out first and qualifies it by the RASx# signal going active (LOW). The column address is then placed on the Memory Address bus and is qualified by the CASXx# signals going active (LOW). This pin is disabled when SUS_STAT# is active (low) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
MASTER#	**MASTER:** This active LOW input indicates that an ISA bus peripheral is controlling the bus. The peripheral device asserts this signal in conjunction with a DMA request (DRQ) line to gain control of the bus. MASTER# should be asserted when receiving the corresponding DMA Acknowledge (DACK#) from the corresponding DMA channel that the DMA requests when the DMA is configured in cascade mode. When MASTER# is asserted LOW along with HRQ being asserted HIGH, the Intel486 SL CPU will float all address data and control signals on the ISA bus.
MD[31:0]	**Memory Controller Local Memory Data Bus:** This is the bi-directional data bus of the Memory Controller Unit. All accesses by the Memory Controller Unit that transfer data between Intel486 SL CPU and DRAM use the Memory Data Bus. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
MEMCS16#	**MEMory Chip Select 16:** This active LOW input indicates that an ISA bus peripheral wishes to execute a 16-bit memory cycle. This signal has an active pull-up; when it is not driven LOW the default memory bus cycle is 8-bits.
MEMR#	**MEMory Read:** This bi-directional active LOW signal indicates that a memory read access is taking place on the ISA bus. When the Intel486 SL CPU is performing a memory read to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA device or Master drives MEMR#.
MEMW#	**MEMory Write:** This bi-directional active LOW signal indicates when a memory write access is taking place on the ISA bus. When the Intel486 SL CPU is performing a memory write to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA controller or Bus Master drives MEMW#.
NMI	**Non-Maskable Interrupt:** This rising edge sensitive input will latch a request to Intel486 SL CPU for a non-maskable interrupt on a LOW-to-HIGH transition.

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
ONCE#	**On-Board Circuit Emulation:** This active LOW input signal floats the necessary outputs from the Intel486 SL CPU allowing an in-circuit emulation (ICE™) module to drive the Intel486 SL CPU signals. This allows an emulator or function board tester to be used for system testing and development while the Intel486 SL CPU and the 82360SL I/O are still physically populated on the system motherboard. When ONCE# is asserted, all output pins except TDO are tristated.
PCMD#	**PI-bus CoMmanD:** This active LOW output indicates that valid write data is on the System data bus (SD[15:0]) signals, or that the Intel486 SL CPU is ready to sample valid read data from the PI-bus for Peripherial Interface bus cycles. This signal is similar to the ISA-Bus command signals (MEMR#, MEMW# or IOR#, IOW#) for bus cycle definition and control but is also used in conjunction with PM/IO#, PSTART# and PW/R#. Devices which reside on the PI-bus use PCMD#, PM/IO#, PSTART# and PW/R# to decode and control PI-bus cycles.
PD[3:0]	**Parity Data 0–3.** These four bi-directional signals are part of the 36-bit Intel486 SL CPU On-board Memory bus. For DRAM subsystems which provide a parity bit for each byte these bits provide even parity error generation and checking. PD0 corresponds to memory data byte 0, and PD1–3 correspond to memory data bytes 1–3 respectively. The parity bits are driven during DRAM writes either HIGH if the 8-data bits of the associated bytes are an even number or LOW if the 8-data bits are an odd number. Parity error generation and checking is enabled through the Intel486 SL CPU MCU MCPARITY configuration register and ISA control Port 61 hex in the 82360SL I/O.
PERR#	**Parity ERRor:** This active LOW output indicates to an external device that the Intel486 SL CPU Memory Controller Unit has detected a memory parity error. The Intel486 SL CPU PERR# signal is used by the 82360SL I/O to generate NMI back to the Intel486 SL CPU. The NMI received by Intel486 SL CPU provides a mechanism for PC/AT compatible memory parity error detection which is typically handled by the system BIOS.
PM/IO#	**PI-bus Memory or I/O:** This output indicates the type of bus cycle being executed on the Peripheral Interface Bus (PI-bus): Either a Memory (HIGH) or I/O (LOW) cycle. This signal is similar to the i486 CPU M/IO# and is used for bus cycle definition for devices residing on the PI-bus.
PRDY#	**PI-bus Ready:** This active LOW input is used to terminate Peripheral Interface bus cycles. The Peripheral Interface Bus is a normally not-ready bus, and will continue the bus cycle until the PRDY# is activated or a Peripheral Interface Bus Time-out occurs.
PSTART#	**PI-bus Start:** This active LOW output indicates that the address (SA[19:0], LA[23:17], SBHE#), command signals (PM/IO# and PW/R#) and chip-selects (VGACS# or FLSHDCS#) are valid for a Peripheral Interface Bus cycle. This signal is similar to BALE and i486 CPU ADS# signals which are used by devices on the PI-bus to indicate valid Address and PI-Bus cycle definition signals.
PW/R#	**PI-bus Write or Read:** This output indicates the type of bus cycle being executed on the Peripheral Interface Bus: Either a Write (HIGH) or Read (LOW) cycle. This signal is similar to the i486 CPU W/R# and is used for bus cycle definition by devices residing on the PI-bus.
PWRGOOD	**PoWeR GOOD:** This active HIGH input indicates that power to the system is good. This signal is generated by the power supply circuitry. A logic LOW level on this signal causes the Intel486 SL CPU system to totally reset: The CPU core is reset, internal state machines are reset, all configuration registers are reset. Power Good should be low for a specified minimum number of CPU clocks for valid recognition in order to perform a global Intel486 SL CPU reset.

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
RAS0#	**Row Address Strobe, bank 0:** This LOW true output of the Memory Controller Unit is a row address strobe for physical DRAM bank 0. When this signal is low the multiplexed memory address signals (MA[12:0]) are clocked into the DRAM row address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 0, bytes 0–3, RAS# signal. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS1#	**Row Address Strobe, bank 1:** This LOW true output of the Memory Controller Unit is a row address strobe for physical DRAM bank 1. When this signal is low the multiplexed memory address signals (MA[12:0]) are clocked into the DRAM row address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 1, bytes 0–3, RAS# pins. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS2#	**Row Address Strobe, bank 2:** This LOW true output of the Memory Controller Unit is a row address strobe for physical DRAM bank 2. When this signal is low the multiplexed memory address signals (MA[12:0]) are clocked into the DRAM row address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 2, bytes 0–3, RAS# pins. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS3#	**Row Address Strobe, bank 3:** This LOW true output of the Memory Controller Unit is a row address strobe for physical DRAM bank 3. When this signal is low the multiplexed memory address signals (MA[12:0]) are clocked into the DRAM row address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 3, bytes 0–3, RAS# pins. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS4#	**Row Address Strobe, bank 4:** This LOW true output of the Memory Controller Unit is a row address strobe for physical DRAM bank 4. When this signal is low the multiplexed memory address signals (MA[12:0]) are clocked into the DRAM row address. When the memory controller is configured to support x1, x4, x8/9 DRAMs or x8/9, x32/16 DRAM SIMMs this signal is connected to the bank 4, bytes 0–3, RAS# pins. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
REFREQ	**REFresh REQuest:** This active HIGH input indicates that the Memory Controller should perform an internal DRAM refresh cycle to the on-board local DRAM memory. REFREQ is typically furnished by the 82360SL I/O from one of two internal 82360SL I/O clock sources: the internal 8254 Timer Counter 1 Channel 1 for Normal AT refresh or the internal Real Time Clock 32 KHz oscillator for suspend refresh.
ROM16/8#	**ROM 16-Bit or 8-Bit:** This input configuration signal pin selects if the BIOS interface is a 16-bit (when high) or 8-bit interface (when low). This pin has an internal pull-up resistor defaulting to a 16-bit BIOS EPROM interface.
ROMCS0#	**ROM Chip Select 0:** This LOW true output provides the chip select for the System BIOS EPROM. This signal is driven LOW when an address range for off-board memory accesses occur as defined by the Intel486 SL CPU External Bus Controller's Configuration Register #1 and ISA Sliding Window Configuration Register.

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
ROMCS1#	**ROM Chip Select 1:** This LOW true output provides the chip select for the System BIOS EPROM. This signal is driven LOW when an address range for off-board memory accesses occur as defined by the Intel486 SL CPU External Bus Controller's Configuration Register #1 and ISA Sliding Window Configuration Register.
SA[19:0]	**System Address bus:** This is the bi-directional system address of the ISA bus, as well as the Peripherial Interface Bus. SA[19:0] are inputs during DMA and Master operation. SA[19:17] are outputs since the 8237 compatible DMA controller can accesses only 64 Kbytes at a time. The 74LS612 module in the 82360SL I/O is used to furnish the DMA upper addresses for DMA access to 16 megabyte.
SBHE#	**System Byte High Enable:** When this output signal is LOW, it indicates that data is being transferred on the upper byte of the 16-bit data bus (SD[15:8]).
SD[15:0]	**System Data bus:** This 16-bit bi-directional data bus is used to transfer data between Intel486 SL CPU and the ISA-BUS. The system data bus is also used to transfer data between Intel486 SL CPU and the Peripherial Interface (PI-BUS) and to transfer data between the Intel486 SL CPU and the 82360SL I/O.
SELFTEST	**SELF-TEST:** This HIGH true input will invoke the built-in self-test. The BIST is functionally equivalent to the i486 CPU BIST. To invoke BIST, the SELFTEST signal is asserted after PWRGOOD is high and must remain HIGH for at least 50 EFIs.
SMI#	**System Management Interrupt:** This falling edge sensitive input latches the System Management interrupt request with a High-to-Low edge. The SMI# is the highest priority interrupt in Intel486 SL CPU.
SMRAMCS#	**System Management RAM Chip Select:** This LOW true output indicates that the Intel486 SL CPU has received an SMI# and is currently in System Management Mode. This signal may be used by external logic to decode and support SMRAM accesses. The 82360SL I/O uses this signal to indicate any access to SMRAM space. If the Intel486 SL CPU has declared SMRAM as off-board, 82360SL I/O will enable the X-bus to support external SRAM used as SMRAM when the Intel486 SL CPU is in SMM. This signal is driven during any access to SMRAM space whether it is off-board or on-board.
STPCLK#	**SToP CLocK:** This active LOW input stops the clock to the internal CPU core. This signal is typically driven by the 82360SL I/O and will stop the Intel486 SL CPU and FPU clocks internally.
SYSCLK	**SYStem CLocK:** This Intel486 SL CPU clock output is used by the ISA bus and 82360SL I/O as a timing reference for off-board memory and I/O bus cycles. The SYSCLK is equal to one half of the ISACLK2 frequency. This signal is typically 8 MHz.
SUS_STAT#	**SUSpend_STATe:** This active LOW input indicates that system power is being turned off. The Intel486 SL CPU will respond by electrically isolating selected pins.
TCK	**Test ClocK:** This input clock is used to support IEEE 1149.1 JTAG boundary scan in the Intel486 SL CPU. The test clock input is used to clock state information and data into the Test Access Port (TAP) controller. Test select information (TMS) and test data (TDI) are clocked into the boundary scan logic on the rising edge of TCK. Test data out (TDO) is clocked out on the falling edge of TCK.
TDI	**Test Data Input:** This input is used to shift serial IEEE 1149.1 JTAG instructions and serial data into the boundary scan logic. The TDI input is sampled on the rising edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. During all other TAP states the TDI input is a "don't care".
TDO	**Test Data Output:** This output is used to shift serial IEEE 1149.1 JTAG instructions and serial data out of the boundary scan logic. The TDO output is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. During all other times the TDO output is in a high impedance state.

2.2 Intel486™ SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
TMS	**Test Mode Select:** This input is used by the Intel486 SL CPU IEEE 1149.1 JTAG TAP to select the operation of the test logic. TMS is sampled on the rising edge of TCK. TMS is provided with an internal pull-up to guarantee deterministic behavior of the TAP controller and boundary-scan logic.
TRST#	**Test ReSeT:** This LOW true input is used to asynchronously reset the Intel486 SL CPU TAP controller and associated boundary scan logic.
TURBO	**TURBO:** This active HIGH input signal indicates when to enter "Turbo Mode". Turbo Mode is defined as the CPU executing at full speed, the default speed for the system. When this signal is forced inactive LOW, Intel486 SL CPU executes from a divide-by-four or a divide-by-eight clock as defined by the De-turbo bit in the CPUPWRMODE register. When this signal is HIGH, the CPU executes from a clock source defined by the Fast CPU clock field in the CPUPWRMODE register.
$V_{CC1,4,7,11}$	**System Power:** Provides the +3.3V nominal D.C. supply inputs to the CPU, Cache, FPU and other internal modules. The designation is for the 196-lead PQFP only.
$V_{CC2,9,10,12,13}$	**System Power:** Provides the +3.3V or +5V nominal D.C. supply inputs to the DRAM memory controller external interface buffers. The designation is for the 196-lead PQFP only.
$V_{CC3,5,6,8}$	**System Power:** Provides the +5V nominal D.C. supply inputs to the external bus controller interface buffers. The designation is for the 196-lead PQFP only.
VGACS#	**VGA Chip-Select:** This active LOW output is asserted anytime an access occurs to the user defined VGA address space.
V_{SS}	**System Ground:** Provides the 0V reference for all inputs and outputs.
WEC#	**Write Enable Common:** This active LOW output indicates that a write access to the entire dword (32 bits) of the memory bus is occurring. This output should be connected to the write enable of DRAM memory cards. This pin is driven during a suspend operation.
WE0#	**Write Enable, Byte 0:** This active LOW output indicates that a write access to the lower byte of the memory bus is occurring. This output should be connected to the write enable of the byte 0, banks 0–4 DRAM memory subsystems. This pin is driven during a suspend operation.
WE1#	**Write Enable, Byte 1:** This active LOW output indicates that a write access to the lower byte of the memory bus is occurring. This output should be connected to the write enable of the byte 1, banks 0–4 DRAM memory subsystems. This pin is driven during a suspend operation.
WE2#	**Write Enable, Byte 2:** This active LOW output indicates that a write access to the lower byte of the memory bus is occurring. This output should be connected to the write enable of the byte 2, banks 0–4 DRAM memory subsystems. This pin is driven during a suspend oeration.
WE3#	**Write Enable, Byte 3:** This active LOW output indicates that a write access to the lower byte of the memory bus is occurring. This output should be connected to the write enable of the byte 3, banks 0–4 DRAM memory subsystems. This pin is driven during a suspend operation.
ZEROWS#	**ZERO Wait State (ISA Bus Signal):** This active LOW input indicates that an ISA bus peripheral wishes to execute a zero wait state bus cycle (the normal default 16-bit ISA bus memory or I/O cycle is 3 SYSCLKs or one PC/AT equivalent wait state). When ZEROWS# is driven LOW, a 16-bit bus cycle will occur in two SYSCLKs. When ZEROWS# is driven LOW for an 8-bit memory cycle the default 6 SYSCLK bus cycle is shortened to 3 SYSCLKs.

2.3 Intel486™ SL Microprocessor D.C. Specifications

Functional Operating Range: V_{CC5V} = 5.0V ±10%; T_{case} = 0°C to +90°C

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC5V}	Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Low Voltage	−0.3		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
I_{CC}	Supply Current		23	35	mA	
C_{OUT}	I/O or Output Capacitance		20		pF	Not Tested
V_{OL}	Output Low Voltage I_{OL} = 4 mA at Buffer Strength 1X I_{OL} = 7 mA at Buffer Strength 2X I_{OL} = 13 mA at Buffer Strength 4X			 0.4 0.4 0.4	 V V V	(Note 1)
	I_{OL} = 7 mA at Buffer Strength 2X			0.4	V	(Note 2)
	I_{OL} = 12 mA at Buffer Strength 3X			0.4	V	(Note 3)
	I_{OL} = 13 mA at Buffer Strength 4X			0.4	V	(Note 4)
V_{OH}	Output High Voltage I_{OH} = −2 mA at Buffer Strength 1X I_{OH} = −4 mA at Buffer Strength 2X I_{OH} = −8 mA at Buffer Strength 4X	 2.4 2.4 2.4			 V V V	(Note 1)
	I_{OH} = −4 mA at Buffer Strength 2X	2.4			V	(Note 2)
	I_{OH} = −6 mA at Buffer Strength 3X	2.4			V	(Note 3)
	I_{OH} = −8 mA at Buffer Strength 4X	2.4			V	(Note 4)
	I_{OH} = −0.8 mA at Buffer Strength 4X	2.4			V	(Note 5)

NOTES:
1. Applicable for pins IOR#, IOW#, MEMR#, MEMW#, BALE, SA[19:0], LA[23:17] and SD[15:0]. The strengths of the output buffers on these signals range from 1X to 7X. They are resulted from the grouping of the three types of buffer strengths: 1X, 2X and 4X. For corresponding drive currents to all buffer strengths, please refer to Intel486 SL Microprocessor SuperSet System Design Guide.
2. Applicable for pins HLDA, SYSCLK, PSTART#, PCMD#, PM/IO#, PW/R#, IOCHRDY, IOCS16#, MEMCS16#, ROMCS[1:0]#, FLSHDCS#, and SMRAMCS#.
3. Applicable for pins INTA# and VGACS#.
4. Applicable for pin HALT#.
5. Applicable for pins IOCHRDY, 1OCS16# and MEMCS16# when the 1K pull-up is active.

2.3 Intel486™ SL Microprocessor D.C. Specifications (Continued)

Functional Operating Range: $V_{CC3.3V}$ = 3.3V ±0.3V; T_{case} = 0°C to +90°C

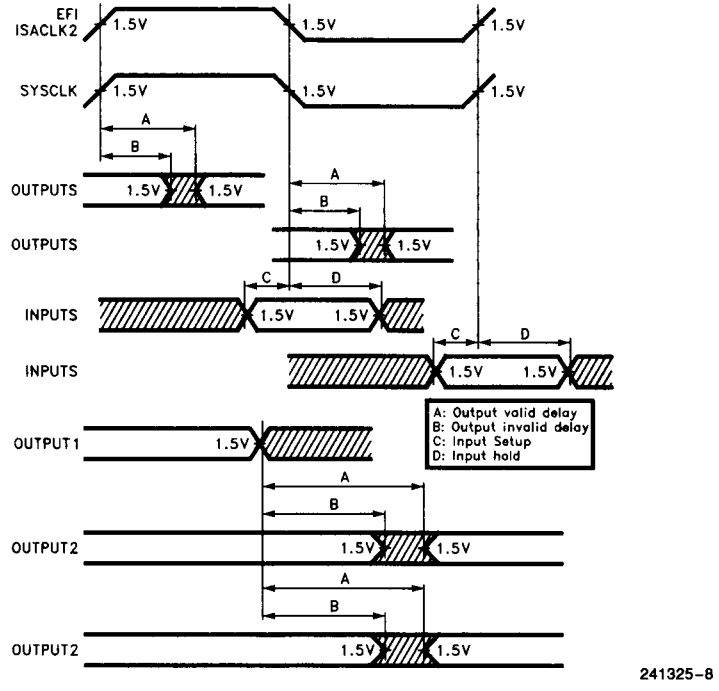
Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{CC3.3V}$	Supply Voltage	3.0	3.3	3.6	V	
V_{IL}	Input Low Voltage	−0.3		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage I_{OL} = 4 mA at Buffer Strength 1X I_{OL} = 7 mA at Buffer Strength 2X I_{OL} = 13 mA at Buffer Strength 4X			 0.4 0.4 0.4	 V V V	(Note 1)
V_{OL}	Output Low Voltage I_{OL} = 4 mA at Buffer Strength 1X I_{OL} = 12 mA at Buffer Strength 3X I_{OL} = 17 mA at Buffer Strength 5X			 0.4 0.4 0.4	 V V V	(Note 2)
V_{OH}	Output High Voltage I_{OH} = −2 mA at Buffer Strength 1X I_{OH} = −4 mA at Buffer Strength 2X I_{OH} = −8 mA at Buffer Strength 4X	 2.4 2.4 2.4			 V V V	(Note 1)
V_{OH}	Output High Voltage I_{OH} = −2 mA at Buffer Strength 1X I_{OH} = −6 mA at Buffer Strength 3X I_{OH} = −10 mA at Buffer Strength 5X	 24 24 24			 V V V	(Note 2)
I_{CC} @ 25 MHz	Supply Current EFI = 50 MHz		250	350	mA	
I_{CC1}	Supply Current with the STPCLK# Signal Asserted		50		mA	
I_{CC2}	Supply Current in Suspend Mode with Oscillators Off and RTC Refresh On		0.45		mA	
I_{CC3}	Supply Current in Suspend Mode with Oscillators Off and RTC Refresh Off		0.35		mA	
C_{IN}	Input Capacitance		20		pF	Not Tested

NOTES:
1. Applicable to pins MD[31:0], PD[3:0], MA[12:0], WEC and WE[3:0]#. The strengths of the output buffers on these signals range from 1X to 7X. They are resulted from the grouping of the three types of buffer strengths: 1X, 2X and 4X. For corresponding drive currents to all buffer strengths, please refer to Intel486 SL Microprocessor SuperSet System Design Guide.
2. Applicable to pins RAS[4:0]#, and CAS[43:00]#.

2.4 Intel486™ SL Microprocessor Timing Specifications

A.C. Specification Definitions

The A.C. specifications given in the tables of the following pages consist of output delays, input setup and hold requirements. They may be relative to a clock edge or another signal edge. ALL Intel486 SL CPU clock related specifications reference EFI except ISA bus timings which reference ISACLK2. A.C. specifications are defined in Figure 2.4.1. All clock related specifications are tested at the voltage levels shown. Output specifications are derived from tested clock related timings.



NOTE:
Signal waveforms are not drawn to scale

Figure 2.4.1. Drive Levels and Measurement Points for A.C. Specifications

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

ISA-Bus Clock Timings

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 201	ISACLK2 Period	62.5		ns		2.5.2	
Ct 202	ISACLK2 High Time at 2.0V	21		ns			
Ct 203	ISACLK2 Low Time at 0.8V	21		ns			
Ct 204	ISACLK2 Rise Time from 0.2 V_{CC} to 0.8 V_{CC}		8	ns			
Ct 205	ISACLK2 Fall Time from 0.8 V_{CC} to 0.2 V_{CC}		8	ns			
Ct 206	ISACLK2 to SYSCLK Delay Falling to Rising Edge	2	50	ns			
Ct 207	ISACLK2 to SYSCLK Delay Falling to Falling Edge	2	50	ns			
Ct 211	SYSCLK Period	125		ns			
Ct 212	SYSCLK High Time at 1.5V	56		ns			
Ct 213	SYSCLK Low Time at 1.5V	57		ns			
Ct 214	SYSCLK Fall Time from (V_{CC}5V−0.8V)		10	ns			
Ct 215	SYSCLK Rise Time from 0.8V to (V_{CC}5V−0.8V)		10	ns			
Ct 272a	A20GATE Setup to EFI (phi 1)	11		ns			
Ct 272b	A20GATE Hold Time	16		ns			

NOTE:
The buffer strength of SYSCLK is 2X.

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

ISA-Bus Timings

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 221	BALE Active Delay from Ts phi 2 Low		52	ns		2.5.8	
Ct 222	BALE Inactive Delay from Tc phi 1 Low	5	52	ns			
Ct 223	LA17–23 Valid Delay from Tc phi 2 Low		52	ns			
Ct 224	LA17–23 Invalid Delay from Tc phi 2 Low	0		ns			
Ct 225	SA2–19 Valid Delay from Ts phi 2 Low		45	ns			
Ct 227	SA2-19 Invalid Delay from Ts or Ti phi 2 Low	0		ns			
Ct 228	SA1–0, SBHE# Valid Delay from Ts phi 2 Low		52	ns			
Ct 229	SA1–0, SBHE# Invalid Delay from Ts or Ti phi 2 Low	0		ns			
Ct 230	MEMR#, MEMW# Active from Tc phi 1 Low (16-bit MEMR#/MEMW#, HALT# Cycles)	7	45	ns		2.5.14	
Ct 231	Command Active Setup to phi 2 Low (External Master)	18		ns		2.5.23	
Ct 232	HALT# Valid Delay from phi 1 Low		38	ns		2.5.20a	
Ct 233	Command Inactive to Float Delay from Ti phi 1 Low (External Master)		45	ns		2.5.23	
Ct 234	Command Active Delay from Tc phi 2 Low (IOR#/IOW# 8, 16-bit MEMR#/MEMW# 8-bit)	7	45	ns		2.5.8	
Ct 235	Command Inactive Delay from Teoc phi 1 Low (MEMR#/MEMW#, IOR#/IOW# and HALT#)	7	45	ns		2.5.8	
Ct 236	SA[19:2] Delay to MEMCS16#		24.5	ns			
Ct 238	MEMCS16# Setup to Tc phi 1 Low	0		ns		2.5.9	
Ct 239	MEMCS16# Hold from Tc phi 1 Low	25		ns		2.5.9	
Ct 240	IOCS16# Setup to Tc phi 2 Low	45		ns		2.5.11	
Ct 241	IOCS16# Hold from Teoc phi 1 Low	0		ns		2.5.12	
Ct 242	ZEROWS# Setup to phi 1 Low	40		ns		2.5.11	
Ct 244	ZEROWS# Hold from phi 1 Low	20		ns		2.5.11	
Ct 245	MEMCS16# Active Delay from Valid Address (External Master Cycles)		64	ns		2.5.24b	
Ct 246	SD0–15 Valid Setup to IOR#/MEMR#, INTA# Inactive	63		ns		2.5.9	
Ct 247	SD0–15 Hold from IOR#/MEMR#, INTA# Inactive	0		ns		2.5.8	
Ct 248	SD0–7 Valid Delay from Tc phi 1 Low		65	ns		2.5.8	
Ct 249	SD8–15 Valid Delay from Tc phi 1 Low		65	ns		2.5.14	
Ct 250	SD0–15 Invalid Delay from Teoc phi 2 Low	5		ns		2.5.8	

NOTES:
The timings are based on the following load ranges for all ISA/PI bus signals:
1. For 1X–3X buffer strengths (BALE, LA[23:17], SA[19:0], SBHE#, and SD[15:0])

Strength	Min Load (pF)	Max Load (pF)
3X	65	160
2X	45	110
1X	10	45

2. For 1X–4X buffer strengths (MEMR#, MEMW#, IOR#, and IOW#)

Strength	Min Load (pF)	Max Load (pF)
4X	80	160
3X	65	120
2X	45	80
1X	10	35

3. The buffer strength on the following pins is not programmable and is specified as follows: HLDA, IOCHRDY, IOCS16#, MEMCS16#, ROMCS[1:0]#, FLSHDCS#, and SMRAMCS#: 2X SYSCLK, INTA#, and VGACS#: 3X, HALT#: 4X.

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

ISA-Bus Timings (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 251	IOCHRDY Setup to Tc phi 1 Low	6		ns		2.5.10	
Ct 251a	IOCHRDY Inactive Setup to Tc phi 2 Low	10		ns		2.5.16	
Ct 252	IOCHRDY Hold from Tc phi 1 Low	8		ns		2.5.10	
Ct 259	INTA# Active Delay from Tc phi 2 Low		45	ns		2.5.19	
Ct 260	INTA# Inactive Delay from Teoc phi 1 Low		60	ns		2.5.19	
Ct 261	HRQ Setup to Th phi 1 Low	15		ns		2.5.20	
Ct 262	HRQ Hold from Th phi 1 Low	5		ns			
Ct 263	HLDA Active Delay from Th phi 2 Low		40	ns			
Ct 264	HLDA Inactive Delay from Th phi 2 Low		40	ns			
Ct 265	DMA8/16# Setup to Th phi 2 Low	15		ns			
Ct 266	MASTER# Setup to Th phi 2 Low	15		ns		2.5.22	
Ct 267	REFREQ Setup to Ti or Th phi 1 Low	16		ns		2.5.21	
Ct 268	VGACS# Active Delay from LA[23:17]		39			2.5.6	
Ct 269	VGACS# Inactive Delay from LA[23:17]		41	ns		2.5.6	
Ct 269a	VGACS# Active Delay from Ts phi 2 Low		35	ns		2.5.15	
Ct 269b	VGACS# Inactive Delay from Ts phi 2 Low		41	ns		2.5.15	
Ct 270	ROMCS0#/ROMCS1# Active Delay from Ts phi 2 Low		41	ns		2.5.7	
Ct 271	ROMCSO#/ROMCS1# Inactive Delay from Ts phi 2 Low	0		ns		2.5.7	
Ct 272	ROMCS0#/ROMCS1# Active Delay from MEMR#		41	ns		2.5.5	
Ct 273	ROMCS0#/ROMCS1# Inactive Delay from MEMR#		41	ns		2.5.5	
Ct 274	SMRAMCS# Active Delay from Ts phi 2 Low	5	49	ns		2.5.7	
Ct 275	SMRAMCS# Inactive Delay from Ts or Ti phi 2 Low	5	49	ns		2.5.7	
Ct 275a	TURBO Setup	16		ns			
Ct 276	SD15–0 Valid Delay from IOCHRDY Asserted (External Master)		25	ns		2.5.24b	
Ct 277	SD15–0 Data Invalid Delay from MEMR# Inactive (External Master)	7		ns			
Ct 279	SD15–0 Data Setup to MEMW# Active (External Master)	−45		ns			
Ct 280	SD15–0 Data Hold from MEMW# Inactive (External Master)	0		ns			
Ct 281	SD15–0 Data Setup to IOW# Active (External Master)	0		ns		2.5.24a	

NOTES:
The timings are based on the following load ranges for all ISA/PI bus signals:
1. For 1X–3X buffer strengths (BALE, LA[23:17], SA[19:0], SBHE#, and SD[15:0])

Strength	Min Load (pF)	Max Load (pF)
3X	65	160
2X	45	110
1X	10	45

2. For 1X–4X buffer strengths (MEMR#, MEMW#, IOR#, and IOW#)

Strength	Min Load (pF)	Max Load (pF)
4X	80	160
3X	65	120
2X	45	80
1X	10	35

3. The buffer strength on the following pins is not programmable and is specified as follows: HLDA, IOCHRDY, IOCS16#, MEMCS16#, ROMCS[1:0]#, FLSHDCS#, and SMRAMCS#: 2X SYSCLK, INTA#, and VGACS#: 3X, HALT#: 4X.

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

ISA-Bus Timings (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 282	BALE Active Delay from Th phi 2 Low (External Master)		45	ns		2.5.22	
Ct 283	BALE Inactive from Th phi 2 Low (External Master)		50	ns			
Ct 284	LA23–17, SA19–0, SBHE# Float to Valid Delay from Th phi 1 (External Master)		54	ns		2.5.22	
Ct 285	LA23–17, SA19–0, SBHE# Valid to Float Delay from Th phi 2 (External Master)		54	ns			
Ct 286	SA19–17 Delay from LA19–17 (DMA Cycle)	0	45	ns		2.5.20	
Ct 287	Command Float to Inactive from Th phi 1 Low (External Master)		50	ns			
Ct 288	SA15–0, LA23–17 Setup to Command Active (External Master)	28		ns		2.5.24a	
Ct 289	SA15–0, LA23–17 Hold After IOR# or IOW# Inactive (External Master)	15		ns			
Ct 290	IOCS16# Active Delay from Valid Address (External Master)		64	ns			
Ct 293	SD15–0 Hold After IOW# Inactive (External Master)	15		ns			
Ct 294	Byte Swap Delay (External Master)	0	72	ns		2.5.22	
Ct 295	IOCHRDY Invalid from Command Active (External Master)		44	ns		2.5.24b	
Ct 296	IOCHRDY Active from phi 2 Low (External Master)		85	ns		2.5.24b	
Ct 298	IOCS16# Inactive from Valid Address (External Master)		110	ns		2.5.24a	

NOTES:
The timings are based on the following load ranges for all ISA/PI bus signals:
1. For 1X–3X buffer strengths (BALE, LA[23:17], SA[19:0], SBHE#, and SD[15:0])

Strength	Min Load (pF)	Max Load (pF)
3X	65	160
2X	45	110
1X	10	45

2. For 1X–4X buffer strengths (MEMR#, MEMW#, IOR#, and IOW#)

Strength	Min Load (pF)	Max Load (pF)
4X	80	160
3X	65	120
2X	45	80
1X	10	35

3. The buffer strength on the following pins is not programmable and is specified as follows: HLDA, IOCHRDY, IOCS16#, MEMCS16#, ROMCS[1:0]#, FLSHDCS#, and SMRAMCS#: 2X SYSCLK, INTA#, and VGACS#: 3X, HALT#: 4X.

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

EFI Clock Timings: 50 MHz Intel486™ SL Microprocessor @ 25 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 101	EFI Period	20		ns		2.5.1	
Ct 102	EFI High Time at 2.0V	7		ns			
Ct 103	EFI Low Time at 0.8V	7		ns			
Ct 104	EFI Rise Time from 0.2 V_{CC} to 0.8 V_{CC}		4	ns			
Ct 105	EFI Fall Time from 0.8 V_{CC} to 0.2 V_{CC}		4	ns			

General Timings: 25 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 111	PWRGOOD Minimum Pulse Width	2/1		EFI/ ISACLK2			1, 2
Ct 111a	PWRGOOD Setup to EFI	5		ns			2
Ct 111b	PWRGOOD Hold Time	10		ns			
Ct 112	CPURESET Minimum Pulse Width	2/1		EFI			1, 2
Ct 112a	CPURESET Setup to EFI	5		ns			1
Ct 112b	CPURESET Hold Time	10		ns			
Ct 113a	STPCLK# Setup to EFI	0		ns			
Ct 113b	STPCLK# Hold Time	30		ns			
Ct 114	SUS_STAT# Pulse Width	1		EFI			
Ct 115	ONCE# Minimum Pulse Width	35		ns			
Ct 115a	ONCE# Setup to EFI	10		ns			
Ct 115b	ONCE# Hold Time	3		ns			
Ct 116a	SMI# Setup to EFI	0		ns			
Ct 116b	SMI# Hold Time	30		ns			
Ct 117a	INTR Setup to EFI	0		ns			
Ct 117b	INTR Hold Time	30		ns			
Ct 118a	NMI Setup to EFI	0		ns			
Ct 118b	NMI Hold Time	30		ns			

NOTES:
1. Testing is done to guarantee the greater of the two, 2 EFI or 1 ISACLK2.
2. All signals are asynchronous inputs to the Intel486 SL CPU. The setup and hold times are specified for test purpose only. The setup and hold times may cover two EFI clock periods in some cases.

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

PI-Bus Timings: 25 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 301	Min Chip Select and Command Setup to PSTART# Active	10		ns		2.5.3	
Ct 302	Min Chip Select and Command Hold from PSTART# Active	38		ns			
Ct 304	Min Read Data Setup Time to PCMD# Inactive	48		ns			
Ct 305	Min Read Data Hold Time from PCMD# Inactive	12		ns			
Ct 307	Max Write Data Valid Delay from PSTART# Active		52	ns			
Ct 308	Min Write Data Invalid Delay from PSTART# Inactive	20		ns			
Ct 309	Min Address Setup Time to PSTART# Active	10		ns			
Ct 310	Min Address Hold Time from PSTART# Active	40		ns			
Ct 311	PSTART# Pulse Width	35		ns			
Ct 312	Min Delay from PSTART# Active to PCMD# Active	20		ns			
Ct 313	Min Delay from PRDY# Active to PCMD# Inactive	65		ns			
Ct 314	Min Delay from PCMD# Inactive to PSTART# Active	0		ns			
Ct 315	PRDY# Hold from PCMD# Inactive	0	20	ns			

NOTE:
1. The minimum load on all pins is 10 pF and maximum load on all pins except address and data is 50 pF. The maximum load on address and data is 150 pF.

External Master Timings: SYSCLK at 8 MHz (Slave CPU)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 321	PW/R# Valid Delay		60	ns		2.5.4	
Ct 325	PSTART# Valid Delay		70	ns			
Ct 326	PCMD# Valid Delay		50	ns			
Ct 327a	PRDY# Setup	5		ns			
Ct 327b	PRDY# Hold	25		ns			

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

DRAM Mode Timings: 25 MHz @ 50 pF for 3.3V or 5V—Normal Burst Mode

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 601	tASR	Row Addr Setup to RAS# Active	12		ns		2.5.25	1, 2
Ct 605	tRAH	Row Addr Hold from RAS# Active	22		ns			1, 2
Ct 609	tASC	Col Addr Setup to CAS# Active	12		ns			1, 2
Ct 613	tCAH	Col Addr Hold from CAS# Active	18		ns			1, 2
Ct 617	tRCD	RAS# to CAS# Delay	30		ns			2, 3
Ct 621	tCSH	CAS# Hold Time from RAS# Active	75		ns			2
Ct 625	tRSH	RAS# Hold Time from CAS# Active	30		ns			2
Ct 629	tWCS	WE# Setup to CAS# Active (Write)	15		ns			1, 2
Ct 633	tWCH	WE# Hold from CAS# Active (Write)	28		ns			1, 2
Ct 637	tRCS	WE# Inactive Setup to CAS# Active (Read)	12		ns			1, 2
Ct 641	tRCH	WE# Inactive Hold from CAS# Inactive (Read)	14		ns			1, 2
Ct 645	tWDS	Write Data Setup to CAS# Active	3		ns			1, 2
Ct 649	tWDH	Write Data Hold from CAS# Active	20		ns			1, 2
Ct 653	tRAC	Access Time from RAS# Active	55		ns			1, 2, 3
Ct 657	tCAC	Access Time from CAS# Active	19		ns			1, 2, 3
Ct 661	tRDH	Read Data Hold from CAS# Inactive	0		ns			1, 2
Ct 665	tRAS	RAS# Active Pulse Width	65		ns			2, 3
Ct 669	tCAS	CAS# Active Pulse Width	25		ns			2, 3
Ct 673	tRP	RAS# Precharge Pulse Width	65		ns			2, 3
Ct 677	tCP	CAS# Precharge Pulse Width	30		ns			2
Ct 681	tPSW	PARx# Setup to CAS# Active (Write)	3		ns			1, 2
Ct 685	tPHW	PARx# Hold from CAS# Active (Write)	20		ns			1, 2
Ct 689	tPVR	PARx# Valid from CAS# Active (Read)	19		ns			1, 2
Ct 693	tPHR	PARx# Hold from CAS# Inactive (Read)	0		ns			1, 2
Ct 702	tCSR	CAS# Setup to RAS# Active (DRAM Refresh)	20		ns		2.5.26	2
Ct 703	tCHR	CAS# Hold from RAS# Active (DRAM Refresh)	20		ns			2
Ct 704	tWSR	WE# Setup to RAS# Active (DRAM Refresh)	13		ns			1, 2
Ct 705	tWHR	WE# Hold from RAS# Active (DRAM Refresh)	13		ns			1, 2

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

DRAM Mode Timings: 25 MHz @ 50 pF for 3.3V or 5V—Normal Burst Mode (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 710	tRSF	RAS# Pulse Width in Suspend Refresh Mode	160		ns		2.5.26a	2
Ct 711	tCSRS	CAS# Setup to RAS# Active (Self Refresh)	30		ns			2
Ct 712	tCHRS	CAS# Hold from RAS# Active (Self Refresh)	40		ns			2
Ct 720	tAA	Access Time from Column Address (Read)	32		ns			1, 2, 3

NOTES:
1. Buffer strengths for MA, MD, PD and WE are programmed to x3 for the timings specified. Timings for other buffer strengths can be derived from derating curves.
2. Buffer strengths for RAS# and CAS# are programmed to x5 for the timings specified. Timings for other buffer strengths can be derived from derating curves.
3. Parameters tRCD, tRP and tRAS are programmable.
4. For buffer strength programming, please refer to the Intel486 SL Microprocessor SuperSet Programmer's Reference Manual.

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DRAM Mode Timings: 25 MHz @ 50 pF for 3.3V or 5V—Fast Burst Mode

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 601	tASR	Row Addr Setup to RAS# Active	12		ns		2.5.25	1, 2
Ct 605	tRAH	Row Addr Hold from RAS# Active	18		ns			1, 2
Ct 609	tASC	Col Addr Setup to CAS# Active	12		ns			1, 2
Ct 613	tCAH	Col Addr Hold from CAS# Active	18		ns			1, 2
Ct 617	tRCD	RAS# to CAS# Delay	30		ns			2, 3
Ct 621	tCSH	CAS# Hold Time from RAS# Active	58		ns			2
Ct 625	tRSH	RAS# Hold Time from CAS# Active	30		ns			2
Ct 629	tWCS	WE# Setup to CAS# Active (Write)	15		ns			1, 2
Ct 633	tWCH	WE# Hold from CAS# Active (Write)	28		ns			1, 2
Ct 637	tRCS	WE# Inactive Setup to CAS# Active (Read)	12		ns			1, 2
Ct 641	tRCH	WE# Inactive Hold from CAS# Inactive (Read)	14		ns			1, 2
Ct 645	tWDS	Write Data Setup to CAS# Active	3		ns			1, 2
Ct 649	tWDH	Write Data Hold from CAS# Active	20		ns			1, 2
Ct 653	tRAC	Access Time from RAS# Active	55		ns			1, 2, 3
Ct 657	tCAC	Access Time from CAS# Active	16		ns			1, 2, 3
Ct 661	tRDH	Read Data Hold from CAS# Inactive	0		ns			1, 2
Ct 665	tRAS	RAS# Active Pulse Width	65		ns			2, 3
Ct 669	tCAS	CAS# Active Pulse Width	20		ns			2, 3
Ct 673	tRP	RAS# Precharge Pulse Width	65		ns			2, 3
Ct 677	tCP	CAS# Precharge Pulse Width	10		ns			2
Ct 681	tPSW	PARx# Setup to CAS# Active (Write)	3		ns			1, 2
Ct 685	tPHW	PARx# Hold from CAS# Active (Write)	20		ns			1, 2
Ct 689	tPVR	PARx# Valid from CAS# Active (Read)	16		ns			1, 2
Ct 693	tPHR	PARx# Hold from CAS# Inactive (Read)	0		ns			1, 2

2.4 Intel486™ SL Microprocessor Timing Specifications (Continued)

DRAM Mode Timings: 25 MHz @ 50 pF for 3.3V or 5V—Fast Burst Mode (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 702	tCSR	CAS# Setup to RAS# Active (DRAM Refresh)	20		ns		2.5.26	2
Ct 703	tCHR	CAS# Hold from RAS# Active (DRAM Refresh)	20		ns			2
Ct 704	tWSR	WE# Setup to RAS# Active (DRAM Refresh)	13		ns			1, 2
Ct 705	tWHR	WE# Hold from RAS# Active (DRAM Refresh)	13		ns			1, 2
Ct 710	tRSF	RAS# Pulse Width in Suspend Refresh Mode	160		ns		2.5.26a	2
Ct 711	tCSRS	CAS# Setup to RAS# Active (Self Refresh)	30		ns			2
Ct 712	tCHRS	CAS# Hold from RAS# Active (Self Refresh)	40		ns			2
Ct 720	tAA	Access Time from Column Address (Read)	28		ns			1, 2, 3

NOTES:
1. Buffer strengths for MA, MD, PD and WE are programmed to x3 for the timings specified. Timings for other buffer strengths can be derived from derating curves.
2. Buffer strengths for RAS# and CAS# are programmed to x5 for the timings specified. Timings for other buffer strengths can be derived from derating curves.
3. Parameters tRCD, tRP and tRAS are programmable.
4. For buffer strength programming, please refer to the Intel486 SL Microprocessor SuperSet Programmer's Reference Manual.

2.5 Intel486™ SL Microprocessor Timing Diagrams

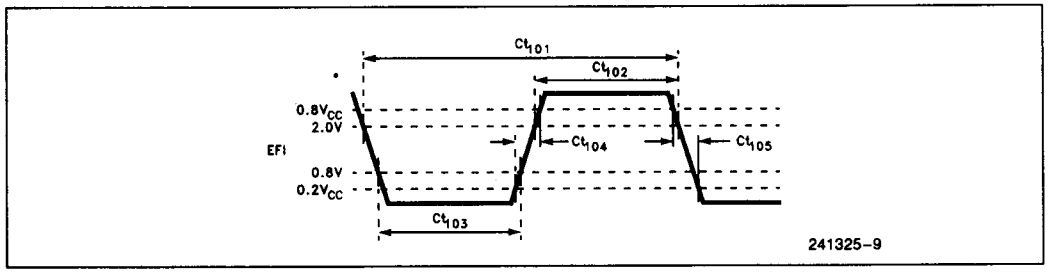


Figure 2.5.1. EFI

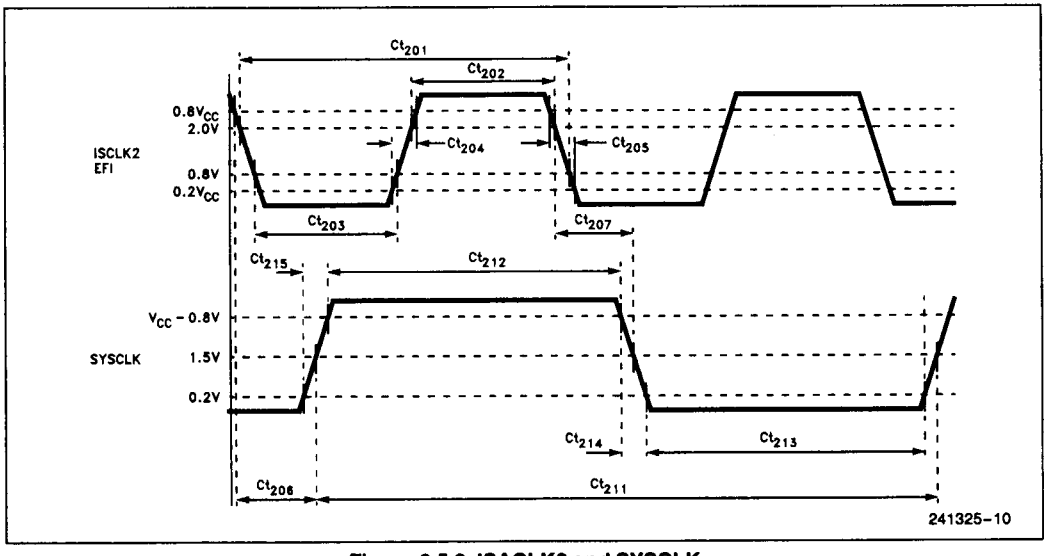


Figure 2.5.2. ISACLK2 and SYSCLK

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

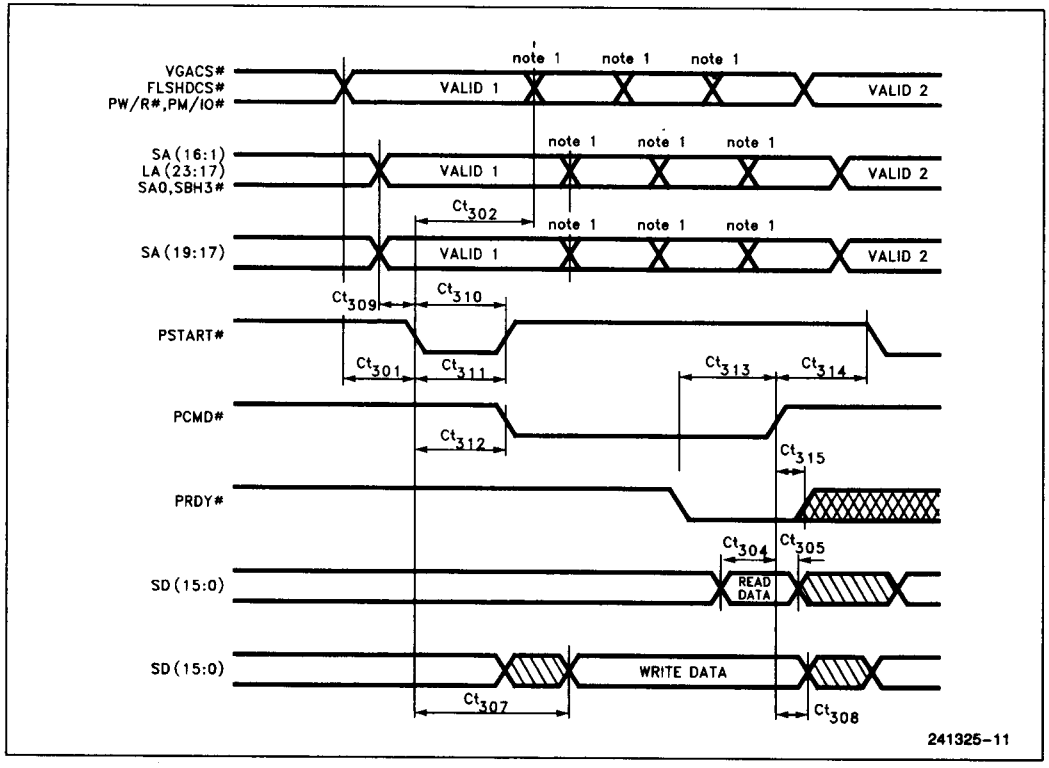


Figure 2.5.3. PI-Bus Timings

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

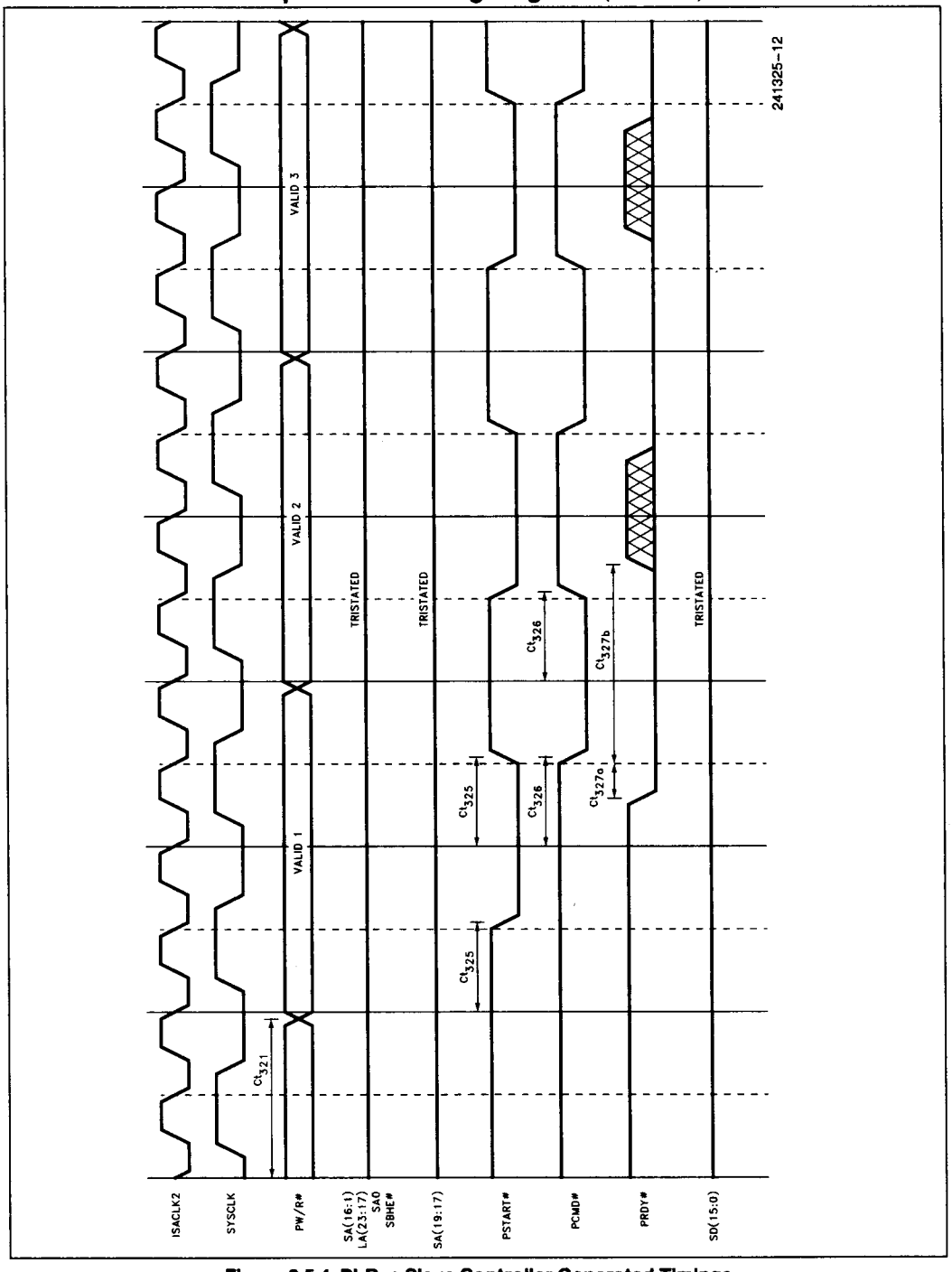


Figure 2.5.4. PI-Bus Slave Controller Generated Timings

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

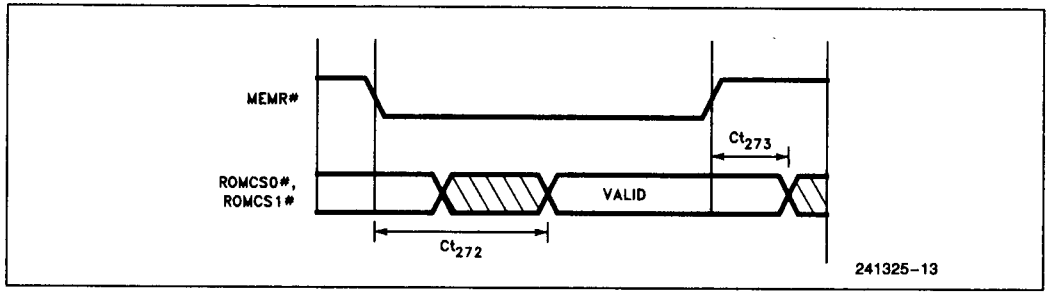


Figure 2.5.5. ISA-Bus Slave Controller Generated Timings (ROMCS0#/1# with Respect to MEMR#)

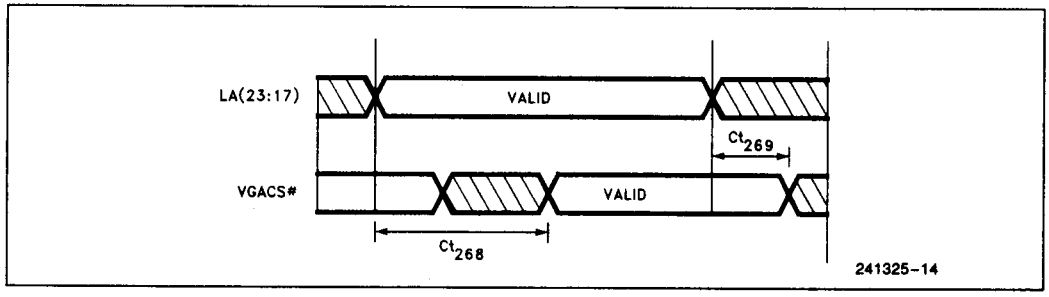


Figure 2.5.6. ISA-Bus Master Controller Generated Timings (VGACS# with Respect to Address)

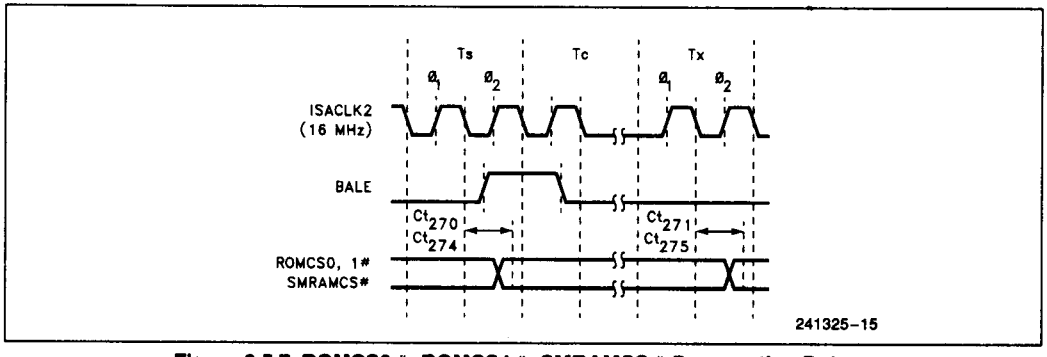


Figure 2.5.7. ROMCS0#, ROMCS1#, SMRAMCS# Propagation Delays

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

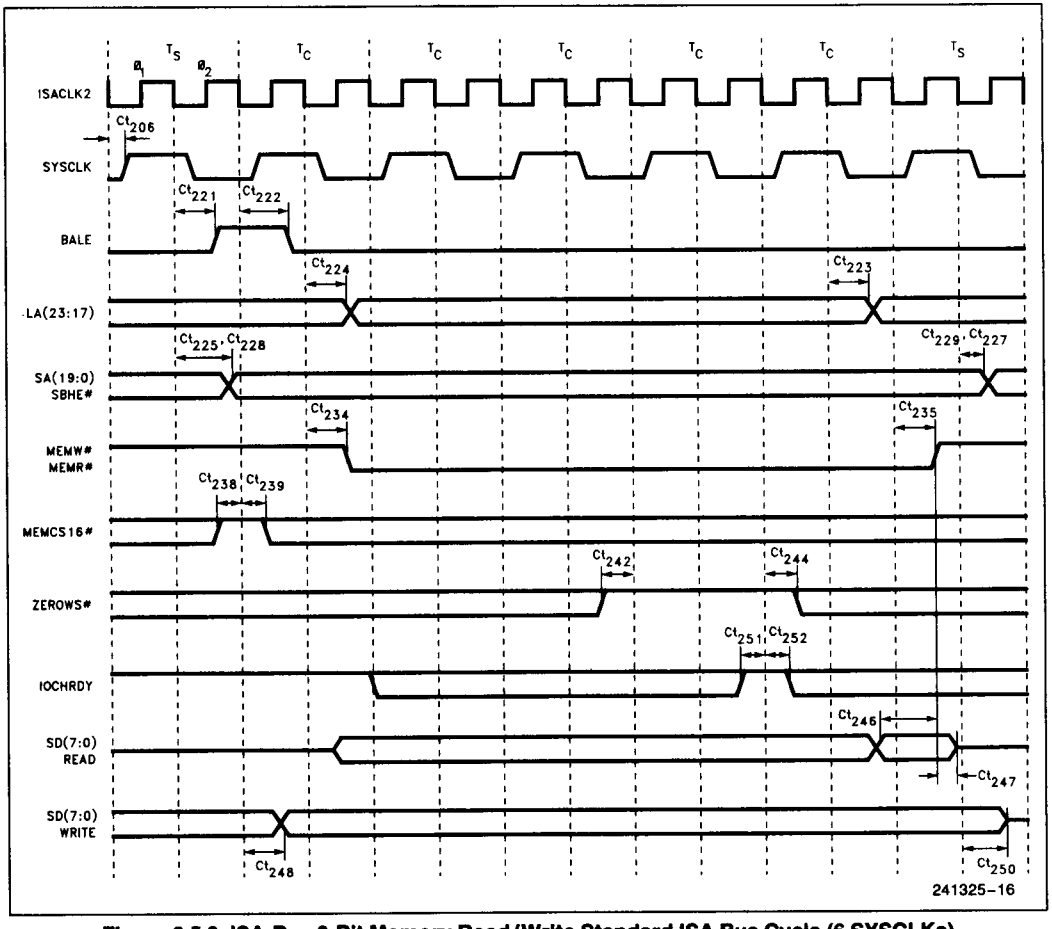


Figure 2.5.8. ISA-Bus 8-Bit Memory Read/Write Standard ISA Bus Cycle (6 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

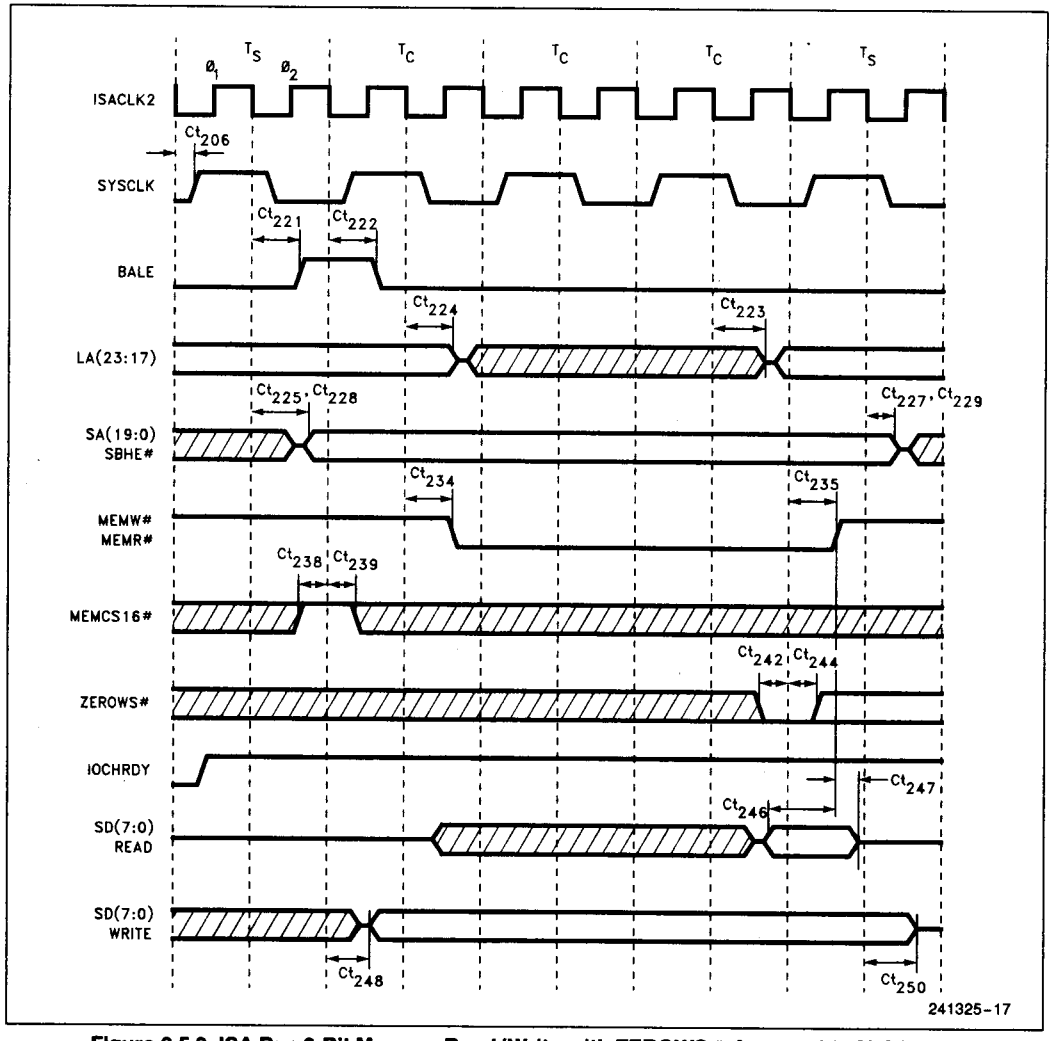


Figure 2.5.9. ISA Bus 8-Bit Memory Read/Write with ZEROWS# Asserted (3 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

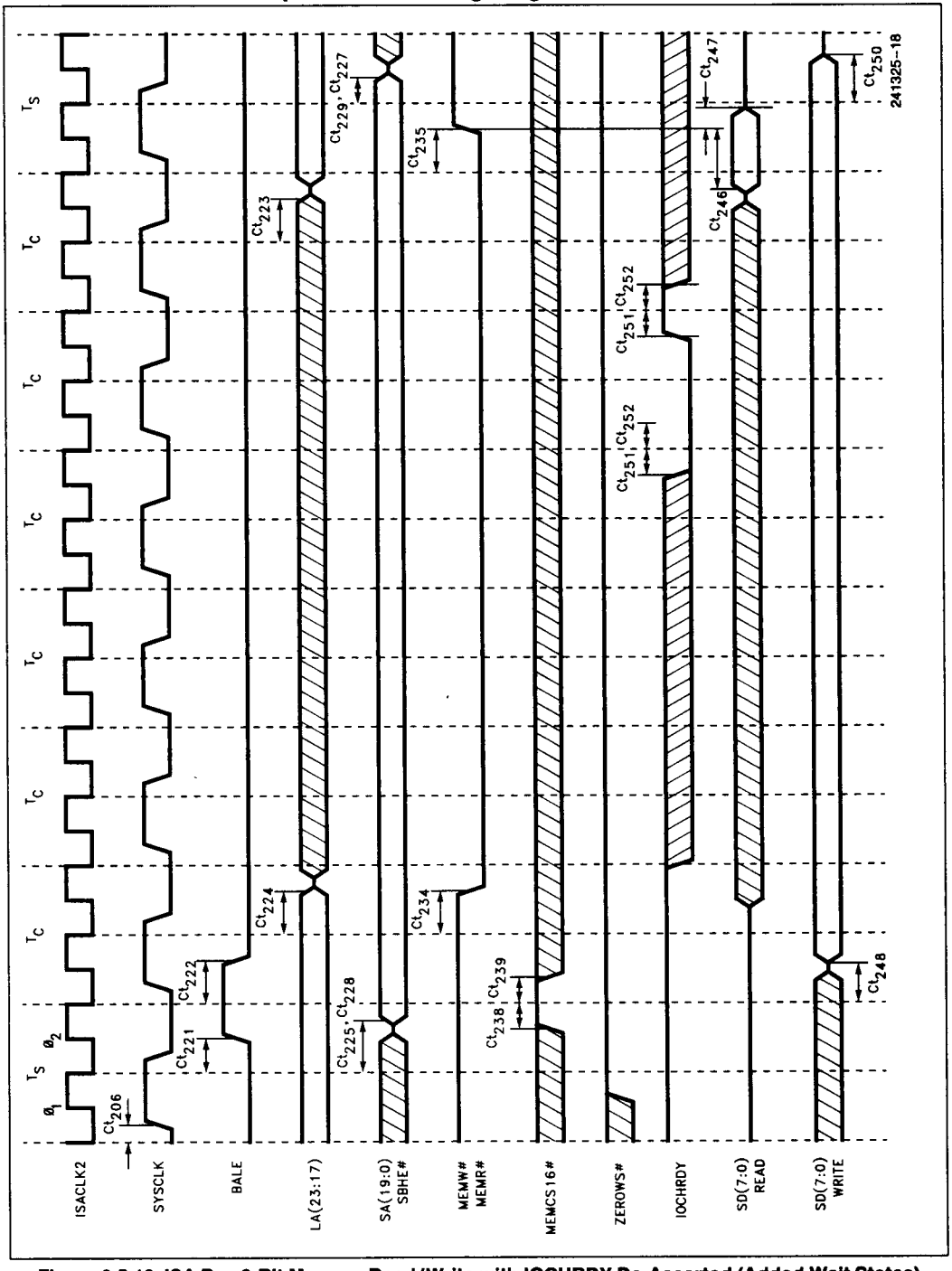


Figure 2.5.10. ISA Bus 8-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

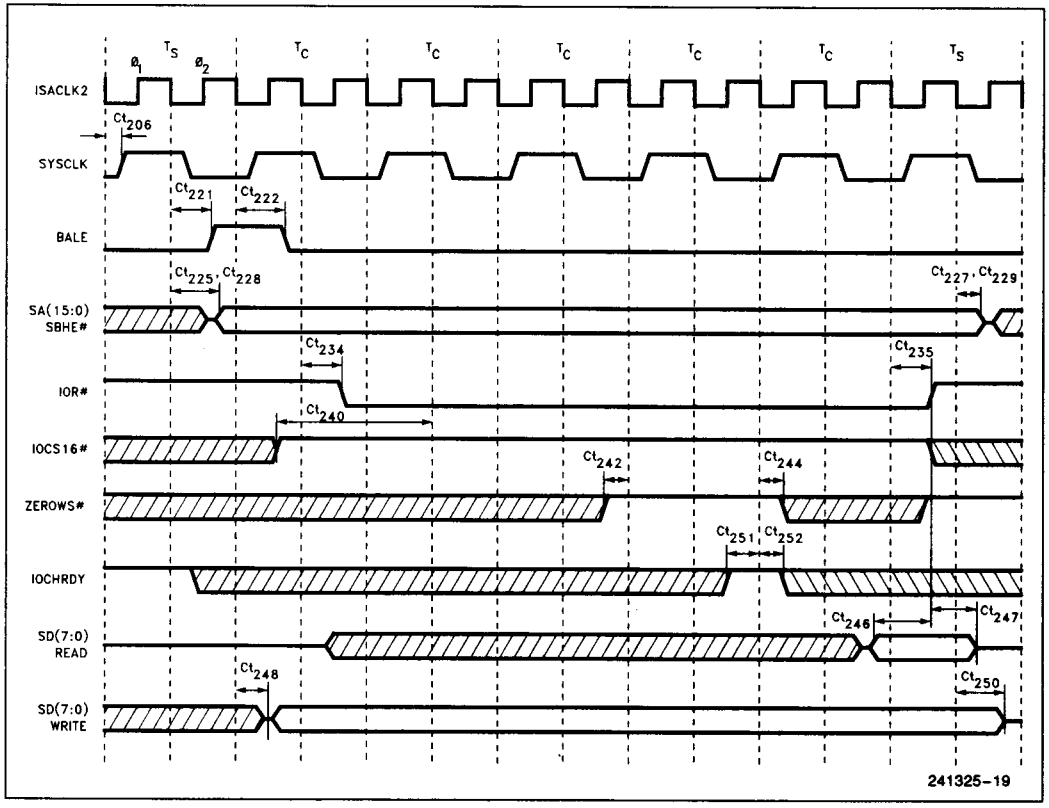


Figure 2.5.11. ISA Bus 8-Bit I/O Read/Write Standard ISA Bus Cycles (6 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

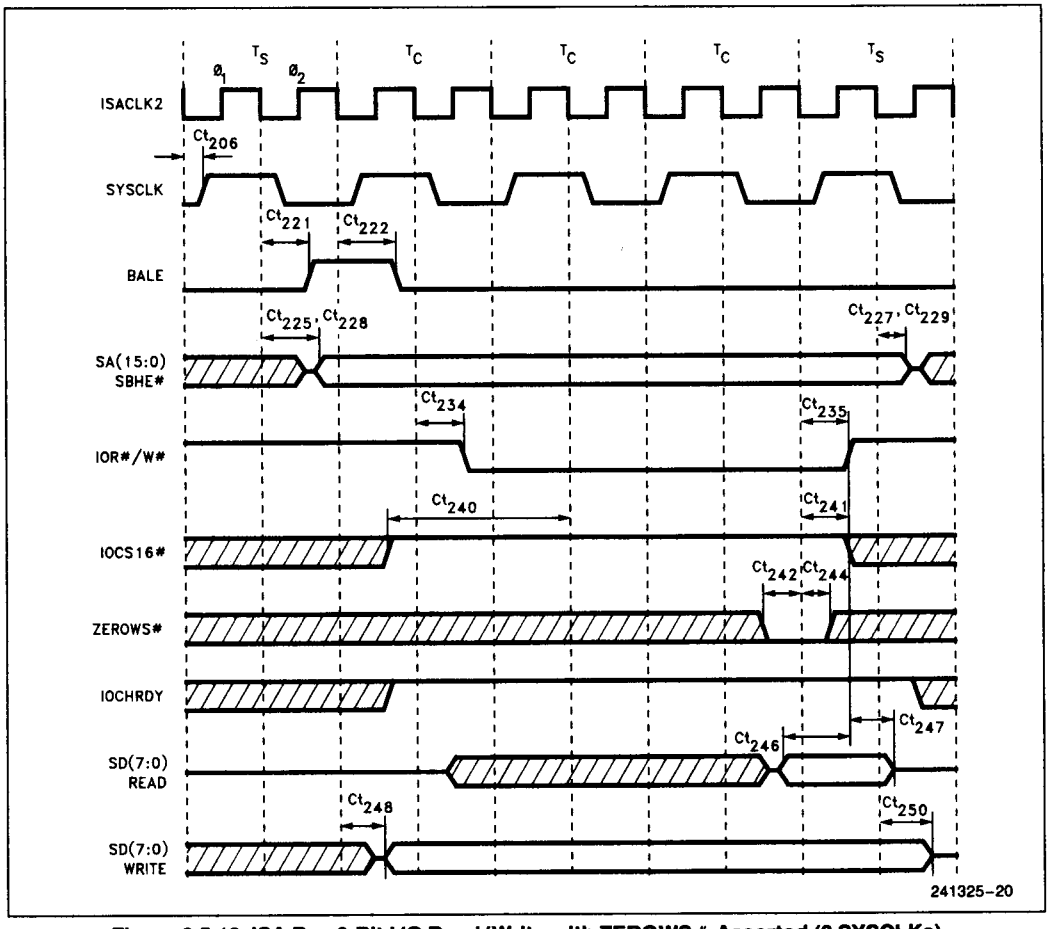


Figure 2.5.12. ISA Bus 8-Bit I/O Read/Write with ZEROWS# Asserted (3 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

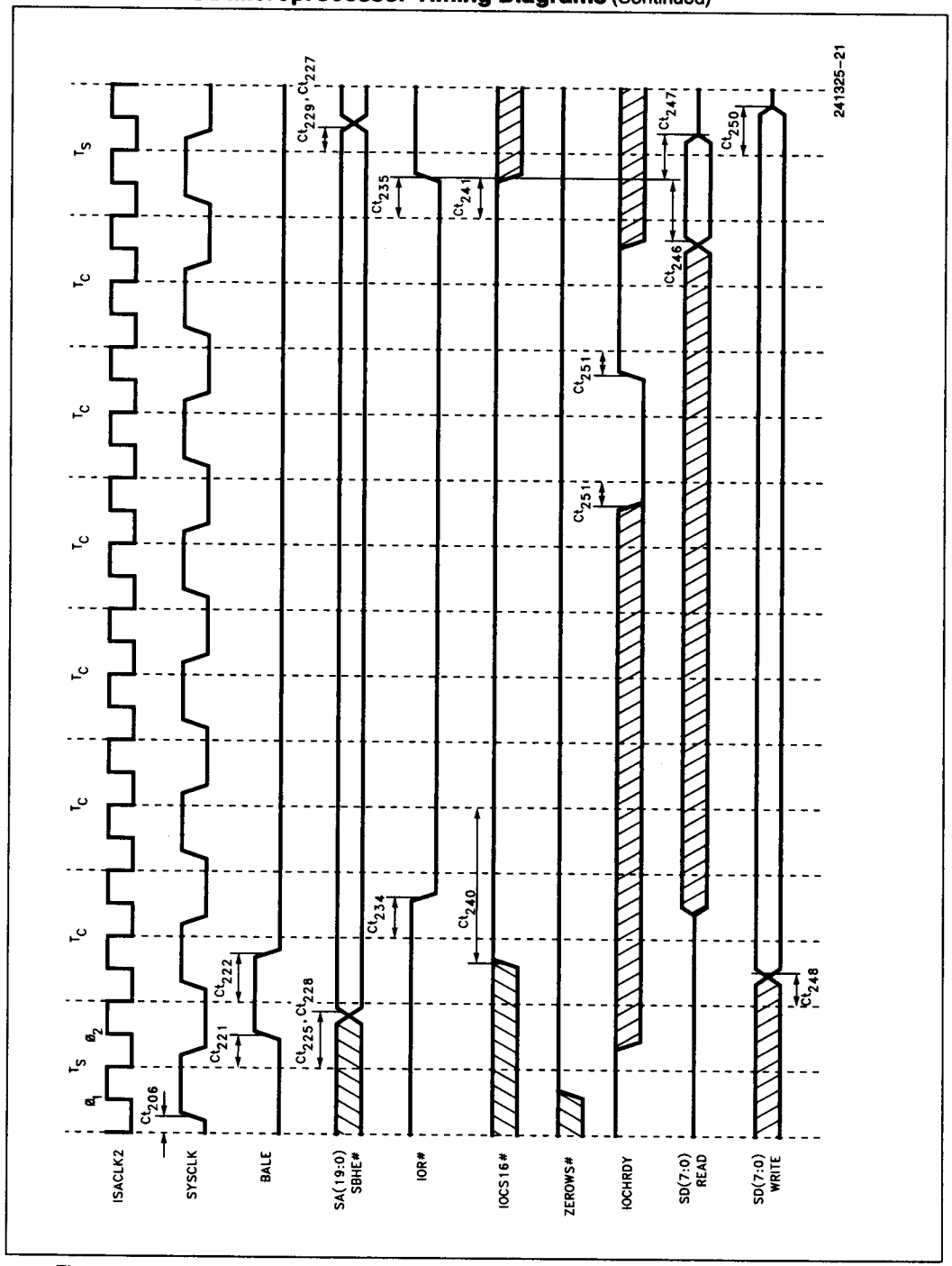


Figure 2.5.13. ISA Bus 8-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

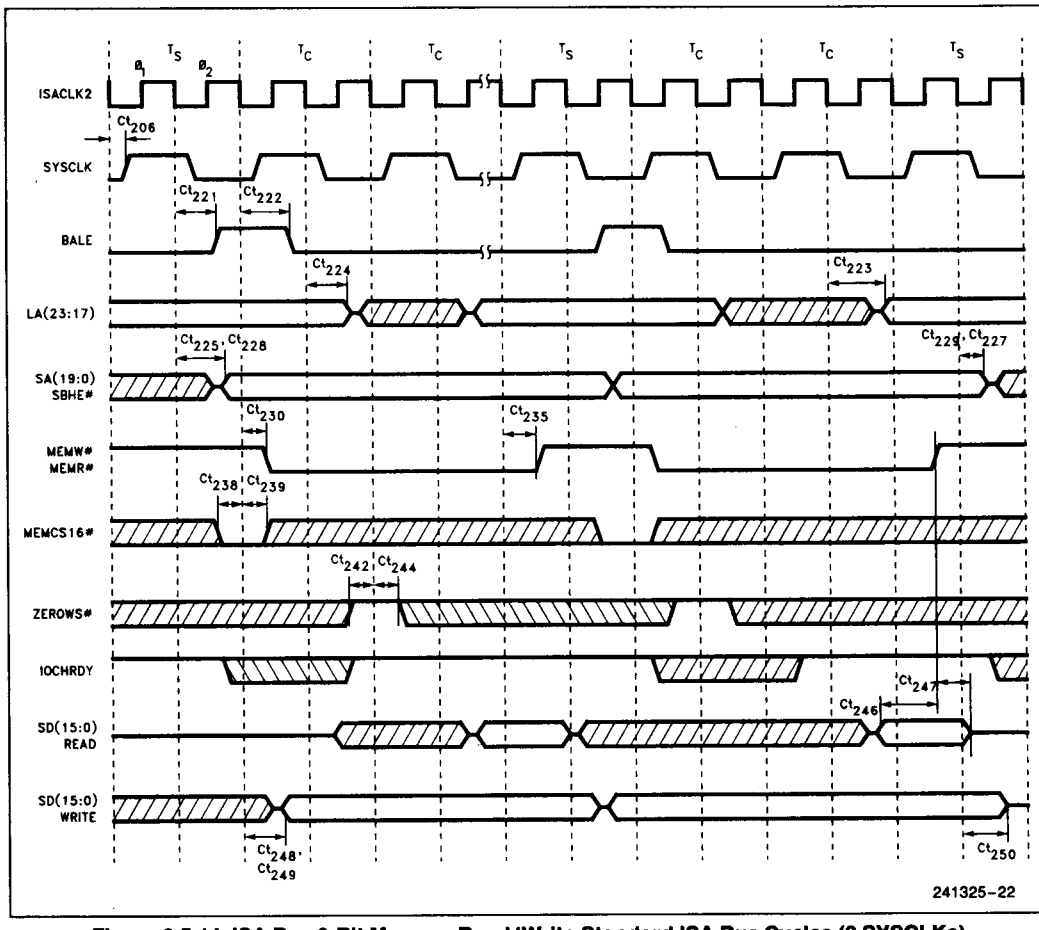


Figure 2.5.14. ISA Bus 8-Bit Memory Read/Write Standard ISA Bus Cycles (3 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

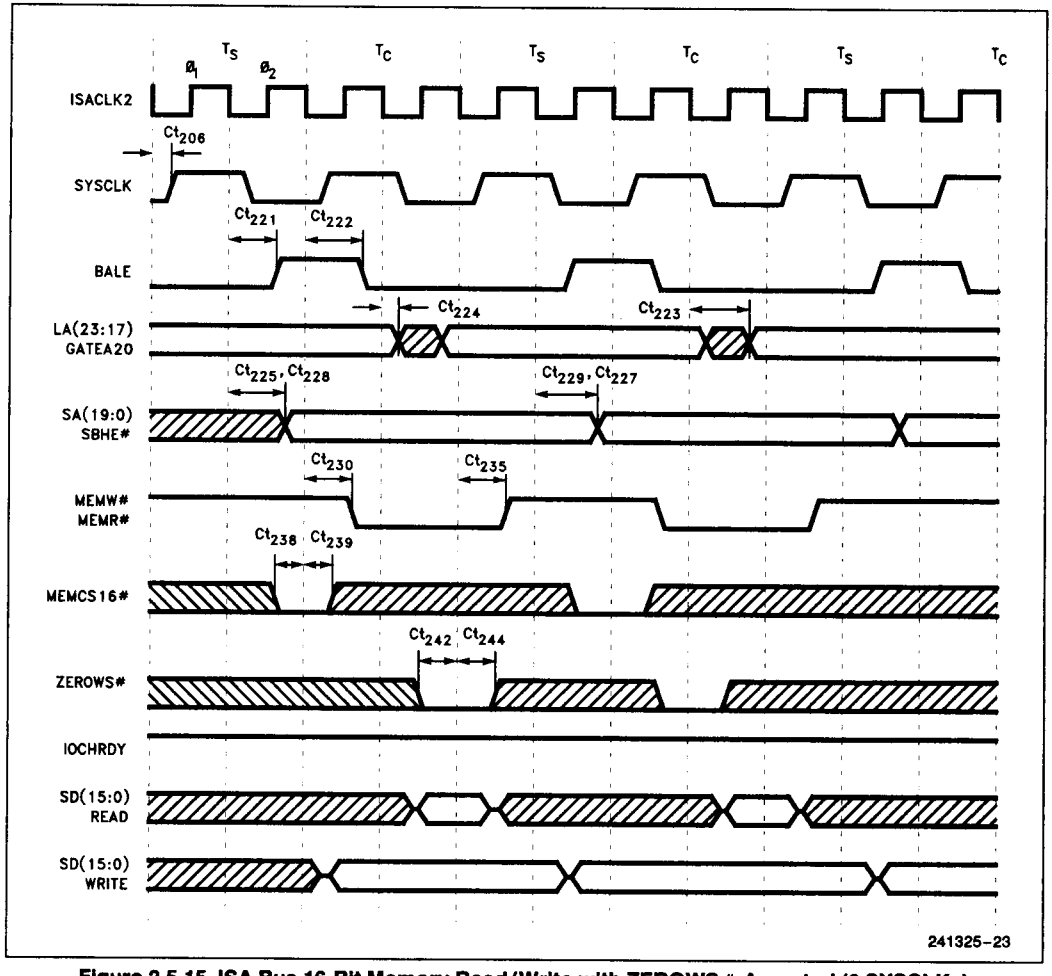


Figure 2.5.15. ISA Bus 16-Bit Memory Read/Write with ZEROWS# Asserted (2 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

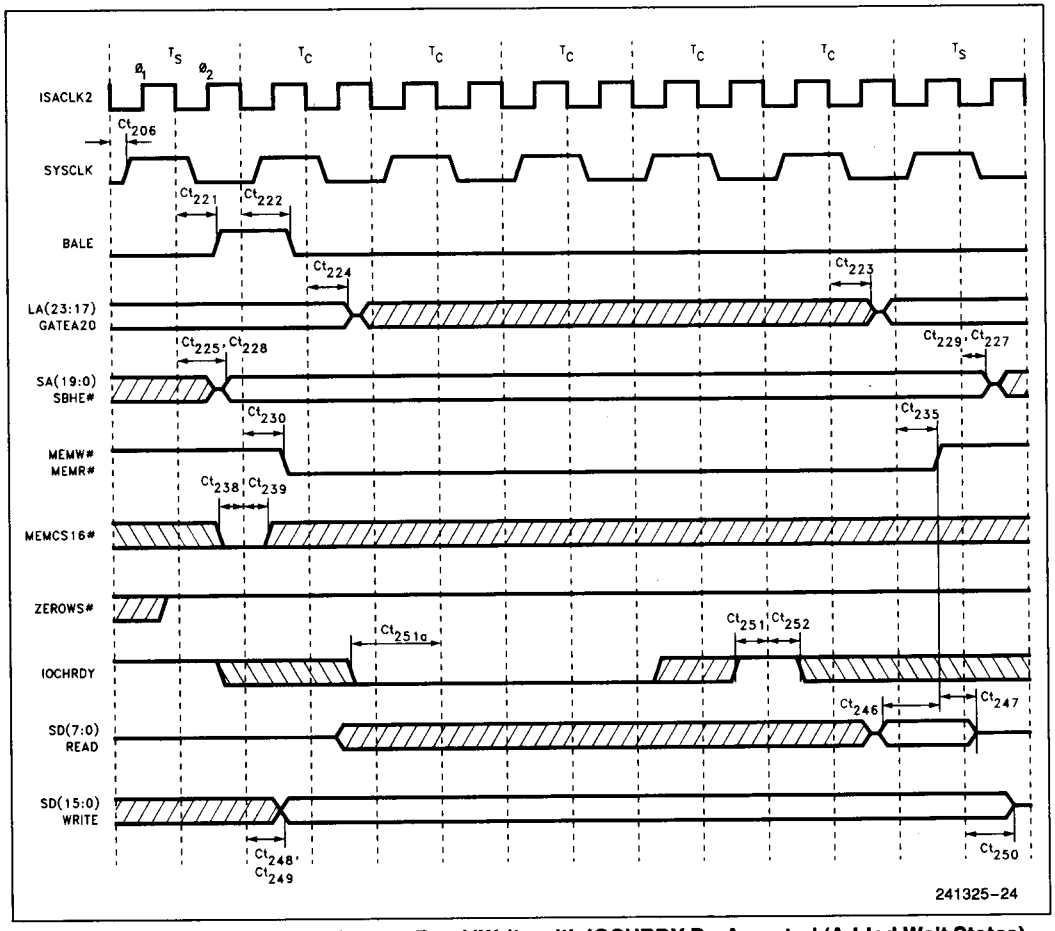


Figure 2.5.16. ISA Bus 16-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

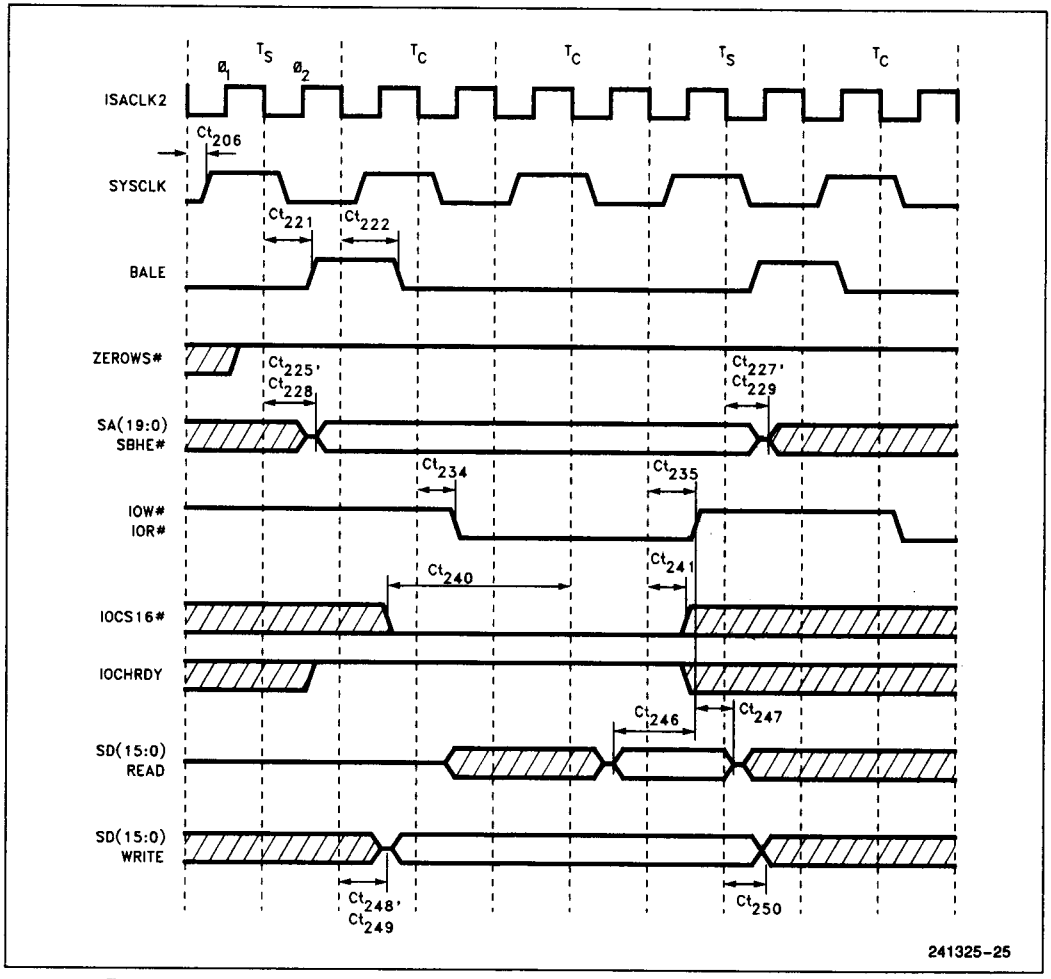


Figure 2.5.17. ISA Bus 16-Bit I/O Read/Write Standard ISA Bus Cycles (3 SYSCLKs)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

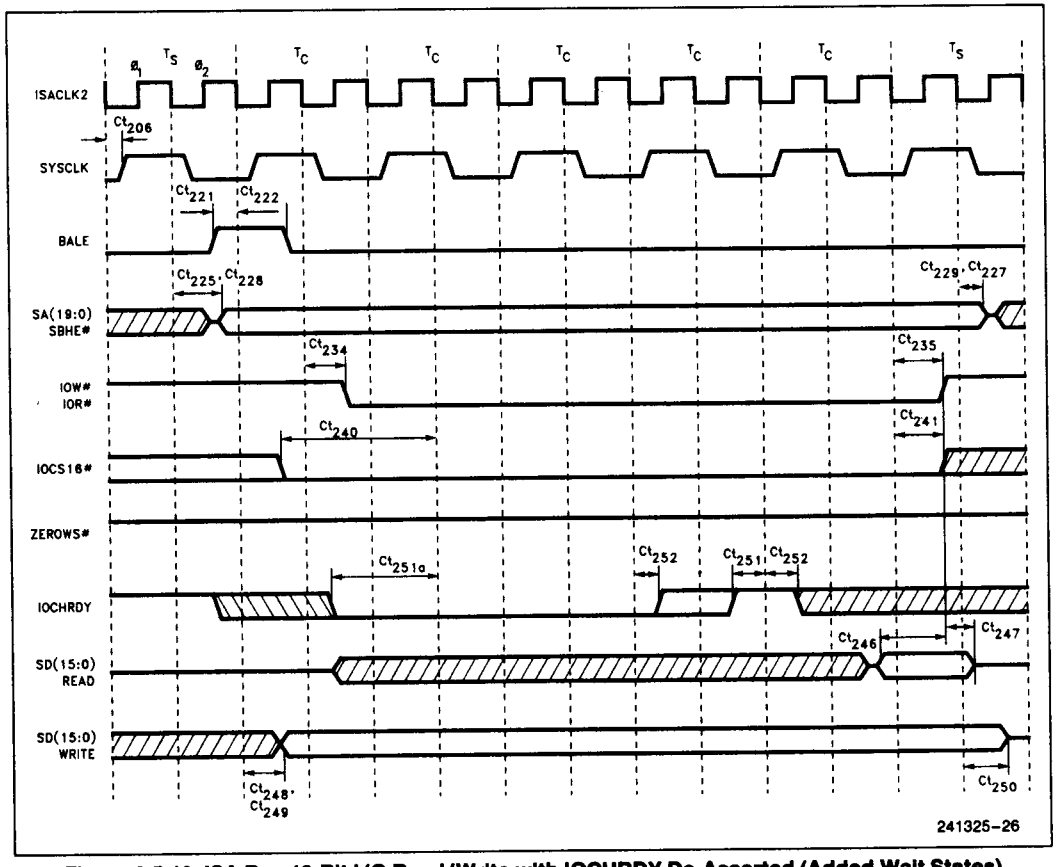


Figure 2.5.18. ISA Bus 16-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

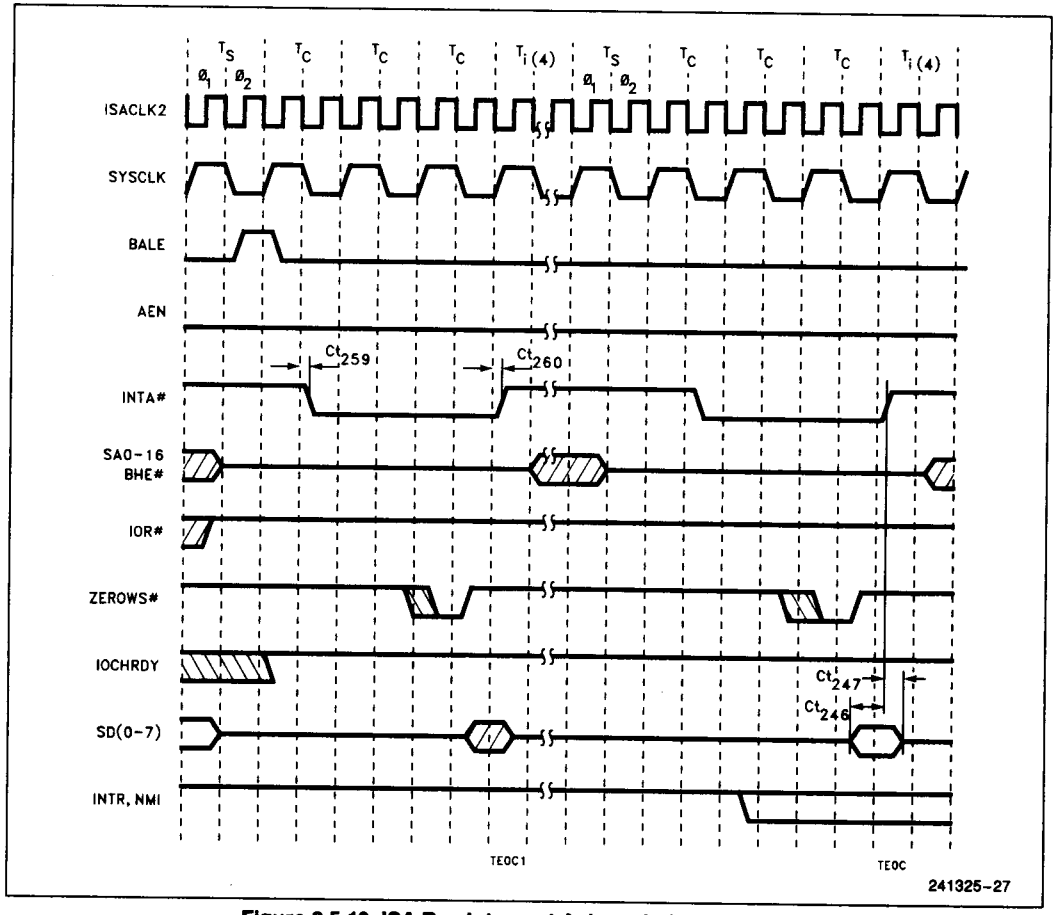


Figure 2.5.19. ISA Bus Interrupt Acknowledge Bus Cycle

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

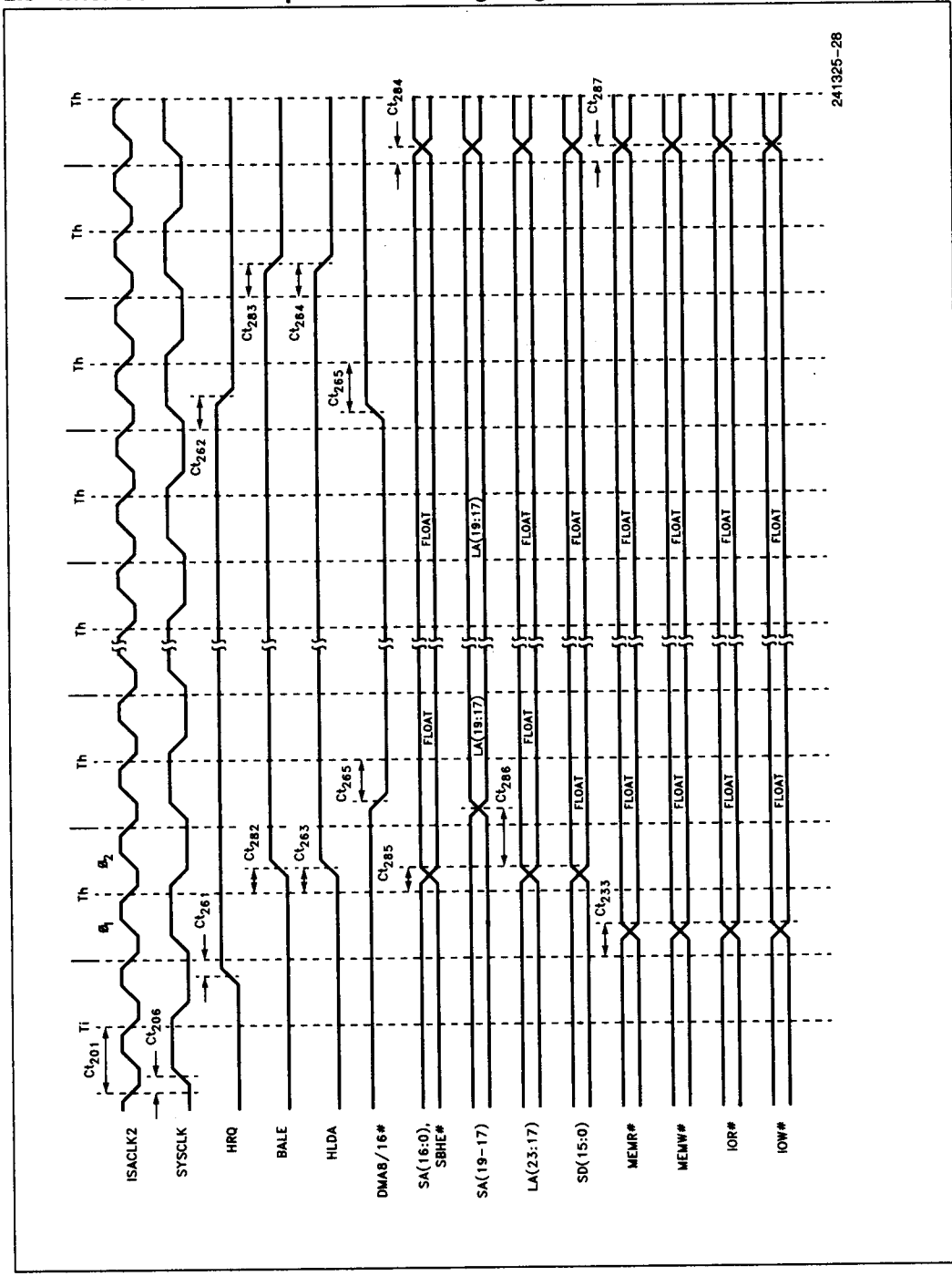


Figure 2.5.20. ISA Bus Controller DMA Cycles

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

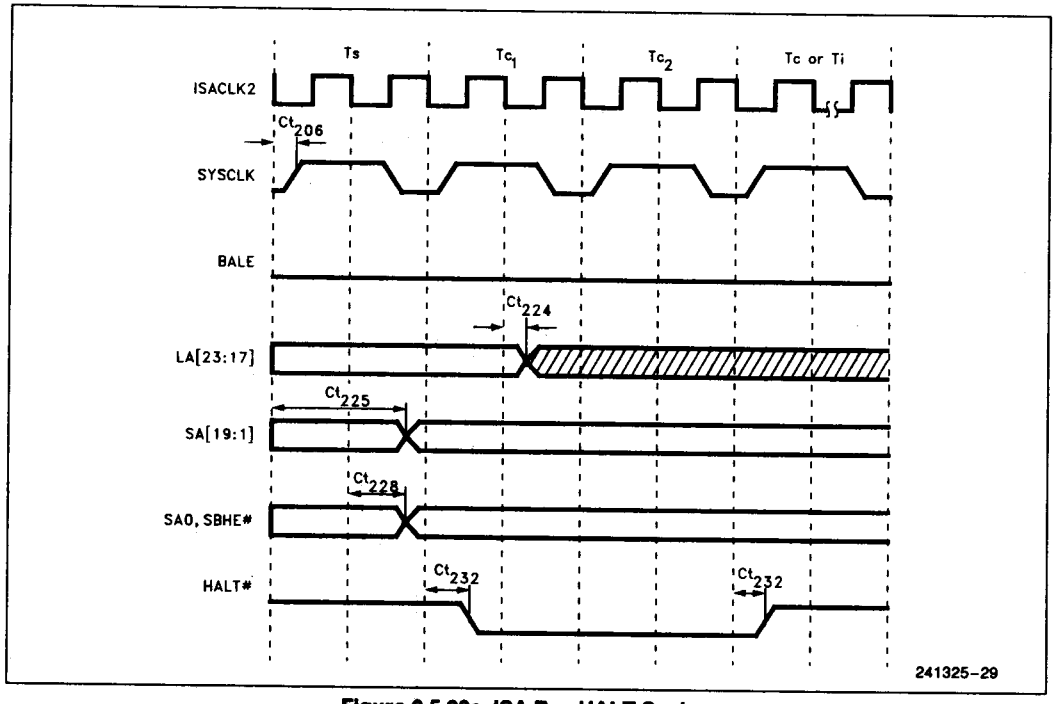


Figure 2.5.20a. ISA Bus HALT Cycles

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

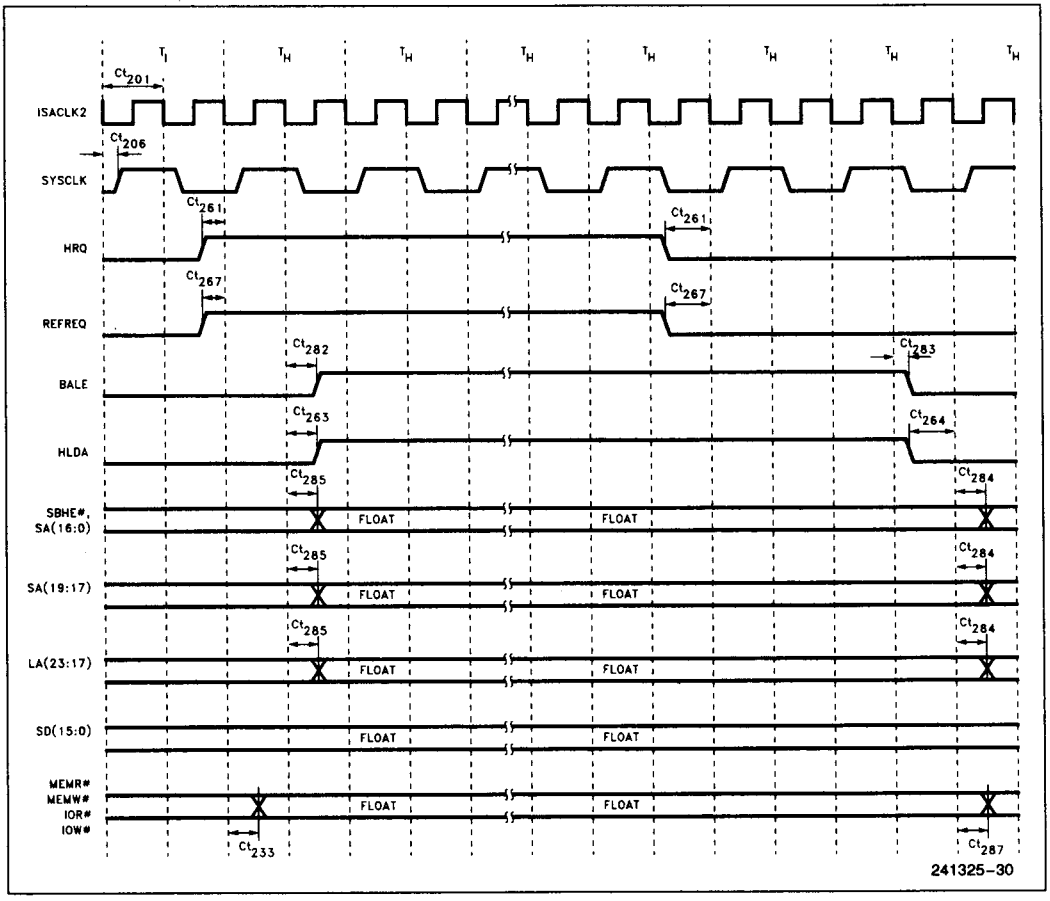


Figure 2.5.21. ISA Bus Controller Refresh Cycle

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

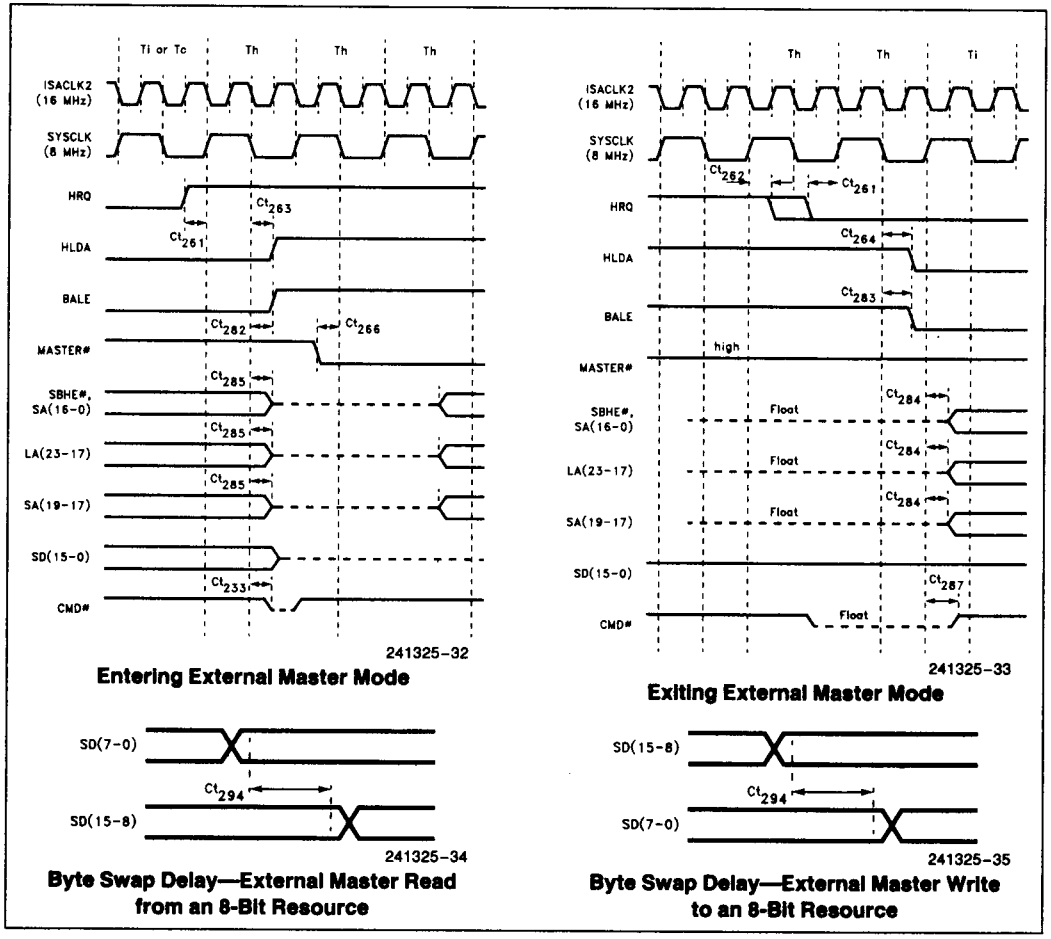


Figure 2.5.22. ISA Bus External Master

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

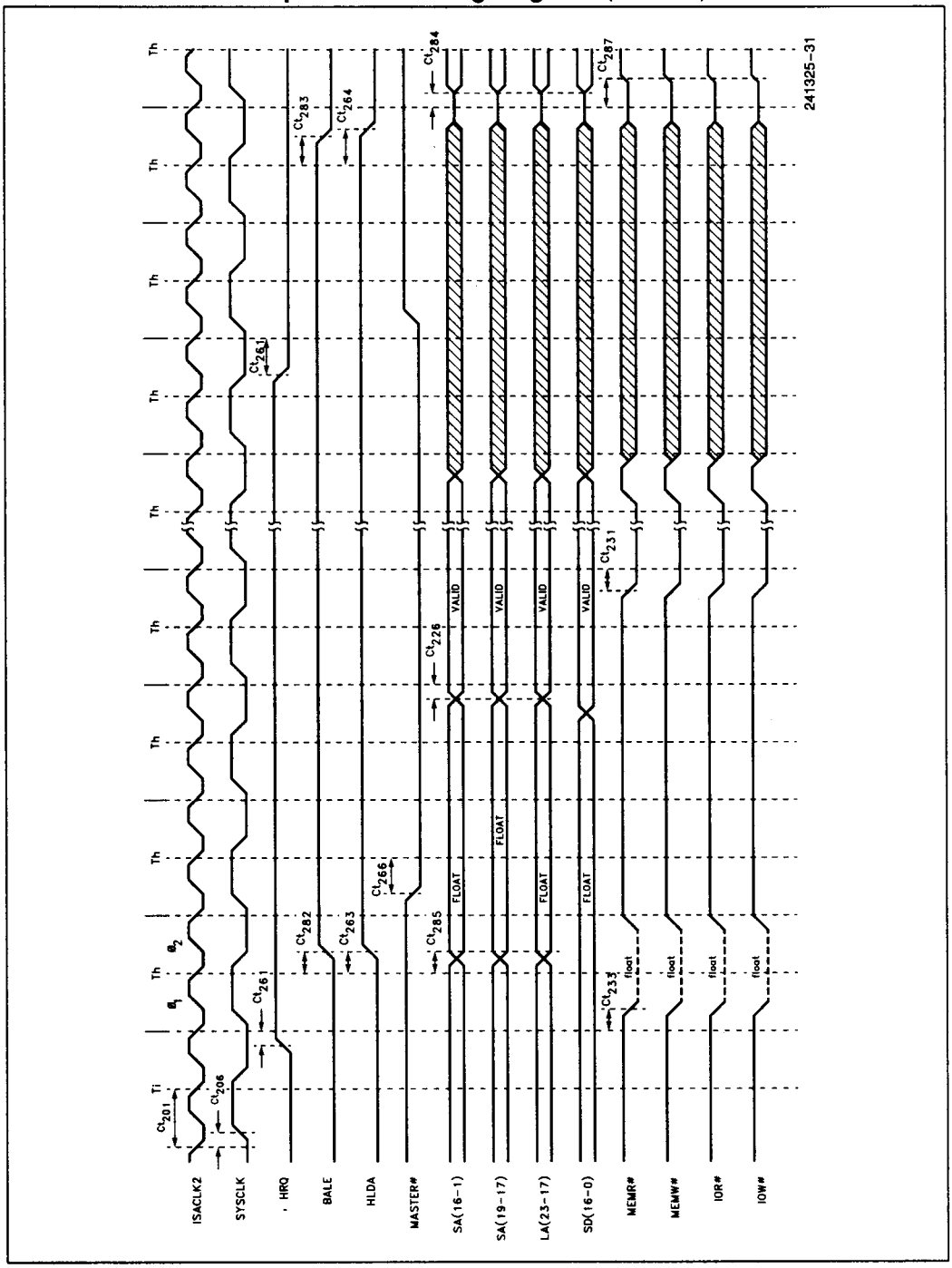


Figure 2.5.23. ISA Bus External Bus Master to Off-Board I/O Ports (No Byte Swapping)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

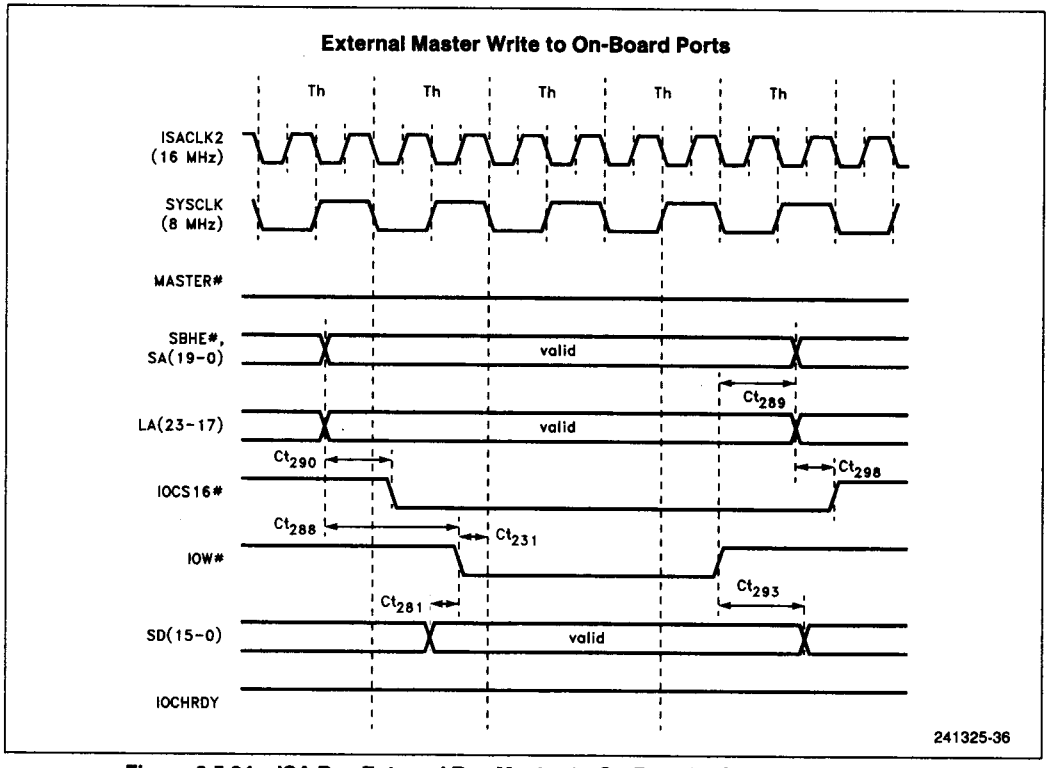


Figure 2.5.24a. ISA Bus External Bus Master to On-Board I/O Ports (Write Only)

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

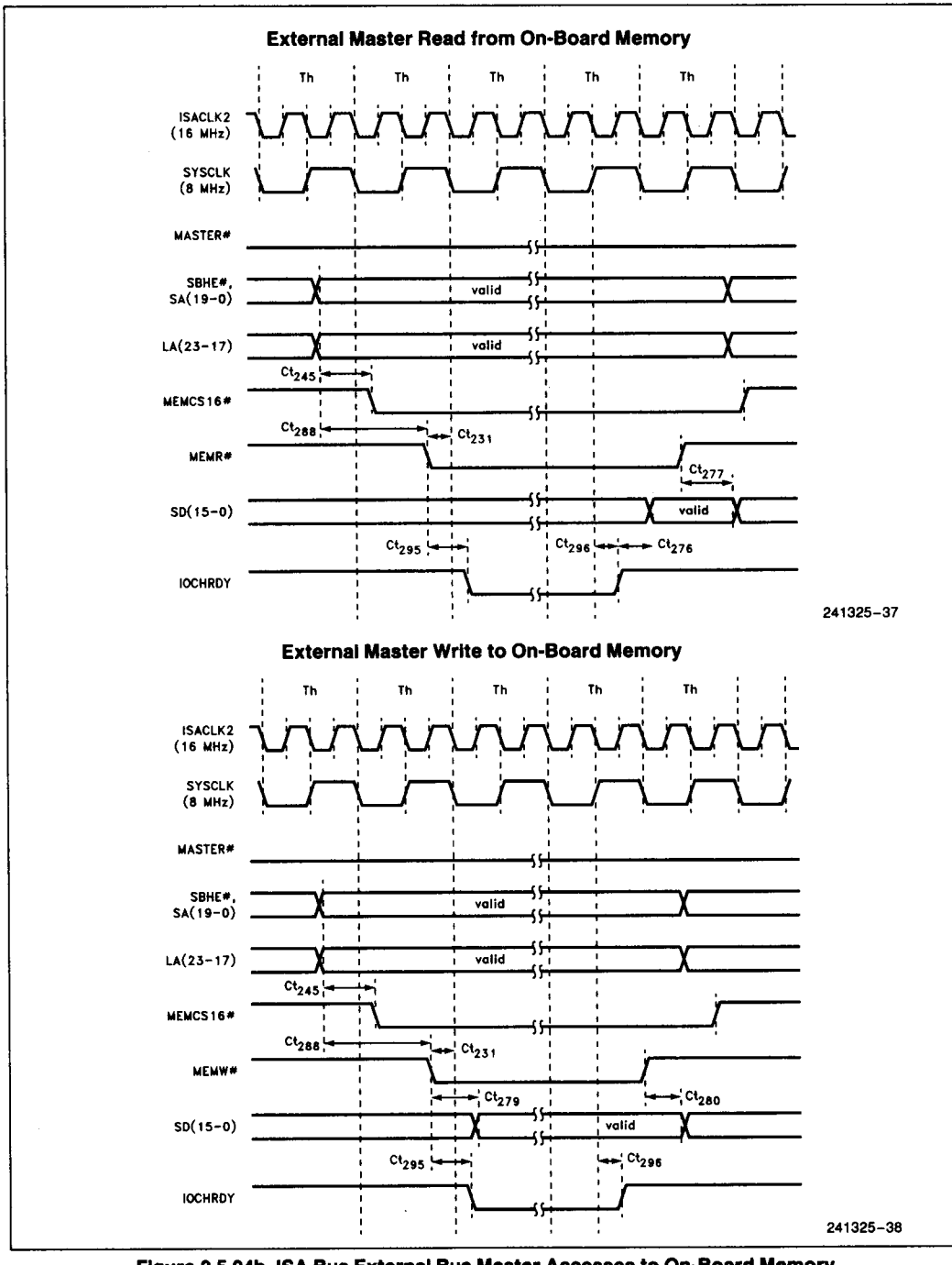


Figure 2.5.24b. ISA Bus External Bus Master Accesses to On-Board Memory

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

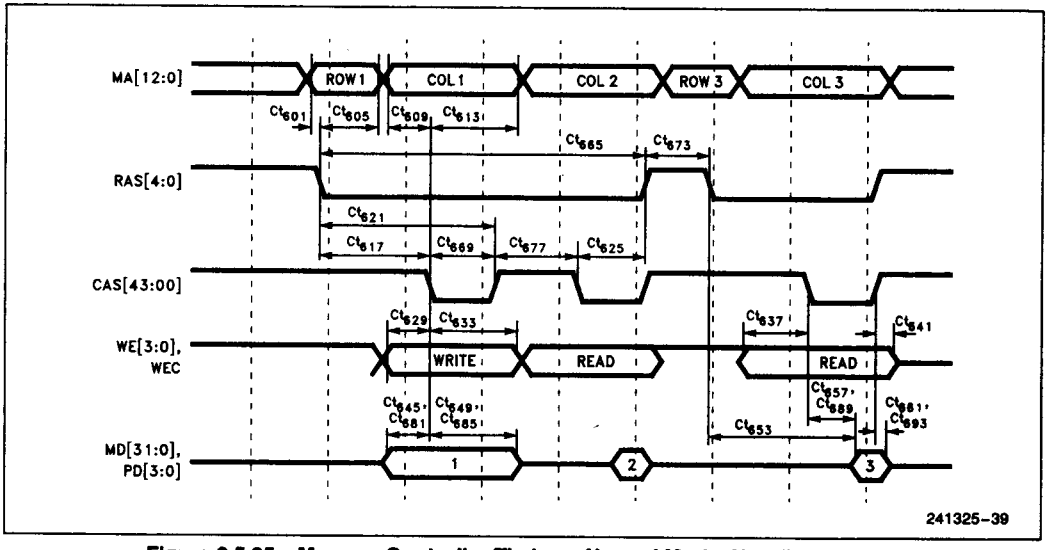


Figure 2.5.25a. Memory Controller Timings: Normal Mode, Non-Burst Cycle

2.5 Intel486™ SL Microprocessor Timing Diagrams (Continued)

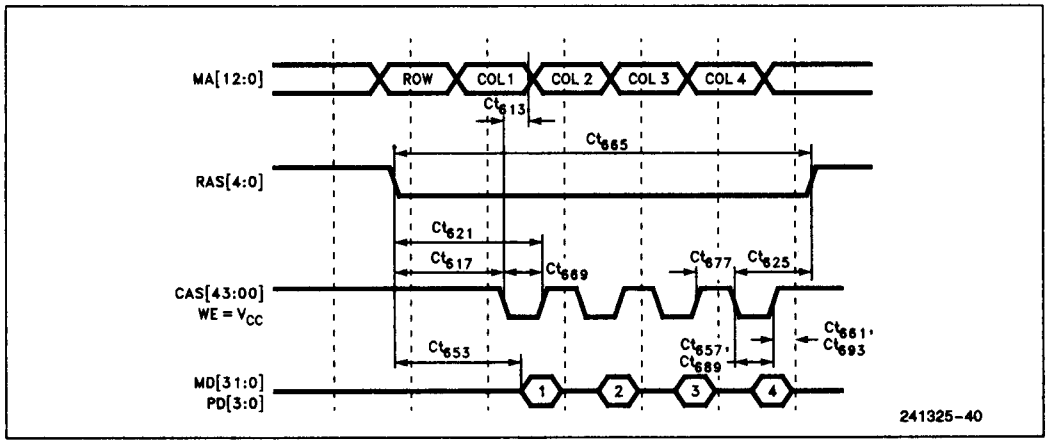


Figure 2.5.25b. Memory Controller Timings: Fast Mode, Burst Cycle

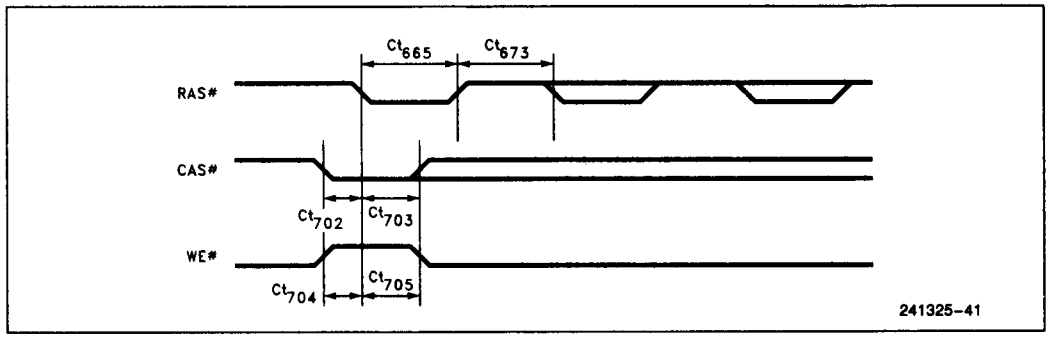


Figure 2.5.26. CAS# before RAS# Refresh Timings

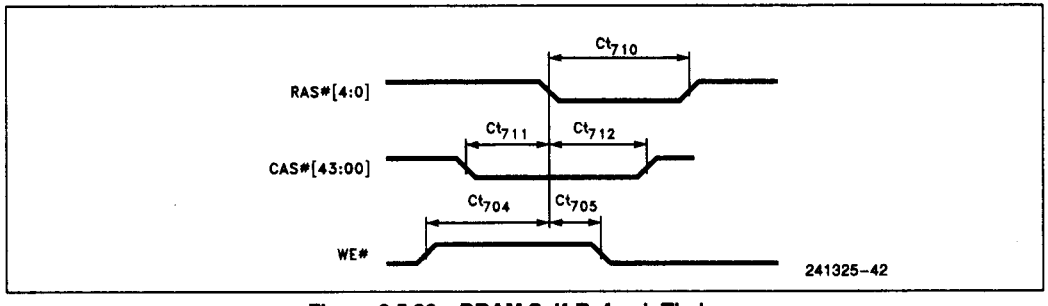


Figure 2.5.26a. DRAM Self-Refresh Timings

2.6 Power Sequencing Specifications

Special attention must be given to turning on the power supplies for a high integration processor system. The 5V power supply must be guaranteed to reach its nominal voltage at the same time or before the 3.3V power supply reaches its nominal voltage. The following timing diagram and timings must be met in order to guarantee proper operation of the high integration processor device.

Table 2.6.1. Power Sequencing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
t_3	PWRGOOD active delay from V_{CC3} = 3.0V and V_{CC5} = 4.5V while both power planes are ramping up.	50		ms	
t_5	PWRGOOD inactive setup time to V_{CC3} = 3.0V and V_{CC5} = 4.5V when both supplies are being turned off.	10		µs	1
t_7	PWRGOOD hold from SUS_STAT# active	5		ns	
t_8	CPURESET and RESETDRV Active Pulse Width	50		ms	
t_9	CPURESET Active Hold from PWRGOOD Active	3		ns	
t_{10}	EFI and ISACLK2 Stable Hold from SUS_STAT# Active		40	ms	
t_{10a}	EFI and ISACLK2 Stable Hold from V_{CC3} = 3V and V_{CC5} = 4.5V	8		µs	2, 3
t_{11a}	V_{CC3} Ramps to 3.0V from Inactive SUS_STAT#		75	ms	
t_{11b}	V_{CC5} Ramps to 4.5V from Inactive SUS_STAT#		75	ms	
t_{11c}	V_{CC5} Turn On Delay from Inactive SUS_STAT#	0		µs	2, 3
t_{11d}	V_{CC3} Turn On Delay from Inactive SUS_STAT#	0		µs	
t_{11e}	V_{CC5} Turn Off Delay from Active SUS_STAT#	0		µs	
t_{11f}	V_{CC3} Turn Off Delay from Active SUS_STAT#	0		µs	
t_{11g}	V_{CC3} = 3.3V Lag from V_{CC5} = 4.5V	0		µs	
t_{20}	CPURESET Active Delay from SUS_STAT# Inactive	125		ms	
t_{21}	Resume CPURESET Pulse Width from 5V or 3.3V Suspend	90		µs	
t_{22}	RESETDRV Inactive Delay from CPURESET Inactive	30		µs	
t_{23}	EFI and ISACLK2 Stable before PWRGOOD Active	10		µs	
t_{23a}	EFI and ISACLK2 Stable before CPURESET Active	10		µs	

NOTES:
1. If a system initialization via RESETDRV (e.g., IDE HD park) is required during power down, 10 ms is recommended for this specification.
2. System should enter suspend refresh before SUS_STAT# is asserted.
3. EFI and ISACLK2 must hold stable (keep oscillator power) for t10a after SUS_STAT# assertion.

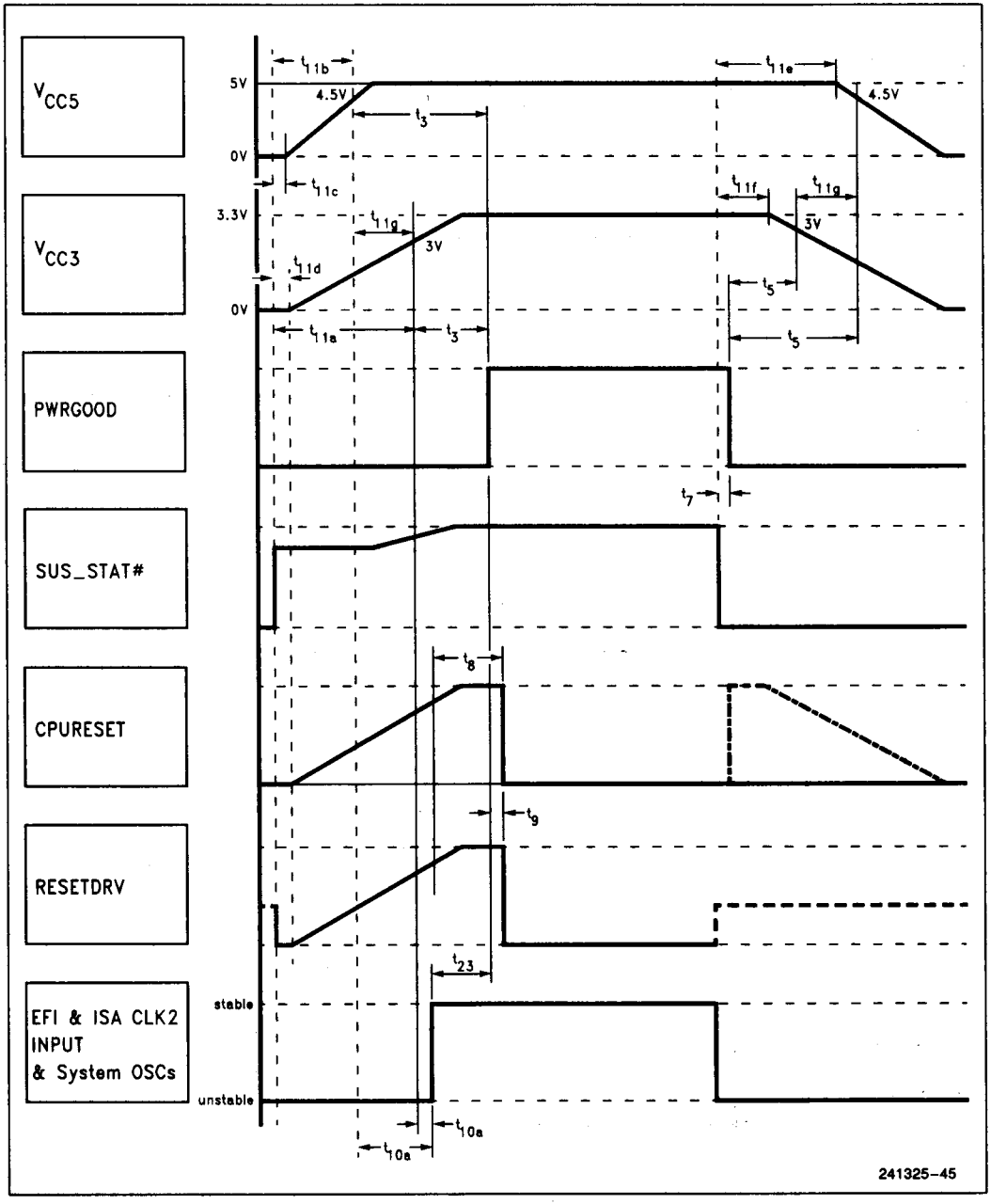


Figure 2.6.1. Power Up/Down Sequencing: 5V Suspend/Resume

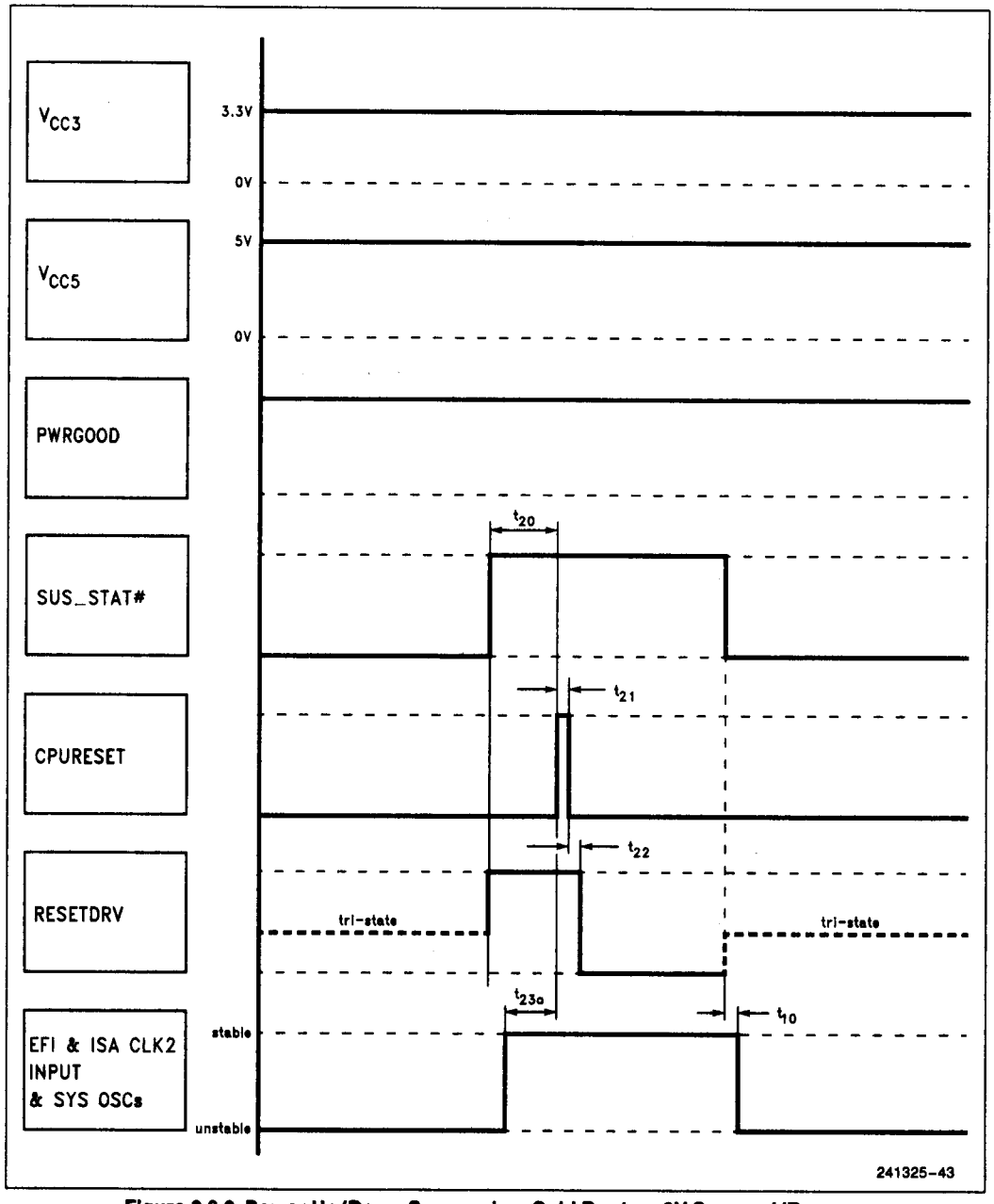


Figure 2.6.2. Power Up/Down Sequencing, Cold Boot on 0V Suspend/Resume

2.7 JTAG Specifications

This section provides the A.C. specifications for the boundary scan (JTAG) testing logic with additional testability features compatible with the IEEE Standard Test Access Port and Boundary Scan Architecture. Table 2.7.1 lists the timing specifications and Figures 2.7.1 through 2.7.3 illustrate the test signals.

Table 2.7.1. Intel486™ SL Microprocessor A.C. Characteristics for Boundary Scan Test Signals

Symbol	Parameter	Min	Max	Unit	Notes
	TCK Frequency		12.5	MHz	1x Clock
t_1	TCK Period	80		ns	1
t_2	TCK High Time @ 2V	20		ns	
t_3	TCK Low Time @ 0.8V	20		ns	
t_4	TCK Rise Time from 0.8V to 2.0V		8	ns	
t_5	TCK Fall Time from 2.0V to 0.8V		8	ns	
t_6	TDI, TMS Setup Time	15		ns	2
t_7	TDI, TMS Hold Time	45		ns	2
t_8	TDO Valid Delay	5	24	ns	5
t_9	TDO Float Delay	5	24	ns	5
t_{10}	All Output (Non-Test) Valid Delay	5	24	ns	5
t_{11}	All Output (Non-Test) Float Delay	5	24	ns	5
t_{12}	All Input (Non-Test) Setup Delay	15		ns	2
t_{13}	All Input (Non-Test) Hold Delay	45		ns	2
t_{14}	TRST# Width	6		TCKs	
t_{15}	TRST# Setup Time	15		ns	3
t_{16}	TRST# Hold Time	35		ns	3

NOTES:
1. TCK period ≥ CPUCLK period.
2. Parameter measured from rising edge of TCK.
3. t15 and t16 are specified for testing purposes. They are to ensure that TRST# is not asserted or deasserted right at the falling edge of TCK.
4. Boundary Scan A.C. Specifications in the above table are target values. They have not been characterized. Therefore they are subject to change.
Parameter measured from falling edge of TCK.

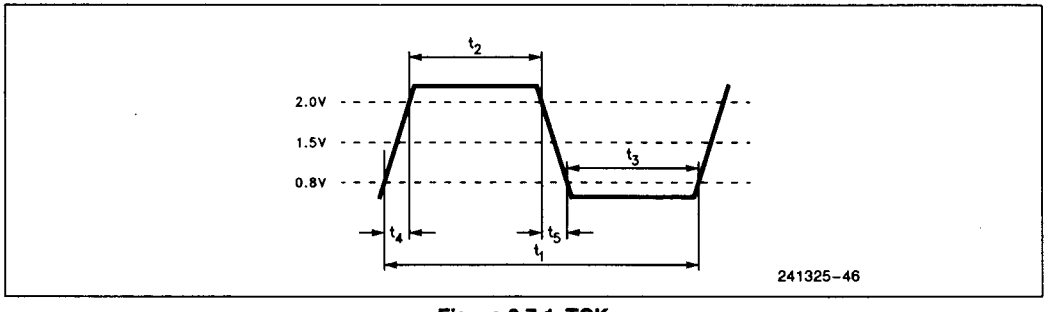


Figure 2.7.1. TCK

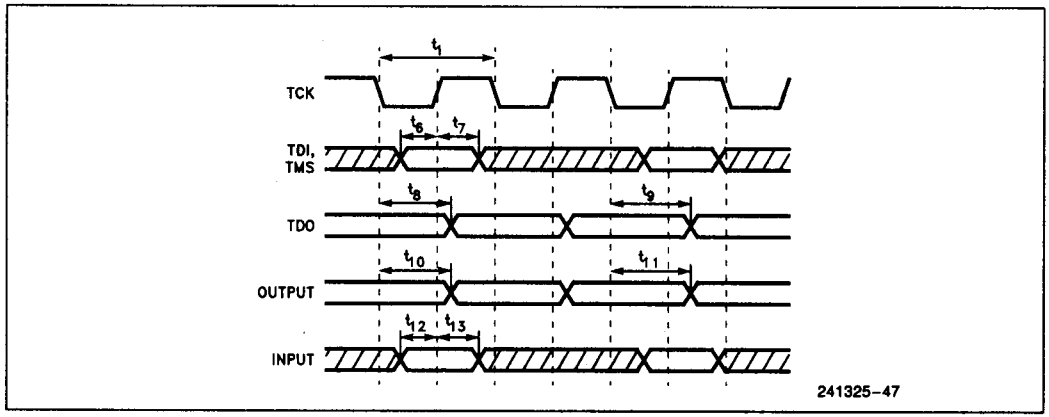


Figure 2.7.2. Boundary Scan Testing Signals

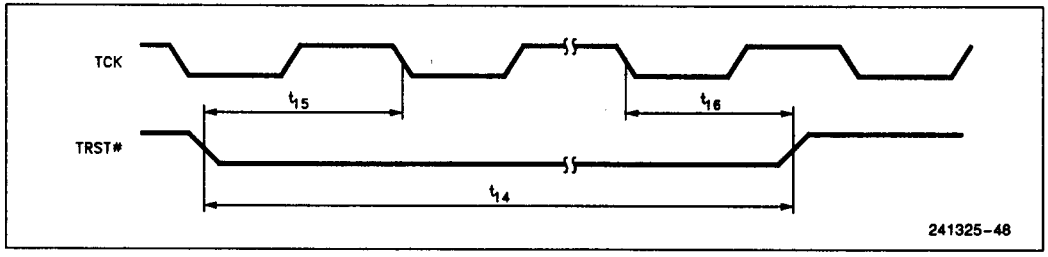


Figure 2.7.3. TRST Timing Diagram

2.8 Capacitive Derating Information

Capacitive derating can be performed based on the derating curves provided in Sections 2.8.1 and 2.8.2. The derating data is provided throughout the capacitive load ranges corresponding to each signal pin and the delays are a function of programmed output buffer strengths and capacitive loads connected to the pin. In order to derate a timing specification, the buffer strength(s) and capacitive load(s) associated with the output signal pin(s) need to be determined first. If derating is to be performed based on the maximum load(s) for the signals involved, Maximum Derating Curves are to be used. If based on minimum load(s), Minimum Derating Curves are to be used. For intermediate loads, both should be used and the longer delay of the two should be selected. For an output-to-output timing specification, a combination of Maximum and Minimum Derating Curves needs to be used in order to ensure an absolute worst case. For those signals that could be either active high or active low, derating should be done for both rise and fall cases and the worst delay will be used to obtain the derated timing specification.

2.8.1 DERATING CURVES FOR PI- AND ISA-BUS SIGNAL PINS

Maximum Derating Curves

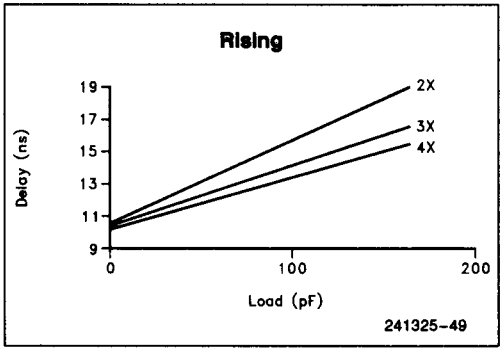


Figure 2.8.1a

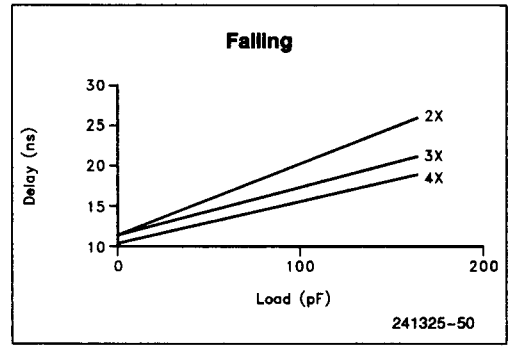


Figure 2.8.1b

Minimum Derating Curves

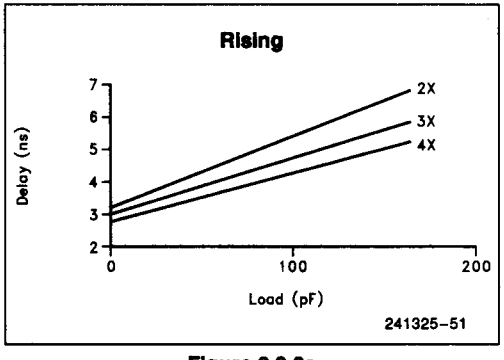


Figure 2.8.2a

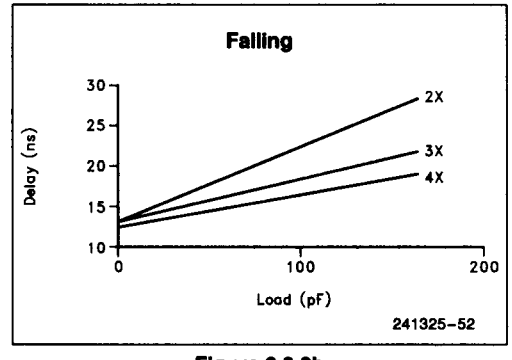


Figure 2.8.2b

2.8.2 DERATING CURVES FOR MEMORY CONTROLLER SIGNAL PINS

Maximum Derating Curves

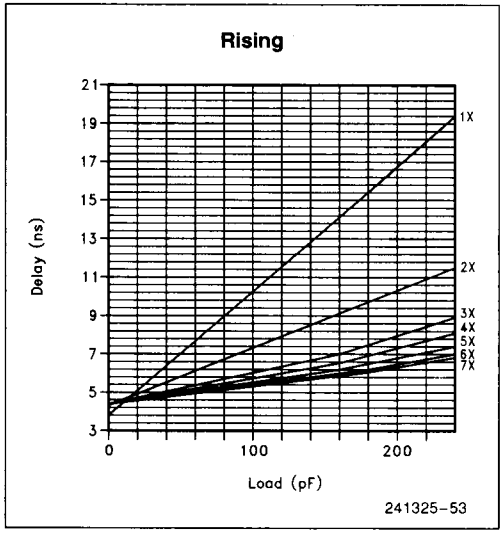


Figure 2.8.3a

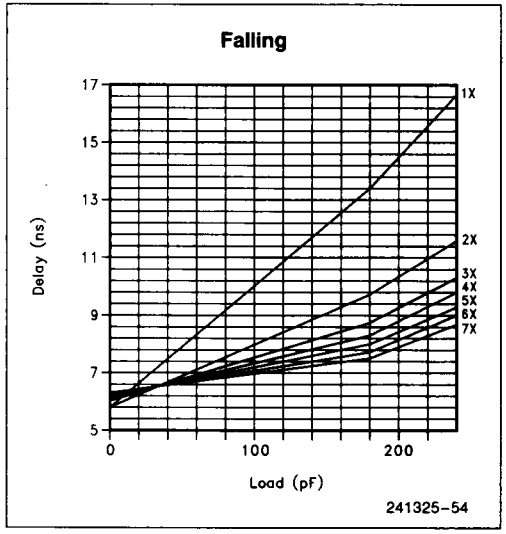


Figure 2.8.3b

Minimum Derating Curves

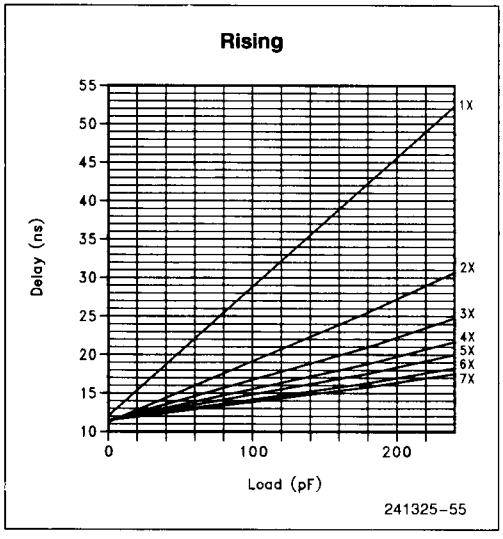


Figure 2.8.4a

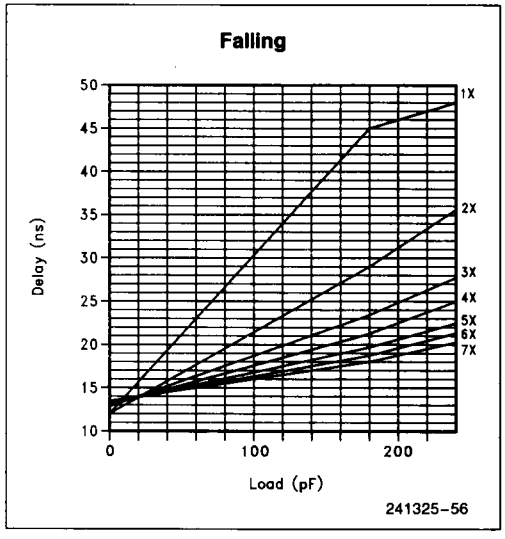


Figure 2.8.4b

3.0 82360SL I/O SPECIFICATIONS

3.1 82360SL I/O Pin Assignment and Signal Characteristics

Section 3.1 provides information for the 82360SL I/O pin assignment with respect to the signal mnemonics. In addition to the package pin out diagrams, a table is provided for easy location of signals. The table lists the device pinouts in the 208-lead SQFP and 196-lead JEDEC PQFP and also includes additional information for the signals and associated pin numbers. A brief explanation of each column of the table is given in Table 3-1.

Table 3-1. Description of the Columns of 82360SL I/O Pin Characteristics

Mnemonic	Signal Name Associated with the Package Pinouts and Signal Descriptions
SQFP	This column lists the pin numbers of the 82360SL I/O in a 208-Lead Quad Flat Package.
PQFP	This column lists the pin numbers of the HRI I/O in a 196-Lead Plastic Quad Flat Package.
Signal Name	This column lists the signal name associated with the package pins.
Type	Indicates whether the pin is an Input (I), an Output (O) or an Input-Output (I/O).
Term	Specifies the internal termination resistor on the pin. This could be an internal pull-up or pull-down resistor value or a hold circuit. To find out whether a pull-up or a pull-down is provided, use the STPCLK (Stop Clock) column for the 82360SL I/O.
Drive	Specifies the drive current I_{OL} and I_{OH} in mA for output (O), and bidirectional (I/O) pins.
Load	This column lists the maximum and minimum specified capacitive loads which the buffer can directly drive in pF for each signal. This is specified for output and input-output pins only.
Susp	This column specifies the state of the pin during a suspend operation. Input signals have the representation Tri. This indicates that input is internally isolated and that the internal termination on the pin is tri-state or disabled. The additional output buffers abbreviations are explained below. Tri —Tri-state Actv —Active 0 —held low 1 —held high Hold —held at last state
ONCE	This column specifies the state of the pin when the ONCE# pin is asserted, allowing in-circuit testing while the device is still populated on the logic board. Tri —Floats Actv —Active 0 —held low 1 —held high Hold —held at last state
Derating Curve	This column specifies derating curve number for the corresponding pin.

The 82360SL I/O Pinout Diagram for 208-Lead SQFP

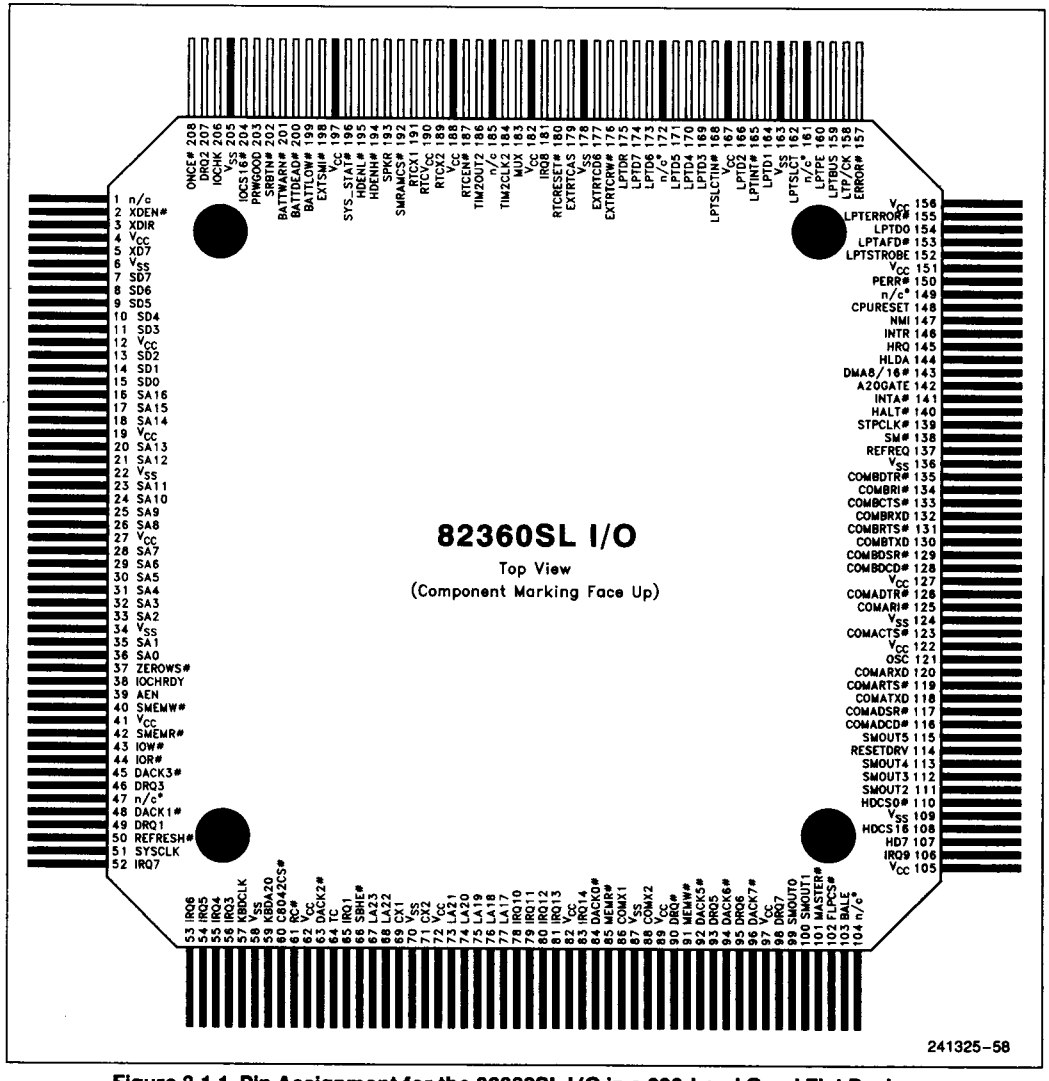


Figure 3.1.1. Pin Assignment for the 82360SL I/O in a 208-Lead Quad Flat Package

The 82360SL I/O Pinout Diagram for 198-Lead PQFP

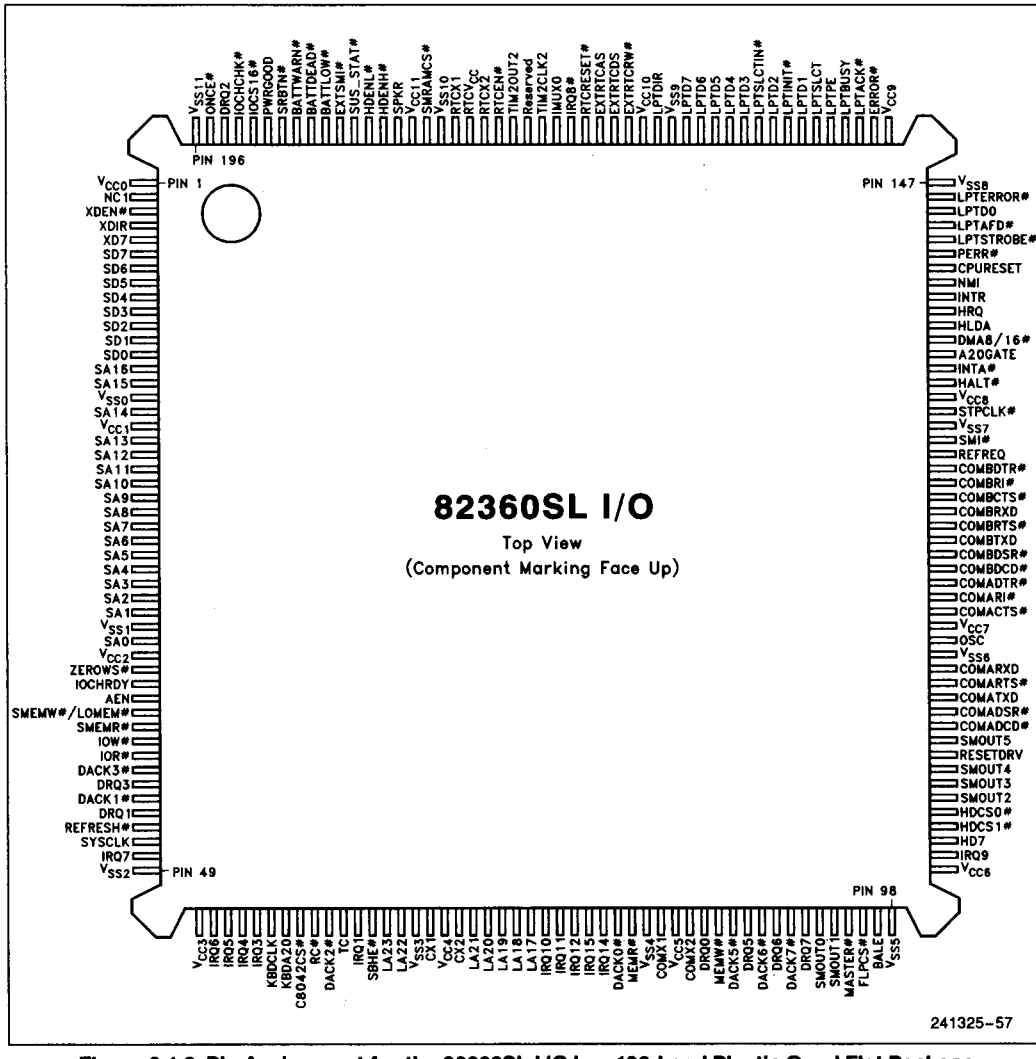


Figure 3.1.2. Pin Assignment for the 82360SL I/O in a 196-Lead Plastic Quad Flat Package

Table 3-2. 82360SL I/O Pin Characteristics

Signal Name	SQFP	PQFP	Type	Term	Drive (5V) I_{OL}, I_{OH}	Drive (3.3V) I_{OL}, I_{OH}	Load (5V) Min, Max	Load (3.3V) Min, Max	Susp	Once	Derating Curve (5V)	Derating Curve (3.3V)
A20GATE	142	B135	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
AEN	39	B037	O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-4	C-4
BALE	103	B097	I						Tri	Tri		
BATTDEAD#	200	B188	I						Actv	Tri		
BATTLOW#	199	B187	I						Actv	Tri		
BATTWARN#	201	B189	I	60K PU					Tri	Tri		
C8042CS#	60	B057	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
COMACTS#	123	B117	I	60K PU					Tri	Tri		
COMADCD#	116	B109	I	60K PU					Tri	Tri		
COMADSR#	117	B110	I	60K PU					Tri	Tri		
COMADTR#	126	B119	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
COMARI#	125	B118	I	60K PU					Actv(1)	Tri		
COMARTS#	119	B112	O		12, 2	12, 2	20, 50	20, 50	Tri		B-7	C-7
COMARXD	120	B113	I	20K PD					Tri	Tri		
COMATXD	118	B111	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
COMBCTS#	133	B125	I	60K PU					Tri	Tri		
COMBDCD#	128	B120	I	60K PU					Tri	Tri		
COMBDSR#	129	B121	I	60K PU					Tri	Tri		
COMBDTR#	135	B127	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
COMBRI#	134	B126	I	60K PU					Actv(1)	Tri		
COMBRTS#	131	B123	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
COMBRXD	132	B124	I	20K PU					Tri	Tri		
COMBTXD	130	B122	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
COMX1	86	B082	I						Tri	Tri		
COMX2	88	B084	O						1	1	B-7	C-7
CPURESET	148	B141	O		12, 2	12, 2	20, 50	20, 50	Actv	Tri	B-7	C-7
CX1	69	B066	I						Tri	Tri		
CX2	71	B068	O						1	1	B-7	C-7
DACK0#	84	B079	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DACK1#	48	B044	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DACK2#	63	B059	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DACK3#	45	B042	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DACK5#	92	B087	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DACK6#	94	B089	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DACK7#	96	B091	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7

NOTE:
1. These pins can be programmed to remain isolated during suspend.

Table 3-2. 82360SL I/O Pin Characteristics (Continued)

Signal Name	SQFP	PQFP	Type	Term	Drive (5V) I_{OL}, I_{OH}	Drive (3.3V) I_{OL}, I_{OH}	Load (5V) Min, Max	Load (3.3V) Min, Max	Susp	Once	Derating Curve (5V)	Derating Curve (3.3V)
DMA8/16#	143	B136	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
DRQ0	90	B085	I	20K PD					Tri	Tri		
DRQ1	49	B045	I	20K PD					Tri	Tri		
DRQ2	207	B194	I	20K PD					Tri	Tri		
DRQ3	46	B43	I	20K PD					Tri	Tri		
DRQ5	93	B088	I	20K PD					Tri	Tri		
DRQ6	95	B090	I	20K PD					Tri	Tri		
DRQ7	98	B092	I	20K PD					Tri	Tri		
ERROR#	157	B149	I	60K PU					Tri	Tri		
EXTRTCAS#	179	B168	O	60K PU					Tri	Tri		
EXTRTCDS	177	B167	O	20K PD					Tri	Tri		
EXTRTCRW#	176	B166	O	60K PU	12, 2	12, 2	20, 50	20, 50	1	Tri	B-7	C-7
EXTSMI#	198	B186	I	60K PU	12, 2	12, 2	20, 50	20, 50	0	Tri	B-7	C-7
FLPCS#	102	B096	O		12, 2	12, 2	20, 50	20, 50	1	Tri	B-7	C-7
HALT#	140	B133	I	60K PU					Tri	Tri		
HD7	107	B101	I/O	60K PU	24, 4	12, 4	20, 100	20, 100	Tri	Tri	B-3	C-3
HDCS0#	110	B103	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
HDCS1#	108	B102	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
HDENH#	194	B183	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
HDENL#	195	B184	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
HLDA	144	B137	I	20K PD					Tri	Tri		
HRQ	145	B138	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
IMUX0	183	B171	I	20K PD					Tri	Tri		
INTA#	141	B134	I	60K PU					Tri	Tri		
INTR	146	B139	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
IOCHCK#	206	B193	I	4.7K PU					Tri	Tri		
IOCHRDY	38	B036	I/O OD		24, 4	12, 4	20, 240	20, 160	Tri	Tri	B-8	C-8
IOCS16#	204	B192	I						Tri			
IOR#	44	B041	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
IOW#	43	B040	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
IRQ1	65	B061	I	10K PU					Tri	Tri		
IRQ3	56	B054	I	10K PU					Tri	Tri		
IRQ4	55	B053	I	10K PU					Tri	Tri		
IRQ5	54	B052	I	10K PU					Tri	Tri		
IRQ6	53	B051	I	10K PU					Tri	Tri		
IRQ7	52	B048	I	10K PU					Tri	Tri		

Table 3-2. 82360SL I/O Pin Characteristics (Continued)

Signal Name	SQFP	PQFP	Type	Term	Drive (5V) I_{OL}, I_{OH}	Drive (3.3V) I_{OL}, I_{OH}	Load (5V) Min, Max	Load (3.3V) Min, Max	Susp	Once	Derating Curve (5V)	Derating Curve (3.3V)
IRQ8	181	B170	I	20K PD					Actv	Tri		
IRQ9	106	B100	I	10K PU					Tri	Tri		
IRQ10	78	B074	I	10K PU					Tri	Tri		
IRQ11	79	B075	I	10K PU					Tri	Tri		
IRQ12	80	B076	I	10K PU					Tri	Tri		
IRQ14	83	B078	I	10K PU					Tri	Tri		
IRQ15	81	B077	I	10K PU					Tri	Tri		
KBDA20	59	B056	I	60K PU					Tri	Tri		
KBDCLK	57	B055	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
LA17	77	B073	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LA18	76	B072	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LA19	75	B071	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LA20	74	B070	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LA21	73	B069	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LA22	68	B064	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LA23	67	B063	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
LPTACK#	158	B150	I	60K PU					Tri	Tri		
LPTAFD#	153	B144	I/O OD(1)	4.7K PU	12	12	20, 100	20, 100	Tri	Tri	B-6	C-6
LPTBUSY	159	B151	I	20K PU					Tri	Tri		
LPTD0	154	B145	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD1	164	B154	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD2	166	B156	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD3	169	B158	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD4	170	B159	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD5	171	B160	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD6	173	B161	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTD7	174	B162	I/O	20K PD	8, 2	8, 2	20, 100	20, 100	Tri	Tri	B-5	C-5
LPTDIR	175	B164	I/O OD(1)	4.7K PU	12	12	20, 100	20, 100	Tri	Tri	B-6	C-6
LPTERROR#	155	B146	I	60K PU					Tri	Tri		
LPTINIT#	165	B155	I/O OD(1)	4.7K PU	12	12	20, 100	20, 100	Tri	Tri	B-10	C-10
LPTPE	160	B152	I	20K PD					Tri	Tri		
LPTSLCT	162	B153	I	20K PD					Tri	Tri		
LPTSLCTIN#	168	B157	I/O OD(1)	4.7K PU	12	12	20, 100	20, 100	Tri	Tri	B-6	C-6
LPTSTROBE#	152	B143	I/O OD(1)	4.7K PU	12	12	20, 100	20, 100	Tri	Tri	B-6	C-6

NOTE:
1. These outputs become CMOS drivers when bit 7 of the FPP_CNTL register is set.

Table 3-2. 82360SL I/O Pin Characteristics (Continued)

Signal Name	SQFP	PQFP	Type	Term	Drive (5V) I_{OL}, I_{OH}	Drive (3.3V) I_{OL}, I_{OH}	Load (5V) Min, Max	Load (3.3V) Min, Max	Susp	Once	Derating Curve (5V)	Derating Curve (3.3V)
MASTER#	101	B095	I						Tri	Tri		
MEMR#	85	B080	I/O		24, 4	12, 4	20, 240	20, 160	Tri	Tri	B-2	C-2
MEMW#	91	B086	I/O		24, 4	12, 4	20, 240	20, 160	Tri	Tri	B-2	C-2
NC		B002										
NMI	147	B140	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
ONCE#	208	B195	I	60K PU					Tri	Actv		
OSC	121	B115	O		24	12	50, 240	50, 160	Tri	Tri	B-4	C-4
PERR#	150	B142	I	60K PU					Tri	Tri		
PWRGOOD	203	B191	I						Actv	Tri		
RC#	61	B058	I	60K PU					Tri	Tri		
REFREQ	137	B128	O		12, 2	12, 2	20, 50	20, 50	Actv	Tri	B-7	C-7
REFRESH#	50	B046	I/O OD	1.2K PU	8	8	50, 240	50, 160	Tri	Tri	B-8	C-8
RESETDRV	114	B107	O		24	12	50, 240	50, 160	Tri	Tri	B-9	C-9
RTCEN#	187	B175	I						Actv	Tri		
RTCRESET#	180	B169	I						Actv	Tri		
RTCVCC	190	B177										
RTCX1	191	B178	I						Actv	Tri		
RTCX2	189	B176	O						Actv	1	B-7	C-7
Reserved		B173										
SA0	36	B033	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA1	35	B031	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA2	33	B030	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA3	32	B029	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA4	31	B028	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA5	30	B027	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA6	29	B026	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA7	28	B025	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA8	26	B024	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA9	25	B023	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA10	24	B022	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA11	23	B021	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA12	21	B020	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA13	20	B019	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1

Table 3-2. 82360SL I/O Pin Characteristics (Continued)

Signal Name	SQFP	PQFP	Type	Term	Drive (5V) I_{OL}, I_{OH}	Drive (3.3V) I_{OL}, I_{OH}	Load (5V) Min, Max	Load (3.3V) Min, Max	Susp	Once	Derating Curve (5V)	Derating Curve (3.3V)
SA14	18	B017	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA15	17	B015	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SA16	16	B014	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-1	C-1
SBHE#	66	B062	O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-4	C-4
SD0	15	B013	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD1	14	B012	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD2	13	B011	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD3	11	B010	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD4	10	B009	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD5	9	B008	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD6	8	B007	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SD7	7	B006	I/O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-2	C-2
SMEMR#/ LOMEM#	42	B039	O	60K PU	24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-4	C-4
SMEMW#	40	B038	O	60K PU	24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-4	C-4
SMI#	138	B129	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMOUT0	99	B093	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMOUT1	100	B094	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMOUT2	111	B104	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMOUT3	112	B105	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMOUT4	113	B106	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMOUT5	115	B108	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SMRAMCS#	192	B180	I	60K PU					Tri	Tri		
SPKR	193	B182	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SRBTN#	202	B190	I						Actv	Tri		
STPCLK	139	B131	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
SUS_STAT#	196	B185	O		12, 2	12, 2	20, 50	20, 50	Actv	Tri	B-7	C-7
SYSCLK	51	B047	I						Tri	Tri		
TC	64	B060	O		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-4	C-4
TIM2CLK2	184	B172	I	20K PD					Tri	Tri		
TIM2OUT2	186	B174	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
XD7	5	B005	I/O	60K PU	24, 4	12, 4	20, 100	20, 100	Tri	Tri	B-3	C-3
XDEN#	2	B003	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
XDIR#	3	B004	O		12, 2	12, 2	20, 50	20, 50	Tri	Tri	B-7	C-7
ZEROWS#	37	B035	O OD		24, 4	12, 4	50, 240	50, 160	Tri	Tri	B-8	C-8

Power Pins:

V_{CC}: PQFP—B001, B018, B034, B050, B067, B083, B099, B116, B132, B148, B165, B181
SQFP—4, 12, 19, 27, 41, 62, 72, 82, 89, 97, 105, 122, 127, 151, 156, 167, 182, 188, 197

V_{SS}: PQFP—B016, B032, B049, B065, B081, B098, B114, B130, B147, B163, B179, B196
SQFP—6, 22, 34, 58, 70, 87, 109, 124, 136, 163, 178, 205

No Connect:

PQFP—B2
SQFP—1, 47, 104, 149, 161, 172, 185

3.2 82360SL I/O Signal Description

82360SL I/O ISA Peripheral I/O

The following table provides a brief description of the 82360SL I/O. Signal names which end with the character "#" indicate that the corresponding signal is low true when active.

Symbol	Name and Function
A20GATE	**A20 GATE (Direct to CPU):** This active HIGH output signal allows the CPU to pass A20 on the address bus. When this signal is LOW, A20 is masked to allow emulation of an 8086.
AEN	**Address ENabled (ISA-Bus Signal):** This active HIGH output indicates a DMA access or refresh. The 82360SL I/O drives this signal high to signify a valid DMA address. It is used by bus slaves to decode I/O ports. All ports must be decoded for AEN low. There are no DMA cycles to address I/O ports.
BALE	**Buffered Address Latch Enable (ISA-Bus Signal):** This active HIGH input to the 82360SL I/O is driven by the Intel486 SL CPU during standard ISA Bus cycles. During ISA-bus memory and I/O cycles BALE is used to indicate valid addresses at the start of a bus cycle. SA[19:0] are valid on the falling edge and LA[23:17] are valid while BALE is high. BALE is also driven high by the Intel486 SL CPU and remains high during DMA, REFRESH and Master cycles.
BATTDEAD#	**BATTery DEAD:** This signal acts as a reset to the state machines connected to RTCVCC. This signal must be connected to an RC combination which will allow it to meet the AC specification It250.
BATTLOW#	**BATTery LOW:** This active LOW input indicates that the battery power is low. BATTLOW# is typically driven by a D.D. to D.C. power converter associated with the battery power supply. A thermal power monitor indicates that the main battery power is dropping below the adequate charge level to sustain operation. If this signal is asserted LOW, a SMI request will be generated. The feature is enabled via S/W control. The signal will also prevent a resume operation if asserted LOW.
BATTWARN#	**BATTery WARNing:** This active LOW input indicates the battery has minimal charge left (i.e., one half an hour of full power use remaining). It is used to generate a battery low warning tone.
C8042CS#	**Keyboard Controller Chip Select:** This active LOW output is driven when there is an I/O read or write to the Keyboard Controller Ports 60H or 64H.
COM(A,B)CTS#	**Clear To Send:** This active LOW input indicates to the Serial Port Controller for COMA or COMB that a serial device is clear to accept data. This signal is typically used for a modem control function. A change in the state of this signal generates a modem status interrupt. The modem or data set asserts this signal when it is ready to accept data for transmission.
COM(A,B)DCD#	**Data Carrier Detect:** This active LOW input indicates that the Serial Port Controller COMA or COMB has detected a data carrier from the data set of a serial device. Typically this signal is from a modem.
COM(A,B)DSR	**Data Set Ready:** This active LOW input signal is used by the modem or data set to indicate that the modem or data set is ready to establish the communication link and transfer data with the Serial Port Controller.
COM(A,B)DTR#	**Data Terminal Ready:** This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to communicate.
COM(A,B)RXD	**Serial Data Receive:** This input signal is used to receive serial data. Each character can consist of from five to eight bits of data with one start bit and one, one and half or two stop bits. The least significant bit is received first.

3.2 82360SL I/O Signal Description (Continued)

Symbol	Name and Function
COM(A,B)RI#	**Ring Indicator:** This active LOW input signal is used for a modem control function. A change in the state (either from high to low or from low to high) of this signal generates a modem status interrupt. The modem or data set asserts this signal to indicate that it has detected a telephone ring. This will cause the 82360SL I/O to wake the Intel486 SL CPU from a suspended state if modem ring is enabled as a wake-up event.
COM(A,B)RTS	**Request To Send:** This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to send data.
COM(A,B)TXD	**Serial Data Transmission:** This output signal is used to transmit data serially between the Serial Port Controller and serial device. Each character can consist of five to eight bits of data with one start bit and either one, one and a half, or two stop bits. The least significant bit is transmitted first. The control of the format of a character is defined under S/W control via the Line Control Register. Please consult the Intel486 SL Microprocessor SuperSet Programmer's Reference Manual for additional information. Information regarding the functional timing specifications of transmitted and received serial data may be found in Sections 6 and 7 (A.C. Timing Specifications and Timing Diagrams).
COMX1, COMX2	**Crystal Oscillator Input and Output Pins:** The crystal attached to these signals should be tuned to 1.8432 MHz. The on-chip oscillator uses an external crystal and tank circuit to generate an internal clock. This clock is used to generate the various baud rates for the serial ports. Optionally an external oscillator may be connected to the COMX1 input.
CPURESET	**CPU RESET:** This active HIGH output is connected directly to the Intel486 SL CPU to provide a reset of the Intel486 CPU core. CPURESET always occurs during a PWRGOOD reset. CPURESET may also be generated by RC# from a keyboard controller, Fast Reset from I/O Port 92 or other programmable Reset, or a resume from suspend.
CX1, CX2	**Crystal Oscillator Input and Output Pins:** This crystal should be tuned to 14.31818 MHz. It is used for the ISA bus signal OSC signal and is internally divided by 12 to clock the timer counters. The oscillator input may be directly driven from an external source.
DACK[7:5], [3:0]#	**DMA ACKnowledge Channel n (ISA Bus Signal):** The 82360SL I/O DMA controller drives the respective DMA acknowledge signal low after a device has requested DMA service. The corresponding output signal indicates that the DMA channel transfer may begin.
DMA8/16#	**DMA 8-Bit or 16-Bit Cycle:** This output signal is directly connected to the Intel486 SL CPU. When the signal is HIGH it indicates that the current DMA cycles is 8-bit. When this signal is low it indicates that the DMA cycle is using 16-bit channel.
DRQ[7:5], [3:0]#	**DMA ReQuest Channel n (ISA-Bus Signal):** These input signals are used to request DMA service from devices residing on the ISA-bus. An ISA-bus device drives this signal to request service from the appropriate DMA channel by asserting this signal high.
ERROR#	**MCP ERROR:** This signal is an active LOW input to the 82360SL I/O. The math coprocessor error signal generates an IRQ13 through the 82360SL I/O.
EXTSMI#	**EXTernal System Management Interrupt Request:** This active LOW input will generate an SMI request if the function is enabled.
EXTRTCAS	**EXTernal RTC Address Strobe:** This output signal is active HIGH when there is a write access to the RTC I/O address port and when an external RTC is selected.

3.2 82360SL I/O Signal Description (Continued)

Symbol	Name and Function
EXTRTCDS	**EXTernal RTC Read Data Strobe:** This output signal is active LOW when there is a read access to an external RTC I/O data port and when an external RTC is selected.
EXTRTCRW#	**EXTernal RTC (Read Time Clock) Read/Write:** This output signal is active LOW when there is a write access to an external RTC I/O data port and when an external RTC is selected.
FLPCS#	**FloPpy Chip Select:** This LOW true output signal is the chip select for the floppy disk controller I/O ports 03F0–03F5H and 3F7H.
HALT#	**HALT:** This LOW true input signal is driven by the Intel486 SL CPU and indicates when the CPU has executed an HLT instruction (address = 2) or is in a shutdown condition (address = 0).
HD7	**HD-Bus Data Bit HD7:** The bi-directional System Data bit 7 is controller separately for the Integrated Drive Electronics (IDE) hard disk drive and floppy disk drive. This is provided to accommodate the I/O address 3F7H which is split between the floppy disk drive controller and IDE hard disk. Data transfer between storage peripherals connected to the IDE Hard Disk and Floppy Disk and 82360SL I/O are on separate buses. Data bit 7 has to be separated from data bits [6:0]. The 82360SL I/O controls and buffers data bit 7 separately.
HDCS[1:0]#	**Hard Disk Chip Select:** These LOW true output signals are the IDE hard disk drive chip selects decoded from the I/O address ports 01F0–01F7H (HDCS0#) and 03F6–03F7H (HDCS1#).
HDEN(H,L)#	**Hard Disk Buffer ENable:** These LOW true output signals control the IDE hard disk data buffers, high and low bytes.
HLDA	**HoLD Acknowledge (Direct to CPU):** This HIGH true input signal indicates that the Intel486 SL CPU has released the ISA bus for refresh, DMA or master cycles.
HRQ	**Hold ReQuest (Direct to CPU):** This active HIGH output signal indicates a request to the Intel486 SL CPU to release the ISA bus when the 82360SL I/O requests the bus for ISA-bus-style refresh. DMA or master mode cycles.
IMUX0	This pin is multiplexed. It can be used as Timer 2 Gate 2 input or an external audio input.
INTA#	**INTerrupt Acknowledge (Direct to CPU):** This active LOW input to the 82360SL I/O indicates that the Intel486 SL CPU has recognized an interrupt and will initiate an interrupt acknowledge bus cycle. The INTA bus cycles is comprised of two eight-bit I/O cycles in which the interrupt vector transferred on the second eight-bit I/O write of the INTA cycle.
INTR	**INTerrupt Request (Direct to CPU):** This active HIGH output requests a standard maskable interrupt to the Intel486 SL CPU.
IOCHCK#	**IO CHannel CheckK (ISA Bus Signal):** This maskable active LOW input is driven by a device on the ISA bus typically used to indicate a parity error on the ISA bus. This signal is one of the possible sources which may generate an NMI. NMI generation via I/O Channel Check may be enabled or disabled using PORT 61 (IOCKEN). NMI may be masked using the ISA-bus compatible. NMI control port a I/O 70H bit 7.
IOCHRDY	**I/O CHannel ReaDY (ISA Bus Signal):** This active HIGH I/O signal is used by the 82360SL I/O DMA controller to extend ISA bus cycles. IOCHRDY is also used to extend bus cycles for I/O device trapping. Additional wait states extend the bus cycle, allowing for start up during Resume mode. The ISA bus is a normally ready bus, an external device can extend a DMA cycles or ISA bus cycles be deasserting this signal (driven low). This signal is normally high on the ISA bus.

3.2 82360SL I/O Signal Description (Continued)

Symbol	Name and Function
IOCS16#	**16-Bit I/O Chip Select (ISA Bus Signal):** This signal LOW input signal to the 82360SL I/O is used to indicate a 16-bit I/O bus cycle. The IDE hard disk high byte buffer enable is generated when IOCS16# is driven low during an IDE 16-bit I/O access. IOCS16# is also an input to the Intel486 SL CPU driven by devices residing on the ISA bus to indicate a 16-bit bus cycle.
IOR#	**I/O Read (ISA Bus Signal):** This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O read. This signal is an output from the 82360SL I/O during DMA bus cycles for I/O to memory transfers.
IOW#	**I/O Write (ISA Bus Signal):** This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O write. This signal is an output from the 82360SL I/O during DMA bus cycles for memory to I/O transfers.
IRQ[15,14, 12–9, 7–3, 1]	**Interrupt ReQuest n (ISA Bus Signal):** These active HIGH input signals are used to request interrupt service. The interrupt request lines are driven by devices on the ISA bus which have a corresponding interrupt service routine associated with the interrupt vector and interrupt request.
IRQ8#	**Interrupt ReQuest 8:** This active LOW signal is used by the external Real Time Clock to request interrupt service.
KBDA20	**KeyBoarD A20 Gate:** This active HIGH input is "OR'ed" with internal bits to produce A20GATE which goes to the Intel486 SL CPU. The bit is connected to port 2, bit 1 of an 8042 in a standard ISA bus compatible system.
KBDCLK	**KeyBoarD Clock:** This output signal is used to drive the clock input to the keyboard controller. It is derived from the 8 MHz SYSCLK and can be divided by 1, 2, 4 or stopped.
LA[23:17]	**Local Address Bus (ISA Bus Signal):** These are input signals to the 82360SL I/O during memory transfers (decoding for X-Bus buffer controls) and output signal during DMA accesses and refresh. The latchable address lines allow access to physical memory on the ISA bus to 16 Mbytes.
LPTACK#	**Line PrinTer ACKnowledge:** Active LOW input signal which is part of the parallel port data handshake. The line printer asserts this signal to show that data transfer was complete and that it is ready for the next transfer. If the interrupt enable bit is set in the LPT control register, this signal can be used to generate an interrupt.
LPTAFD#	**Line Printer Auto Line FeeD:** This signal is an active LOW output from 82360SL I/O to a printer. When asserted, it instructs the printing device to insert a line feed at the end of every line. In the Fast Parallel Port mode, this signal is used as a data strobe. It can be used to latch data during write cycles and to enable buffers during read cycles.
LPTBUSY	**Line PrinTer BUSY:** This signal is an active HIGH input to 82360SL I/O. The printer asserts this signal when is not ready to accept further data from 82360SL I/O. In the Fast Parallel Port mode this signal is active LOW.
LPTD[7:0]	**Line Printer Data Bus:** These signals are the 8-bit bi-directional data bus for the parallel port. In PC/AT mode these signals are output only. The 82360SL I/O also supports a bi-directional mode for the PS/2 style parallel port.
LPTDIR	**Line PrinTer DIRection:** This active HIGH output signal is only valid in bi-directional mode for data transfer using the parallel port. This signal is LOW in ISA-compatible and Fast Parallel Port modes. In the PS/2 expanded mode, this signal is LOW for writes and HIGH for reads.
LPTERROR#	**Line PrinTer ERROR:** This active LOW input signal is driven by a peripheral device to flag an error condition.

3.2 82360SL I/O Signal Description (Continued)

Symbol	Name and Function
LPTINIT#	**Line PrinTer InITialize:** This active LOW output from 82360SL I/O instructs the peripheral to initialize itself.
LPTPE	**Line PrinTer Paper End:** This active HIGH input to 82360SL I/O signals that the printer has run out of paper when asserted.
LPTSLCT	**Line PrinTer SeLeCTed:** This active HIGH input signal is asserted by the printer to confirm that it has been selected.
LPTSLCTIN#	**Line PrinTer SeLeCT IN:** This active LOW output signal is asserted to select the printer interfaced to the parallel port. In the Fast parallel port mode, this signal is used as an address strobe. It indicates that an access is being made to the port X7Bh.
LPTSTROBE	**Line PrinTer STROBE:** This active HIGH input signal is used to strobe data into the peripheral device. The parallel port controls are read and written through I/O registers. In the Fast parallel port mode, this signal is used to indicate a write cycle.
MASTER#	**ISA Bus MASTER (ISA Bus Signal):** This active LOW input signal is used by the 82360SL I/O to determine when to go into an external master refresh arbitration mode. In this mode, the master controls the REFRESH signal but the 82360SL I/O generates the address, the REFREQ# signal, the AEN and command signals.
MEMR#	**MEMory Cycle Read (ISA Bus Signal):** This bi-directional active LOW signal indicates a read cycle anywhere in the 16-Mbyte memory address space. During memory read cycles to memory on the ISA bus, this signal is an input into the 82360SL I/O MEMR# is driven by the 82360SL I/O during DMA cycles.
MEMW#	**MEMory Cycle Write (ISA Bus Signal):** This bi-directional active LOW signal indicates a write cycle anywhere in the 16-Mbyte memory address space. During memory write cycles to memory on the ISA bus, this signal is an input. MEMW# is an output from the 82360SL I/O during DMA cycles.
N/C	**No Connection:** These signals must not be connected to any voltage. The No Connection signals must be left floating in order to guarantee proper operation of the 82360SL I/O and compatibility with future Intel processors.
NMI	**Non-Maskable Interrupt (Direct to CPU):** This active HIGH output is directly connected to the Intel486 SL CPU. The 82360SL I/O asserts NMI to request the Intel486 SL CPU to service a high priority non-maskable interrupt. The low to high transition of this signal is recognized by the Intel486 SL CPU.
ONCE#	**ON-board Circuit Emulation:** This active LOW input pin floats the appropriate outputs of the 82360SL I/O as indicated in Section 3.1 pin assignments. This allows the system to be tested with external logic while the HRI I/O is still physically populated on the motherboard. Note that the ONCE# pin on the 82360SL I/O should not be connected to the ONCE# pin on the Intel486 SL CPU.
OSC	**OSCillator (ISA Bus Signal):** This is the 12.21818 MHz output signal with a 50% duty cycle and is asynchronous to SYSCLK.
PERR#	**Parity ERRor (Direct from CPU):** This active LOW input signal is connected to the output of the Intel486 SL CPU. When the Intel486 SL CPU detects a parity error from the local DRAM subsystem it drives this signal to the I/O. The system memory parity error will generate an NMI via the 82360SL I/O when NMI is enabled via I/O port 70H bit 7 and PERR# is enabled via port 61H.
PWRGOOD	**PoWeR GOOD:** This active HIGH input is typically supplied by the power supply. When Power good is activated high this indicates that the supply voltage is stable. Power Good low is also used to generate System Reset, RESETDRV, and CPURESET.
RC#	**Reset CPU:** This active low input is typically driven by the keyboard controller. RC# is "OR'ed" with internal bits to produce a programmable pulse width CPURESET signal. It is connected to port 2, bit 0 of an 8042 in a standard ISA bus compatible system.

3.2 82360SL I/O Signal Description (Continued)

Symbol	Name and Function
REFREQ	**REFresh REQuest (Direct to CPU):** This active HIGH output signal is directly connected to the Intel486 SL CPU. When Refresh Request is asserted it indicates that the Intel486 SL CPU should refresh the local DRAM subsystem.
RESETDRV	**RESET DRIVe (ISA Bus Signal):** This active HIGH output is the main system cold reset, generated from the power supply "power good" signal and by system resume.
RTCEN#	**RTC ENable:** This active LOW input signal should be strapped to GND or RTCVCC depending on whether an internal or external RTC is used in the system. The 82360SL I/O on-chip real time clock and CMOS RAM are enabled by this signal when LOW.
RTCRESET#	**Internal RTC RESET Input:** This active LOW input signal is used to reset the internal RTC status and flag registers, (typically when the RTC battery has been changed).
RTCVCC	This is a separate power supply input for the internal RTC. It should be connected to a 3V battery when the system is fully off and V_{CC} during active operation.
RTCX1, RTCX2	**RTC Crystal Oscillator Input and Output Pins:** The crystal should be tuned to 32.768 KHz. It is used for the RTC and system power management state machines. The oscillator may be driven directly from the input signal.
SA[16:0]	**System Address Bus (ISA Bus Signal):** The active LOW output signal indicates when there is valid data on the upper data byte of the system data bus.
SBHE#	**System Byte High Enable (ISA Bus Signal):** The active LOW output signal indicates when there is valid data on the upper data byte of the system data bus.
SD[7:0]	**System Data Bus (ISA Bus Signal):** This is the bi-directional system data bus. The 82360SL I/O directly drives the ISA bus system data bits [7:0] without external transceivers or buffers. 8-bit data is transferred to and from the 82360SL I/O with these signals.
SMEMR#/LOMEM#	**System Memory Read (ISA Bus Signal):** This multiplexed signal has two functions. When configured as SMEMR#, this signal is driven by the 82360SL to signify a memory read cycle to the bottom 2 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles. When configured as LOMEM#, this signal indicates that the lower 1 Mbyte is being addressed.
SMEMW#	**System Memory Write (ISA Bus Signal):** This signal is driven by the 82360SL to signify memory write cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles.
SMI#	**System Management Interrupt (Direct to CPU):** This active LOW output is directly connected to the Intel486 SL CPU. When the falling edge 4 of SMI# is detected by the Intel486 SL CPU it generates the highest priority interrupt when enabled. The typical use of SMI# is for power management.
SMOUT[5:0]	**System Management OUTput Control:** These six outputs can be connected to control the power circuits for various devices in the system. These output pins are directly controlled by the SMOUT_CNTRL register.
SMRAMCS#	**System Management RAM Chip Select:** This active LOW input is driven by the Intel486 CPU whenever the Intel486 SL CPU is accessing the System Management SM-RAM. It is active even when SM-RAM is part of the Intel486 SL CPU system memory RAM. The 82360SL uses the SMRAMCS# to determine when the SMI code is being executed on the ISA bus, and enables the X-bus control signals.

3.2 82360SL I/O Signal Description (Continued)

Symbol	Name and Function
SPKR	**Speaker Output:** This is the output of the 8254 megacell, timer/counter #1, channel 2, or directly driven through IMUX0, or from the 8254 megacell, timer/counter #2, channel 1 depending on the programming. This output signal is typically connected to an external speaker. There is additional circuitry to ensure that the signal is low when not being used.
SRBTN#	**Suspend/Resume Button:** This active LOW input generates a SMI requesting a system suspend or resume. Activation of this input can be used as a wake up event for the STPCLK# signal.
STPCLK#	**Stop Clock:** This active LOW output signal stops the clock to the Intel486 CPU core of the Intel486 SL Microprocessor. Stop clock is directly connected to the Intel386 SL CPU from the 82360SL. The 82360SL activates this signal upon detection of a halt bus cycle or when an I/O read to the stop clock register in the 82360SL occurs.
SYSCLK	**System Clock (ISA Bus Signal):** This signal is an output from the Intel486 SL CPU and an input to the 82360SL. The SYSCLK signal is used to clock the ISA bus state machines and is also used to derive the internal DMA clock signal and to generate the KBDCLK output in the 82360SL. The SYSCLK is the 8 MHz typical clock which is one half of the frequency of ISACLK2.
SUS_STAT#	**Suspend Status:** The 82360SL power management control this active low output signal to switch the power off to all non-critical devices during a suspend.
TC	**Terminal Count (ISA Bus Signal):** This active HIGH output signal is used to indicate the termination of a DMA transfer.
TIM2CLK2	**Timer 2 CLK:** This is the input clock for timer/counter #2, channel 2 when it is programmed to be used in the General Purpose (GP) mode.
TIM2OUT2	**Timer 2 Output:** This signal is the frequency output from timer/counter #2 and can be used as a general purpose timer/counter output when programmed for GP mode.
V_{CC}	**System Power:** Provides the +5V or 3.3V nominal D.C. supply inputs for the 82360SL.
V_{SS}	**System Ground:** Provides the 0V connection from which all inputs and outputs are referenced.
XD7	**X-bus Data bit XD7:** I/O port 3F7h is split between the floppy and hard disk and the storage peripherals which transfer data reside on separate busses. Data bit XD7 is separated from bits XD[6:0]. The 82360SL separately controls and buffers bit XD7 to isolate data bit 7 from the floppy disk and I.D.E. hard disk.
XDEN#	**X-Bus Data Enable:** This active LOW output signal is used to control the X-bus data transceiver. It is only activated by the 82360SL on valid accesses to X-bus peripherals.
XDIR	**X-Bus Data Direction:** This active HIGH output signal controls the direction of the X-bus and HD-bus data transceivers. XDIR is high for read cycles.
ZEROWS#	**ZERO Wait State (ISA-Bus Signal):** This active LOW output signal is driven by the 82360SL when it can accept a zero wait state write cycle.

3.3 82360SL I/O D.C. Specifications

3.3.1 CAPACITANCE D.C. SPECIFICATIONS

Table 3-1. Capacitance D.C. Specifications

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output or I/O Capacitance		20	pF	
C_{CLK}	All Clocks		15	pF	

3.3.2 3V D.C. SPECIFICATIONS V_{CC} = 3.0V to 3.6V; T_{case} = 0°C to 90°C.

Table 3-2. 82360SL I/O D.C. Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3		0.8	V	(Note 13)
V_{IH}	Input High Voltage	2.0 2.4		V_{CC} + 0.3	V V	(Note 14) (Note 11)
I_{LI}	Input Leakage Current			±15	μA	(Note 1)
I_{LO}	Output Leakage Current			±15	μA	(Note 1)
C_{IN}	Input Capacitance			10	pF	(Note 12)
C_{OUT}	Output or I/O Capacitance			15	pF	(Note 12)
I_{CCS1}	Suspend with Slow Refresh		120	240	μA	(Note 8)
I_{CCS2}	Suspend without Slow Refresh		90	210	μA	(Note 8)
I_{CC}	Power Supply Current		30	60	mA	(Note 9)
D.C. SPECIFICATION FOR STANDARD ISA BUS SIGNALS						
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 6 mA (Note 3)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −2.0 mA (Note 3)
D.C. SPECIFICATION FOR PARALLEL PORT						
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 2 mA (Note 2)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −2.0 mA (Note 2)
D.C. SPECIFICATION FOR OPEN DRAIN OUTPUTS						
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 6 mA (Note 4) I_{OL} = 3 mA (Note 5) I_{OL} = 2 mA (Note 10)
D.C. SPECIFICATION FOR ALL OTHER OUTPUTS						
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 2 mA (Note 6)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −2.0 mA (Note 6)
D.C. SPECIFICATION FOR POWER-DOWN MODE						
VBATT	Battery Supply Voltage	2.5		5.5	V	15
IBATT	Battery Supply Current		20 10	75 35	μA μA	VBATT = 5V (Note 7) VBATT = 2.5V (Note 7)
V_{IL}	PWRGOOD Low Input Voltage			0.8	V	
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 8 mA
V_{OH}	Output High Current	2.0			V	I_{OL} = −2 mA

3.3.3 5V D.C. SPECIFICATIONS V_{CC} = 4.5V to 5.5V; T_{case} = 0°C to 90°C.

Table 3-3. 82360SL I/O D.C. Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3		0.8	V	(Note 13)
V_{IH}	Input High Voltage	2.0 3.4		V_{CC} + 0.3	V V	(Note 14) (Note 11)
I_{LI}	Input Leakage Current			±15	μA	(Note 1)
I_{LO}	Output Leakage Current			±15	μA	(Note 1)
C_{IN}	Input Capacitance			10	pF	(Note 12)
C_{OUT}	Output or I/O Capacitance			15	pF	(Note 12)
I_{CCS1}	Suspend with Slow Refresh		200	400	μA	(Note 8)
I_{CCS2}	Suspend without Slow Refresh		150	350	μA	(Note 8)
I_{CC}	Power Supply Current		50	100	mA	(Note 9)
D.C. SPECIFICATION FOR STANDARD ISA BUS SIGNALS						
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 24 mA (Note 3)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −4.0 mA (Note 3)
D.C. SPECIFICATION FOR PARALLEL PORT						
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 8 mA (Note 2)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −2.0 mA (Note 2)
D.C. SPECIFICATION FOR OPEN DRAIN OUTPUTS						
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 24 mA (Note 4) I_{OL} = 12 mA (Note 5) I_{OL} = 8 mA (Note 10)
D.C. SPECIFICATION FOR ALL OTHER OUTPUTS						
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 12 mA (Note 6)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −2.0 mA (Note 6)

Table 3-3. 82360SL I/O D.C. Specifications (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
D.C. SPECIFICATION FOR POWER-DOWN MODE						
VBATT	Battery Supply Voltage	2.5		5.5	V	(Note 15)
IBATT	Battery Supply Current		20 10	75 35	μA μA	VBATT = 5V (Note 7) VBATT = 2.5V (Note 7)
V_{IL}	PWRGOOD Low Input Voltage			0.8	V	
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 8 mA
V_{OH}	Output High Current	2.0			V	I_{OH} = −2 mA

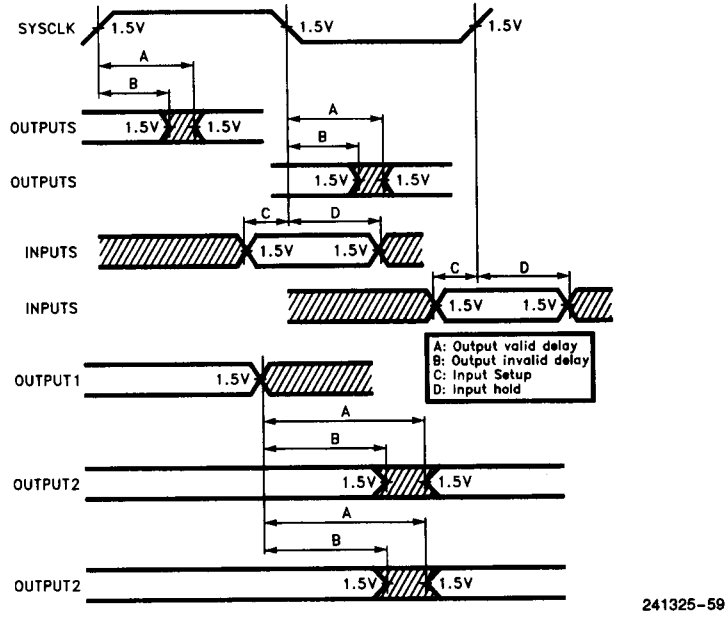
NOTES:
1. No pull-up or pull-down.
2. For outputs—LPTD7:0
3. For outputs—OSC, AEN, SA16:0, LA23:17, MEMR#, MEMW#, IOR#, IOW#, SMEMW#, SMEMR#, SBHE#, TC, SD7:0, XD7, HD7, RESETDRV.
4. ZEROWS#, IOCHRDY.
5. LPTSTROBE#, LPTAFD, LPTINIT#, LPTSLCTIN#, LPTDIR.
6. For all other outputs of the chip.
7. Measured at V_{CC} = 0V, V_{BATT} = 2.5V, 32 kHz RTC clock with input rise time and fall time, $t_r = t_f < 50$ ns.
8. Measured at V_{CC} = 5V, RTC clock at 32 kHz; Timer Clock, Serial clock and SYSCLK internally disabled; CL = 50 pF with outputs unloaded.
9. I_{CC} tests at maximum frequency with no resistive loads on the outputs.
10. REFRESH#
11. For all oscillators.
12. Characterized by design.
13. Min for system design reference only.
14. Max for system design reference only.
15. Power-down means V_{CC} = 0V. During normal operation when V_{CC} is on, the V_{BATT} should meet the following condition: $V_{CC} - 0.6V < RTCV_{CC} < V_{CC} + 0.6V$. Violating this condition may cause either excessive current drain from the V_{CC}/$RTCV_{CC}$ or back-drive into the RTC battery. Neither is desirable.

3.4 82360SL I/O Timing Specifications

A.C. Specification Definitions

The A.C. specifications given in the tables of the following pages consist of output delays, input setup and hold requirements. They may be relative to a clock edge or another signal edge. All 82360SL I/O clock related specifications reference SYSCLK. A.C. specifications are defined in Figure 3.4.1. All clock related specifications are tested at the voltage levels shown with a fully capacitive load only. Output specifications are derived from tested clock related timings.

The 5V and 3V columns in Table 3.4.1 indicate different modes of operation of the 82360SL. The 5V specifications apply when the 82360SL is used with a 5V ±10% power supply while the 3.3V specifications apply when the 82360SL is used with a 3.3V ±0.3V power supply.



NOTE:
Signal waveforms are not drawn to scale.

Figure 3.4.1. Drive Levels and Measurement Points for A.C. Specifications

Table 3-1. 82360SL I/O Timing Specifications

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 1	SYSCLK Period	125		125		ns		3.5.1	
It 2	SYSCLK Low Time @ V_{TT} = 1.5V	55		55		ns			
It 3	SYSCLK High Time @ V_{TT} = 1.5V	50		50		ns			
It 4	SYSCLK Rise Time and Fall Time		10		10	ns		3.5.2	
It 5a	RESETDRV from SYSCLK		125		125	ns	S		
It 6a	A20GATE Active (HIGH) Delay from KBDA20 Active (HIGH)		30		32	ns	SR	3.5.1	
It 6b	A20GATE Active (HIGH) Delay from SYSCLK		45		55	ns	SR		4
It 7	SYSCLK to KBDCLK Delay		30		60	ns			3, 4
It 8a	RC#/PERR#/IOCHCK# Pulse Width	250		250		ns		3.5.2	
It 8b	RC#/PERR#/IOCHCK# Setup to SYSCLK Falling Edge	12		12		ns		3.5.1	3
It 9a	Programmable CPURESET Active (HIGH) from SYSCLK	5	50	5	62	ns	FR, SR		4
It 10a	NMI Active (HIGH) from SYSCLK		125		130	ns	SR		3
It 10b	NMI Inactive from IOW# Active (LOW)	0		0		ns	FF		
It 11	RTCRESET# Pulse Width	5		5		ns			
It 14	BALE Hold from SYSCLK	2	45	2	45	ns		3.5.3, 3.5.7	
It 15	IOR#/IOW#/INTA# Input Active (LOW) Delay from SYSCLK Low		20		20	ns		3.5.1	
It 15a	IOR#/IOW#/MEMW# Output Active (LOW) Delay from SYSCLK		90		90	ns	SF	3.5.8	
It 16	IOR#/IOW#/INTA#/ MEMW#/MEMR# Input Inactive from SYSCLK		35		35	ns		3.5.3	
It 16a	IOR#/IOW# Output Inactive from SYSCLK		120		120	ns	SR	3.5.8	
It 17	ZEROWS# Output Active from SYSCLK		65		75	ns	SF	3.5.4	4
It 18	ZEROWS# Output Inactive from SYSCLK	0		0		ns	SR	3.5.4	

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 19	BALE Setup to SYSCLK (DMA Cycle)	18		18		ns		3.5.7	
It 20	IOCHRDY Input Active Setup to SYSCLK	15		15		ns			
It 20a	IOCHRDY Input Inactive Setup to SYSCLK	15		15		ns			
It 21	DMA8/16# Active Delay from SYSCLK		65		90	ns	SF		4
It 22	DMA8/16# Inactive Delay from SYSCLK (4 MHz DMACLK)		65		90	ns	SR		4
It 22a	DMA8/16# Inactive Delay from SYSCLK Low (8 MHz DMACLK)		65		90	ns	SR	3.5.23	4
It 23	AEN Active from HLDA Active		35		45	ns	SR	3.5.7	4
It 24	AEN Inactive Delay from HLDA Inactive		35		45	ns	SF	3.5.7	4
It 25	SA15:0, SBHE# Valid Delay from SYSCLK	10	120	10	135	ns	F, S	3.5.7	4
It 26	SA16 (Only if DMA8/16# = 0) SA15:0, SBHE# Valid Output Hold from SYSCLK	6		6		ns		3.5.10	
It 26a	SA16 (Only if DMA8/16 = 1), LA17:23 Valid Output Hold from IOR#/IOW#/MEMR#/ MEMW# Output	10		10		ns		3.5.24	
It 26f	SA16:0, LA17:23, SBHE# Float Delay from SYSCLK		90		90	ns	S	3.5.10	4
It 27	DACKx# Active Delay from SYSCLK (4 MHz DMACLK)		75		92	ns	SF	3.5.7	4
It 27a	DACKx# Active Delay from SYSCLK Low (8 MHz DMACLK)		75		92	ns	SF	3.5.8	4
It 28	DACKx Inactive Delay from SYSCLK (4 MHz DMACLK)		75		92	ns	SR	3.5.7	4
It 28a	DACKx Inactive Delay from SYSCLK (8 MHz DMACLK)		75		92	ns	SR	3.5.8	
It 29	IOR#/IOW#/MEMW# Float-to-Drive-Inactive from SYSCLK		75		75	ns		3.5.23	
It 30	IOR#/IOW#/MEMW# Float Delay from SYSCLK		75		75	ns		3.5.23	
It 30a	SMRAMCS# Setup to MEMR#/MEMW# Active	10		10		ns	FF	3.5.11	

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 31	MEMR#/MEMW# Input Active Delay from SYSCLK		70		70	ns		3.5.11	
It 31a	MEMR#/MEMW# Output Active Delay from SYSCLK		70		70	ns	SF	3.5.8	
It 32a	MEMR#/MEMW# Output Inactive Delay from SYSCLK		75		105	ns	SR	3.5.7	4
It 33	T/C Active Delay from SYSCLK		85		94	ns	SR	3.5.7	4
It 34	T/C Inactive Delay from SYSCLK		85		90	ns	SF	3.5.7	4
It 35	TIM2CLK2 Period	125		125		ns		3.5.2	
It 36	TIM2CLK2 Low Time	55		55		ns			
It 37	TIM2CLK2 High Time	55		55		ns			
It 38	TIM2CLK2 Rise Time		25		25	ns			
It 39	TIM2CLK2 Fall time		25		25	ns			
It 40	TIM2GAT2 High Pulse Width	45		45		ns		3.5.22	
It 41	TIM2GAT2 Low Pulse Width	45		45		ns			
It 42	TIM2GAT2 Setup to TIM2CLK2	45		45		ns			
It 43	TIM2GAT2 Hold from TIM2CLK2	45		45		ns		3.5.22	
It 44	TIM2OUT2 from TIM2CLK2 High to Low		110		110	ns	SR		
It 45	TIM2OUT2 from TIM2GAT2 High to Low		110		110	ns	SR		
It 46	SPKR Active Delay from TIM2GAT2 (When EXTAUD is Set)		120		120	ns	SR		
It 50	REFRESH# Active to MEMR# Output Active	150		150		ns	FF	3.5.10	
It 52	Address Valid to MEMR# Active	40		40		ns	S, SF		
It 53	MEMR# Output Inactive from IOCHRDY Input, Low to High (during a Master Refresh)	125		125		ns	FR		
It 55	IOCHRDY Pulse Width		750		750	ns			
It 56	MEMR# Output Pulse Width for Refresh	2		2		SYSCLK			
It 59	FLPCS#/C8042CS# Active Setup to Command Active	10		10		ns	FF	3.5.13	
It 59a	HDCS0#/NDCS1# Active Setup to Command Active	45		30		ns	FF		
It 60	FLPCS#/C8042CS#/ HDCS0#/HDCS1# Output Hold from Command Inactive	10		10		ns	FR		

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 60a	SMRAMCS# Hold from MEMR#/MEMW#	10		10		ns		3.5.11	
It 69	DRQx Setup to SYSCLK High to Low	0		0		ns		3.5.5	
It 78	EXTSMI# Input Pulse Width	1		1		SYSCLK		3.5.26	
It 79	EXTRTCAS Pulse Width	3	4	3	4	SYSCLK		3.5.14	
It 80	IOCS16# Setup to Command	10		10		ns		3.5.18	
It 81	IOCS16# Hold from Command	10		10		ns		3.5.18	
It 82	STPCLK# Delay from SYSCLK		100		100	ns	SF	3.5.25	
It 82a	STPCLK# Output Pulse Width	2		2		SYSCLK			
It 83	SMI# from SYSCLK		100		100	ns	SF		
It 84	SMOUTx from SYSCLK		110		130	ns	S		4
It 85	SUS_STAT# from SYSCLK		100		100	ns	SF		3
It 86	IOCHRDY Output High to Low from Command		24		34	ns	SF	3.5.23	4
It 94	Delay from IOW# to Modem Output (RTS#, DTR#)		200		200	ns	SF	3.5.20	
It 109	KBDCLK Period (8 MHz)	125		125		ns		3.5.2	
	KBDCLK Period (4 MHz)	250		250		ns			
	KBDCLK Period (2 MHz)	500		500		ns			
It 110	KBDCLK High Time (8 MHz)	40		40		ns			
	KBDCLK High Time (4 MHz)	95		95		ns			
	KBDCLK High Time (2 MHz)	200		200		ns			
It 111	KBDCLK Low Time (8 MHz)	40		40		ns		3.5.2	
	KBDCLK Low Time (4 MHz)	95		95		ns			
	KBDCLK Low Time (2 MHz)	200		200		ns			
It 117	HRQ Inactive to HLDA Inactive	185		185		ns	FF	3.5.5	

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 118	HLDA Inactive to HRQ Active (Back to Back Hold Acknowledge Cycles)	0		0		ns	FR		3
It 120	IRQ1, 6, 10: 12, 14, 15, ERROR#, IRQ# Inactive Pulse Width	100		100		ns			
It 121	INTR Output Delay from IRQ1, 6, 10: 12, 14, 15, ERROR#, IRQ8#		100		100	ns	SR		
It 122	Data Output Valid from INTA# Active		120		154	ns	S	3.5.21	4
It 123	Data Output Hold from INTA# Inactive	5		5		ns	F		
It 123f	Data Float from INTA# Inactive		35		35	ns			
It 124a	SD7 Read Data Output Hold from MEMR# Inactive	5		5		ns		3.5.11	
It 124f	SD7 Float from MEMR# Inactive		35		35	ns		3.5.11	
It 125	Write Data Input Setup to MEMW# Active	40		40		ns			
It 125a	XD7 Output Valid from MEMW# Active		60		65	ns	S		
It 126	Write Data Input Hold from MEMW	15		15		ns		3.5.12	
It 126a	XD7 Output Hold from MEMW# Inactive	5		5		ns	F		
It 126f	XD7 Float from MEMW# Inactive		45		45	ns			
It 129	SMEMR#/SMEMW# Active from MEMR#/MEMW#		30		39	ns	SF		4
It 129a	SMEMR#/SMEMW# Inactive from MEMR#/MEMW# Inactive	3	30	3	35	ns	FR, SR		4
It 130	LOMEM# Output Active Setup to MEMR#/MEMW# Input Active	3		3		ns	FF	3.5.11	
It 130a	LOMEM# Output Inactive Setup to MEMR#/MEMW# Input Active	5		5		ns	FR		

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 140	LPTSTROBE#/LPTSLCTIN#/ LPTAFD# Output Delay from Command		45		60	ns	SF	3.5.27	1, 4
It 141	LPTD Output from LPTSTROBE#/LPTSLCTIN#/ LPTAFD# Active		15		30	ns	SF, S		1, 4
It 142	LPTD Output Hold from LPTSLCTIN#/LPTAFD# Inactive	50		50		ns	SR, S		1
It 143	LPTD Input Setup to LPTSLCTIN#/LPTAFD# Inactive during Read	210		210		ns			1
It 144	LPTD Input Hold from LPTSLCTIN#/LPTAFD# Inactive during Read	0		0		ns			1
It 145	IOCHRDY Output Low from LPTBUSY Low		40		40	ns	SF		1
It 200	BALE Active from SYSCLK Low	2	35	2	35	ns		3.5.3	
It 201	Write Data Input Setup to IOW# Active	40		40		ns		3.5.3	
It 202	Write Data Input Hold from IOW# Inactive	25		25		ns		3.5.3	
It 203	Read Data Output Setup to IOR# Inactive	62		62		ns	F		
It 204	Read Data Output Hold from IOR# Inactive	5		5		ns	F		
It 204f	Data Bus Float from IOR#/ MEMR#		35		35	ns			
It 205	BALE Active Pulse Width	50		50		ns			
It 206	SA Address Input Valid Setup to BALE Inactive	40		40		ns			
It 208a	LA Address Input Valid Setup to BALE Active	40		40		ns		3.5.11	
It 208b	LA Address Input Valid Hold from BALE Inactive	55		55		ns		3.5.11	
It 209	IOW# to EXTRTCAS		130		130	ns	SR	3.5.15	
It 210	XD7 Output Valid from IOW# Active		60		70	ns	S	3.5.14	4
It 211	XD7 Output Hold from IOW# Inactive	5		5		ns	F	3.5.14	
It 211f	XD7 Output Float from IOW# Inactive		45		45	ns		3.5.14	
It 212	EXTRTCRW#/EXTRTCDS Active from Command Active		50		65	ns	SF, SR	3.5.16	4
It 213	EXTRTCRW#/EXTRTCDS Hold from Command Inactive		35		50	ns	SR, SF	3.5.16	4

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 214	XDEN# Output Delay from IOR#/IOW#, MEMR#/MEMW# Inputs	10	75	10	90	ns	FF, SF	3.5.11	4
It 214a	XDEN# Output Delay from IOR#/IOW# Output	5	75	5	75	ns	FF, SF	3.5.24	
It 215a	XDEN# Output Active from XDIR Output Active	0		0		ns	FR, FF	3.5.11	
It 215b	XDIR Output Inactive from XDEN# Output Inactive	5		5		ns	FR, FF	3.5.11	
It 216a	SD7 Read Data Output Delay from XD7 Input		35		50	ns	S	3.5.11	4
It 216b	SD7 Read Data Output Delay from HD7 Input		50		50	ns	S	3.5.18	
It 217	SD7 Read Data Output Hold from IOR# Inactive	5		5		ns	F	3.5.13	
It 217f	SD7 Float from IOR# Inactive		35		35	ns		3.5.13	
It 218	Address Input Hold from Command Inactive	40		40		ns		3.5.3	
It 219	HDENL#/HDENH# Output Active Delay from Command		35		50	ns	SF	3.5.18	4
It 219a	HDENL#/HDENH# Output Inactive Delay from Command Inactive	5		5		ns	FR	3.5.18	
It 220	HD7 Output Valid from IOW# Active		45		70	ns	S	3.5.19	4
It 221	HD7 Output Hold from IOW# Inactive	10		10		ns	F	3.5.19	
It 221f	HD7 Output Float from IOW# Inactive		35		35	ns		3.5.19	
It 223	HALT# Input Valid from SYSCLK Low		20		20	ns		3.5.1	
It 224	XD7/HD7 Input Setup to IOR#/MEMR#	100		115		ns		3.5.13	4
It 225	XD7/HD7 Input Hold from IOR#/MEMR#	5		5		ns		3.5.13	
It 230	XD7 Output Valid from EXTRTCRW# Active		35		35	ns	S	3.5.17	
It 231	XD7 Output Hold from EXTRTCRW# Inactive	0		0		ns	F	3.5.17	

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 231f	XD7 Output Float from EXTRTCRW#		35		35	ns		3.5.17	
It 250	BATTDEAD# Inactive from Stable RTCVCC	2		2		ns		3.5.26	2
It 251	EXTSMI# Active to SMI# Active (for Minimum Programmed Count)	1	2.1	1	2.1	ns			2
It 252	SMI# Active from SRBTN#/BATT Low# Active (for Minimum Programmed Count)	128	256	128	256	ns			2
It 253	Advanced Power Management (APM) SMI# Active from IOW# Active	2	3	2	3	SYSCLK	FF, SF		2
It 254	COMARI#/COMBRI#/ SRBTN# Pulse Width	1		1		RTCCLK			2
It 305	SA16, LA23:17 Valid Delay from SYSCLK	10	165	10	197	ns	F, S	3.5.7	4
It 311	HRQ Output Active from SYSCLK		45		55	ns	SR	3.5.6	4
It 312	HLDA Setup to SYSCLK	18		18		ns			
It 312a	HLDA Hold from SYSCLK	10		19		ns			
It 314	HRQ Inactive from SYSCLK	5		5		ns	FF		
It 317	REFREQ Active from SYSCLK		45		62	ns	SR		4
It 319	REFREQ Inactive from SYSCLK		45		60	ns	SF		4
It 320	Normal REFREQ to Slow REFREQ Delay (when Going to Suspend)	0.5	2	0.5	2	RTCCLK		3.5.24	
It 321	Slow REFREQ Active Delay to SUS_STAT# Active	2	2	2	2	RTCCLK		3.5.24	
It 322	MASTER# Active to REFRESH# Input Active Delay	25		25		ns		3.5.9	
It 324	REFRESH# Output Active from HLDA		35		37	ns	SF	3.5.6	

Table 3-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	5V		3.3V		Unit	Derating	Figure	Notes
		Min	Max	Min	Max				
It 325	REFRESH# Output Inactive from SYSCLK	5		5		ns	FR	3.5.6	
It 326	REFRESH# Input Active to REFREQ Active		30		35	ns	SR	3.5.9	
It 327	REFRESH# Input Inactive to REFREQ Inactive	0		0		ns	FF	3.5.9	
It 328	REFRESH# Pulse Width	4	5	4	5	SYSCLK		3.5.6	
It 329	REFREQ Pulse Width during Master# Cycle	4	5	4	5	SYSCLK		3.5.9	
It 330	DACKx# to MASTER# Delay	0		0		ns	SF, SF		
It 331	AEN Delay from MASTER#	0	49	0	49	ns	FR, FF, SR, SF		
It 332	Alternate Master Drives Address and Data		125		125	ns			
It 333	MASTER# Delay from DRQx Inactive		100		100	ns	SF		
It 334	Alternate Master Tri-States Bus Signal	0		0		ns			

NOTES:
1. Fast parallel port specifications are applicable for I/O accesses to ports 37B–37F and 27B–27F.
2. These specifications are for power management.
3. These specifications are for test purposes only.
4. These specifications have different values for 5V and 3.3V operation.

3.5 82360SL I/O Timing Diagrams

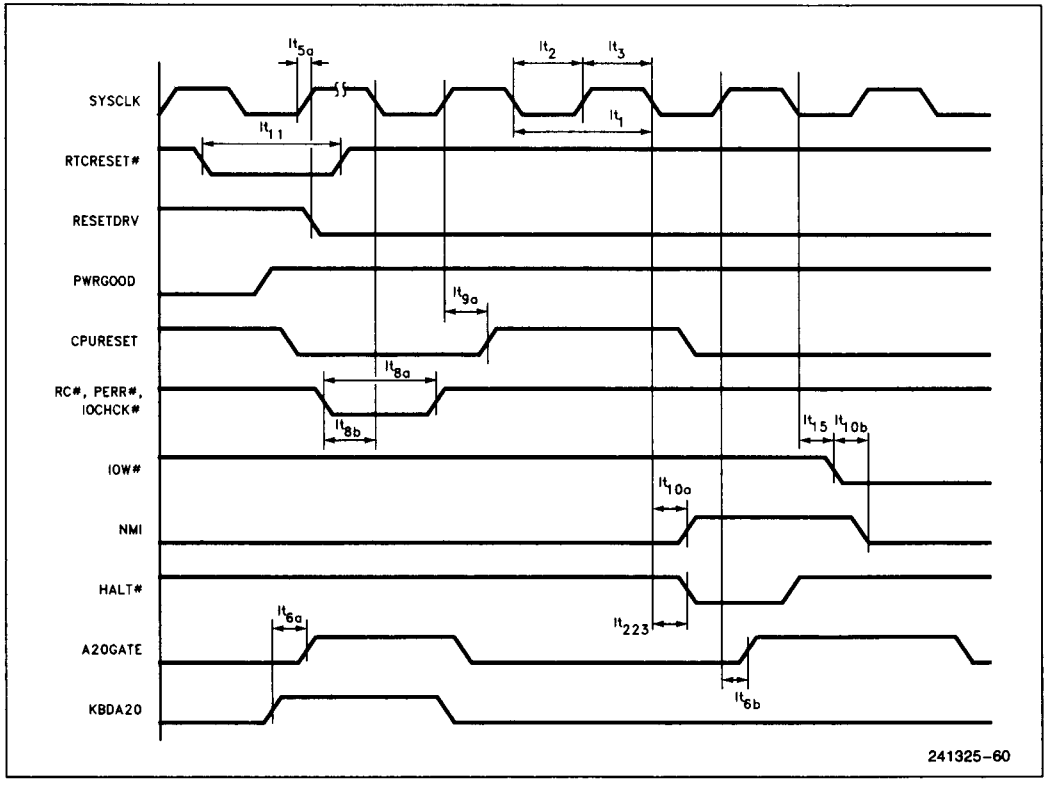


Figure 3.5.1. CPURESET, NMI, A20GATE and RC# Timings

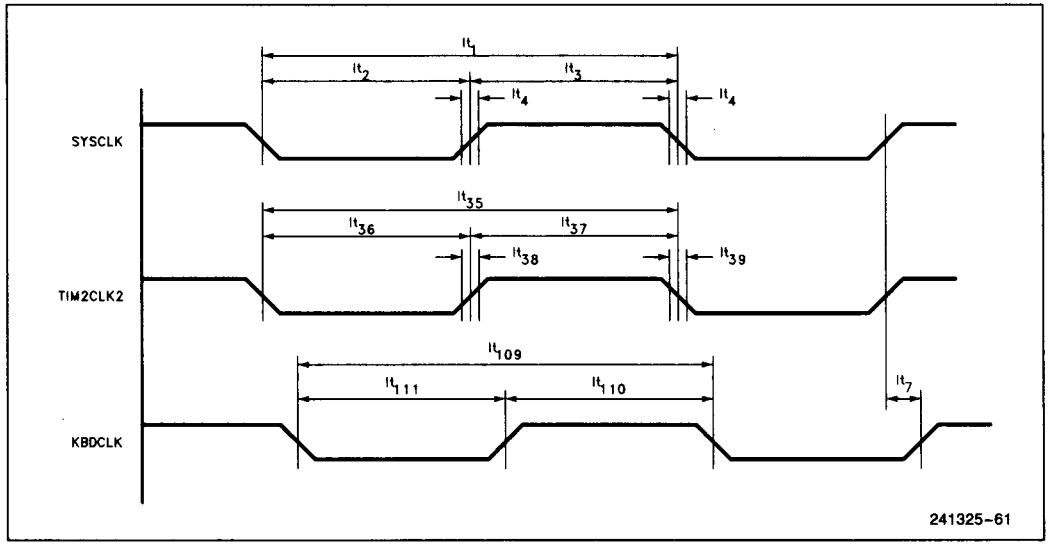


Figure 3.5.2 Clock Timings

3.5 82360SL I/O Timing Diagrams (Continued)

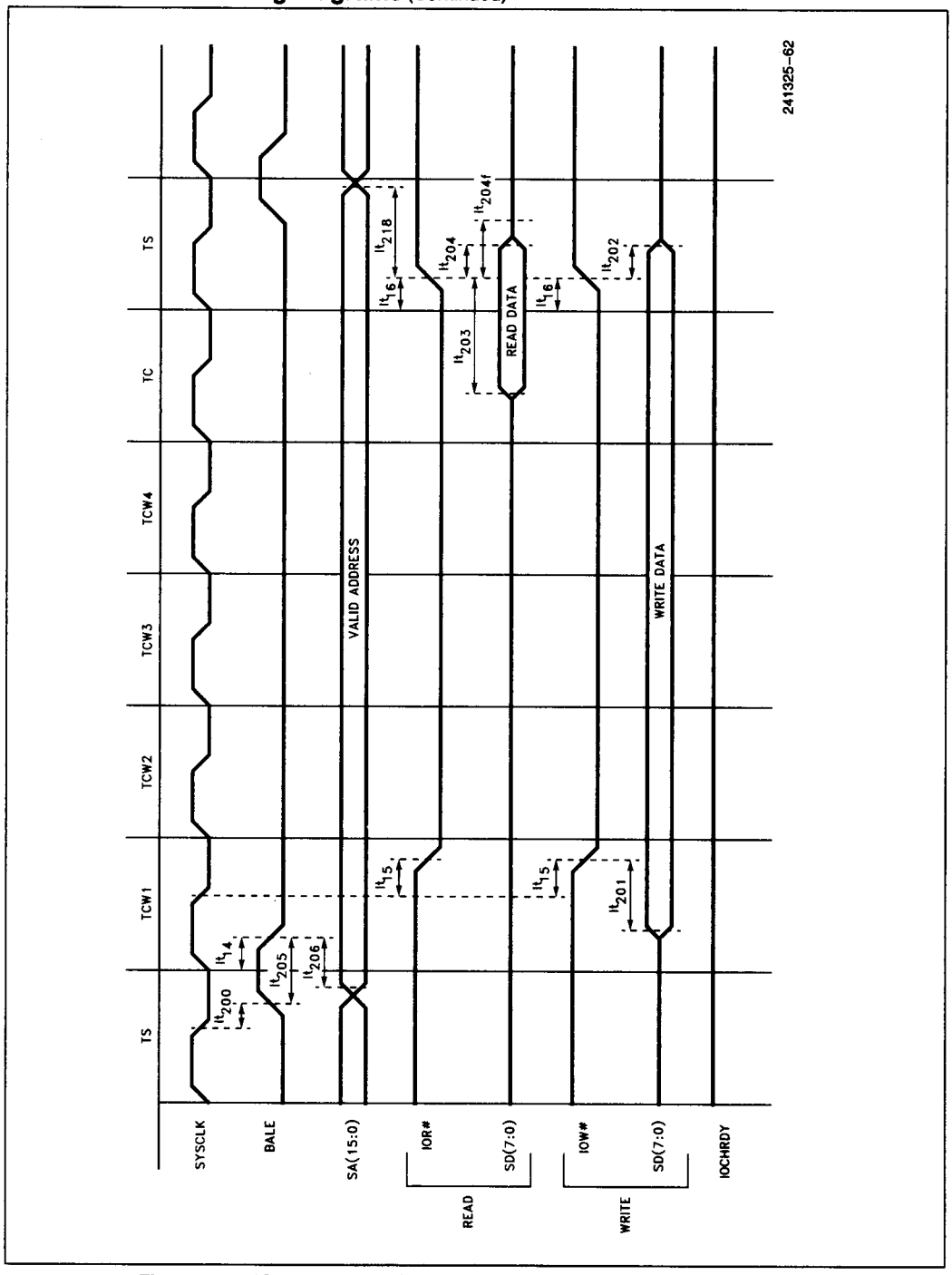


Figure 3.5.3. ISA Bus 8-Bit I/O Read/Write Default Bus Cycle (6 SYSCLKs)

3.5 82360SL I/O Timing Diagrams (Continued)

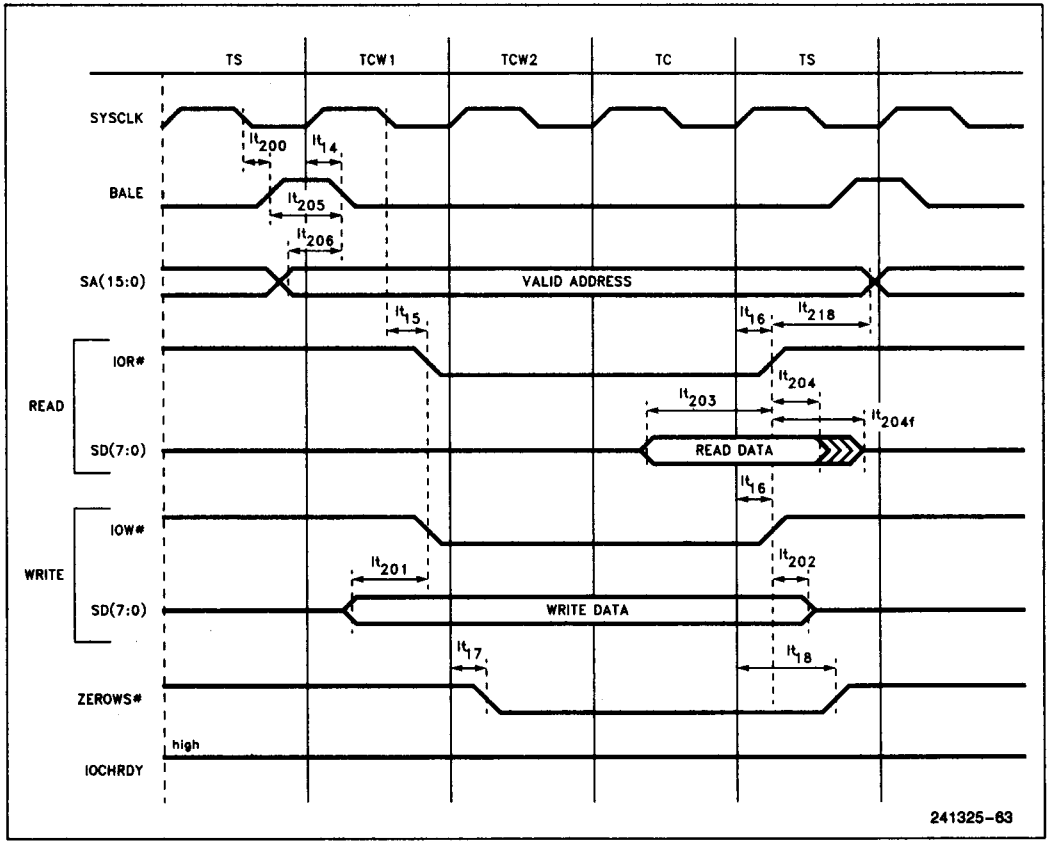


Figure 3.5.4. ISA Bus 8-Bit I/O Read/Write Compressed Bus Cycle

3.5 82360SL I/O Timing Diagrams (Continued)

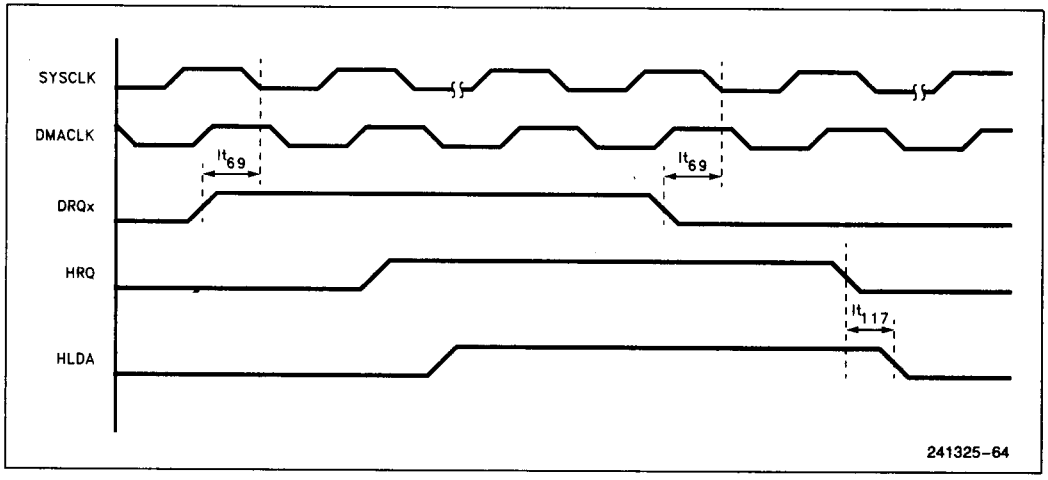


Figure 3.5.5. DMA Controller Timings

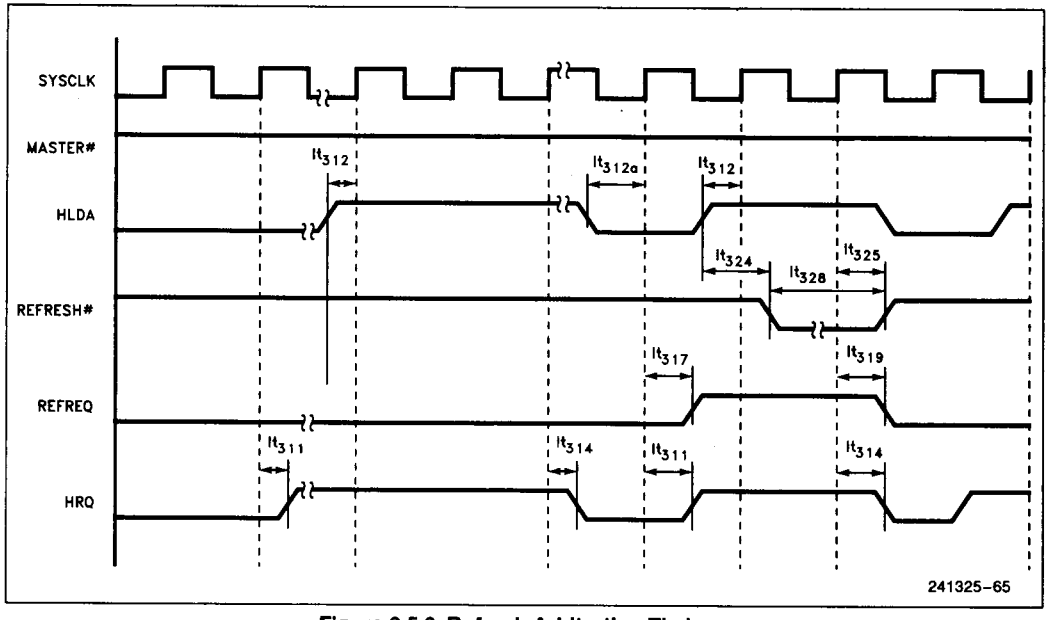


Figure 3.5.6. Refresh Arbitration Timings

3.5 82360SL I/O Timing Diagrams (Continued)

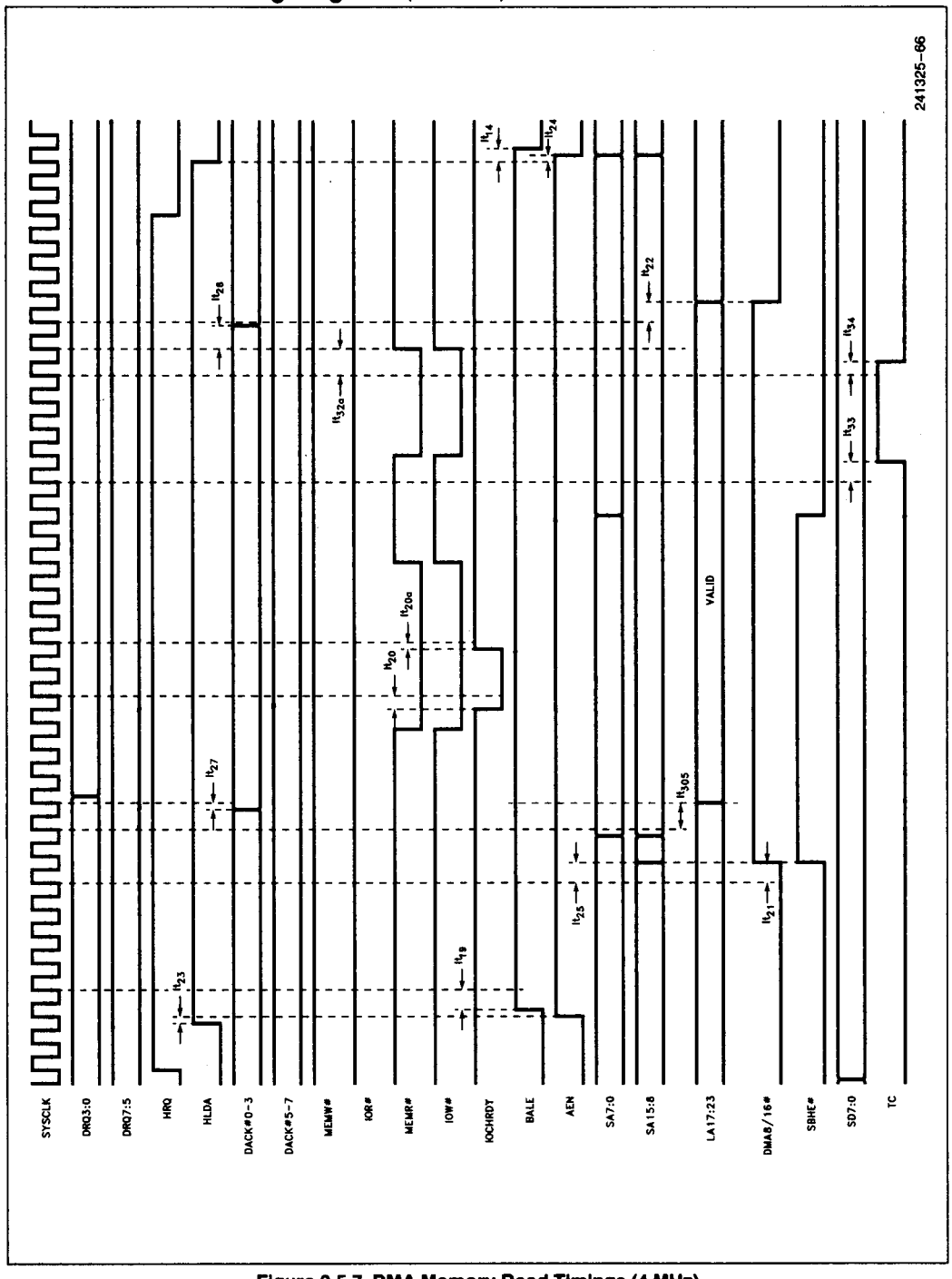


Figure 3.5.7. DMA Memory Read Timings (4 MHz)

3.5 82360SL I/O Timing Diagrams (Continued)

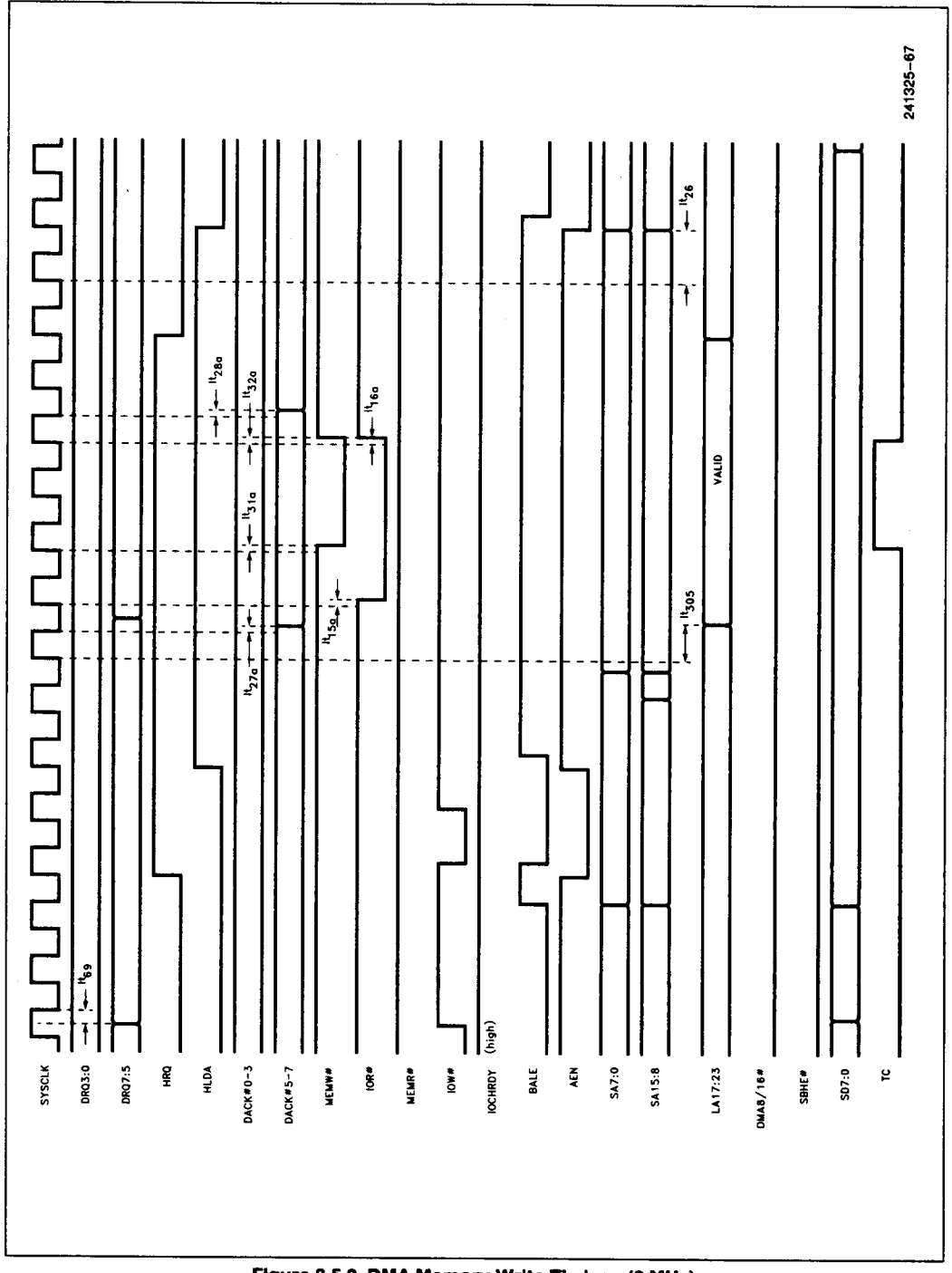


Figure 3.5.8. DMA Memory Write Timings (8 MHz)

3.5 82360SL I/O Timing Diagrams (Continued)

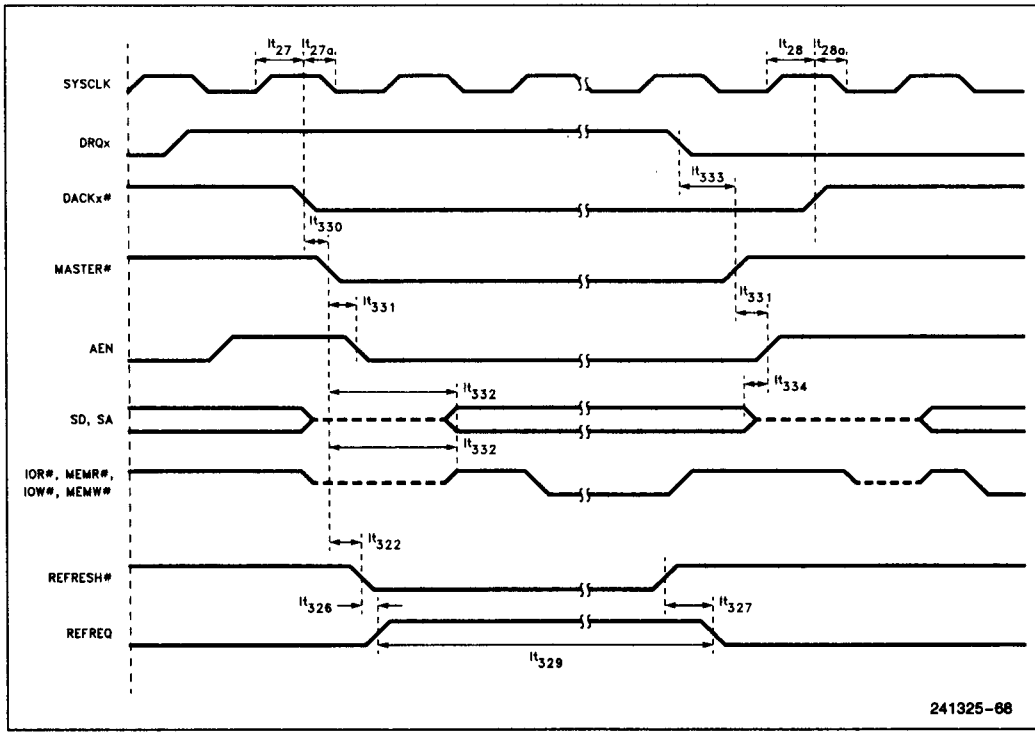


Figure 3.5.9. Bus Master Refresh Cycle Timings

3.5 82360SL I/O Timing Diagrams (Continued)

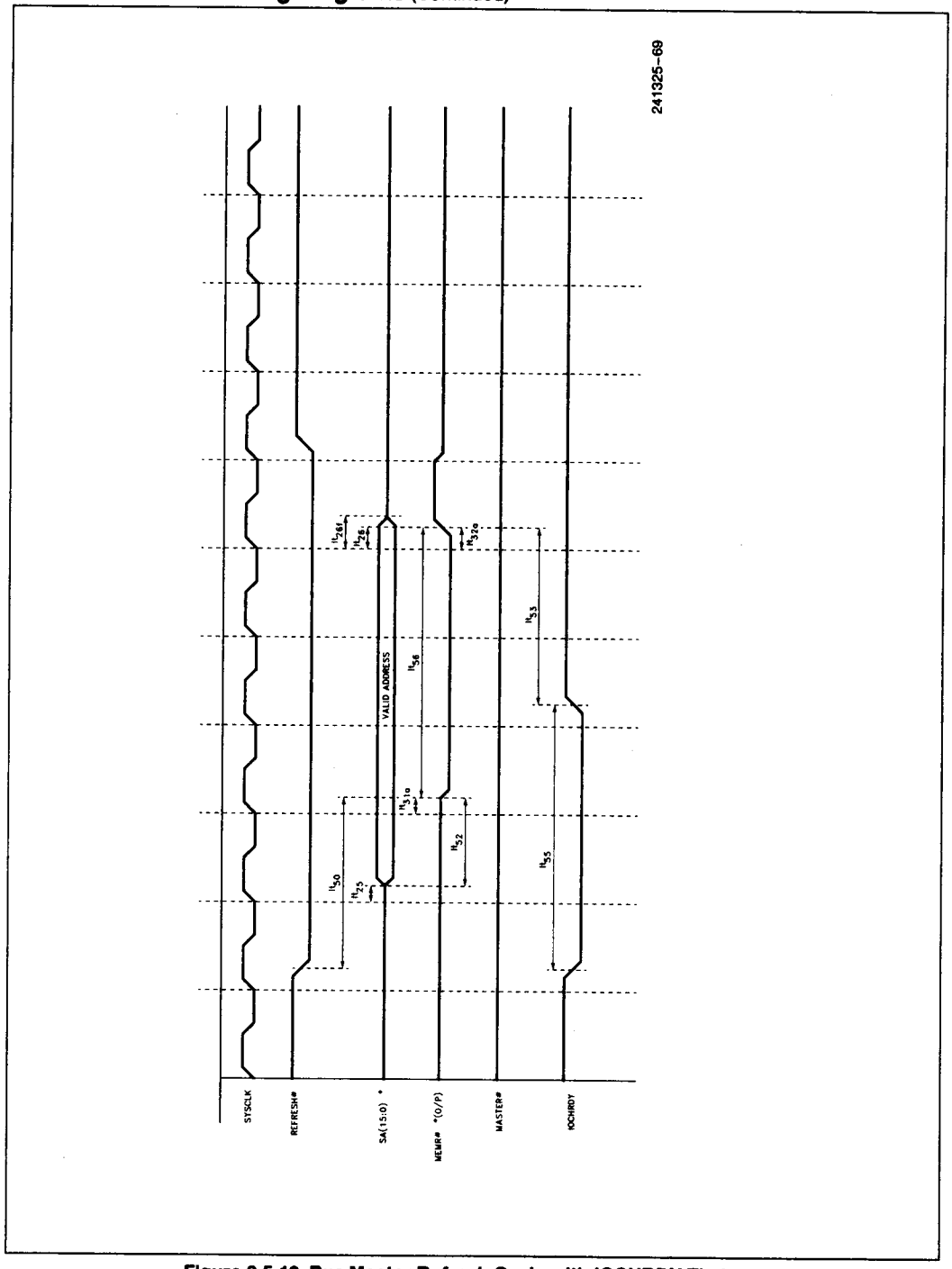


Figure 3.5.10. Bus Master Refresh Cycle with IOCHRDY Timings

3.5 82360SL I/O Timing Diagrams (Continued)

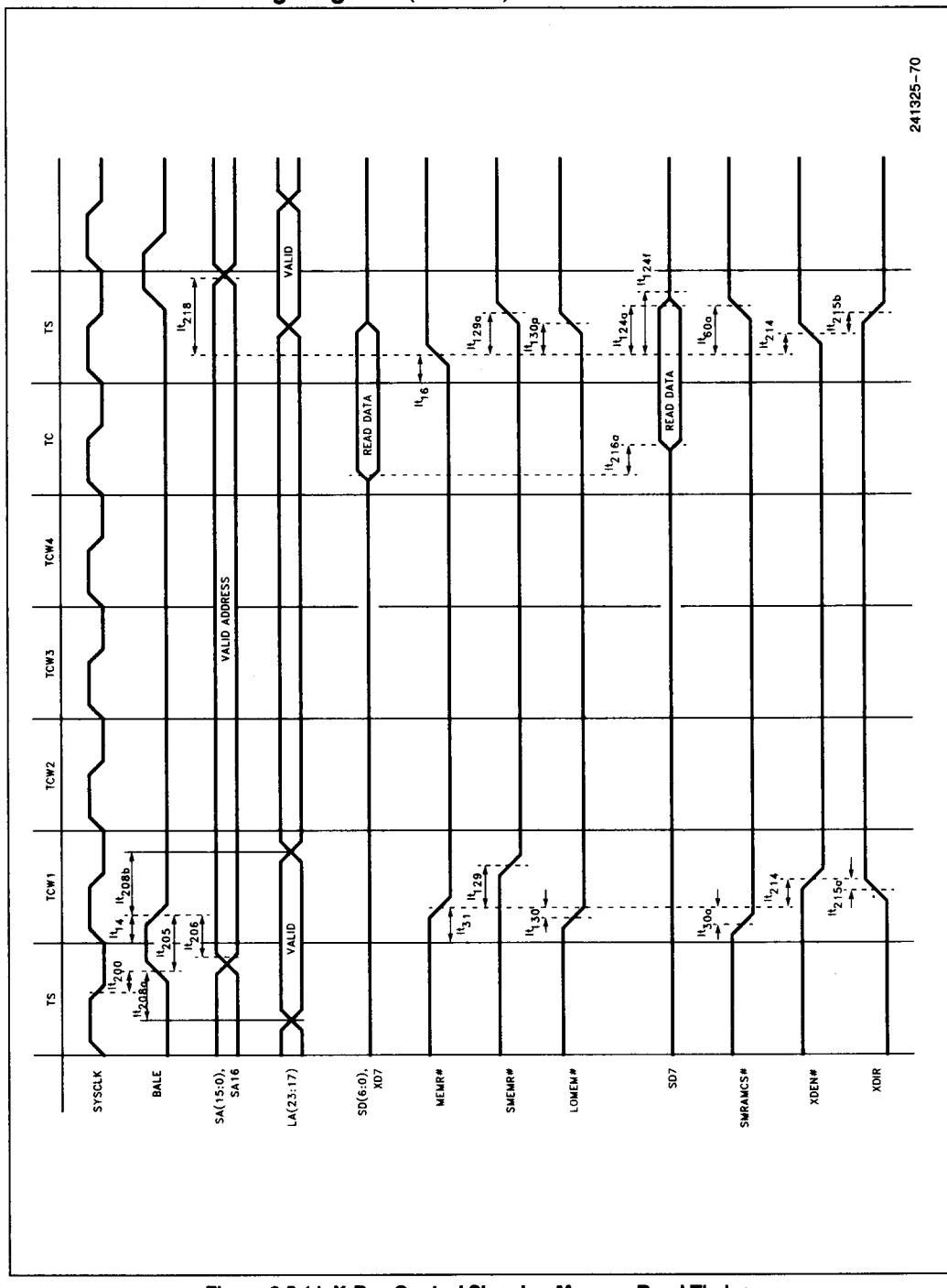


Figure 3.5.11. X-Bus Control Signals—Memory Read Timings

3.5 82360SL I/O Timing Diagrams (Continued)

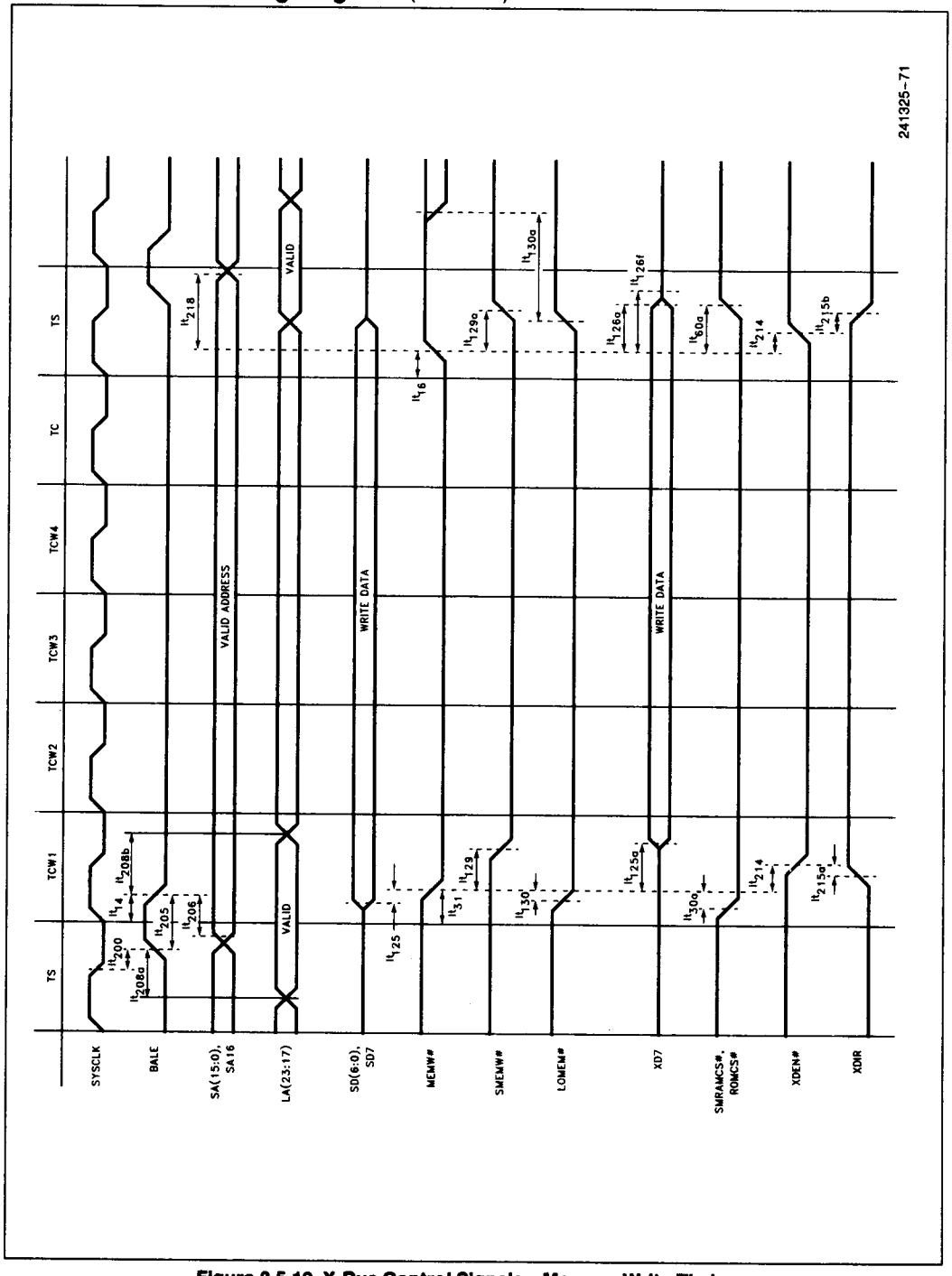


Figure 3.5.12. X-Bus Control Signals—Memory Write Timings

3.5 82360SL I/O Timing Diagrams (Continued)

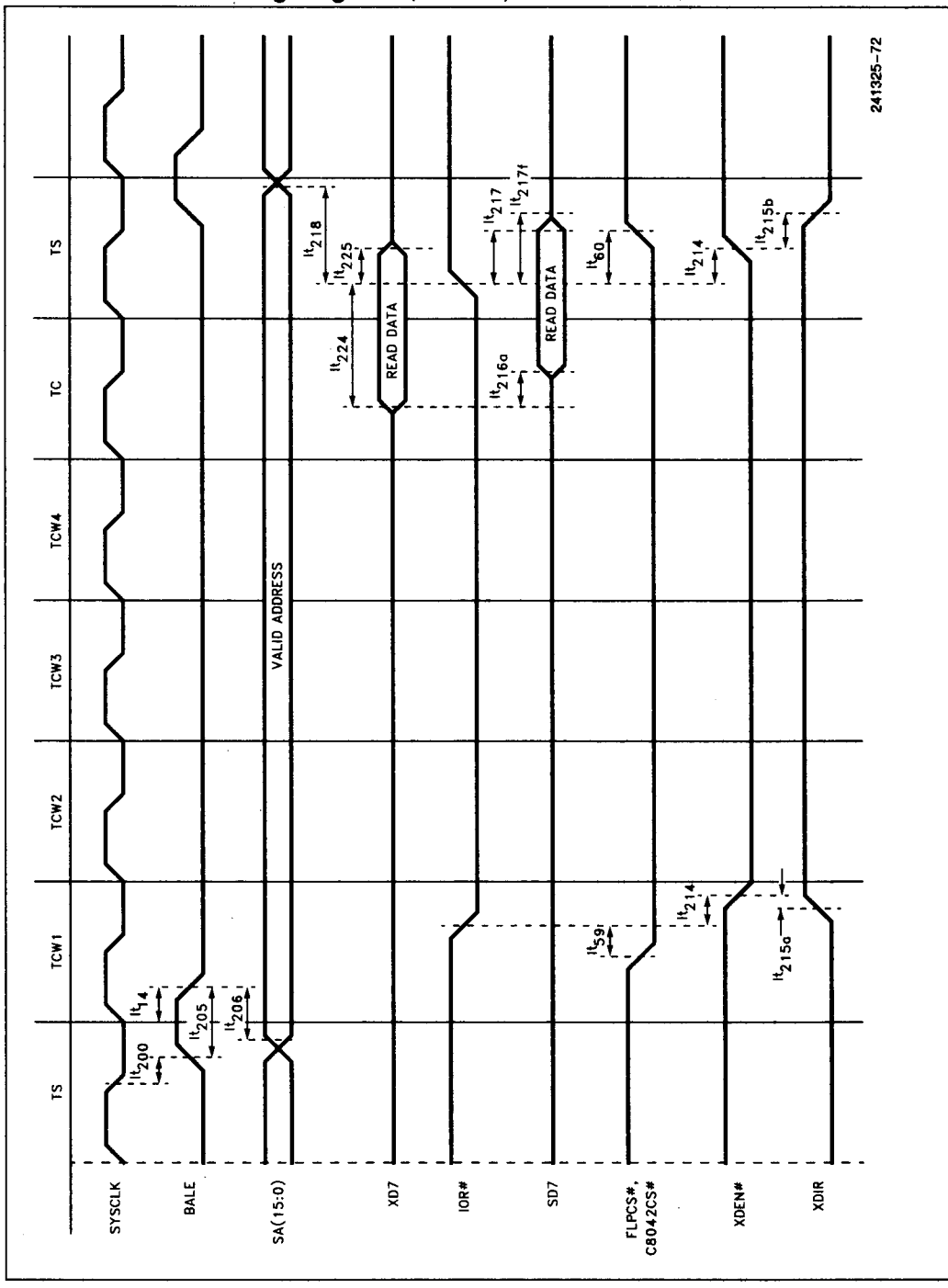


Figure 3.5.13. X-Bus Control Signals—I/O Read Timings

3.5 82360SL I/O Timing Diagrams (Continued)

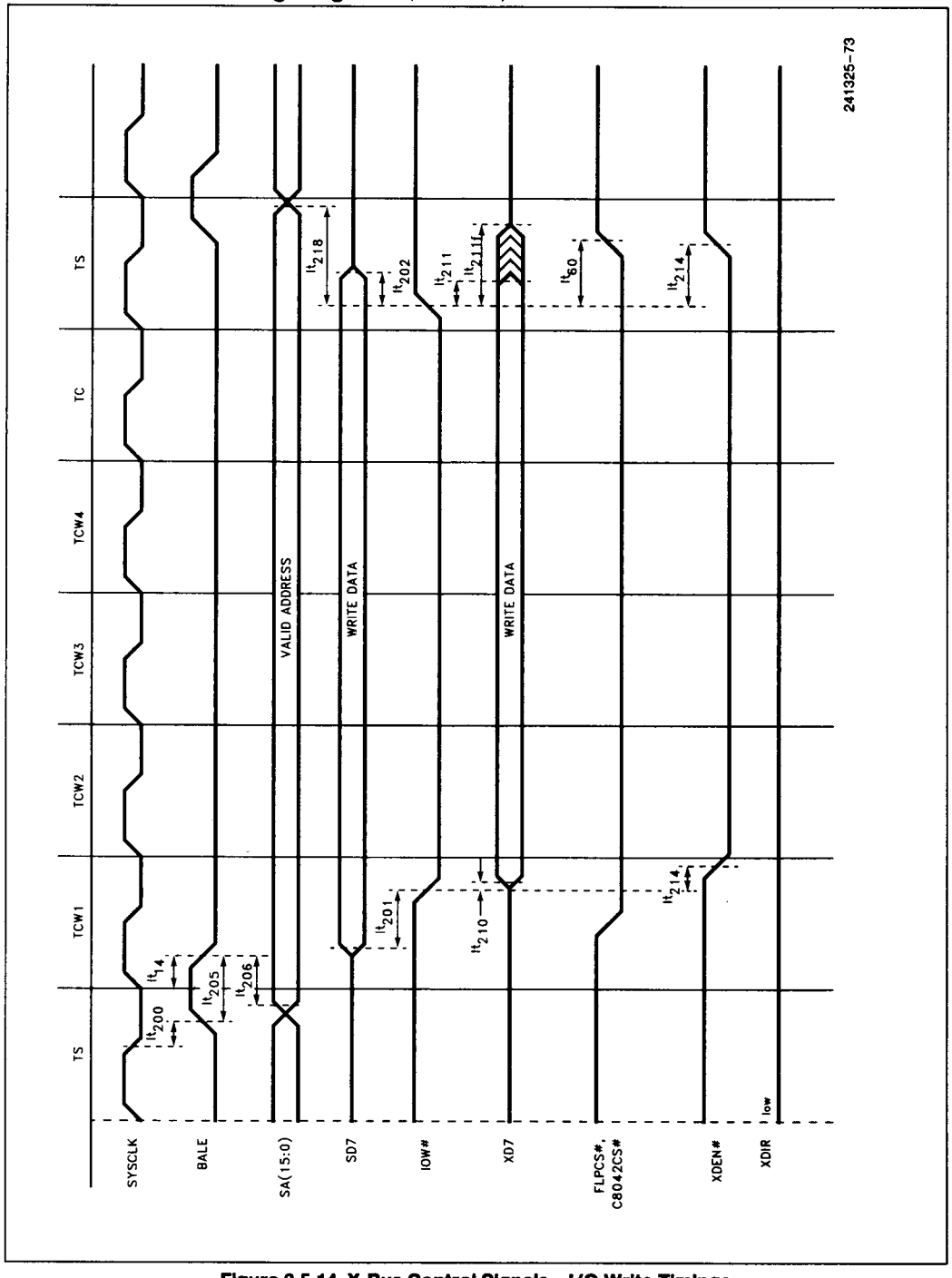


Figure 3.5.14. X-Bus Control Signals—I/O Write Timings

3.5 82360SL I/O Timing Diagrams (Continued)

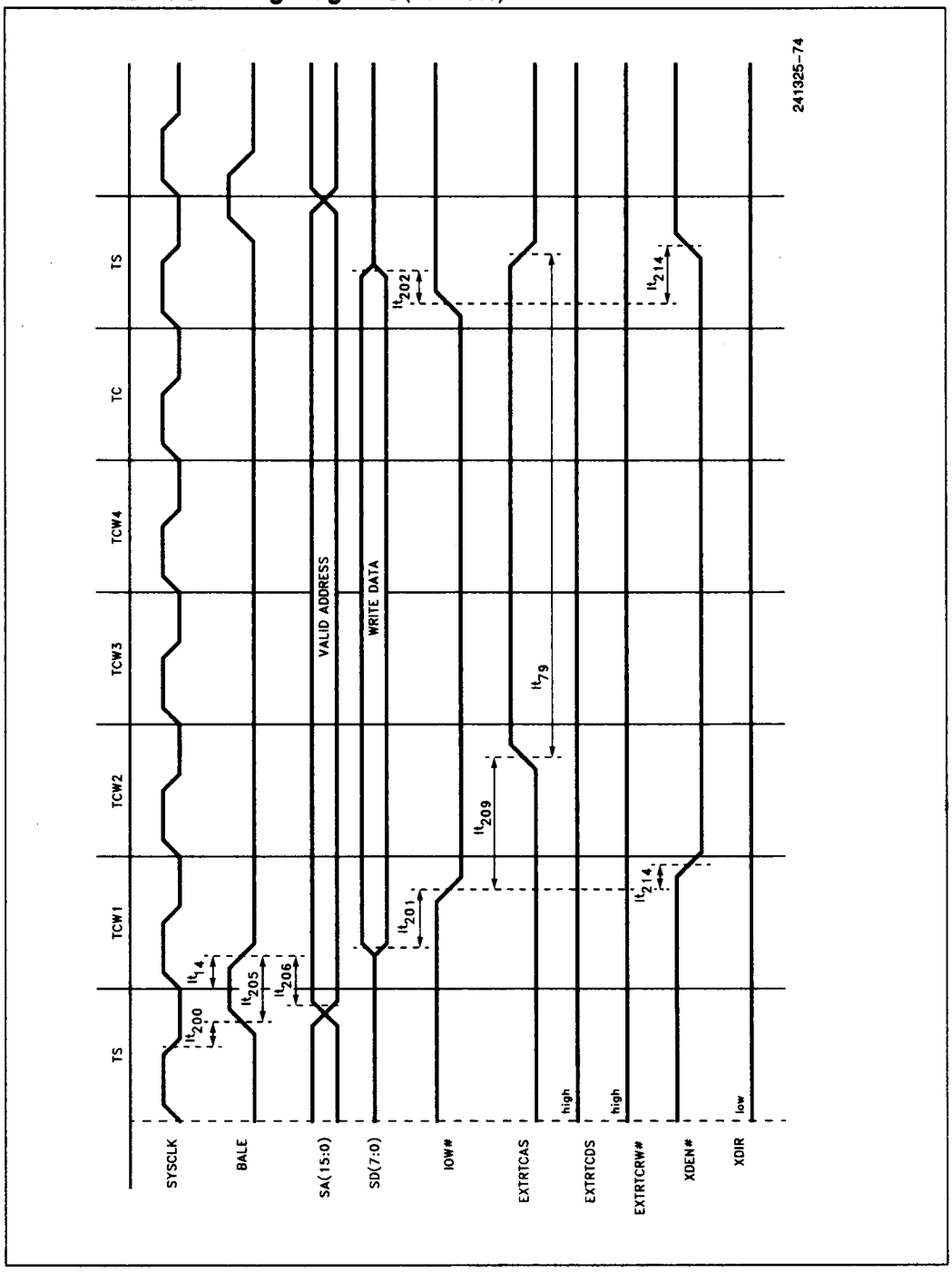


Figure 3.5.15. I/O Port 70 Hex Write—External RTC Timings

3.5 82360SL I/O Timing Diagrams (Continued)

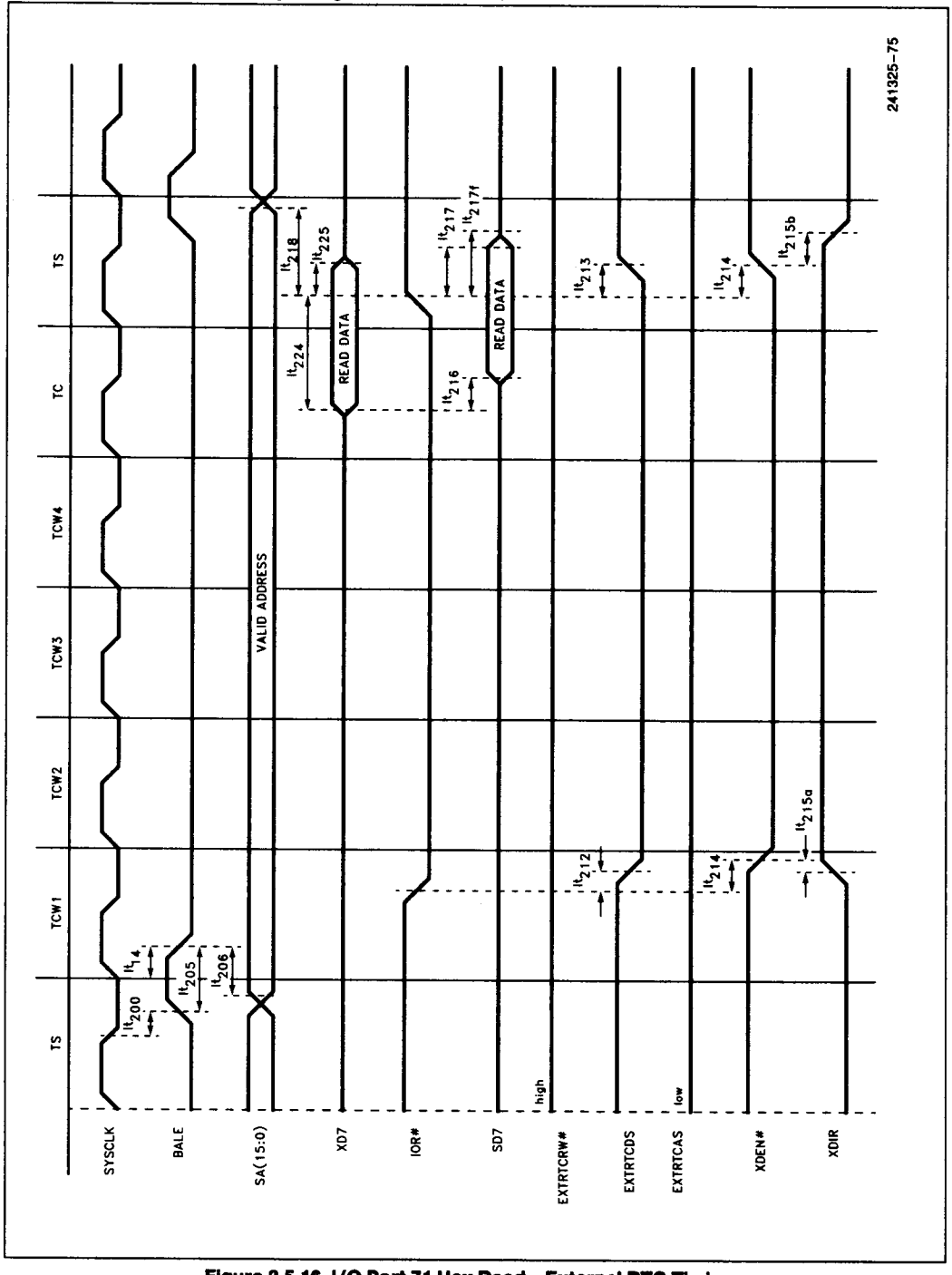


Figure 3.5.16. I/O Port 71 Hex Read—External RTC Timings

3.5 82360SL I/O Timing Diagrams (Continued)

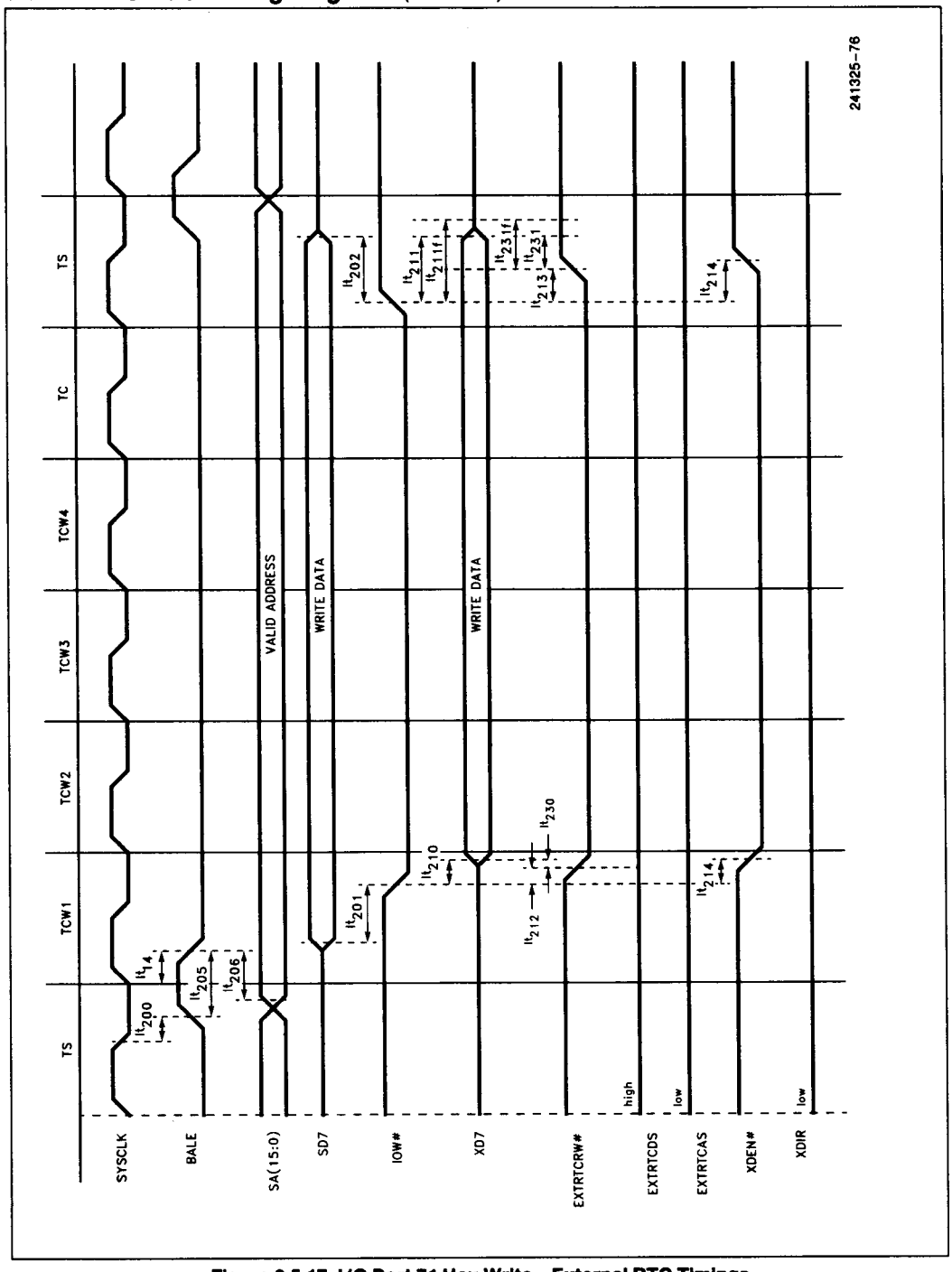


Figure 3.5.17. I/O Port 71 Hex Write—External RTC Timings

3.5 82360SL I/O Timing Diagrams (Continued)

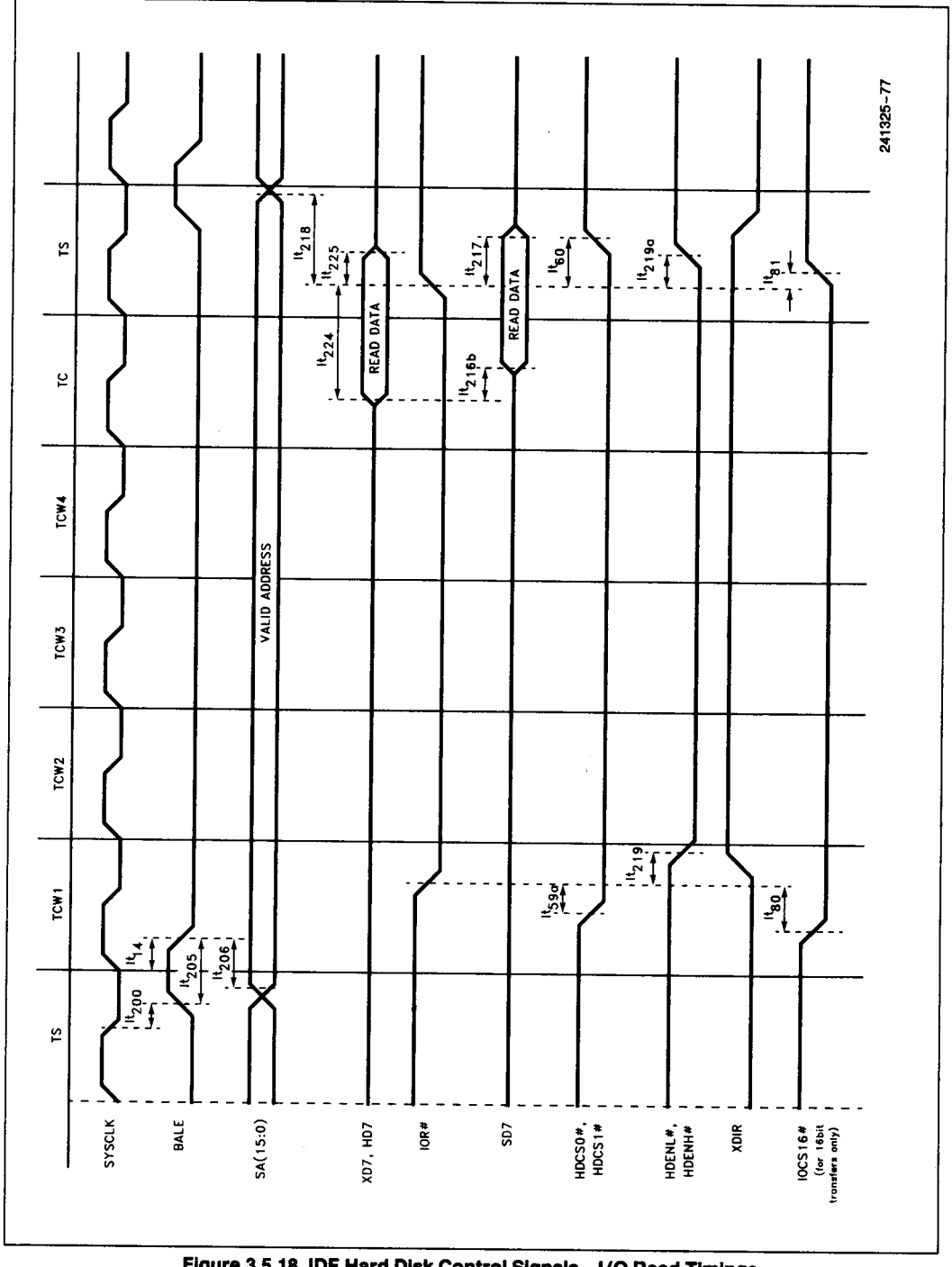


Figure 3.5.18. IDE Hard Disk Control Signals—I/O Read Timings

3.5 82360SL I/O Timing Diagrams (Continued)

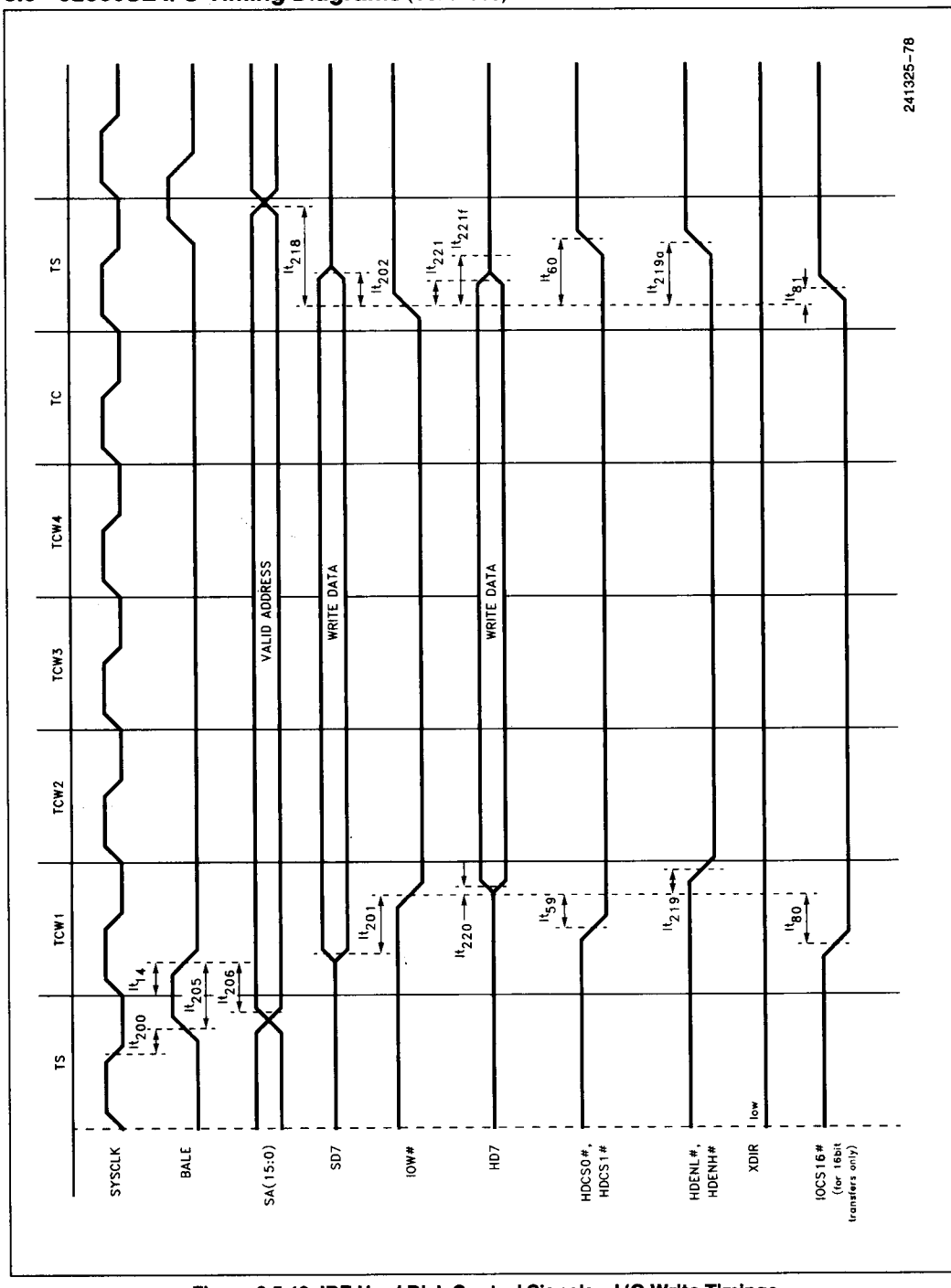


Figure 3.5.19. IDE Hard Disk Control Signals—I/O Write Timings

3.5 82360SL I/O Timing Diagrams (Continued)

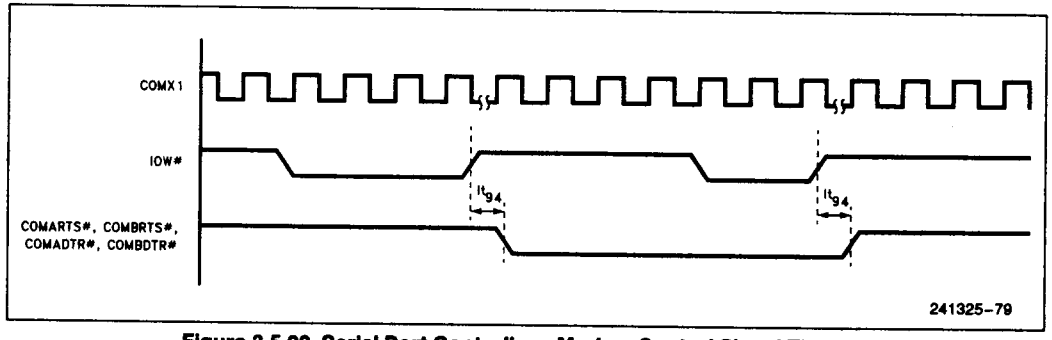


Figure 3.5.20. Serial Port Controller—Modem Control Signal Timings

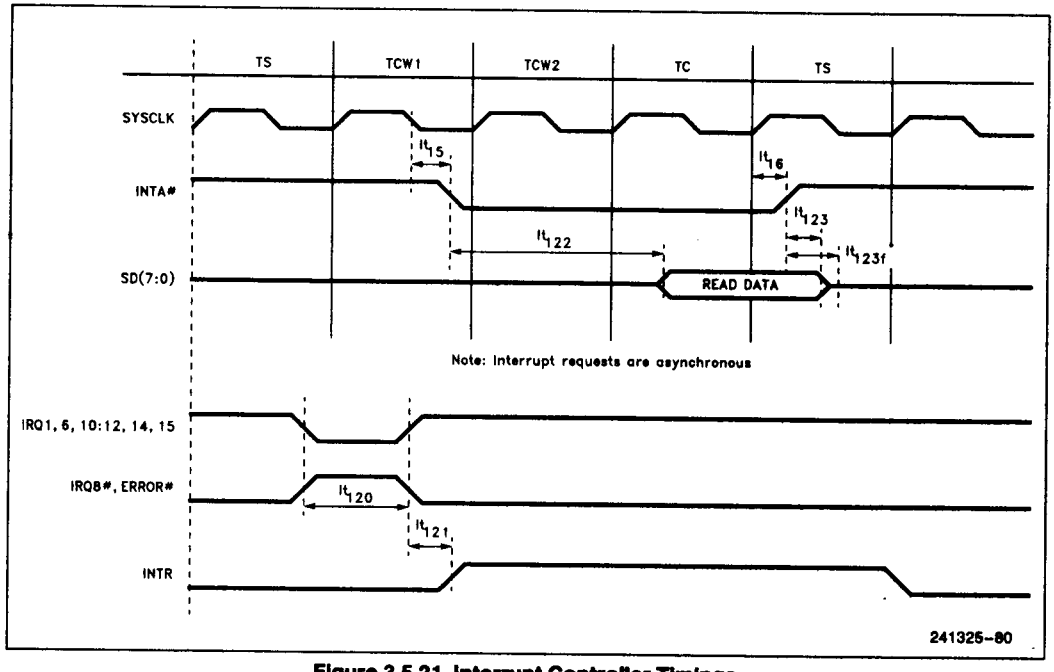


Figure 3.5.21. Interrupt Controller Timings

3.5 82360SL I/O Timing Diagrams (Continued)

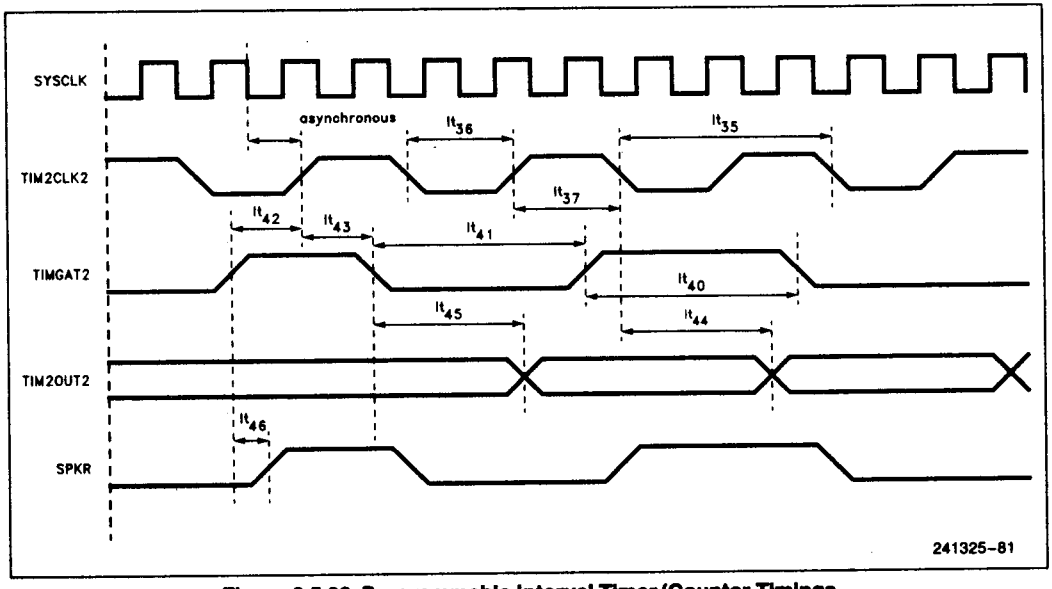


Figure 3.5.22. Programmable Interval Timer/Counter Timings

3.5 82360SL I/O Timing Diagrams (Continued)

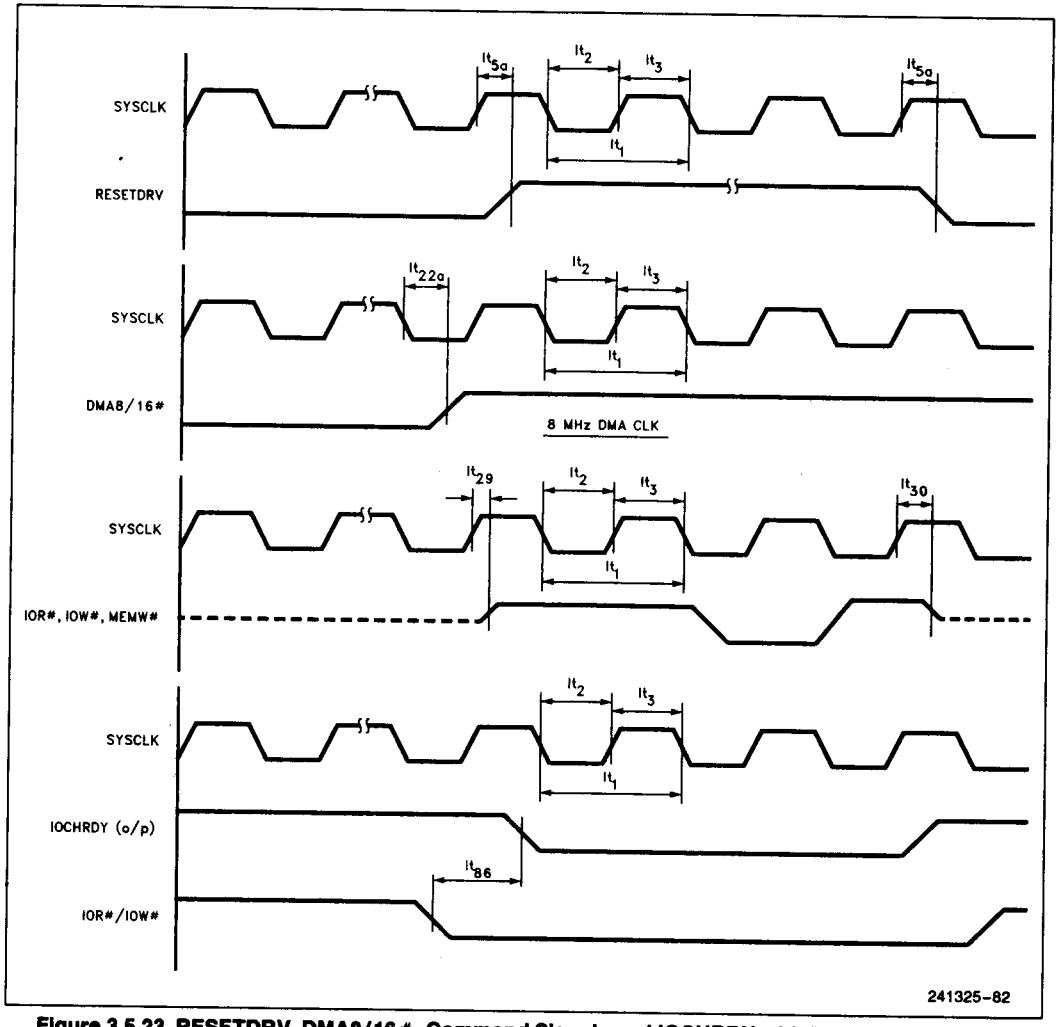


Figure 3.5.23. RESETDRV, DMA8/16#, Command Signals and IOCHRDY with Respect to SYSCLK

3.5 82360SL I/O Timing Diagrams (Continued)

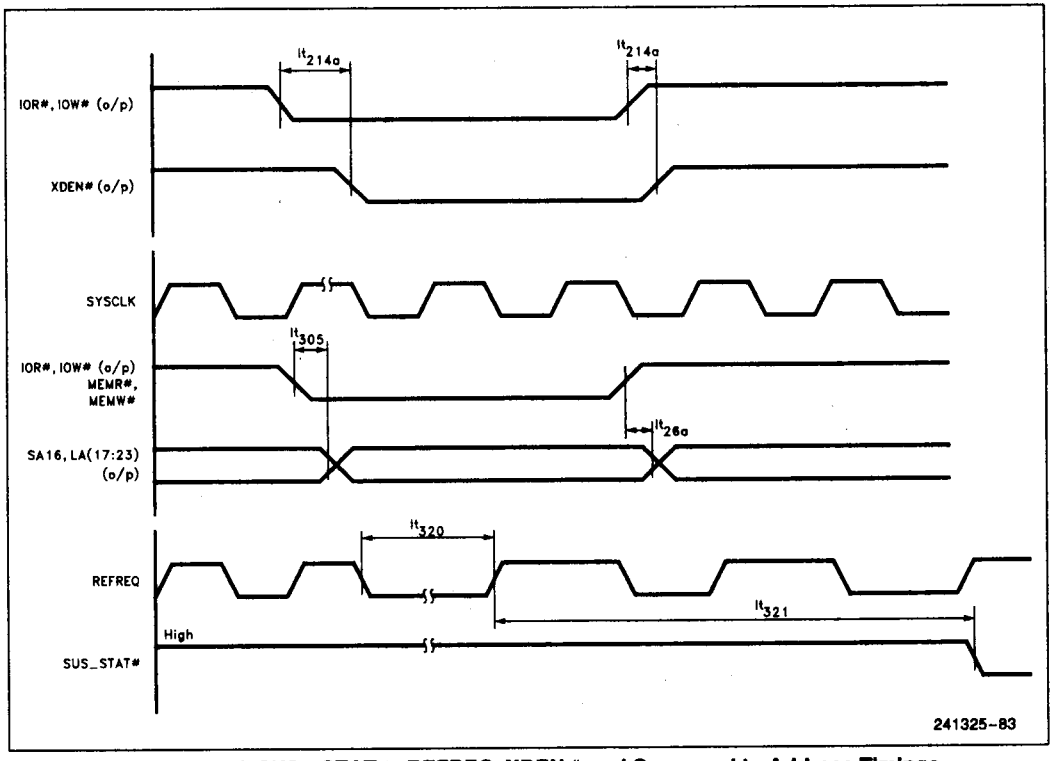


Figure 3.5.24. SUS_STAT#, REFREQ, XDEN# and Command to Address Timings

3.5 82360SL I/O Timing Diagrams (Continued)

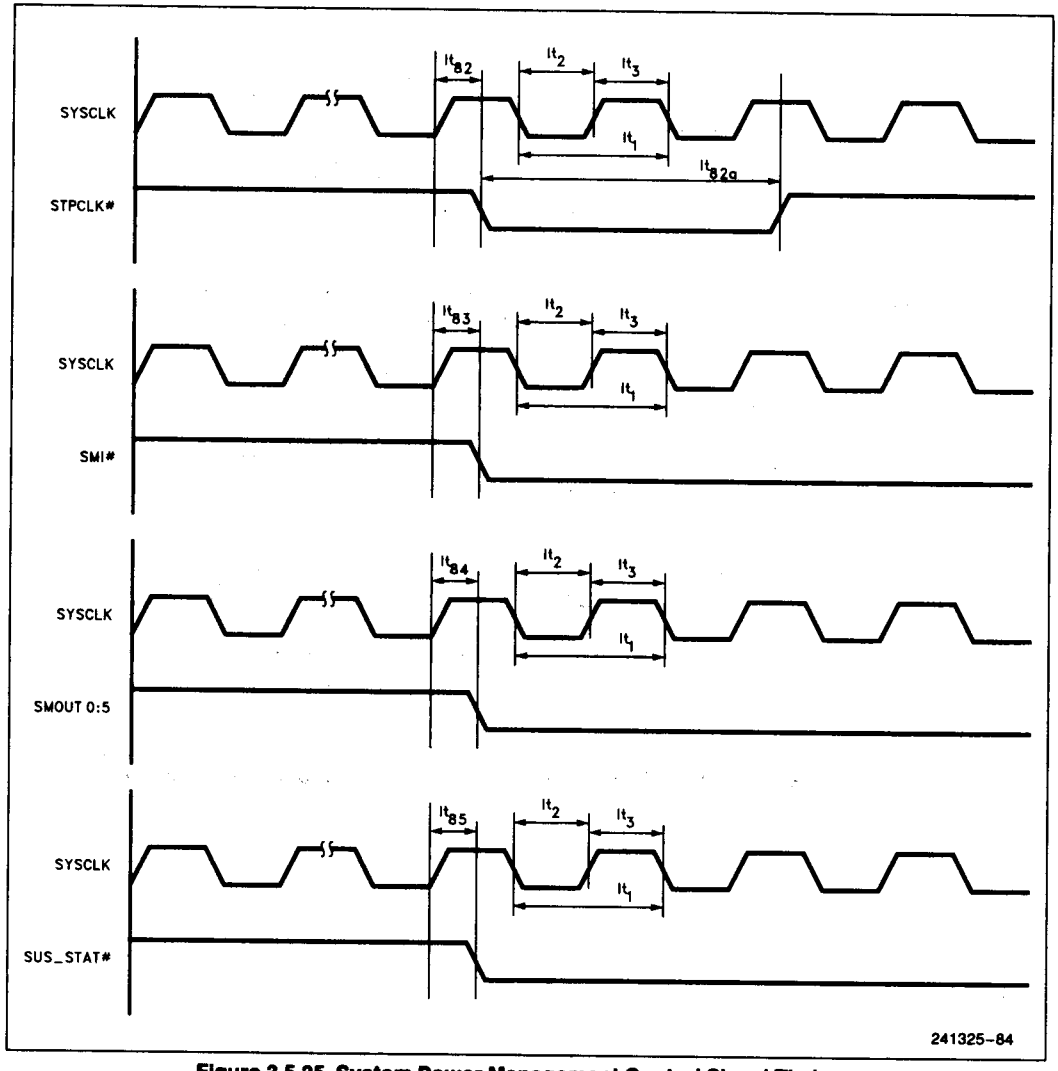


Figure 3.5.25. System Power Management Control Signal Timings

3.5 82360SL I/O Timing Diagrams (Continued)

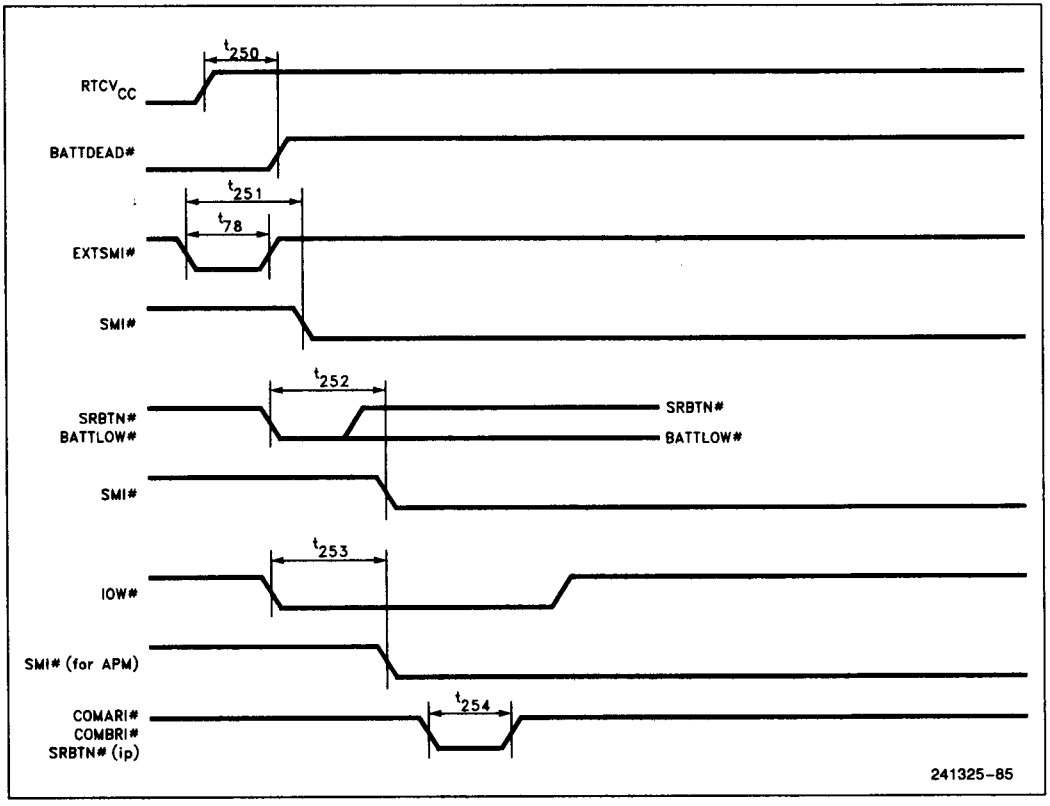


Figure 3.5.26. Power Management Timings

3.5 82360SL I/O Timing Diagrams (Continued)

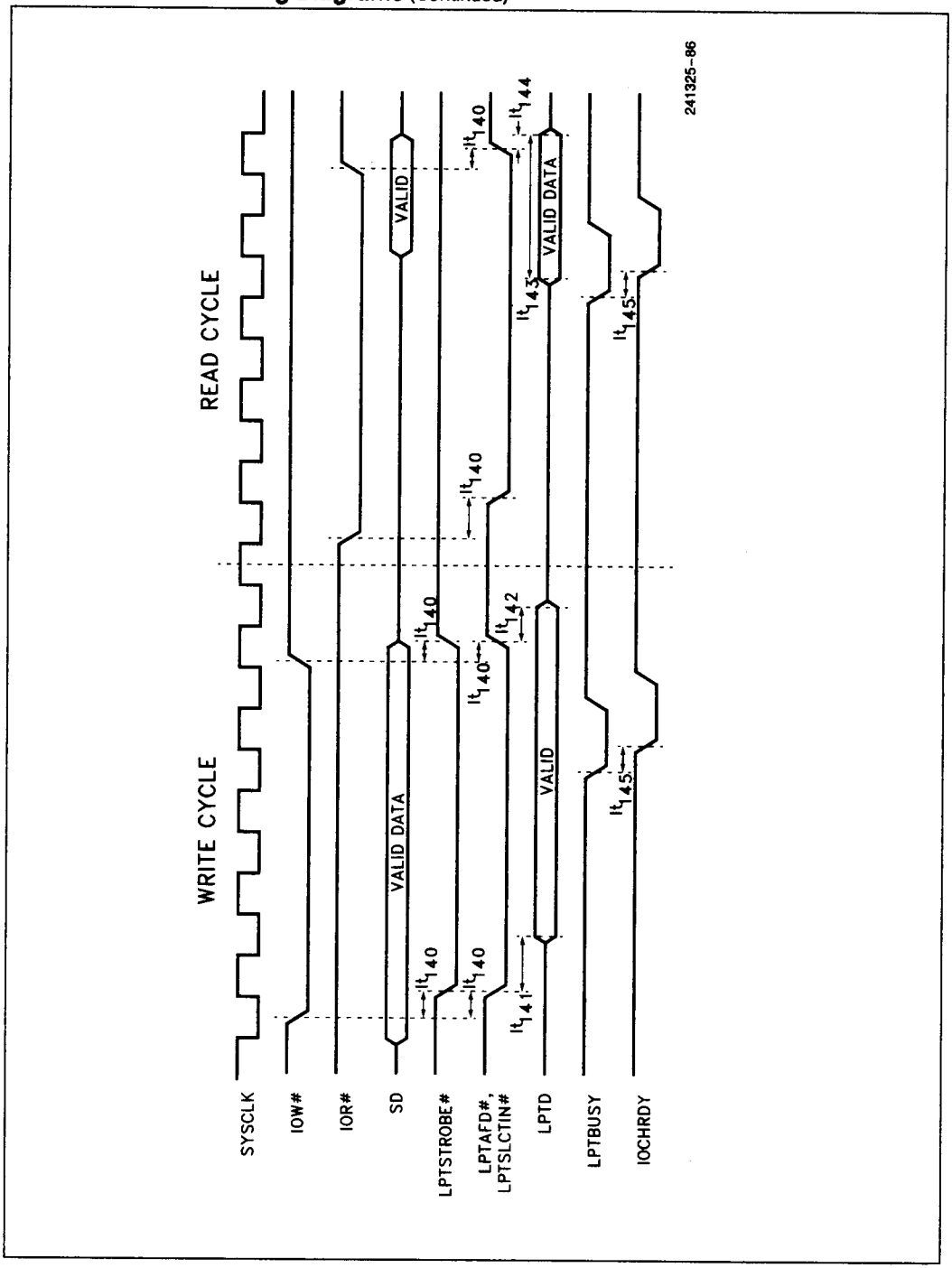


Figure 3.5.27. Fast Parallel Port Timings

3.6 Capacitive Derating Information

In the A.C. timing table presented in Section 3.4, all max and min timings are tested at a load of 50 pF. All max timings are specified at the maximum load condition for the pin and all min timings are specified for the minimum load conditions for the pin.

If the load on a pin falls within the range of the min and max capacitance specified, no derating calculations need to be done for synchronous timings. If a lighter or heavier capacitive load is connected to any pin, signal delay will change. To allow the system designer to account for such loading differences in a system, a family of capacitive derating curves are provided in this section.

The derating curves are divided into four groups—Fast rise, fast fall, slow rise and slow fall curves. Each group has one curve for the buffer type associated with the pin corresponding to a signal. Depending upon the parameter for which the timing is being specified, curves of different groups should be used to derate the specification. The group to be used is given in the column "Derating" associated with each specification. The nomenclature used in this column is as follows: FR = Fast Rise, SR = Slow Rise, FF = Fast Fall, SF = Slow Fall. The curve corresponding to the signal in question may be found from the "Derating Curve" column of the pin assignment table in Section 3.1.

In the case of output timing specifications, two group notations appear in the "Derating" column. The first of these corresponds to the reference signal and the second corresponds to the target signal.

When a specification is made about a bus or the specification is valid for both rise and fall times, only the type of derating is specified. For instance, F = Fast curve, S = Slow curve. Either the rise or the fall time derating may be used. To make a conservation calculation, use the smaller derating value among rise and fall for fast curves and the larger derating value for the slow curves.

When a specification has both a min and a max time, the derating curves for the min and the max times are separated by a semi-colon.

If loading conditions are not specified in the notes column, the timing parameter is specified for the worst case loading possible.

The rationale in the assignment of derating curves to specifications is as follows.

1. For synchronous (Clock related) specifications, all maximum timings are derated from slow curves. This is the worst case situation.
2. For synchronous (Clock related) specifications, all minimum timings are derated from fast curves. The reasoning here is that fast parts cause the worst case for minimum timings since the signal transition occurs earlier than for slow parts. Since these fast parts have fast buffers, the fast derating curves are used.
3. For output to output timings, the derating curve to be chosen depends on a combination of internal delays and buffer delays in fast and slow parts. From an analysis of the worst case situation, appropriate curves are selected for the system designer.

To use the derating curves, follow the procedure outlined here.

1. From the "Derating" column of A.C. timing table in Section 3.4, find the group of curves that must be used for a particular specification.
2. From the Pin assignment chart in Section 3.1, find the letter corresponding to the signal(s) under consideration from the column "Derating Curve".
3. In this section, find the derating curve of the correct group and letter.
4. Calculate the capacitive loading on the signal(s) under consideration.
5. Find this load point on the capacitive load axis of the derating curve.
6. Project a vertical line to the derating curve from the load point and draw a horizontal line and from the point the vertical line intersects the curve.
7. Estimate the amount of time from the Nominal point to the point where the horizontal line meets the delay axis. This is the derating value for the signal under consideration.
8. If the point where the horizontal meets the delay axis is **above** the nominal value, then

   If the signal under consideration is the **reference signal** (in output to output timings) the derating value should be **subtracted** from the timing specification.

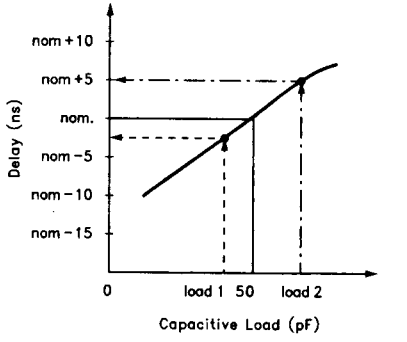
   If the signal under consideration is the **target signal** (in all timings) the derating value should be **added** to the timing specification.
9. If the point where the horizontal meets the delay axis is **below** the nominal value, then

   If the signal under consideration is the **reference signal** (in output to output timings) the derating value should be **added** to the timing specification.

   If the signal under consideration is the **target signal** (in all timings) the derating value should be **subtracted** from the timing specification.

In some output to output specifications, the loads are not at the nominal points for the curves specified. The loads at which the specifications are made are indicated in the notes column. The same procedure as above may be used for derating except that a nominal point corresponding to the load specified must first be found on the curve specified.

Using the Capacitive Derating Curves



241325-87

82360SL I/O Maximum Timing Derating Curves—5V Operation

FALLING

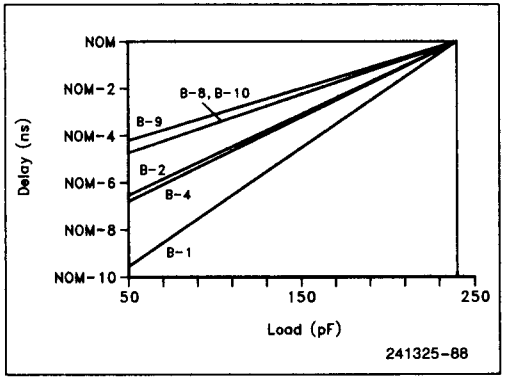


Figure 3.6.1

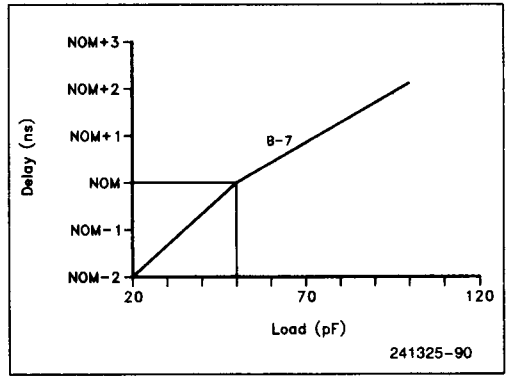


Figure 3.6.3

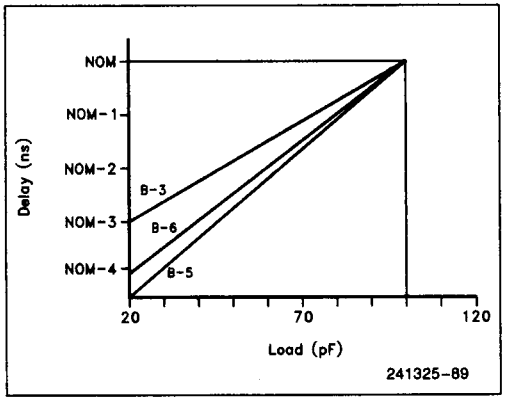


Figure 3.6.2

RISING

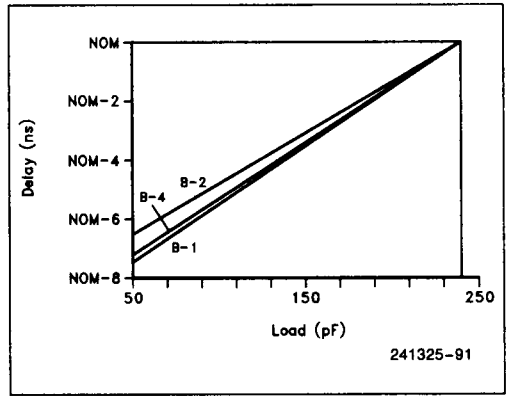


Figure 3.6.4

82360SL I/O Maximum Timing Derating Curves—5V Operation (Continued)

RISING

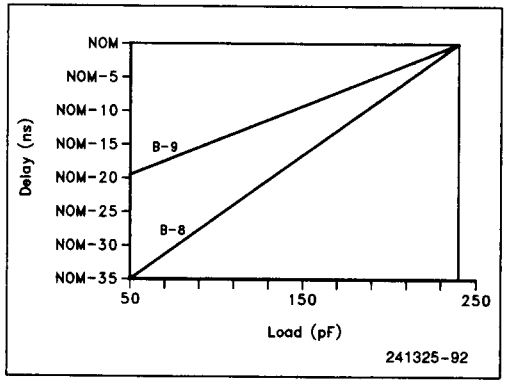


Figure 3.6.5

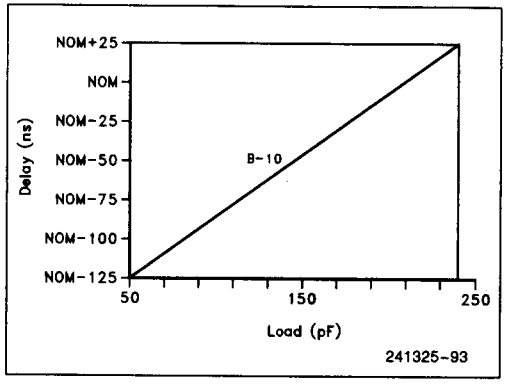


Figure 3.6.6

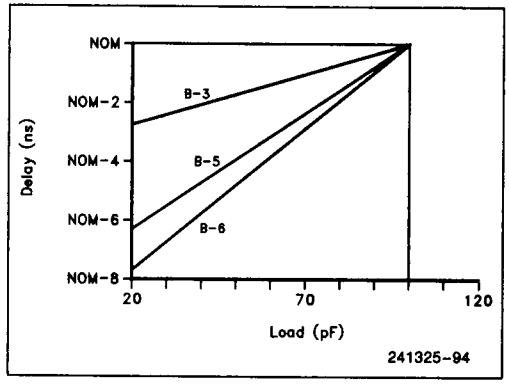


Figure 3.6.7

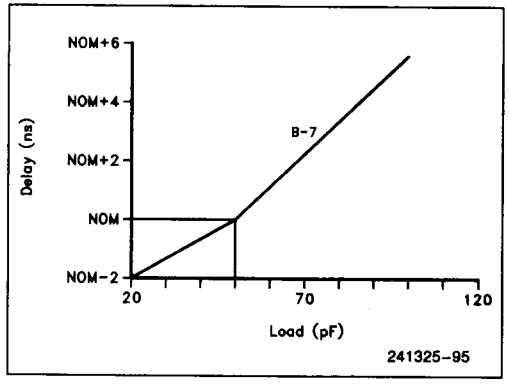


Figure 3.6.8

82360SL I/O Minimum Timing Derating Curves—5V Operation

FALLING

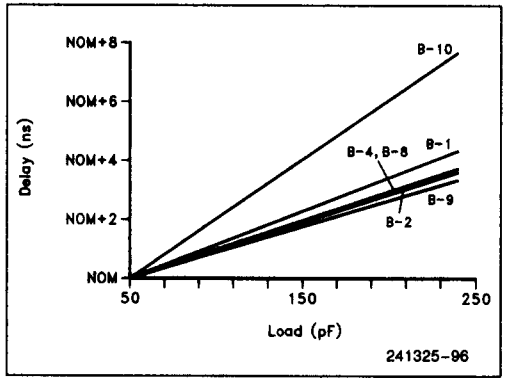


Figure 3.6.9

RISING

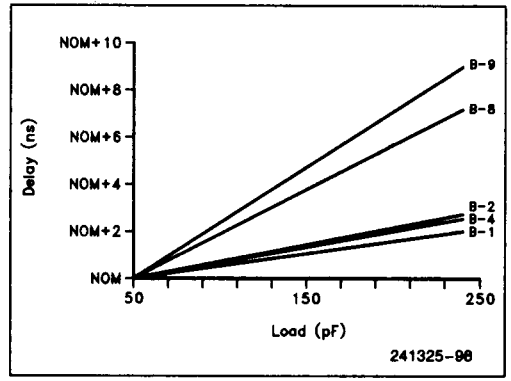


Figure 3.6.11

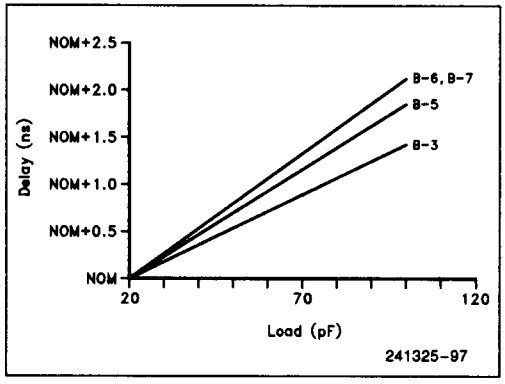


Figure 3.6.10

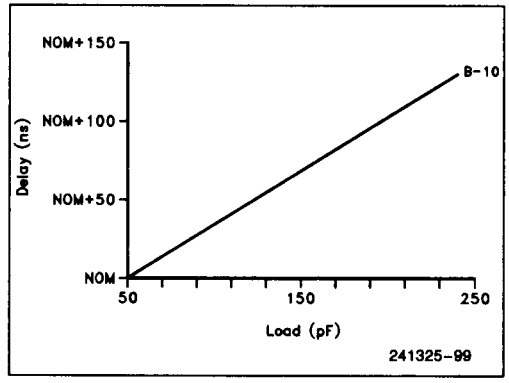


Figure 3.6.12

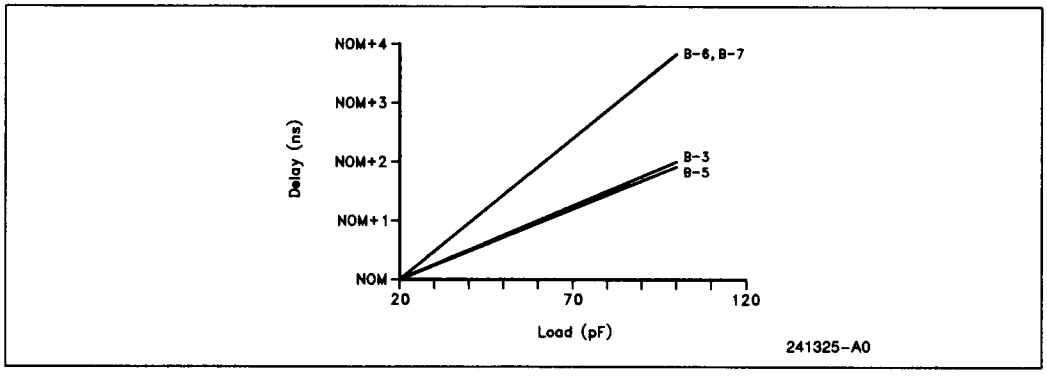


Figure 3.6.13

82360SL I/O Maximum Timing Derating Curves—3.3V Operation

FALLING

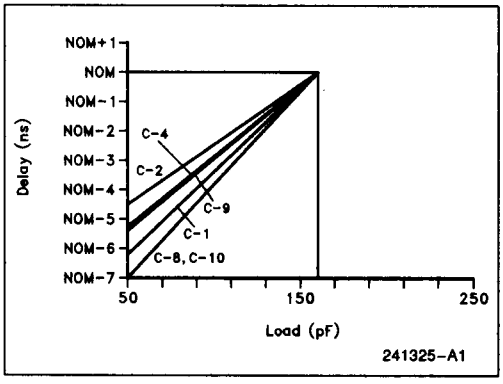


Figure 3.6.14

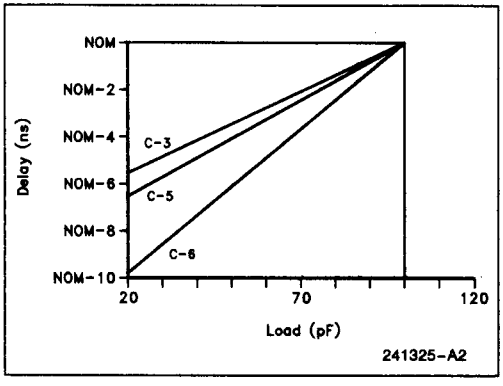


Figure 3.6.15

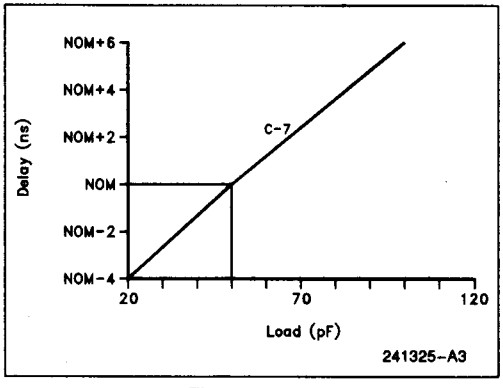


Figure 3.6.16

RISING

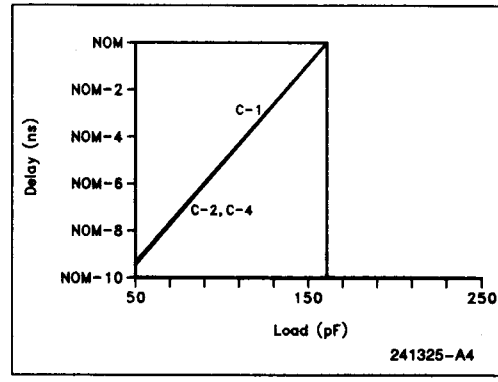


Figure 3.6.17

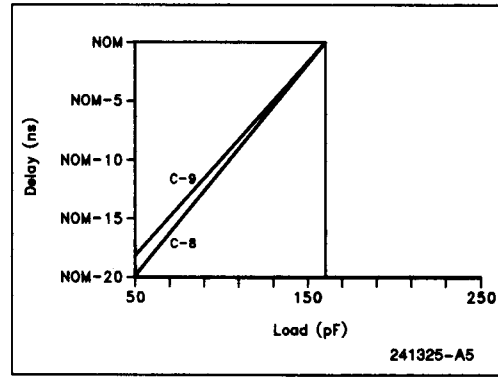


Figure 3.6.18

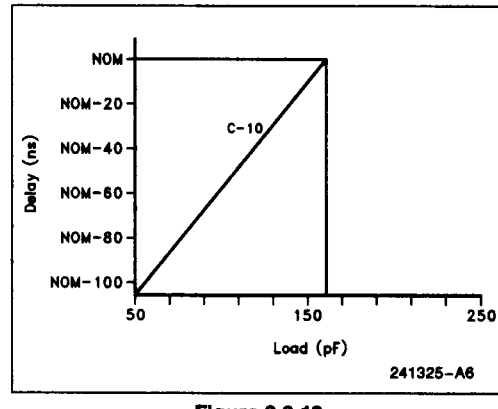


Figure 3.6.19

82360SL I/O Maximum Timing Derating Curves—3.3V Operation (Continued)

RISING (Continued)

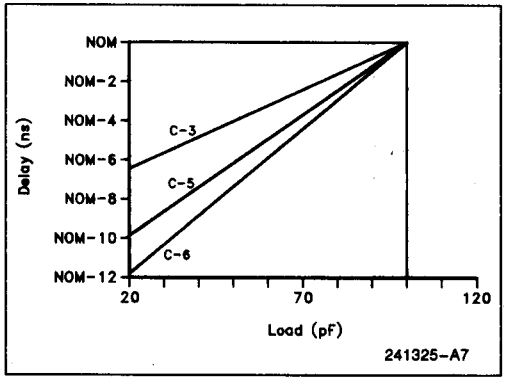


Figure 3.6.20

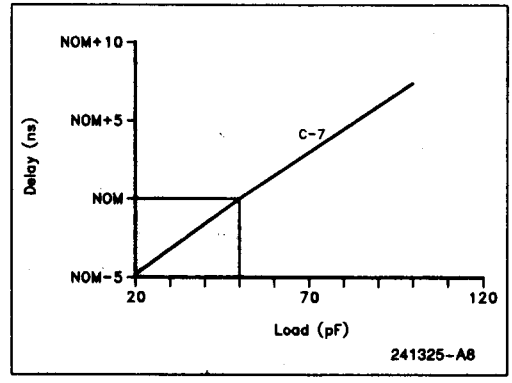


Figure 3.6.21

2

82360SL I/O Minimum Timing Derating Curves—3.3V Operation

FALLING

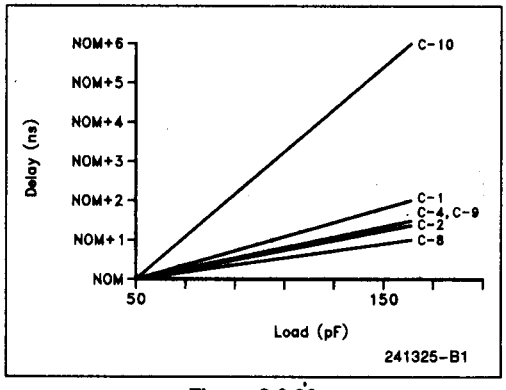


Figure 3.6.22

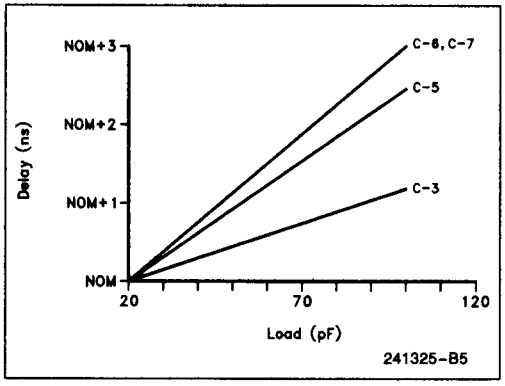


Figure 3.6.23

RISING

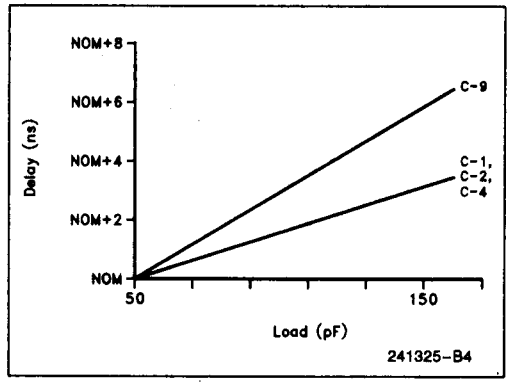


Figure 3.6.24

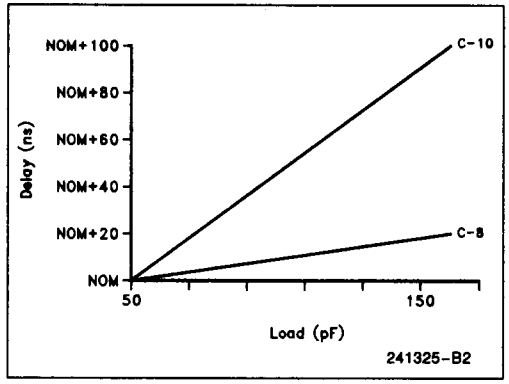


Figure 3.6.25

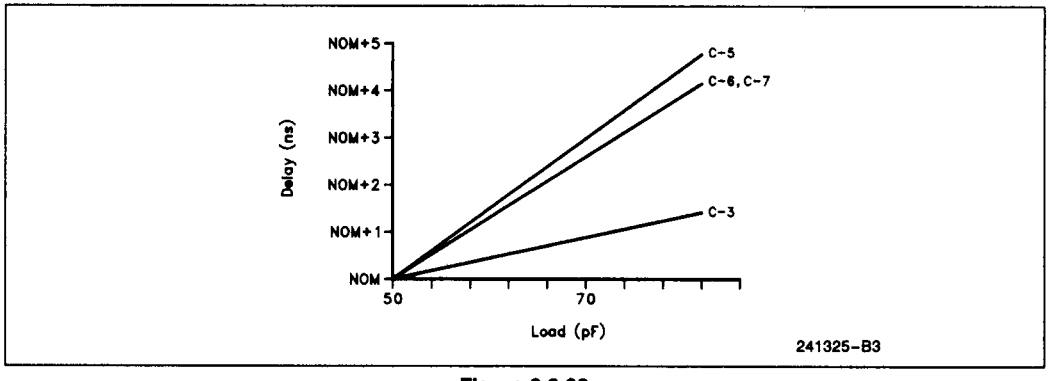


Figure 3.6.26

3.7 Crystal and Oscillator Specifications

The three on-chip oscillators are designed for parallel resonant AT cut crystals at 14.31818 MHz, 1.8432 MHz, and 32.768 KHz frequencies. Figure 3.7.1 shows the equivalent circuit of a crystal with parameters that most vendors use to specify their products.

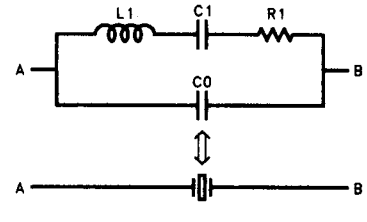


Figure 3.7.1. Equivalent Circuit of Crystal

The parameters for the three crystals used in 82360SL I/O are given in Table 3.7-1.

Table 3.7-1. Crystal Specifications

Pins	CX1, 2	COMX1, 2	RTCX1, 2
Frequency	14.31818 MHz	1.8432 MHz	32.768 KHz
R1	12Ω	100Ω	50 KΩ
C1	0.028 pF	0.012 pF	0.003 pF
L1	4.4 mH	0.65H	8245.5H
C0	7 pF	4 pF	1.7 pF
Q	35K	70K	30K
C_L	15 pF–30 pF	15 pF–40 pF	10 pF–20 pF

NOTES:
Q = Quality Factor
C_L = Load Capacitance

If external oscillators are used instead of crystals and on-chip oscillators, the parameters in Table 3.7-2 should be observed. The parameters are illustrated in Figure 3.7.2.

Table 3.7-2. Oscillator Specifications

	t_r(max)	t_f(max)	t_{hl}(min)	t_{lo}(min)
CX1	10 ns	10 ns	20 ns	20 ns
COMX1	20 ns	20 ns	200 ns	200 ns
RTCX1	20 ns	20 ns	1200 ns	1200 ns

NOTE:
The above data are system specifications and are not tested.

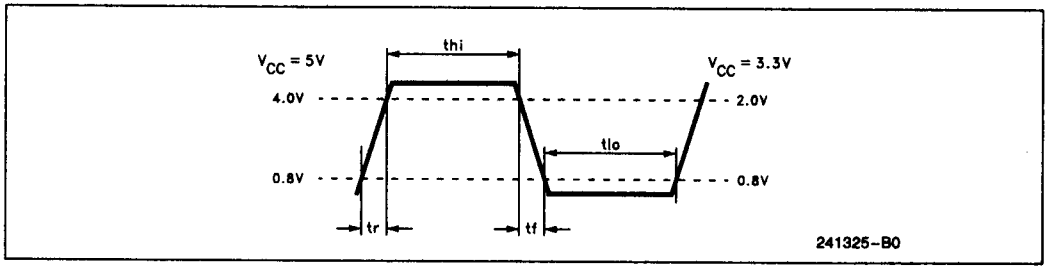


Figure 3.7.2. External Oscillator Waveform

4.0 PACKAGE THERMAL SPECIFICATIONS

The Intel486 SL CPU and the 82360SL I/O are specified for functional operation with a case temperature range from 0°C to 90°C. The case temperature should be measured in the operating environment to determine whether the Intel486 SL CPU and the 82360SL I/O are within the specified operating temperature range. The case temperature should be measured at the center of the top surface of the package. When the CPU and I/O have a voltage applied the operating temperature range is applicable, rather than the storage temperature.

The following definitions and assumptions are used to determine the recommended maximum case temperature for the Intel486 SL CPU and 82360SL I/O:

T_A = Ambient Temperature in °C

T_C = Case Temperature in °C

θ_{JC} = Package Thermal Resistance between Junction and Case

θ_{JA} = Package Thermal Resistance between Junction and Ambient

T_J = Junction Temperature in °C

P = Power Consumption in Watts

The ambient temperature can be evaluated by using the values of thermal resistance between junction and case, θ_{JC} and the thermal resistance between junction and ambient, θ_{JA} in the following equations:

$T_J = T_C + P \times \theta_{JC}$

$T_A = T_J - P \times \theta_{JA}$

$T_C = T_A + P \times [\theta_{JA} - \theta_{JC}]$

Values for θ_{JA} and θ_{JC} are given in Table 4-1 for the 196-lead PQFP, the 208-lead SQFP and the 227-lead LGA packages.

2

Table 4-1. Thermal Resistances (°C/W) θ_{JC} and θ_{JA}

Package	θ_{JC} (°C/W)	θ_{JA} (°C/W) vs Airflow—ft/min (m/sec)			
		0 (0)	200 (1.01)	400 (20.3)	600 (3.04)
196L PQFP	6	23	19	16	13.5
208L SQFP	6	33	23.5	20.5	18.5
227L LGA(1)	5	15	12	10.5	9.5

NOTE:
1. These values reflect the use of a typical LGA socket.

Absolute Maximums

Case Temperature under Bias .....0°C to +90°C

Storage Temperature .....−65°C to +150°C

Maximum Ambient Temperature .....70°C

V_{CC} = 5.0V ±10%

Voltage on Any 5V Interface Pin with Respect to Ground ...−0.5V to V_{CC} + 0.5V

Supply Voltage with Respect to V_{SS} .....−0.5V to +6.5V

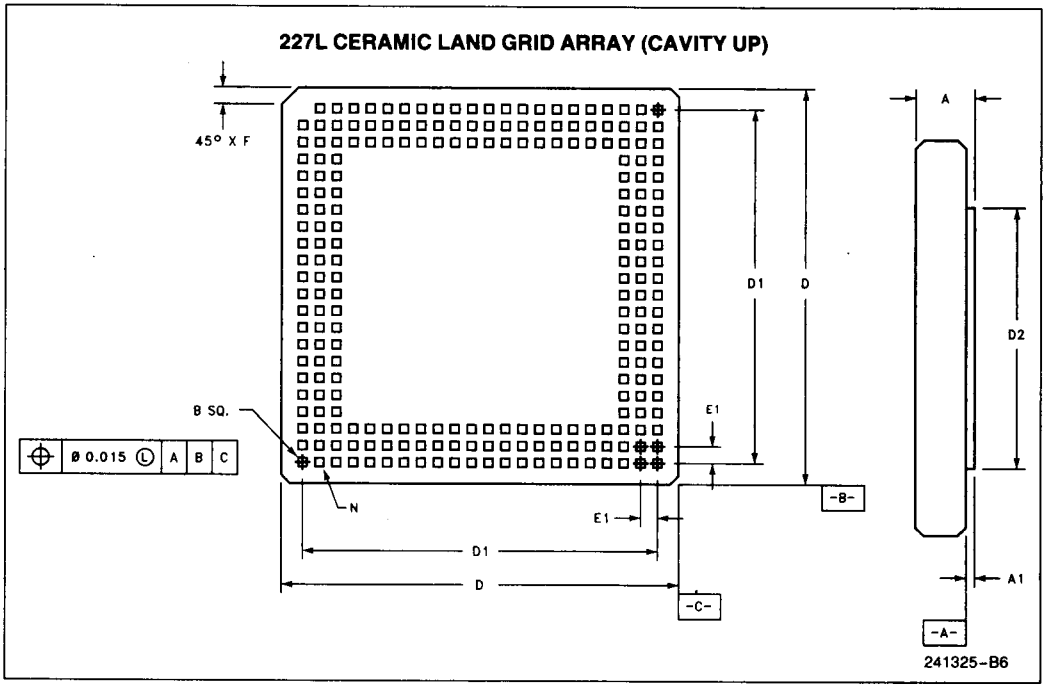
V_{CC} = 3.3V ±0.3V

Voltage on Any 3.3V Interface Pin with Respect to Ground .....−0.5V to +4.6V

Supply Voltage with Respect to V_{SS} .....−0.5V to +4.6V

5.0 MECHANICAL DETAILS OF LGA, SQFP AND PQFP PACKAGES

This section contains mechanical details of the three types of packages used in the Intel486 SL SuperSet to help design the parts in. For more detailed information on packages and package types, please refer to *"Surface Mount Technology Guide"* (Order #240585)



Family: Ceramic Land Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.46	3.18		0.097	0.125	
A1	0.23	0.43		0.009	0.017	
B	0.69	0.84		0.027	0.033	
D	28.96	29.46		1.140	1.160	
D1	26.67		Basic	1.050		Basic
D2		24.13			0.950	
e1	1.27		Basic	0.050		Basic
F	1.65	2.16		0.065	0.085	
N	227			227		
Issue	4/17/90					

Figure 5.1a. Principal Dimensions of the Intel486™ SL CPU in a 227-Lead LGA Package

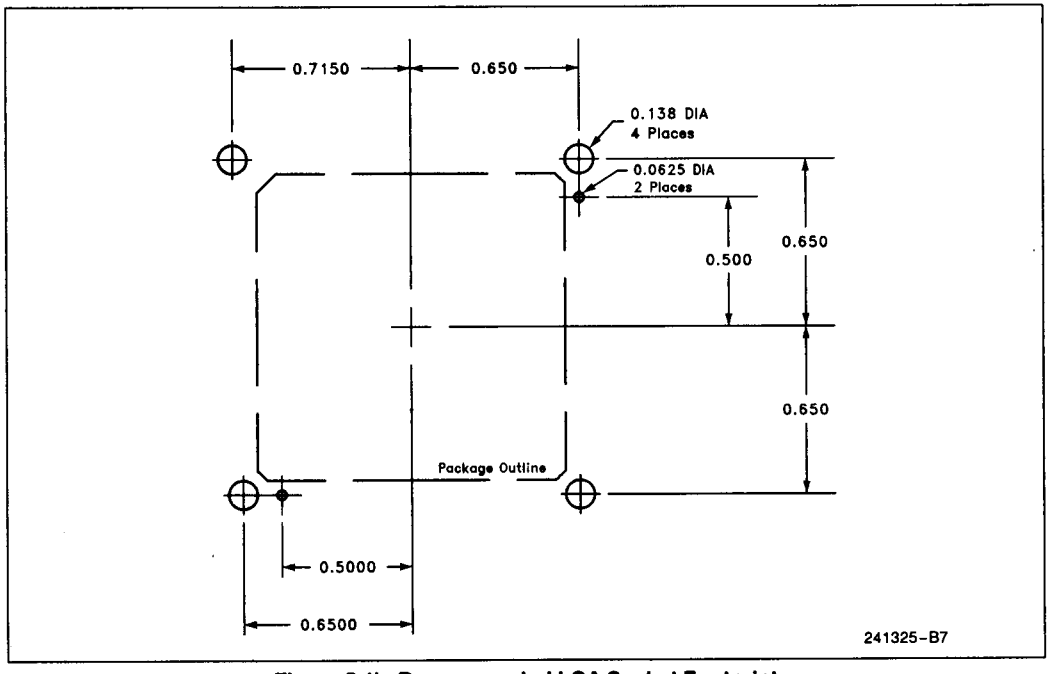
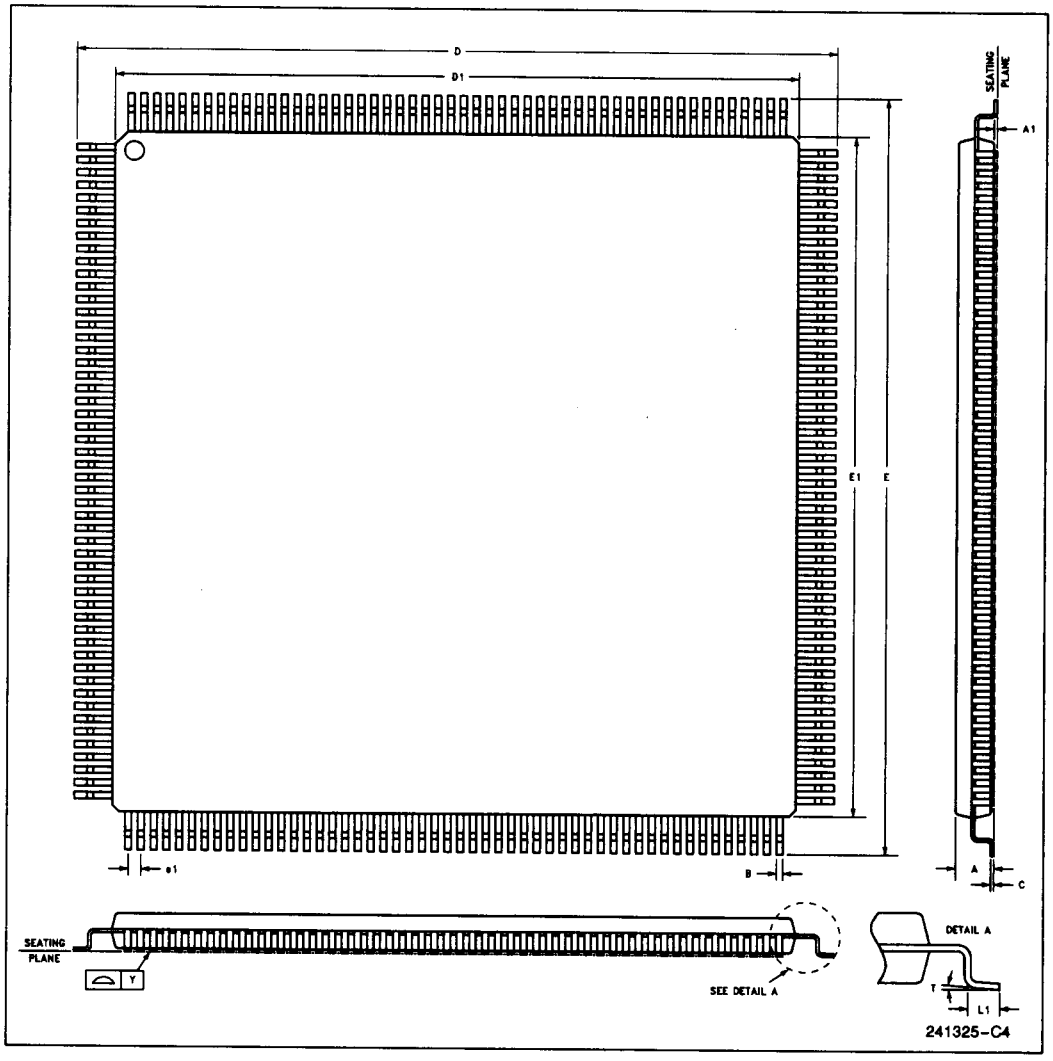


Figure 5.1b. Recommended LGA Socket Footprint



Family: Quad Flatpack Package (Square)				
Symbol	Millimeters			
	Min	Nom	Max	Notes
A		3.52	3.70	
A1	0.00	0.15	0.30	
AAA		0.10		
B	0.10	0.18	0.30	
C	0.13	0.152	0.203	
D	30.30	30.60	30.90	

Figure 5.2. Principle Dimensions of the 82360SL I/O in the 208-SQFP Package

Family: Quad Flatpack Package (Square)				
Symbol	Millimeters			
	Min	Nom	Max	Notes
D1		28.0		
E	30.30	30.60	30.90	
E1		28.0		
e1		0.50 BSC		
L1	0.30		0.70	
T	0.00	0.45		
Y			0.10	
N	208			
Issue	JEDEC			

Figure 5.2. Principle Dimensions of the 82360SL I/O in the 208-SQFP Package (Continued)

NOTE:
Copper lead frame only.

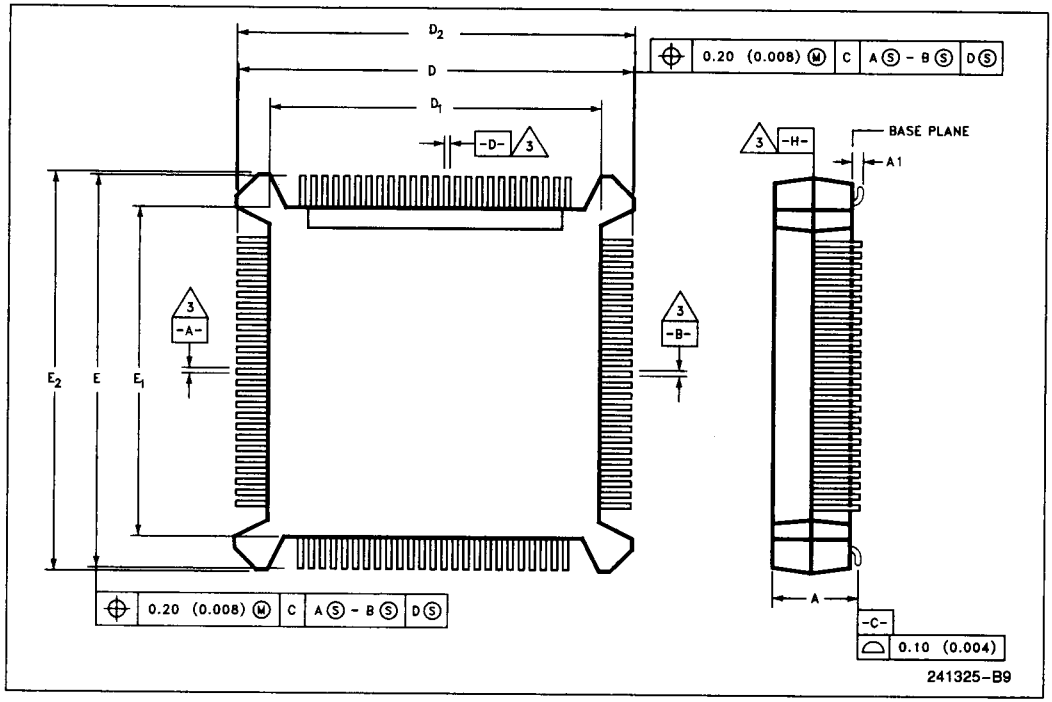


Figure 5.3a. Principle Dimensions of the 82360SL I/O in the 196-Lead PQFP Package

Family: 196-Lead Plastic Quad Flat Package (PQFP) 0.025 Inch (0.635mm) Pitch				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A = Package Height: Distance from seating plane to highest point of the body	4.06	4.32	0.160	0.180
A1 = Standoff: Distance from Seating Plane to Base Plane	0.51	0.76	0.020	0.040
D/E = Overall Package Dimension: Lead Tip to Lead Tip	37.47	37.72	1.470	1.490
D1/E1 = Plastic Body Dimension	34.21	34.37	1.347	1.353
D2/E2 = Bumper Distance	38.02	38.18	1.497	1.503
D3/E3 = Lead Dimension	30.48 Ref		1.200 Ref	
D4/E4 = Foot Radius Location	36.14	36.49	1.423	1.437
L1 = Foot Length	0.51	0.76	0.020	0.030

NOTES:
1. All PQFP case outlines are being presented as standards to the JEDEC.
2. Typical board footprint area for the 196-lead PQFP is 1.500 inches x 1.5000 inches.
3. All dimensions and tolerance conform to ANSI Y14.5M-1982.
4. Datum Plane -H- located at the molding parting line and coincident with the bottom of the lead where the lead exits the plastic body.
5. Datums A-B and -D- to be determined where the center lead exits the plastic body at datum plane -H-.
6. Controlling dimension in inches.
7. Dimensions D1, D2, E1, and E2 are measured at the molding parting line and do not include mold protrusions.
8. Pin 1 identifier is located within one of the two zones indicated.
9. Measured at datum plane -H-.
10. Measured at seating plane datum -C-.

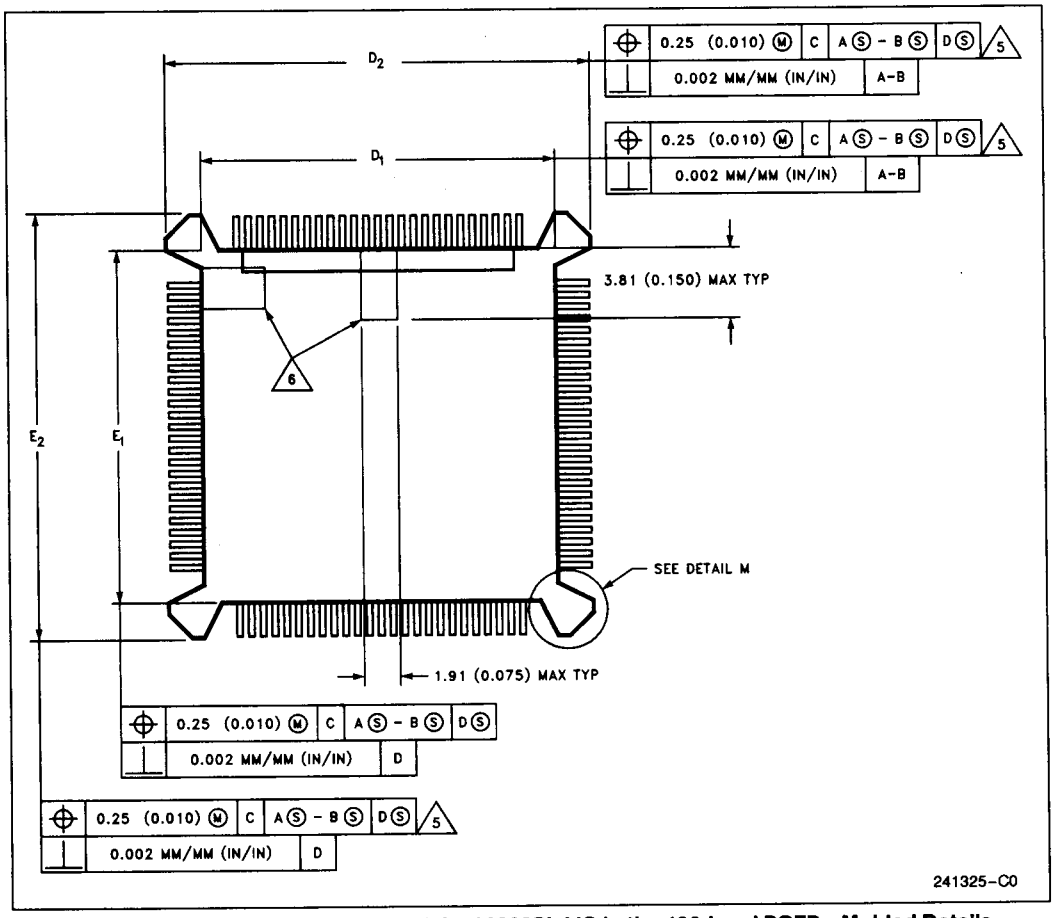


Figure 5.3b. Detailed Dimensions of the 82360SL I/O in the 196-Lead PQFP—Molded Details

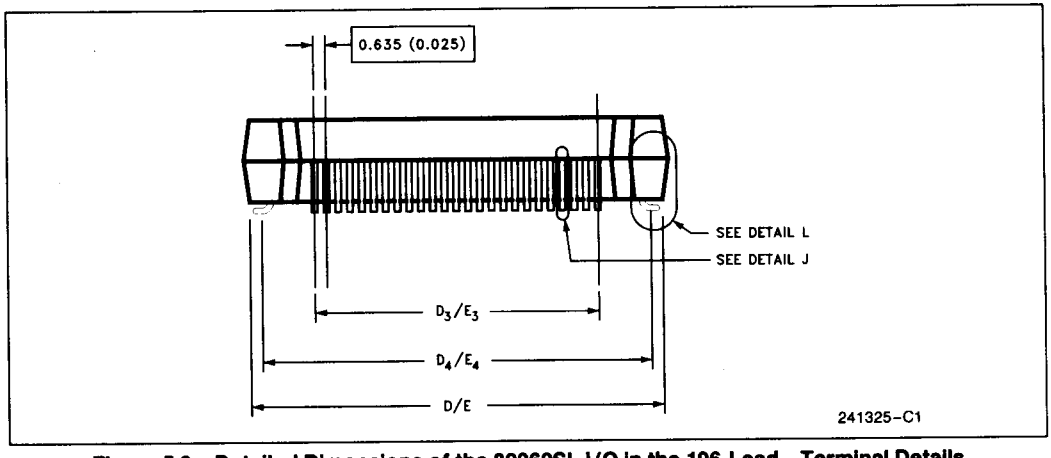


Figure 5.3c. Detailed Dimensions of the 82360SL I/O in the 196-Lead—Terminal Details

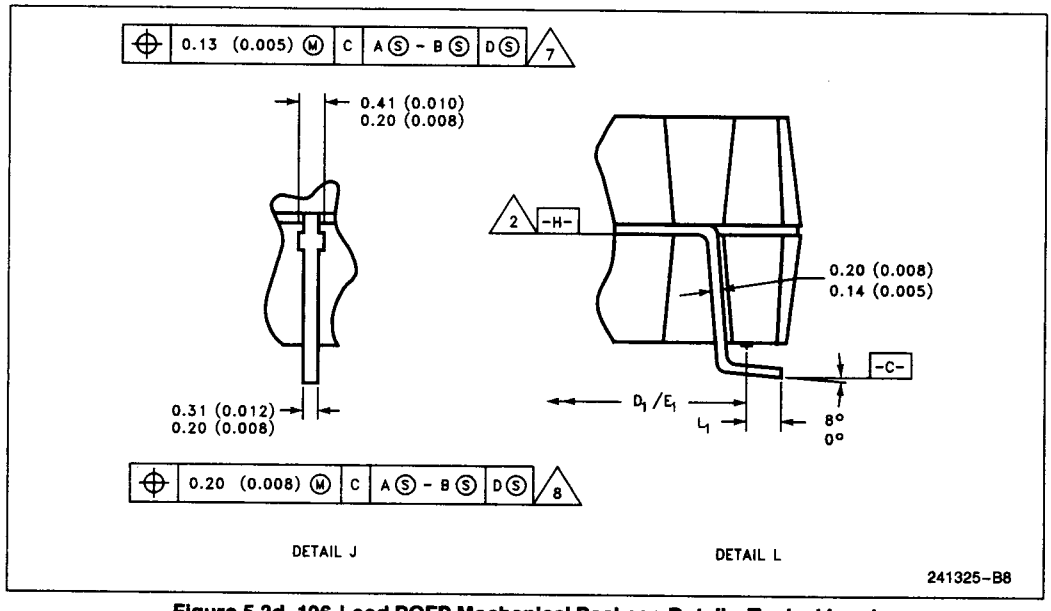


Figure 5.3d. 196-Lead PQFP Mechanical Package Detail—Typical Lead

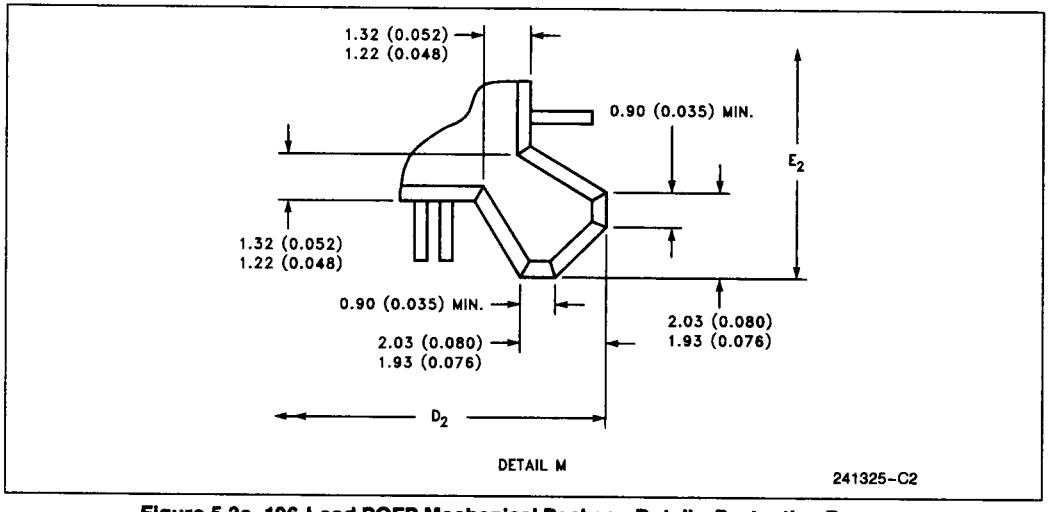


Figure 5.3e. 196-Lead PQFP Mechanical Package Detail—Protective Bumper

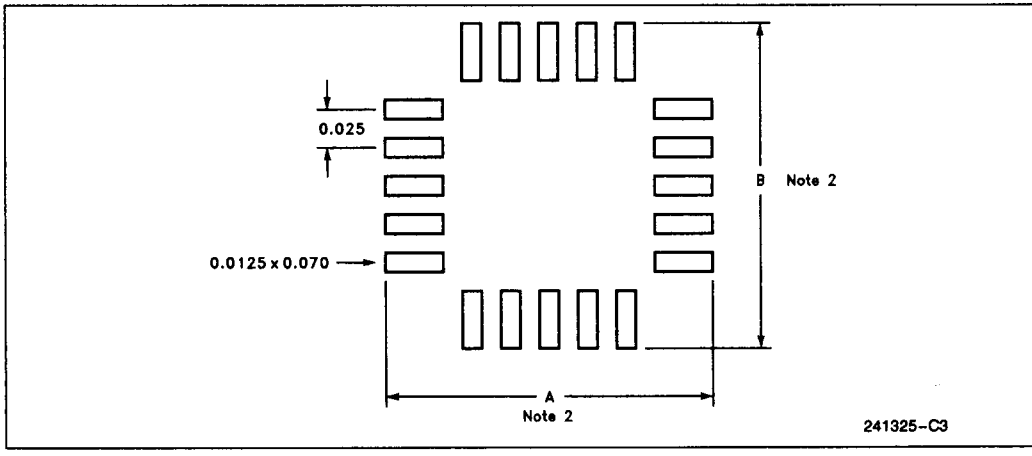


Figure 5.3f. Recommended PQFP Footprint

APPENDIX A
RELATED DOCUMENTS

The following list provides a useful cross-reference of related Intel486 SL SuperSet publications.

- *Intel486™ SL Microprocessor SuperSet System Design Guide,* 1992. Order Number 241326.
- *Intel486™ SL Microprocessor SuperSet Programmer's Reference Manual,* 1992. Order Number 241327.
- *Packaging Handbook,* 1992. Order Number 240800.
- *UPI™ -C42 (80C42) Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *80C51SL-BG Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *82C37A Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *82C54 Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *82C59A Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *82077SL Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *82365SL Data Sheet, Peripheral Components Handbook,* 1992. Order Number 296467.
- *IBM Technical Reference—Personal Computer AT.*
- *Intel486™ Microprocessor Family Hardware Reference Manual,* 1992. Order Number 240552.
- *Intel486™ Microprocessor Family Data Book,* 1992. Order Number 240440.
- *Intel486™ Microprocessor Family Programmer's Reference Manual,* 1992. Order Number 240486.
- Technical Reference Personal Computer AT, 1st Edition (Sept. 1985), Copyright I.B.M.
- I.E.E.E. Personal Computer Bus Standard, Std. P996, DRAFT D.200, (1990), Copyright I.E.E.E. Inc.
- I.E.E.E. Standard Test Access Port and Boundary-Scan Architecture, Std 1149.1-1990, (Feb. 15, 1990), Copyright I.E.E.E. Inc.