82353 Advanced Data Path

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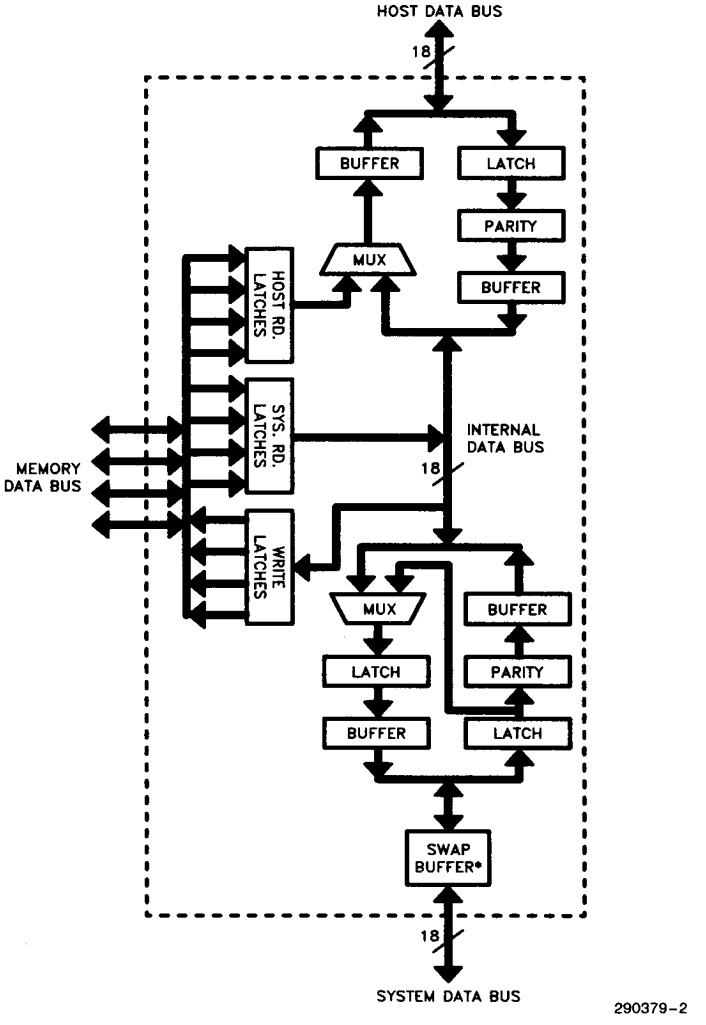
1.0 82353 BLOCK DIAGRAM

The following illustration is a simplified block diagram of the 82353 Advanced Data Path. It is provided for conceptual purposes only.



NOTE:
*The Standard Mode of the System Interface is shown.

Figure 1.1. 82353 Internal Block Diagram

2.0 INTRODUCTION

The 82353 Advanced Data Path (ADP), works closely with the 82359 EISA DRAM Controller to provide an extremely flexible system conforming to the EISA bus specification.

The 82353 ADP and associated 82359 DRAM Controller provide a unique bus structure, utilizing two distinct electrically isolated buses. One bus, labeled "Host Bus", accommodates the host CPU/cache combination. The second bus, labeled "System Bus", accommodates standard I/O and add-in peripherals and follows EISA timings. Each of the busses have their own address/data path to main memory.

The 82353 provides a dual ported data path between the system and host data bus to the DRAM data bus. This dual ported architecture allows accesses to DRAM by host masters without incurring arbitration. Integrated into the 82353 are first and second level posted write latches to support zero wait state writes. A burst read or write capability of up to 16 sequential words is provided.

A single 82353 is a 16-bit data path slice which interfaces to 16-bit host and system data buses. The intent of the 82353 is for two 82353's to be connected in parallel, providing a 32-bit host and system data bus and 32, 64, or 128-bit wide two-way DRAM memory structure. In fact, any number of 82353s can be used in parallel to implement busses in 16-bit multiples.

The DRAM memory structure is very flexible allowing the designer to achieve the desired price/performance objectives. DRAM SIMMs of 64K, 256K, 1M, and 4M in address depth and speeds of 60, 70, 80, or 100 ns are supported in a "mix and match" arrangement, allowing memory expansion without discarding different size or speed memory devices.

3.0 QUICK REFERENCE

3.1 Pin Quick Reference

Signal Name	I/O	Pin #	Full Signal Name
HOST BUS INTERFACE			
HD(15:0)	I/O	Note A	Host Data
HPD(1:0)	I/O	40, 41	Host Parity Data
HAS#	I	73	Host Address Strobe
HARDY	O	75	Host Asynchronous Ready
HBRDY#	I	67	Host Burst Ready
HCK1/2X#	I	69	Host Clock Select
HCLK	I	68	Host Clock
HINTPAR	I	66	Host Internal Parity Select
HIOE#	I	71	Host Internal Output Enable
HRD#	I	63	Host Read
HOE#	I	70	Host Output Enable
HRST	I	64	Host Reset
HWLE#	I	65	Host Write Latch Enable
HWCLKEN#	I	65	Host Write Clock Enable
PERSTB#	O	74	Parity Error Strobe
BT/R#	I	71	82385 BT/R#
HLDSTB	I	63	Host Local Data Strobe
DOE#	I	70	Data Output Enable

3.1 Pin Quick Reference (Continued)

Signal Name	I/O	Pin #	Full Signal Name
SYSTEM BUS INTERFACE			
SD(15:0)	I/O	Note B	System Data
SPD(1:0)	I/O	14, 15	System Parity Data
IDSDLE#	I	5	Internal Data to System Data Latch Enable
SAS#	I	4	System Address Strobe
SBRDY#	I	10	System Burst Ready
SCLK	I	11	System Clock
SDIDLE#	I	9	System to Internal Data Latch Enable (Word)
SDIDLE(1:0)#	I	14, 15	System to Internal Data Latch Enable (Byte)
SDVLD	I	13	System Data Valid Strobe
SINTPAR	I	12	System Internal Parity Select
SOE#	I	8	System Output Enable (Word)
SOE0#	I	12	System Output Enable Byte 0
SOE1#	I	11	System Output Enable Byte 1
CPYEN#	I	10	Copy Enable
CPYUP	I	9	Copy Up
SIOE#	I	8	System Internal Output Enable
RESIST	I	6	Reference Resistor

Signal Name	I/O	Pin #	Full Signal Name
MEMORY MODULE INTERFACE			
MPD(7:0)	I/O	Note C	Memory Parity Data
MD0D(15:0)	I/O	Note D	Memory Data 0
MD1D(15:0)	I/O	Note E	Memory Data 1
MD2D(15:0)	I/O	Note F	Memory Data 2
MD3D(15:0)	I/O	Note G	Memory Data 3
H/S#	I	2	Host/System Port Select
IF(1:0)	I	80, 79	Interleave Factor
MDS#	I	76	Memory Data Strobe
MIOE#	I	1	Memory Internal Output Enable
MWLS#	I	164	Memory Write Latch Select
PER#	O	3	Parity Error
SEL(1:0)	I	78, 77	Selects
WE(3:0)#	I	145, 144, 104, 103	Write Enables

NOTES:
A. 42, 46, 48, 50, 52, 54, 58, 60, 43, 47, 49, 51, 53, 55, 59, 61.
B. 16, 19, 23, 25, 29, 32, 35, 38, 17, 20, 24, 27, 30, 33, 37, 39.
C. 162, 158, 161, 157, 160, 156, 159, 155.
D. 150, 140, 132, 123, 113, 105, 95, 86, 146, 136, 127, 118, 109, 99, 91, 82.
E. 151, 141, 133, 124, 114, 106, 96, 87, 147, 137, 128, 119, 110, 100, 92, 83.
F. 152, 142, 134, 125, 115, 107, 97, 88, 148, 138, 129, 120, 111, 101, 93, 84.
G. 153, 143, 135, 126, 116, 108, 98, 89, 149, 139, 130, 121, 112, 102, 94, 85.

3.2 Multiplexed Pin Listing

Due to the large number of pins required by the 82353, and the fact that not all signals are used in every mode of operation, some of the pins are multiplexed. This means that a given pin may have more than one function dependent upon which mode of operation is selected.

The following tables show which 82353 signals are available in each of the three host modes and each of the two system modes. An "X" indicates that the corresponding signal name is used in that mode.

Signal Name	Host Interface Mode			Multiplexed Pin
	Transparent	Clocked	82385	
HD(15:0)	X	X	X	
HPD(1:0)	X	X	X	
HAS#	X	X	X	
HARDY	X	X	X	
HBRDY#	X	X	X	
HCK1/2X#	X	X	X	
HCLK	X	X	X	
HINTPAR	X	X	X	
PERSTB#	X	X	X	
HRST	X	X	X	
HIOE#	X	X		*
HRD#	X	X		*
HOE#	X	X		*
HWLE#	X			*
HWCLKEN#		X		*
BT/R#			X	*
DOE#			X	*
HLDSTB			X	*

"X" indicates this pin is available in this mode of operation.
*Pin provides a multiplexed signal dependent upon which one of three Host modes is selected.

Multiplexed Host Signal Combinations		
Transparent	Clocked	82385
HIOE#	HIOE#	BT/R#
HRD#	HRD#	HLDSTB
HOE#	HOE#	DOE#
HWLE#	HWCLKEN#	(Reserved)

Signal Name	System Interface Mode		Multiplexed Pin
	Standard	Buffered	
SD(15:0)	X	X	
IDSDLE#	X	X	
SDVLD	X	X	
SIOE#	X		
CPYEN#	X		*
CPYUP	X		*
SDIDLE(1:0)#	X		*
SOE(1:0)#	X		*
SPD(1:0)		X	*
SAS#		X	*
SBRDY#		X	*
SCLK		X	*
SDIDLE#		X	*
SINTPAR		X	*
SOE#		X	*

Multiplexed System Signal Combinations	
Standard Mode	Buffered Mode
SDIDLE(1:0)#	SPD(1:0)
CPYEN#	SBRDY#
SOE0#	SINTPAR
SOE1#	SCLK
CPYUP	SDIDLE#
(Reserved)	SAS#
SIOE#	SOE#

4.0 82353 FUNCTIONAL DESCRIPTION

The internal structure of the 82353 consists of four functional blocks as shown in Figure 4.1. Three of these blocks interface the 82353 to the external host, system and memory busses. The fourth block's function is for parity checking.

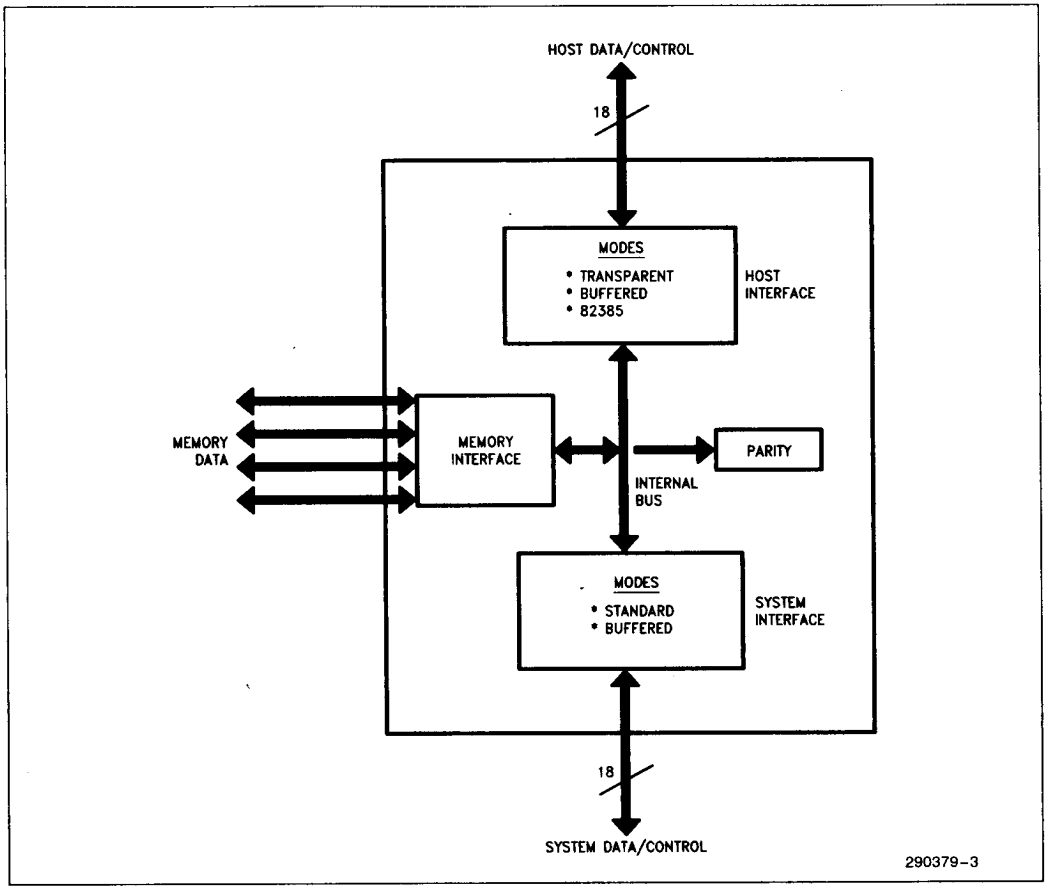


Figure 4.1. 82353 Functional Blocks

These blocks are connected together through the 82353's internal bus. This bus is 18-bits wide and consists of 16 data bits and two parity bits. It is through this bus that data is transferred between the host, system and memory interfaces.

The host interface is responsible for transferring data between the 82353's internal bus and the host Bus. This interface has three modes of operation, each differing in the way data is latched off the host bus. These three modes, labeled "Transparent Mode", "Clocked Mode", and "82385 Mode", allow the 82353 to perform optimally for a wide variety of system designs.

The system interface is responsible for data transfers between the system and the internal bus. The 82353 has two modes of operation. The standard mode incorporates internal latches and swap buffers for byte assembly and disassembly operations. It also internally generates parity for system-to-memory or system-to-host data transfers. The incorporation of the assembly/disassembly and parity generation logic make this mode ideally suited for a direct connection to the EISA bus. The buffered mode disables the internal latches and swap buffers and incorporates a burst bus similar to the host interface. In the buffered mode, the 82353 also provides the option for parity to be generated internally or externally. This mode of operation is ideal for a custom-

ized system bus that supports high performance peripherals with a "i486-like" burst capability.

The memory interface is responsible for transferring data between the internal bus and the external DRAMS. It can support a 16, 32, or 64-bit memory data bus. This block also supports burst reads or writes of up to 16 words in length in zero wait states.

During memory accesses, the parity checking circuit monitors the word of data on the internal bus and its associated two parity bits (one parity bit per byte). All parity errors which occur are indicated to external circuitry via a synchronous and an asynchronous parity error signal.

4.1 Host Interface

The host interface has three user selectable modes: Transparent Mode, Clocked Mode, and 82385 Mode. These three modes allow the system designer to have plenty of flexibility in designing the host subsection and allow the 82353 to achieve very high performance with various types of host CPUs.

The 82353 determines which mode to operate in by sampling HRD#//HLDSTB and HWCLKEN#// HWLE# pins on the falling edge of HRST (Host Reset). Table 4.1 lists the state of these pins at reset time to select the appropriate mode.

These three modes differ primarily in the way the 82353 transfers data to/from the host bus. Transparent Mode captures its data from the host bus on the rising edge of HWLE# and provides data to the host Bus when HOE# is low. Clocked Mode is very similar to transparent Mode and differs only in that it uses HWCLKEN# qualified by HCLK to latch data from the host bus. The 82385 Mode allows the 82353 to support systems utilizing the 82385 Cache Controller. In this mode, the 82385 signals BT/R#, LDSTB and DOE# control both the latching and driving of data to/from the host Bus. A full discussion and conceptual diagram of each of the three modes follows.

Although 82385 mode specifically interfaces to the 82385 Cache Controller, a variety of cache configurations are supported by using either clocked or transparent mode, including the 485Turbocache and 82395 DX Smart Cache Cache Controllers.

The host interface drives data onto the host bus under control of the HOE# signal. The source of this data is determined by the state of MIOE#. If MIOE# is asserted, data from the memory read latches will be driven; if de-asserted, data from the system interface will be driven.

Table 4-1. Selection of Host Interface Modes

Value at Falling Edge of HRST		Mode
HRD#// HLDSTB	HWCLKEN#// HWLE#	
1	0	Transparent Mode
1	1	Clocked Mode
0	x	82385 Mode

x = "Don't Care"

4.1.1 HOST TRANSPARENT MODE

Figure 4.2 shows a conceptual diagram of the host interface in Transparent Mode. Transparent Mode differs from the other host modes in the way it latches data from the host bus. Data is latched into the host interface on the rising edge of HWLE# asynchronous to HCLK.

Host Input Latch — The Host Input Latch is used for capturing data from the host bus. This is closed on the rising edge of HWLE#.

Host Read Mux — The Host Read Mux is used for selecting data from directly off the host bus or data from the Host Input Latch. Reading the Host bus directly is provided for designs which may incorporate slaves on the host bus (typically not used).

Selectable Parity Generator — The Selectable Parity Generator provides parity generation for devices on the host bus which do not provide their own parity. If HINTPAR is asserted, the 82353 will internally generate parity for the host data and ignore any parity information on the host parity inputs (HPD(1:0)).

IBus Output Buffer The IBus (internal bus) Output Buffer controls the driving of host data onto the internal bus. Data and parity information from the host interface will be driven when HIOE# is asserted.

Mem/IBus Mux The Mem/IBus Mux selects between the memory interface and the internal bus for its source of data to be sent to the host bus.

Host Output Buffer The Host Output Buffer controls the driving of data onto the host bus. Data and parity information from the host Interface will be driven to the host bus when HOE# is asserted.

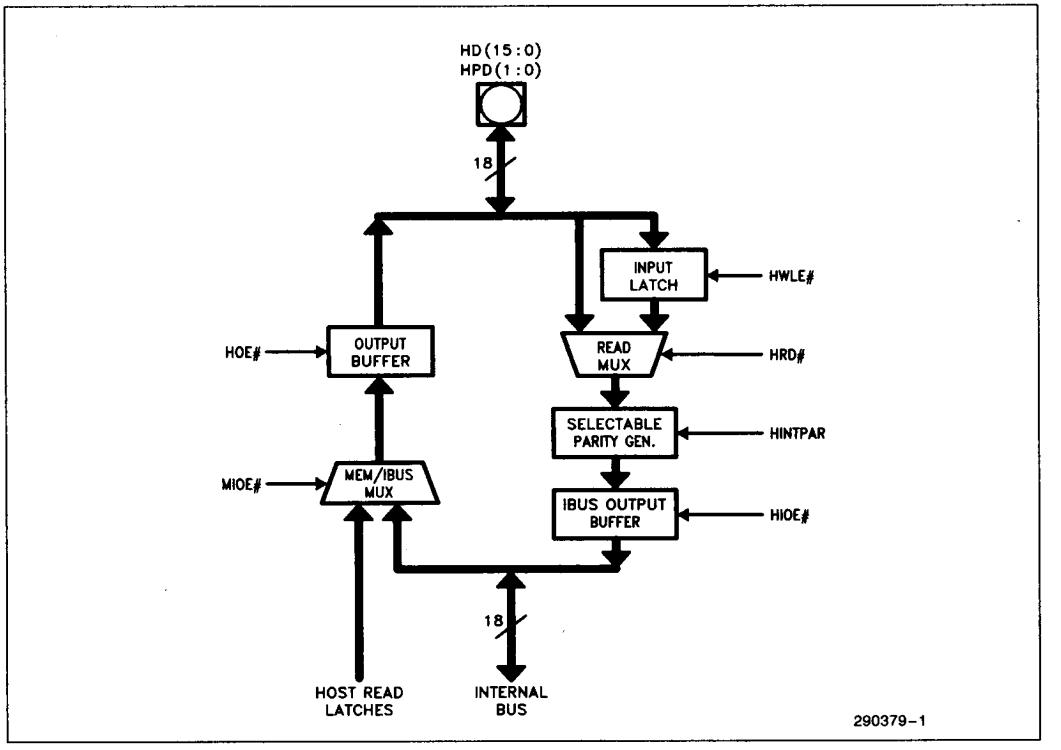


Figure 4.2. Host Transparent Mode

4.1.2 HOST CLOCKED MODE

Clocked Mode is very similar to the Transparent Mode except for one point. In this mode, host data off the host bus will be latched into the 82353 on HCLK's rising edge qualified by HWCLKEN# (Host Write Clock Enable) asserted.

Host Read Mux, Selectable Parity Generator, IBus Output Buffer, Mem/IBus Mux, and Host Output Buffer function as in Transparent Mode.

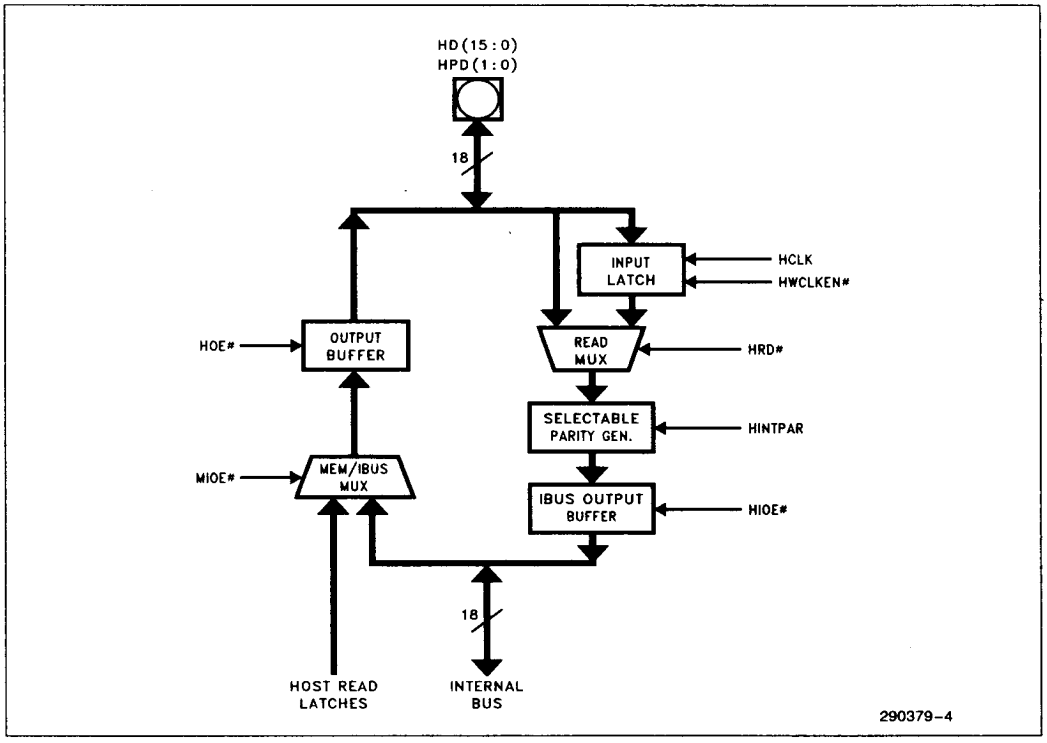


Figure 4.3. Clocked Host Mode

4.1.3 HOST 82385 MODE

Figure 4.4 shows a conceptual diagram of 82385 Mode of the host interface. The 82385 mode provides the optimum interface for systems utilizing the 82385 Cache Controller. In this mode, host data is latched off the host bus on the rising edge of HLDSTB#. (HLDSTB# should be connected directly to the 82385 LDSTB# signal.) The data is driven from the host interface onto the internal bus or host bus under control of BT/R# and DOE#, both of which should be connected to the 82385 signals of the same name.

Host Input Latch The Host Input Latch is used for capturing data from the host bus. This latch is closed on the rising edge of HLDSTB#.

IBus Output Buffer The IBus Output Buffer controls the driving of Host data onto the 82353's internal bus. Data and parity information from the host interface will be driven when the 82385 signal BT/R# is asserted (one) and DOE# is asserted.

Host Output Buffer The Host Output Buffer controls the driving of data onto the host bus. Data and parity information from the host interface will be driven to the host bus when BT/R# is deasserted (zero) and DOE# is asserted.

The Selectable Parity Generator and Mem/IBus MUX function exactly the same as Clocked and Transparent Mode.

4.2 System Interface

The System Interface can take on one of two modes of operation: Standard Mode or Buffered Mode. The desired mode is selected at reset time by state of HINTPAR when HRST is asserted. The differences between the two modes are summarized in Table 4-2.

Table 4-2. System Mode Differences

Standard Mode (HINTPAR = 0 at HRST)	Buffered Mode (HINTPAR = 1 at HRST)
System Master Can Not Provide Parity	System Master May Provide Parity
Parity Automatically Generated	Parity Can Be Generated
"i486-Like" System Burst NOT Supported	"i486-Like" System Burst Supported
Byte Output Enables	Word Output Enables
Swap Buffers Provided	Swap Buffers NOT Provided

Implementing two different modes, and the signals associated with these modes, requires that several of the system interface pins be multiplexed. These multiplex pins will have different signal names and functions dependent upon which system mode is selected. Table 4-3 lists the system signals which use a multiplexed pin.

Table 4-3. System Multiplexed Signals

Standard Mode	Buffered Mode
SDIDLE(1:0)#	SPD(1:0)
CPYEN#	SBRDY#
SOE0#	SINTPAR
SOE1#	SCLK
CPYUP	SDIDLE#
(Reserved)	SAS#
SIOE#	SOE#

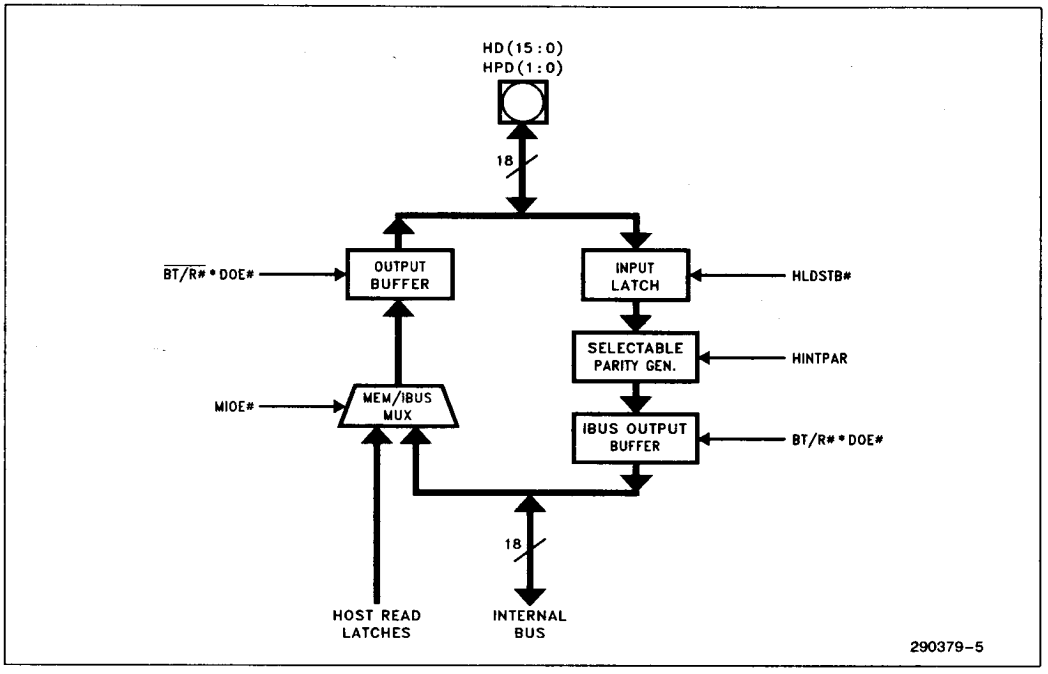


Figure 4.4. 82385 Host Mode

4.2.1 BUFFERED MODE

Figure 4.5 presents the conceptual block diagram of the Buffered Mode. The Buffered Mode is used when the system design implements a buffered bus separated from the EISA bus. This mode of operation provides the system designer with the choice of having parity generated by the 82353 or allowing the system device to provide its own parity. In addition, Buffered Mode supports the Buffered bus for "i486-like" burst transfers. Since this bus is intended to be used with masters which are the same width as the bus, Buffered Mode does not support internal byte swapping.

System Input Latch The System Input Latch consists of one 16-bit latch under control of SDIDLE#. This provides for latching data into the 82353 from the system bus. SDVLD, HBRDY#, and HAS# are used during system-to-host transfers for holding system data in the System Input Latch until the host has had a chance to read it.

Selectable Parity Generator The Selectable Parity Generator will generate parity for system devices which do not provide their own. If SINTPAR is asserted, parity will be generated by the 82353 and any parity data provided by the system device will be ignored.

IBus Output Buffer The IBus Output Buffer allows data from the system interface to be driven onto the 82353's internal bus. Data and parity information is driven when MIOE# and HIOE# are both de-asserted.

System Output Latch The System Output Latch is used for latching data bound for the system bus. The data is latched under control of IDSDLE#.

System Output Buffer The System Output Buffer controls the re-driving of system data back to the system bus. Unlike Standard Mode, this buffer is 16-bits wide and is under control of SOE#.

4.2.2 STANDARD MODE

The Standard Mode conceptual diagram is shown in Figure 4.6. Standard Mode is used when the Buffered Bus is not implemented, and the system port is directly connected to the EISA bus. The Standard Mode incorporates internal swap buffers, byte-wide output enables, byte assembly, and automatic parity generation but does not support "i486-like" system port burst transfers (although EISA Burst transfers are supported.)

Swap Buffer All transfers from the system port originate with the data entering the swap buffer structure and appearing at the System Input Latch. The swap buffer allows data appearing on either the high byte or the low byte of the system bus to be placed on the opposing byte's data lines. Swapping is enabled under control of CPYEN# and the direction of the swap is determined by the state of CPYUP. (The implementation of the 32-bit EISA bus requires that two 82353 devices be used and that external hardware be implemented to perform part of the byte swap logic. See Figure 4.9 for details.)

System Input Latch The System Input Latch consists of two 8-bit latches, the upper under control of SDIDLE1# and the lower under control of SDIDLE0#. These provide for latching data into the 82353 from the system bus. Since each 8-bit latch has its own control signal, these latches, along with the swap buffers, may be used for byte assembly. SDVLD, HBRDY#, and HAS# are used during system to host transfers for holding system data in the System Input Latch until the host has had a chance to read it.

Automatic Parity Generator The Automatic Parity Generator will generate parity for all data bound for either main memory or the host bus. Unlike Buffered Mode, there is no provision for system devices to provide their own parity.

IBus Output Buffer The IBus Output Buffer allows data from the system interface to be driven onto the 82353's internal bus. Data and parity information is driven when MIOE# and HIOE# are both de-asserted.

Loop-Back Mux The System Loop-Back Mux selects either the loop-back path (used for byte assembly and re-drive) or the 82353's internal bus (main memory or host bus data) to supply data to be driven to the system bus.

System Output Latch The System Output Latch is used for latching data bound for the system bus. The data is latched under control of IDSDLE#.

System Output Buffer The System Output Buffers control driving data to the system bus. These buffers are each byte-wide and are under control of SOE1# and SOE0#.

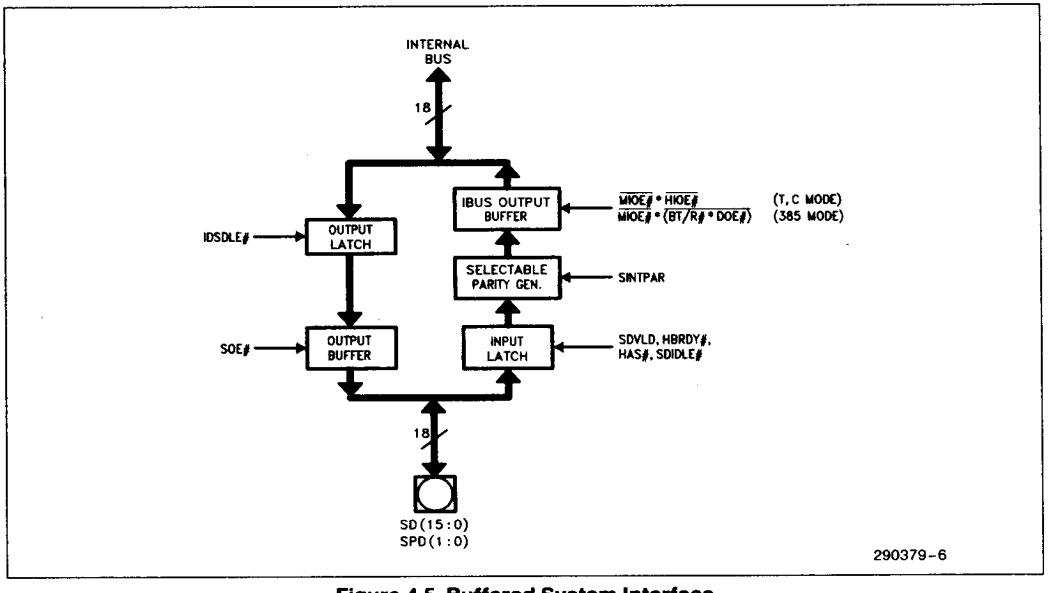


Figure 4.5. Buffered System Interface

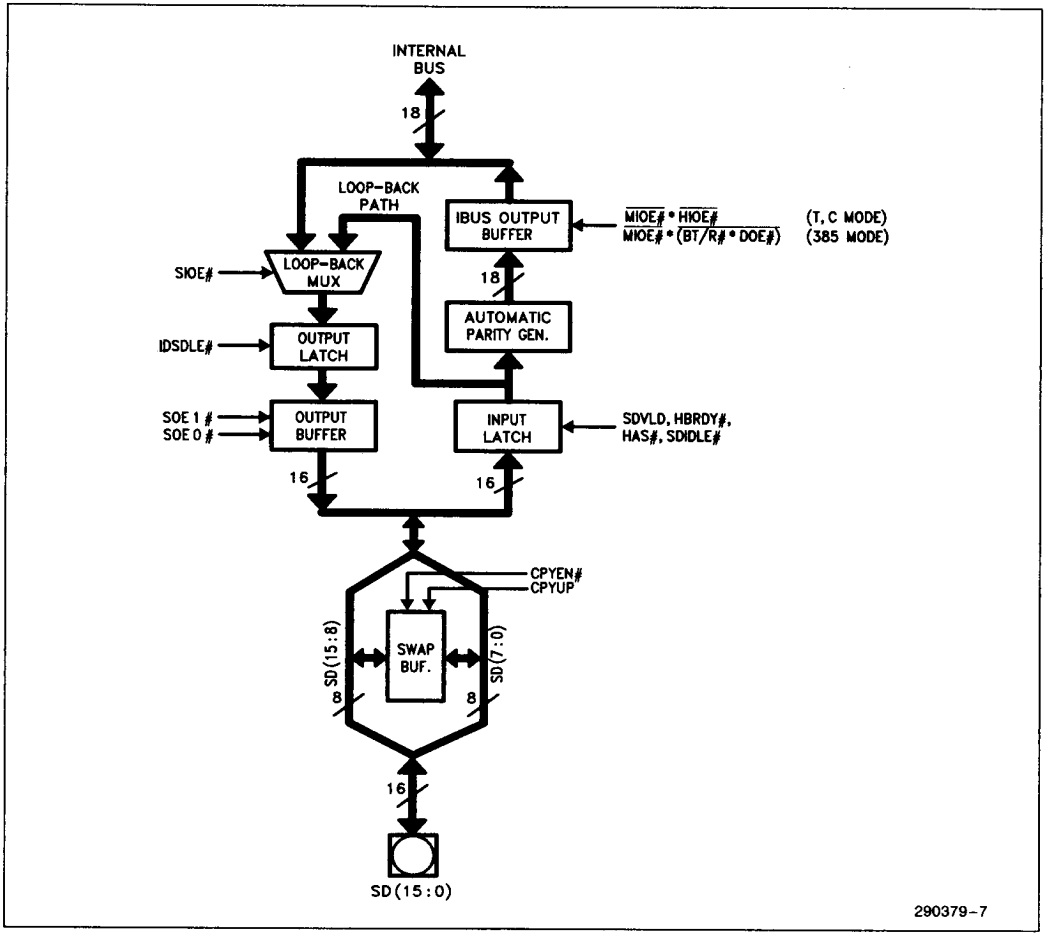


Figure 4.6. Standard System Mode

4.3 Memory Interface

As shown in Figure 4.1, the memory interface is divided into two halves: the read interface and the write interface. The purpose of these interfaces is to route data between the internal bus and the DRAM data lines. The memory interface provides single cycle or burst, read and write capability to a one, two or four word-wide main memory bus.

4.3.1 MEMORY WRITE INTERFACE

The conceptual memory write interface is shown in Figure 4.7. The second level posted write latches can be seen at the right hand side. Separate write latches are provided for host and system words, both receiving their data from the internal bus. These latches are under control of the internal state machines.

Following the write latches are the H/S# muxes. These muxes are under control of the H/S# signal (from the 82359 DRAM Controller) and their purpose is to select either the host or system write latch.

The data selected by the H/S# mux enter a second level of muxes which selects data from the write latches or directly off the internal bus. The write latches are used only during burst writes; single cycle write data takes the faster route past the write latches and H/S# mux directly to the output buffers.

The write data is placed on the DRAM data lines by the write enable buffers. WE(3:0)#, asserted by the 82359, control which combination of data words are presented to the DRAM and when each will be driven.

4.3.2 MEMORY READ INTERFACE

The conceptual Memory Read Interface is shown in Figure 4.8. The interface has separate read latches for system and host memory reads. Both Host and System Read Latch structures contain four sets of internal latches, a 16 word to 1 word mux, and a tri-state buffer. Each memory read latch is opened and closed under control of the internal state machines and each set contains four word latches; one for each of the four memory words (MD0D–MD3D). Both the Host Read Latch structure and the System Read Latch structure can hold 16 words of memory data at one time.

During burst reads, sequential memory data will be placed in either the Host or System Read Latches, dependent upon the state of H/S#. The four sets of 4-word-wide latches provide for a maximum burst read length of 16 words before the latches overflow. (Note that the 16 word burst requires 4 way word interleaved memory. Two and one way word interleaved memory structures can accommodate a maximum 8 and 4 word bursts respectively.)

The outputs of the four sets of latches are routed to a 16 word to 1 word mux. This mux is also under control of the internal state machines and IF(1:0), SEL(1:0) which select one of the 16 words in the memory read latches to be routed towards the internal bus. During burst reads the controlling state machines sequence the mux through a series of words from the latches until the burst transfer is complete. The sequence of words in the burst is determined by the value of SEL(1:0) and IF(1:0) during the lead-off cycle.

A tri-state buffer under control of HIOE# and MIOE# drives System Read Latch data onto the internal bus. No buffer is required to route data to the Host Port since the read data bypasses the internal bus and goes directly to a mux in the Host Interface.

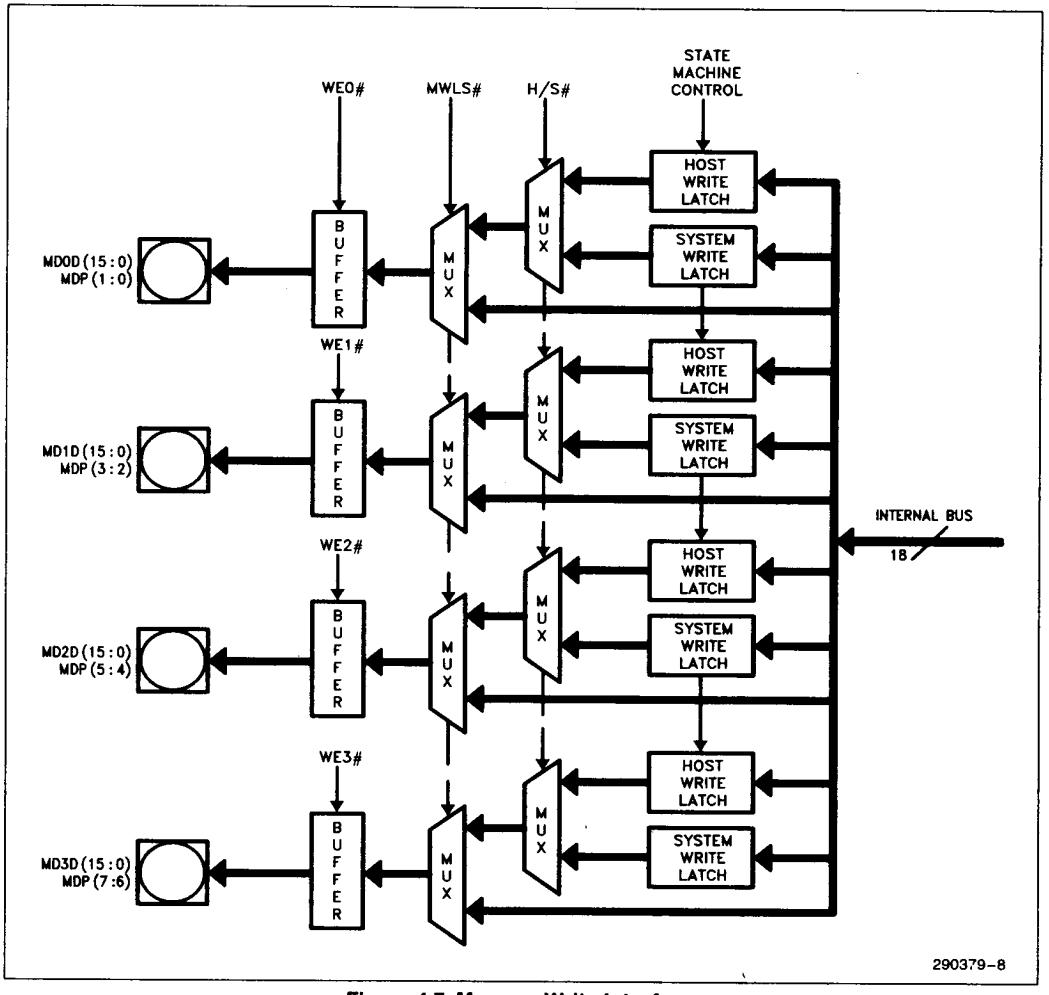


Figure 4.7. Memory Write Interface

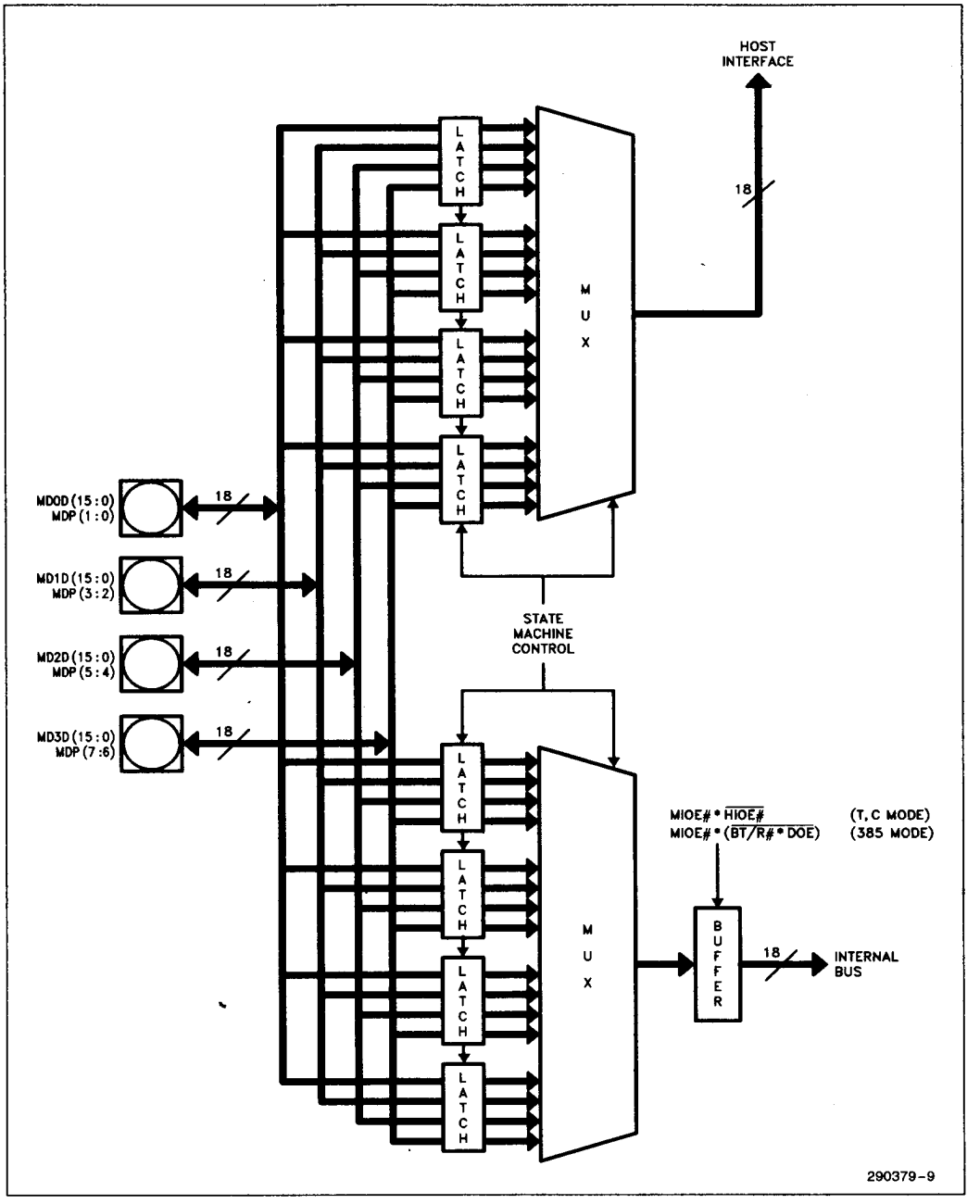


Figure 4.8. Memory Read Interface

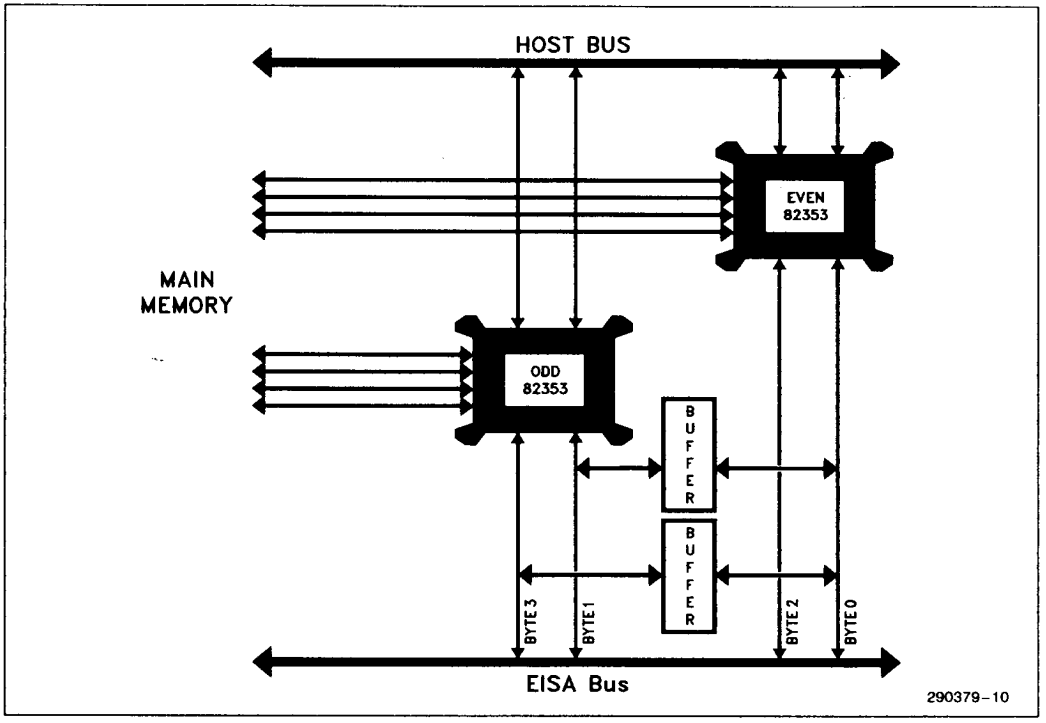


Figure 4.9. 32-Bit Data Bus Implementation Showing External Swap Buffers

5.0 DETAILED PIN DESCRIPTIONS

The following sections describe each 82353 signal in detail. The signals have been broken into three groups according to which interface the signal belongs. These groups are (1) the Host Interface; (2) The System Interface, and; (3) the Memory Interface.

5.1 Host Interface

5.1.1 HOST PINS AVAILABLE TO ALL MODES

Symbol	Type	Name and Function
HD(15:0)	I/O	**HOST DATA:** Word-wide bi-directional host data bus. HD pins are tri-stated when the signal HOE# is high (Clocked, Transparent Mode), or DOE# is de-asserted (82385 Mode). Host data pins are driven when HOE# is asserted (Clocked, Transparent Mode), or when DOE# is asserted with BT/R# low.
HPD(1:0)	I/O	**HOST PARITY DATA:** HPD pins function as parity inputs during write cycles and parity outputs during read cycles. Even parity is supported and HPD signals follow the same timings as HD(15:0).
HAS#	I	**HOST ADDRESS STROBE:** This signal is used as a host cycle strobe. The falling edge of HAS# indicates the start of a host PST cycle and the rising edge indicates the end, resetting all host clock-driven state machines. HAS# should remain asserted throughout the entire host cycle.
HARDY	O	**HOST ASYNCHRONOUS READY:** HARDY is used during host-to-system burst read cycles to indicate to the host PST that valid data is available from the system with its rising edge. Note that the 82359 DRAM Controller also has its own HARDY signal. The 82353 HARDY and the 82359 HARDY are typically 'OR'ed together. The 82359's HARDY determines the state of HARDY for host-to-system single dword cycles and the lead-off access of a host-to-system burst cycles. The 82353 controls the state of HARDY for the subsequent cycles of the host-to-system burst. In the lead-off cycle of a host burst read of the system, HARDY is controlled by the 82359 DRAM Controller. The DRAM Controller will de-assert HARDY in the lead-off cycle until it has ownership of the system bus and has completed the first fetch. From this point, HARDY is controlled by the 82353. For each of the subsequent system reads in the burst sequence, SDVLD is asserted when the 82358DT Bus Controller has finished its EISA cycle. (SDVLD indicates that an EISA bus cycle has been completed and the data has been latched into the 82353.) Upon sampling the rising edge of SDVLD, the 82353 asserts HARDY to indicate to the host PST that the current word of the burst is ready for reading. When the host reads the data word as indicated by HBRDY#, HARDY becomes de-asserted until the next rising edge of SDVLD. This sequence is repeated until the burst transfer is completed.

5.1.1 HOST PINS AVAILABLE TO ALL MODES (Continued)

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>HBRDY#</td><td>I</td><td>
HOST BURST READY: HBRDY# is sampled by the 82353 on the rising edge of HCLK and indicates when the host is ready for the next word of a burst read cycle. During a burst read cycle, HBRDY# asserted indicates to the 82353 that the previous word of the burst has been read and the host is requesting the next word.

In a write cycle, HBRDY# asserted during the rising edge of HCLK indicates to the 82353 that a next word of the burst is valid on HD(15:0), at which time one of the 82353 write latches is closed. Which write latch is closed is determined by the combination of IF(1:0) and SEL(1:0) as sampled on the first active HBRDY#.
<table>
<tr><th colspan="3">IF(1:0)</th><th colspan="2">SEL(1:0)</th><th>Write Latch Close Sequence</th></tr>
<tr><td>(4-way)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0-1-2-3</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>1-0-3-2</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>2-3-0-1</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>3-2-1-0</td></tr>
<tr><td>(2-way)</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0-1-0-1</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>1-0-1-0</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>2-3-2-3</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>3-2-3-2</td></tr>
<tr><td>(1-way)</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0-0-0-0</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>1-1-1-1</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>2-2-2-2</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>3-3-3-3</td></tr>
<tr><td></td><td>1</td><td>1</td><td>X</td><td>X</td><td>System Port Access</td></tr>
</table>
</td></tr>
<tr><td>HCLK1/2X#</td><td>I</td><td>
HOST CLOCK SELECT: This pin is strapped to indicate the type of HCLK being used. The strapping of this pin selects between the either a 2x 386-like clock or a 1x 486-like clock. If strapped high, then the HCLK input is 1x the operating frequency of the 82353, TTL clock levels are expected, and the HRST input is asynchronous.

If strapped low, the HCLK input is divided by two by the 82353 before being used internally, CMOS clock levels are expected, and HRST must be synchronous. (The falling edge of HRST causes the internal clock phase to be set.)
</td></tr>
<tr><td>HCLK</td><td>I</td><td>
HOST CLOCK: This is the clock reference for operations related to the host port of the 82353. HCLK can be either 1x or 2x of the internal operating frequency of the 82353, dependent upon the strapping of HCLK1/2X#.
</td></tr>
<tr><td>HINTPAR</td><td>I</td><td>
HOST INTERNAL PARITY SELECT: HINTPAR specifies whether the 82353 or the host will be generating/checking parity for host port cycles. If HINTPAR is de-asserted, host data parity is generated/checked by host masters and the PERSTB# signal is disabled for host read cycles. If HINTPAR is asserted, parity is generated/checked by the 82353 and PERSTB# is enabled to indicate parity errors.

At reset time, HINTPAR determines which system port mode (Buffered or Standard Mode) is desired by sampling the value of HINTPAR on the falling edge of HRST.
<table>
<tr><th colspan="2">HINTPAR at HRST System Mode</th></tr>
<tr><td>0</td><td>Standard Mode</td></tr>
<tr><td>1</td><td>Buffered Mode</td></tr>
</table>
</td></tr>
</table>

5.1.1 HOST PINS AVAILABLE TO ALL MODES (Continued)

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>HRST</td><td>I</td><td>HOST RESET: HRST resets the 82353 internal state machines when asserted. The falling edge of HRST configures the host interface Mode and system interface mode as given in the following tables:

Host Interface Mode Selection
<table><tr><th colspan="2">At HRST Falling Edge</th><th rowspan="2">Host Interface Mode</th></tr><tr><th>HRD#// HLDSTB</th><th>HWCLKEN#/ / HWLE#</th></tr><tr><td>1</td><td>0</td><td>Transparent Latch Mode</td></tr><tr><td>1</td><td>1</td><td>Clocked Latch Mode</td></tr><tr><td>0</td><td>x</td><td>82385 Mode</td></tr></table>x = "Don't Care"

System Interface Mode Selection
<table><tr><th>At HRST Falling Edge HINTPAR</th><th>System Interface Mode</th></tr><tr><td>0</td><td>Standard Mode</td></tr><tr><td>1</td><td>Buffered Mode</td></tr></table>If HCK1/2X# is strapped for 2x, HRST falling edge must be synchronous to phase 1 of the HCLK to set the 82353's internal clock phase. If HCLK1/2X# is strapped for 1X, HRST is asynchronous.</td></tr>
<tr><td>PERSTB#</td><td>OC</td><td>PARITY ERROR STROBE: PERSTB# is an open collector signal which indicates to the host or system master that a parity error has occurred. PERSTB# is valid only when internal parity checking is enabled (HINTPAR = 1 or SINTPAR = 1), the memory access is to main memory (IF(1:0) < >11), and SBRDY# or HBRDY# is asserted. This is an active low, one SCLK or HCLK period wide pulse (dependent on which port currently owns the internal bus).</td></tr>
<tr><td>RESIST</td><td>I</td><td>CURRENT DRIVE REGULATOR: Connect through a 900Ω ±5% resistor to GND.</td></tr>
</table>

5.1.2 TRANSPARENT MODE PINS

Symbol	Type	Name and Function
HIOE#	I	**HOST INTERNAL OUTPUT ENABLE:** This pin enables host data onto the 82353's internal data bus. HIOE# is controlled by the 82359 DRAM Controller. The assertion of HIOE# always overrides the setting of MIOE#. (See MIOE# for related information.)
HRD#	I	**HOST READ:** Assertion of HRD# enables a data path from the host bus towards the internal bus, bypassing all write latches. HRD# is provided for designs which allow a system master to read a host bus slave. The typical system design would tie HRD# to logical "1".
HOE#	I	**HOST OUTPUT ENABLE:** Enables data to be driven from the 82353's internal bus to the host bus.
HWLE#	I	**HOST WRITE LATCH ENABLE:** The host write latch is transparent when HWLE# is low and latches host data on its rising edge.

5.1.3 CLOCKED MODE PINS

Symbol	Type	Name and Function
HIOE#	I	**HOST INTERNAL OUTPUT ENABLE:** This pin enables host data onto the 82353's internal data bus. HIOE# is controlled by the 82359 DRAM Controller. The assertion of HIOE# always overrides the setting of MIOE#. (See MIOE# for related information.)
HRD#	I	**HOST READ:** Assertion of HRD# enables a data path from the host bus towards the internal bus, bypassing all write latches. HRD# is provided for designs which allow a system master to read a host bus slave. The typical system design would tie HRD# to logical "1".
HOE#	I	**HOST OUTPUT ENABLE:** Enables data to be driven from the 82353's internal bus to the host bus.
HWCLKEN#	I	**HOST WRITE CLOCK ENABLE:** HWCLKEN# asserted enables the host write latch to capture host bus data on HCLK rising edge.

5.1.4 82385 MODE PINS

Symbol	Type	Name and Function
BT/R#	I	**82385 BT/R#:** This pin determines the direction of data flow in the host interface and should be connected to the BT/R# of the 82385. (See DOE#).
HLDSTB	I	**HOST LOCAL DATA STROBE:** The rising edge of this signal latches data into the posted write buffer inside the 82353. HLDSTB should be connected to LDSTB of the 82385.
DOE#	I	**DATA OUTPUT ENABLE:** This pin is directly connected to the 82385 DOE#. This pin, together with the BT/R# signal, decides when data on the internal bus is driven onto the host bus.

DOE#	BT/R#	82353 Action
0	0	Host Interface drives Host Bus
0	1	Host Interface drives Internal Bus
1	x	Host and Internal Bus not driven

5.2 System Interface

5.2.1 SYSTEM PINS AVAILABLE IN BOTH MODES

Symbol	Type	Name and Function
SD(15:0)	I/O	**SYSTEM DATA:** Bi-directional system data bus. In Buffered Mode, SD pins are tri-stated when signal SOE# is high, and driven when SOE# is low. See SOE(1:0) for a description of the driving and tri-stating of the SD(15:0) pins in Standard Mode.
IDSDLE#	I	**INTERNAL DATA TO SYSTEM DATA LATCH ENABLE:** IDSDLE# is generated by the bus controller for host-to-system write cycles to latch host data into a second level posted write buffer on the system port of the 82353. Data going into this latch can come from one of the two sources: (1) the 82353's internal bus (data coming from either host or memory ports), or; (2) data from the loop-back path in which an EISA master cycle requires byte assembly (in Standard Mode only).
SDVLD	I	**SYSTEM DATA VALID STROBE:** Indicates to the 82353 that valid system data has been latched off the system bus. SDVLD's rising edge causes the system latch to ignore any further SDIDLE#'s until the host is finished reading the data (signified by either the rising edge of HAS# or HBRDY being sampled asserted).

Output Path

82353 Inputs				82353 Outputs		Transfer Type
CPYEN#	CPYUP	SOE1#	SOE0#	SD(15:8)	SD(7:0)	
1	X	1	1	HI-Z	HI-Z	
1	X	1	0	HI-Z	ID(7:0)	H, M, L → SD
1	X	0	1	ID(15:8)	HI-Z	H, M, L → SD
1	X	0	0	ID(15:8)	ID(7:0)	H, M, L → SD
0	0	0	0	*** Invalid ***		
0	0	0	1	ID(15:8)	ID(15:8)	H, M, L → SD
0	0	1	0	*** Invalid ***		
0	0	1	1	HI-Z	SD(15:8)	S → SD
0	1	0	0	*** Invalid ***		
0	1	0	1	*** Invalid ***		
0	1	1	0	ID(7:0)	ID(7:0)	H, M, L → SD
0	1	1	1	SD(7:0)	HI-Z	S → SD

IB = Internal Data
SD = System Data Bus
HI-Z = High Impedence
H = Host Data
M = Main Memory Data
L = Loop-back Data
S = System Data

5.2.2 STANDARD MODE PINS

Symbol	Type	Name and Function
SDIDLE(1:0)#	I	**SYSTEM TO INTERNAL DATA LATCH ENABLES (BYTE 1,0):** Used for latching system data into the 82353. On SDIDLE#'s rising edge, a data passing through the swap buffer structure is latched into the 82353. Since a SDIDLE# is provided for each byte, these may be used for byte assembly with 8-bit peripherals.
CPYEN#	I	**COPY ENABLE:** CPYEN# enables the internal byte swapping logic. CPYEN# de-asserted causes CPYUP to be ignored.
SOE(1:0)#	I	**SYSTEM OUTPUT ENABLES (BYTE WIDE):** SOE(1:0) controls the system output buffers which drive data from the system interface to the SD pins. Two SOE# bits are provided, one for each byte. When CPYEN# is not asserted (no byte swapping taking place), SOE1# directly controls the driving of the high SD byte and SOE0# directly controls driving of the low SD byte. When CPYEN# is asserted, byte swapping is enabled, and the output buffers are under control of a combination of SOE(1:0)# and CPYUP. **Input Path** CPYEN# / CPYUP / IB(15:8) / IB(7:0) 0 / 0 / SD(15:8) / SD(15:8) 0 / 1 / SD(7:0) / SD(7:0) 1 / x / SD(15:8) / SD(7:0)
CPYUP	I	**COPY UP:** CPYUP determines the direction of the byte swap. CPYUP asserted places the low order byte data SD(7:0) on the high order byte SD(15:8). CPYUP de-asserted places the high order byte data on the low order byte, SD(15:8) on to SD(7:0). When copying occurs, the SD pins being copied to should not be driven by the master since the copied data will be duplicated on the destination SD pins. (See SOE(1:0)# for more details.)
SIOE#	I	**SYSTEM INTERNAL OUTPUT ENABLE:** SIOE# selects the source of SD data as either the internal bus or the loop-back data path. (See Figure 4.8). SIOE# asserted selects data from the SD input latch to be re-routed back the SD pins via the loop-back path, as required for byte assembly. SIOE# de-asserted selects data from the internal bus to be used for driving to the SD(15:0) pins.

5.2.3 BUFFERED MODE PINS

Symbol	Type	Name and Function
SPD(1:0)	I/O	**SYSTEM PARITY DATA:** SPD pins function as parity inputs during write cycles and parity outputs during read cycles. Even parity is supported and SPD indicates are expected to follow the same timings as SD.
SBRDY#	I	**SYSTEM BURST READY:** SBRDY# is sampled by the 82353 on the rising edge of SCLK and indicates when the system master is ready for the next word of a burst. During a system PST master burst read cycle, the assertion of SBRDY# indicates to the 82353 that the current data of the burst has been read by the system PST master and the master is ready for the next word. In a system PST master write cycle, SBRDY# indicates to the 82353 that the next data word of the burst is valid on the system data lines. The assertion of SBRDY# causes the one of the four 82353 memory write latches to close, latching the data into the memory interface. Which one of the four write latches is closed is determined by the initial sampling of IF(1:0) and SEL(1:0) on the first active SBRDY# of the burst.
SINTPAR	I	**SYSTEM INTERNAL PARITY SELECT:** A strap which specifies whether the 82353 or the system PST master is responsible for system bus parity generation/checking. If SINTPAR is low, it is the system PST master's responsibility to generate and test system bus data parity and the PERSTB# signal will not respond to system cycle. If SINTPAR is high, parity on the SP(1:0) is ignored, the 82353 will generate and check system bus data parity, and PERSTB# will respond to indicate any system bus parity errors.
SCLK	I	**SYSTEM CLOCK:** SCLK is the system state machines clock source. SCLK should be connected to the system bus clock used by system masters.
SDIDLE#	I	**SYSTEM DATA TO INTERNAL DATA LATCH ENABLE:** SDIDLE# latches system data into system interface on its rising edge. (SDVLD must be de-asserted for SDIDLE# to have any effect on the latch.)
SAS#	I	**SYSTEM ADDRESS STROBE:** The falling edge of SAS# indicates the start of a system transfer cycle. SAS# should remain asserted throughout the entire system access and will reset the system state machines on its rising edge.
SOE#	I	**SYSTEM OUTPUT ENABLE:** SOE# controls the system interface output buffer. When SOE# is asserted, data from the internal bus is driven on to the system bus. SOE# de-asserted causes the SD oins to be tri-stated. SOE# is controlled by the system PST (in Buffered Mode).

5.3 Memory Interface

Symbol	Type	Name and Function
MD0D(15:0)	I/O	**MEMORY DATA 0:** Bi-directional data bus to/from DRAMs for word 0
MD1D(15:0)	I/O	**MEMORY DATA 1:** Bi-directional data bus to/from DRAMs for word 1
MD2D(15:0)	I/O	**MEMORY DATA 2:** Bi-directional data bus to/from DRAMs for word 2
MD3D(15:0)	I/O	**MEMORY DATA 3:** Bi-directional data bus to/from DRAMs for word 3
MPD(7:0)	I/O	**MEMORY PARITY DATA:** Parity bits for DRAM word 0-3. The 82353 expects even parity when checking for parity errors. Bits are assigned as follows: Bits 0,1 word 0 Bits 2,3 word 1 Bits 4,5 word 2 Bits 6,7 word 3
H/S#	I	**HOST/SYSTEM PORT SELECT:** H/S# indicates which port (host/system) of the dual port owns the memory interface. During a write to memory, H/S# is used to select either the host write latches or the system write latches in the memory interface. During a read of memory, H/S# determines whether the host or system memory read latches are used in latching data from main memory, and which set of read latches provides data to the parity checking circuitry.
IF(1:0)	I	**INTERLEAVE FACTOR:** IF(1:0) is input from the 82359 DRAM Controller that reflects the DRAM interleave configuration for the row being accessed. The IF(1:0) combination allows for intelligent data multiplexing during memory burst read cycles, and for correct data routing during burst writes. During burst accesses to main memory, IF(1:0) is sampled and latched on the rising edge of HCLK/SCLK during the first HBRDY/SBRDY. Burst reads require that IF(1:0) be setup one HCLK/SCLK prior the first HBRDY/SBRDY of the burst. During non-burst accesses to main memory, IF(1:0) is not latched and must be valid throughout the entire access. (See the functional timing diagrams for examples.)
MDS#	I	**MEMORY DATA STROBE:** When MDS# is asserted, the memory read latches are opened. MDS# rising edge causes the 82353 to close the memory read latches in the memory interface, latching DRAM data. MDS# is generated by the 82359 DRAM Controller to indicate that DRAM data is valid and present on the memory data bus.
MIOE#	I	**MEMORY INTERNAL OUTPUT ENABLE:** MIOE#, along with HIOE#, control the ownership of the 82353's internal bus. When HIOE# is asserted, the host interface drives the Internal bus regardless of the state of MIOE#. When HIOE# is de-asserted, MIOE# controls whether the memory interface or system interface will drive the internal bus.

Dword Interleave Factor

IF(1:0)		Memory Dword Interleave Factor
0	0	4-way
0	1	2-way
1	0	1-way
1	1	System Port access*

*IF(1:0) = 11 causes a non-deterministic cycle to occur.

HIOE#	MIOE#	Driving Internal Bus
0	x	Host Interface
1	0	Memory Interface
1	1	System Interface

x = "Don't Care"

5.3 Memory Interface (Continued)

Symbol	Type	Name and Function
MWLS#	I	**MEMORY WRITE LATCH SELECT:** MWLS# controls the memory write latch mux'es. MWLS# asserted allows the data held in either the host or system memory write latches to reach the memory data bus output buffers. If MWLS# is de-asserted, data directly from the 82353's internal bus is allowed to reach the memory output buffers.
PER#	O	**PARITY ERROR:** PER# is a combinatorially generated parity error signal. PER# asserted indicates that a parity error has been detected on the data word being read out of either the host or system memory read multiplexer (which multiplexer is checked is determined by the state of H/S#). PER# is asserted only for parity errors during main memory reads.
SEL(1:0)	I	**SELECTS:** SEL(1:0) are input from the 82359 DRAM Controller which selects which one of four possible dwords was requested by the memory cycle's originator. For non-burst cycles, SEL(1:0) is latched on the rising edge of MDS#. During burst reads and writes, SEL(1:0) is sampled on the rising edge HCLK/SCLK during the first HBRDY#/SBRDY# of the burst. The status of SEL(1:0) determines the order words will be stored for the predictable order burst cycle ("i486-like" burst cycle). **i486 Burst Order** SEL(1:0) → Burst Dword Order 0 0 → 0-1-2-3 0 1 → 1-0-3-2 1 0 → 2-3-0-1 1 1 → 3-2-1-0 During burst read sequences, SEL must be valid and stable one HCLK/SCLK edge prior to the first HBRDY#/SBRDY# of the burst. During single word reads, SEL determines which one of the four memory read latches will supply data to the internal bus. In this case, SEL(1:0) is not latched and must be valid throughout the entire main memory cycle.
WE(3:0)#	I	**WRITE ENABLES:** WE(3:0)# act as output enables for data being written to main memory. A WE# asserted allows the corresponding memory write buffer of the 82353 to drive its data on to the memory bus. Any given WE# must be delayed from another WE# by at least 10 ns to comply with the internal noise minimization requirement. (Only 16 data signals and 2 parity bits are allowed to switch at any time to avoid excessive noise from being generated inside the 82353.) The 82353 WE# are connected to the WE(3:0) signals of the 82359 DRAM Controller.

6.0 FUNCTIONAL DIAGRAMS

The following section presents several key functional timing diagrams. These diagrams show functional signal generation only and no A.C. specifications should be implied.

6.1 Single Read of Memory

The start of a system single cycle read of main memory differs depending on the source of the request. If the system design incorporates a high speed system bus (82353 Buffered Mode), the 82353 system port requests may originate from masters on either this Buffered Bus or the EISA bus. For systems which do not implement the Buffered bus, system port requests originate only from EISA or ISA bus masters.

System PST masters may request a single word read of memory through their PST. This high speed bus does not follow EISA cycle definitions and requires that bus masters have a PST to communicate with the 82359 DRAM Controller. The PST will signal the start and end of a system originated cycle by falling and rising edge of SAS#.

EISA or ISA masters must follow their bus cycle definitions, starting cycles with START#, MRDC#, or

MWTC# and ending cycles with CMD#. The 82359 DRAM Controller monitors the EISA and ISA control signals and knows when to start cycles.

A host single word read of memory always begins on the falling edge of HAS# and ends on the rising edge, requiring all host bus masters to have a PST.

Once the cycle has started, MIOE# is asserted and HIOE# is de-asserted to enable a data path from memory to the 82353 Internal bus. Either SOE# or HOE# is asserted dependent upon the data destination of either system or host bus.

The memory read latches are opened at the start of the cycle by the falling edge of MDS#. One of the memory bus data words, selected by IF(1:0) and SEL(1:0), will propagate to the host or system outputs if the host or system output drivers are enabled (See HOE#, SOE#, and SOE(1:0)#). The data will be captured in the memory read latches on the rising edge of MDS#.

The cycle ends by HAS# or SAS# being de-asserted, at which time IF(1:0), SEL(1:0), HIOE#, and MIOE# become invalid. The data is removed from the destination bus by SOE#, SOE(1:0)# or HOE# being de- asserted.

System Single Word Read of Main Memory

Figure 6.1 shows a system read of main memory. Note that SAS# may or may not be asserted dependent on the type of bus master who originates the request as discussed above. One to four words are provided by main memory dependent upon the memory interleave factor for the memory bank being accessed. The correct word, as specified by SEL(1:0) and IF(1:0), will be sent to the system bus.

Host Single Read of Main Memory

Figure 6.2 shows a host single word read of main memory. Unlike system accesses, host accesses always start with HAS#'s falling edge and end on the rising edge.

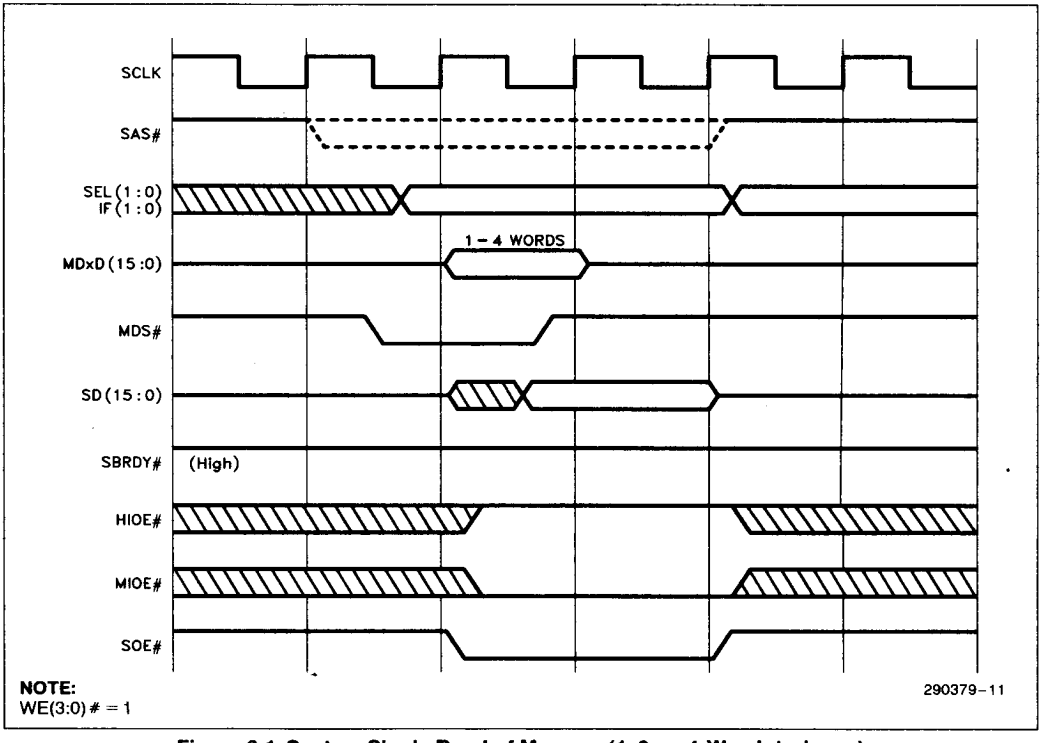
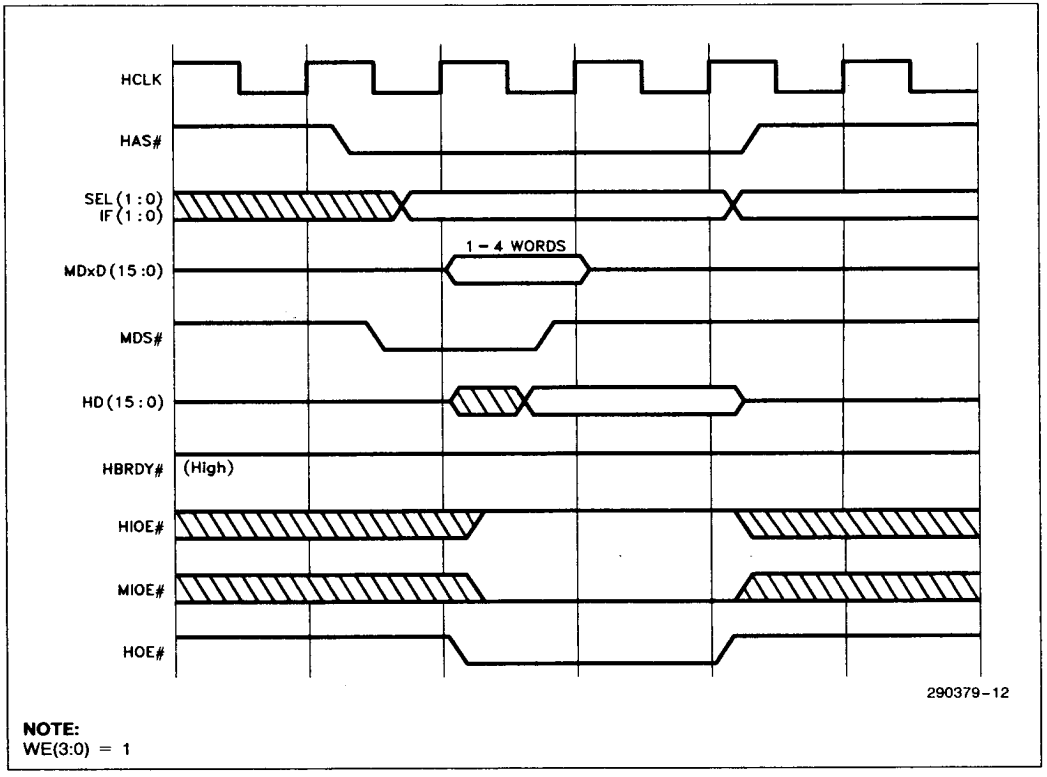


Figure 6.1. System Single Read of Memory (1, 2, or 4-Way Interleave)



NOTE:
WE(3:0) = 1

Figure 6.2. Host Single Read of Memory (1, 2, or 4-Way Interleave)

6.2 Burst Read of Memory

An i486-type burst read of memory is available only to the host bus and Buffered bus masters. Like any host (or system PST master) bus cycle, the burst begins with a HAS# (or SAS#) falling edge and ends on its rising edge. IF(1:0) and SEL(1:0) are sampled on the first HBRDY# (or SBRDY#) and provide the interleave information and burst word order. Unlike burst writes, burst reads require that IF(1:0) and SEL(1:0) be setup one clock edge prior to the first HBRDY# (or SBRDY#) being asserted.

MIOE# is asserted and HIOE# is de-asserted to enable a path from memory to the 82353 internal bus. Either SOE# or HOE# is asserted dependent upon the data destination of system or host bus.

MDS# asserted opens the memory read latches and allows the first word in the burst (determined by IF and SEL) to propagate to the internal bus. Depending on IF(1:0), one, two, or four words of memory are latched into the 82353 read latches on the rising edge of MDS#. Due to HOE# (SOE#, SOE(1:0)#) being asserted, the data on the internal bus appears on the host or system bus. If the host or system outputs are enabled, data from memory will propagate to the host or system bus.

If memory is four words wide, only one memory fetch is required for a four word burst. Two word wide memory requires 2 fetches, and one word wide memory requires four fetches. Each extra fetch causes MDS# to be asserted then de-asserted, latching the new memory data required to continue the burst. The extra memory fetches may introduce wait states depending on the CPU and memory speed, therefore four word wide memory is optimal for masters/CPU's which utilize burst transfers.

Each time HBRDY# (or SBRDY#) is sampled asserted on the rising edge of HCLK (or SCLK), the next word in the burst sequence is provided to the host (or system) bus. If the next word is not in the memory read latches, an extra memory fetch is started, and the next word in the burst will be available before the next rising edge of MDS#.

The burst transfer is ended by HAS# (or SAS#) being de-asserted, at which time IF(1:0), SEL(1:0), HIOE#, and MIOE become invalid. The data is removed from the destination bus by SOE#, or HOE# going high.

Burst Read of Memory, Four Way Word interleaved Structure

Figure 6.3 shows a host or system burst read of four way word interleaved main memory. Since four word interleaved memory is used, all four words of data needed for the burst are fetched with one memory access. This allows the 82353 to provide a zero wait-state burst, one word of data per clock cycle.

Burst Read of Memory, 2 Word Interleaved Structure

Figure 6.4 shows the sequence of events for a burst read of two-way word interleaved memory. Two-way word interleaved memory requires two memory accesses to complete a four word burst. The requirement of the second memory access may place a one clock wait state between the second and third word of the burst depending on the speed of memory and the CPU clock period.

Burst Read of Memory, 1 Word Interleaved Structure

Figure 6.5 shows a burst read of one word interleaved main memory. Four memory fetches are required to complete the burst, each causing a wait-state to be added between words. Again, one-way word interleaved memory is less desireable than either two-way or four-way word interleaved memory due to the added memory fetches required to complete the burst transfer.

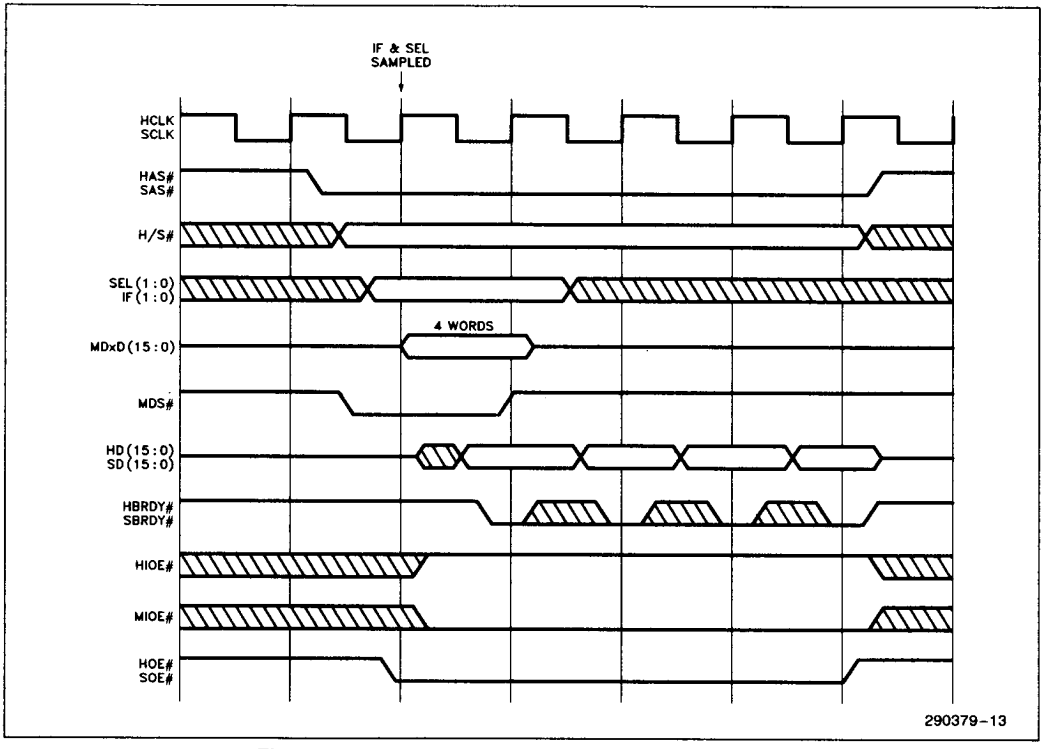


Figure 6.3. Burst Read of Memory (4-Way Interleave)

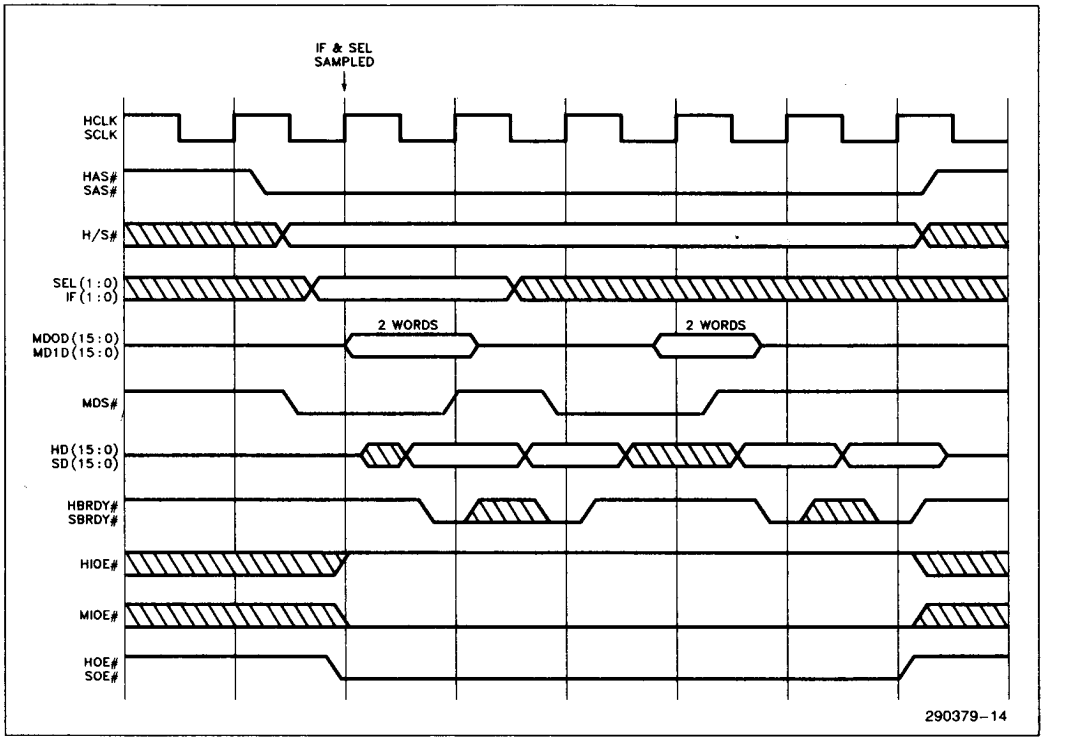


Figure 6.4. Burst Read of Memory (2-Way Interleave)

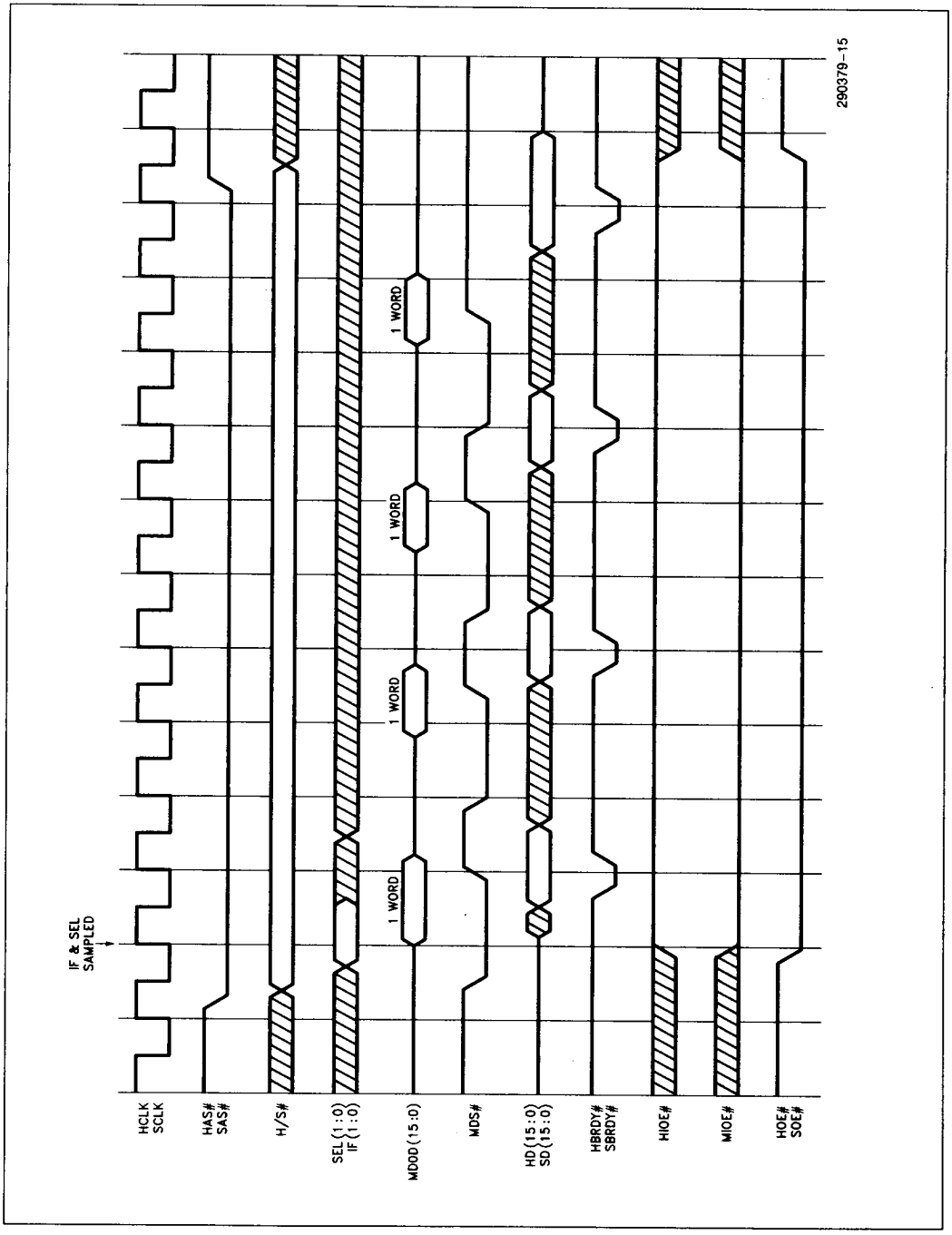


Figure 6.5. Burst Read of Memory (1-Way Interleave)

6.3 Single Write of Memory

A single word write to memory may originate from the host CPU, a system PST master, or an EISA bus master. The cycle start and end indicators are dependent on which bus the master resides.

If the host originates the single word write request, HAS#'s falling edge begins the cycle and rising edge ends the cycle. If the design incorporates a Buffered bus and the cycle originates from there, SAS# controls the start and end of the cycle similar to the host. If the request is from the EISA bus, no SAS# is needed since the 82359 DRAM Controller monitors START#, MRDC#, MWTC#, etc. and from this knows when to run the cycle.

The correct WE# is asserted by the 82359 DRAM Controller dependent upon the address and interleave factor of the current main memory cycle. MIOE# and HIOE# are configured to enable a data path from the host or system port to memory. MWLS# should be de-asserted, enabling the data to bypass the memory write latches and proceed to the memory output buffers. The state of H/S# is not needed because the data is bypassing the memory write latches.

The assertion of WE# acts as an output enable on the corresponding 18 bits of the main memory data lines. This data may be invalid until the data from the host (or system) bus has a chance to propagate through to the memory bus.

Data is written to memory on the falling edge of CAS#. (CAS# is generated by the DRAM Controller.) When the WE# is de-asserted, the memory bus is tri-stated.

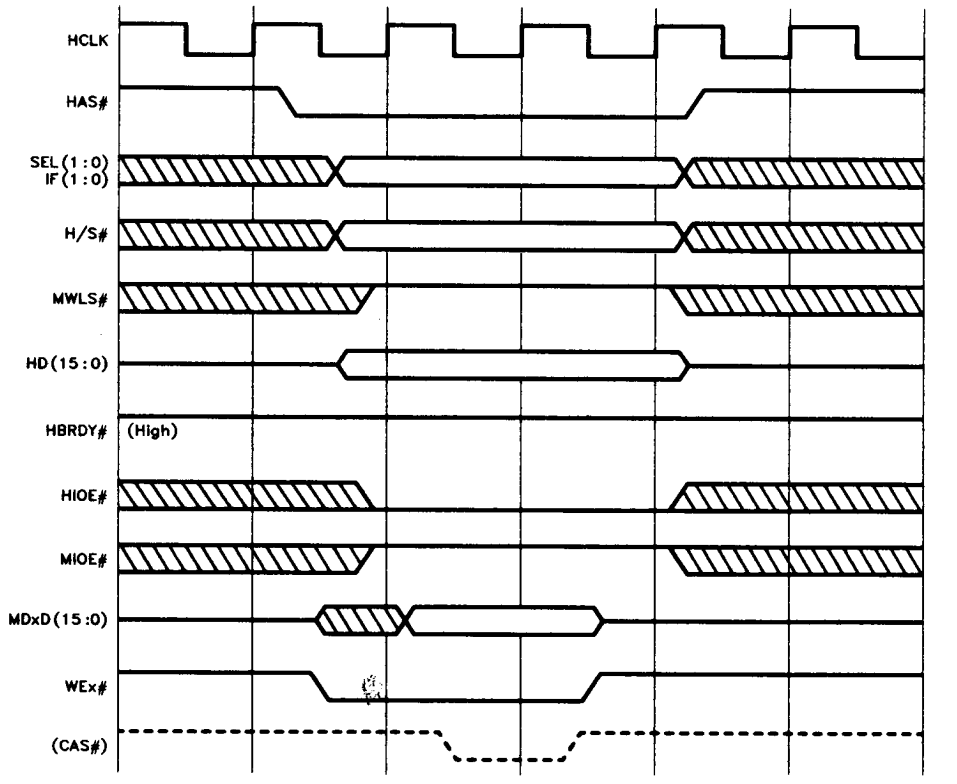
The write cycle terminates by the rising edge of HAS# or SAS# (which ever was originally asserted to start the cycle) or CMD# in EISA accesses.

Host Single Word Write to Memory

Figure 6.6 is a host single word write to main memory. This figure shows a general timing diagram, with the specific WEx# and MDxD(15:0) not specified. The 82359 DRAM Controller knows the destination address for the word, and will assert the appropriate WEx#.

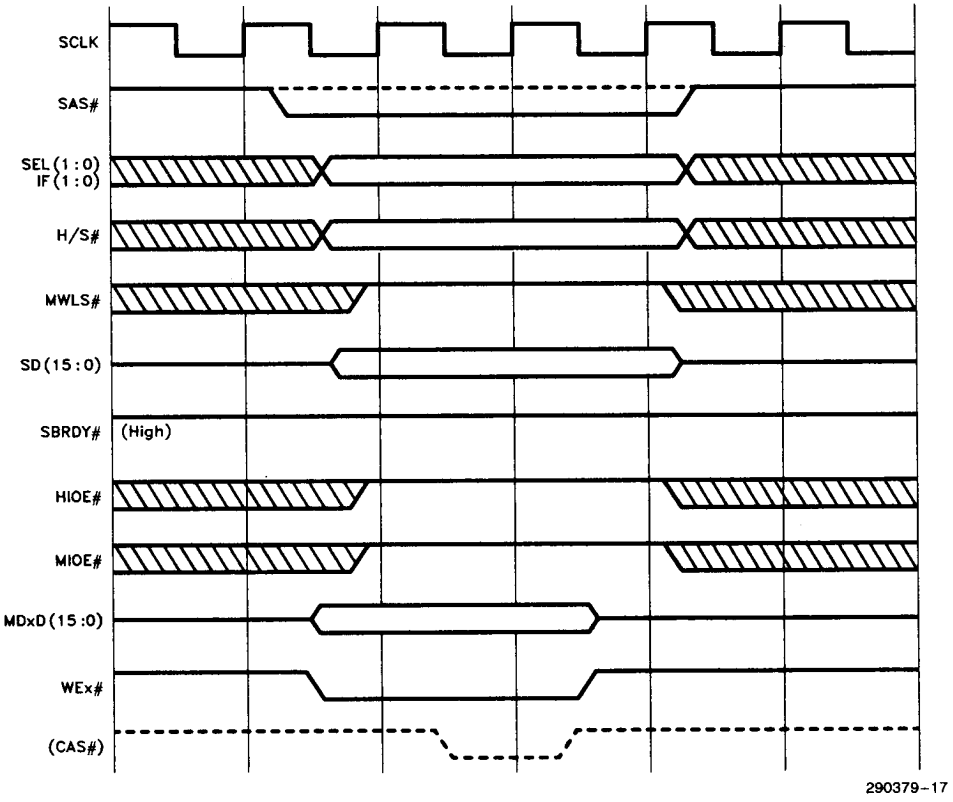
System Single Word Write to Memory

Figure 6.7 is a system port single word write to main memory. Notice that SAS# may or may not be asserted, depending on whether the cycle originates from a system PST master or the EISA bus.



NOTE:
CAS# is not an 82353 signal. It is shown only for completeness.

Figure 6.6. Host Single Write to Memory



NOTE:
CAS# is not an 82353 signal. It is shown only for completeness.

Figure 6.7. System Single Write to Memory

6.4 Burst Write of Memory

A burst write cycle to main memory begins with HAS# (or SAS#) falling. MIOE# and HIOE# are configured for a memory write, either from host or system port.

IF(1:0) and SEL(1:0) are sampled during the first HBRDY# (or SBRDY#). SEL(1:0) determines the first word of the burst and IF(1:0) determines the remaining burst sequence. Both signals originate from the 82359 DRAM Controller. Unlike burst reads, IF(1:0) and SEL(1:0) must be setup to the first HBRDY# (or SBRDY#) rather than the clock edge prior to the first HBRDY# (or SBRDY#).

Each word of the burst is latched into the 82353 on the rising HCLK (or SCLK) edge qualified by HBRDY# (or SBRDY#), at which time the host or system PST master may provide the subsequent word of the burst.

A sequence of words is provided by the host or system PST master until the end of the burst is signaled by HAS# (or SAS#) rising edge. Although optimum performance is achieved by providing words on a one-per- clock basis, this need not be the case. Peripherals not capable of a one-word-per-clock transfer, or with one-way or two-way word interleaved memory organizations may delay HBRDY# (or SBRDY#) to insert wait-states in the burst. In systems with one-way or two-way word interleaved memory, delaying HBRDY# (or SBRDY#) allows for the insertion of DRAM write cycles (see Figures 6.10 and 6.11).

The burst will continue as long as HAS# (or SAS#) is asserted. If the burst is extended past the usual "i486-like" burst, the burst write latch sequence will start over, repeating the same sequence indicated by the sampled IF(1:0) and SEL(1:0) until HAS# (or SAS#) is de-asserted. This allows for essentially unlimited burst lengths.

The 82353 is limited to 16 memory data bits changing at any given time to minimize the amount of internal noise. This can be accomplished in one of two ways, depending on how the DRAM controller asserts WE#'s. (WE#'s control the driving of memory data, thus can be used to control the noise requirement.) If the DRAM controller asserts all WE#'s in the same clock period, the DRAM Controller should stagger any one WE# from another by a minimum of 10 ns (as is the case for the 82359 DRAM Controller). This guarantees that only one word changes at any given time to minimize internal noise (Figure 6.9).

A second approach is for the DRAM controller not to assert a WE# until the data is available (Figure 6.8). Since each word of the burst is separated by at least one clock, this approach guarantees WE# separation by at least one clock.

All the figures show a burst sequence of 1-0-3-2. These figures are only examples. The actual sequence is determined by the value of SEL(1:0) and IF(1:0) during the first SBRDY#.

Burst Write to Memory, Four-Way Word Interleaved Main Memory

Figure 6.8 shows a burst write to four-way word interleaved main memory from either host or buffered system bus. This figure illustrates an example of separated WE#'s. In this diagram, each of the four words of the burst are written to memory as soon as they are available. The WEx#'s are each enabled only when their data is available, satisfying the condition that at least 10 ns separate WE#'s.

Burst Write to Memory, Staggered WEx#'s, Four-Way Word Interleaved Main Memory

Figure 6.9 shows a burst write to four-way word interleaved main memory. This differs from Figure 6.8 in that staggered WEx#'s are used rather than separated WEx#'s. Also different, the four words are written to memory all at the same time with a single occurrence of CAS# rather than one at a time with multiple occurrences of CAS#. Note that the WE# signals are staggered by at least 10 ns to limit noise generated by driving the memory data lines.

Burst Write to Memory, Staggered WEx#'s, Two-Way Word Interleaved Main Memory

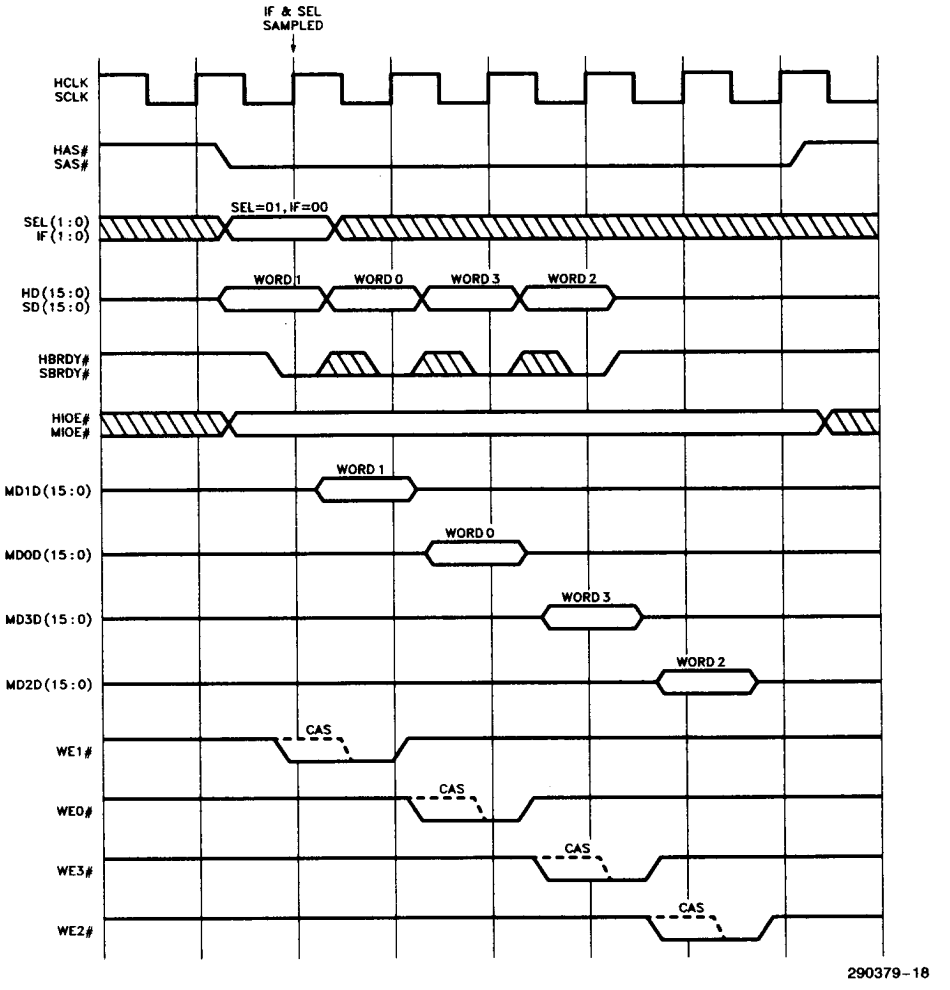
Figure 6.10 shows a burst write to two-way word interleaved main memory. One wait-state is inserted between the second and third word in the burst by delaying HBRDY# (or SBRDY#) to allow the data to be written to memory.

Burst Write to Memory, One-Way Word Interleaved Main Memory

Figure 6.11 is a burst write to one-way word wide memory. Here delaying of HBRDY# (or SBRDY#) is used to insert the memory write to occur before proceeding with the burst.

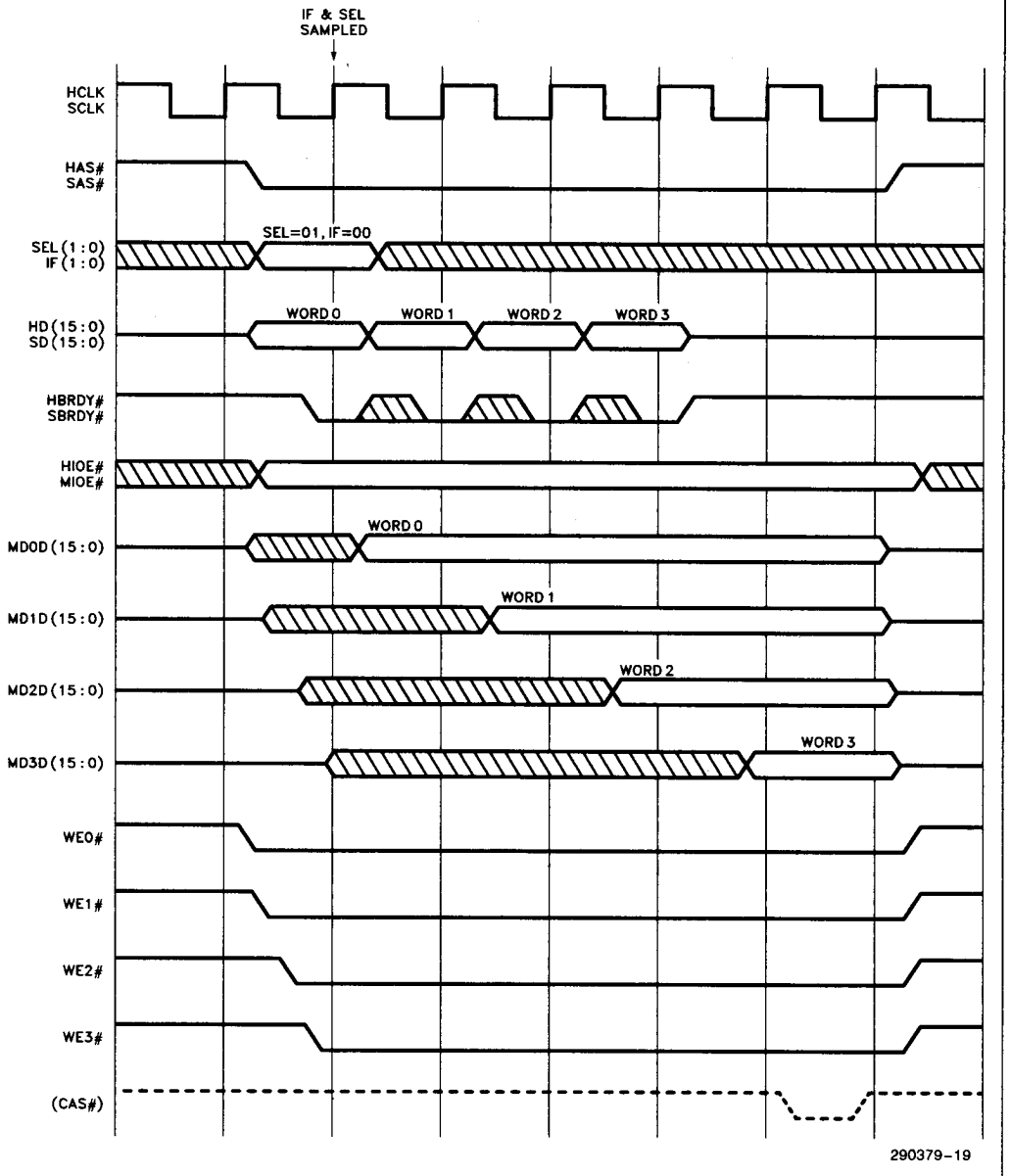
Burst Write to Memory, Sustained 0 Wait-State, Four-Way Word Interleaved Memory

Figure 6.12 shows an example of burst write cycles to four word interleaved memory providing essentially a sustained zero wait-state write capability.



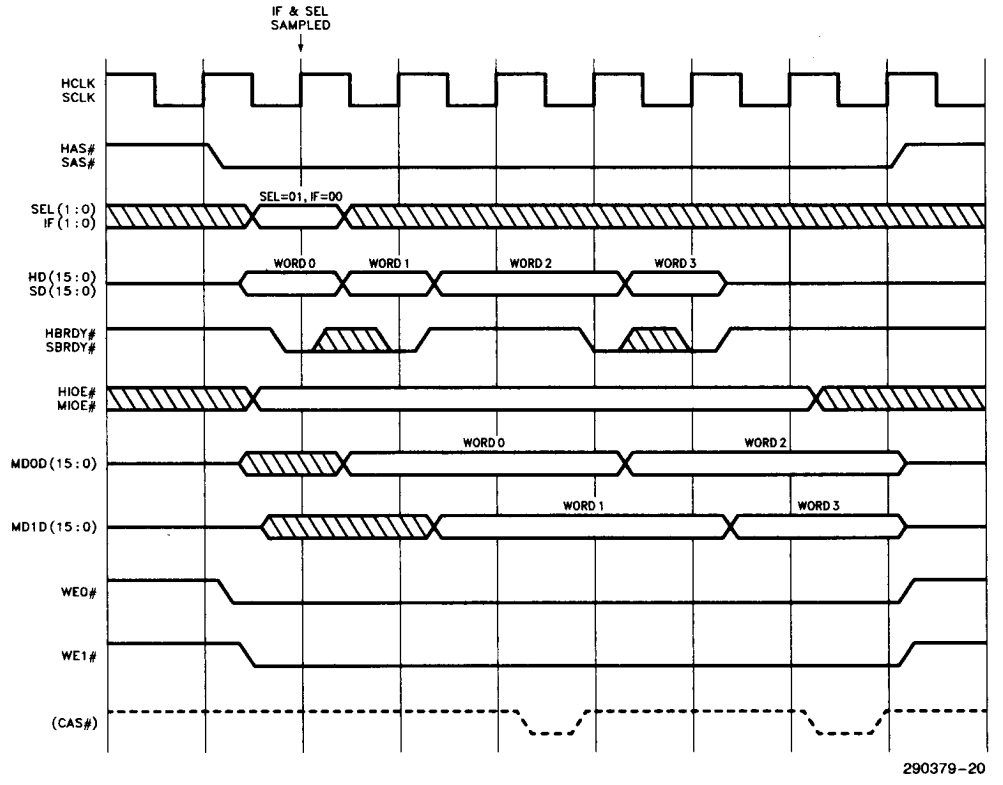
NOTE:
Burst Sequence: (1 0 3 2) due to SEL(1:0) = 01 during the first SBRDY#. CAS# is not an 82353 signal. They are shown only for completeness.

Figure 6.8. Burst Write to Memory (4-Way Interleave, Separate CAS# Cycles)



NOTE:
Burst Sequence: (1 0 3 2) due to SEL(1:0) = 01 and IF(1:0) = 00 during the first SBRDY#. CAS# is not an 82353 signal. They are shown only for completeness.

Figure 6.9. Burst Write to Memory (4-Way Interleave, Single CAS# Cycle)



NOTE:
CAS# is not an 82353 signal. It is shown only for completeness. The burst sequence (1 0 1 0) is due to SEL(1:0)=01 and IF(1:0) = 01 during the first HBRDY#.

Figure 6.10. Burst Write to Memory (2-Way Interleave)

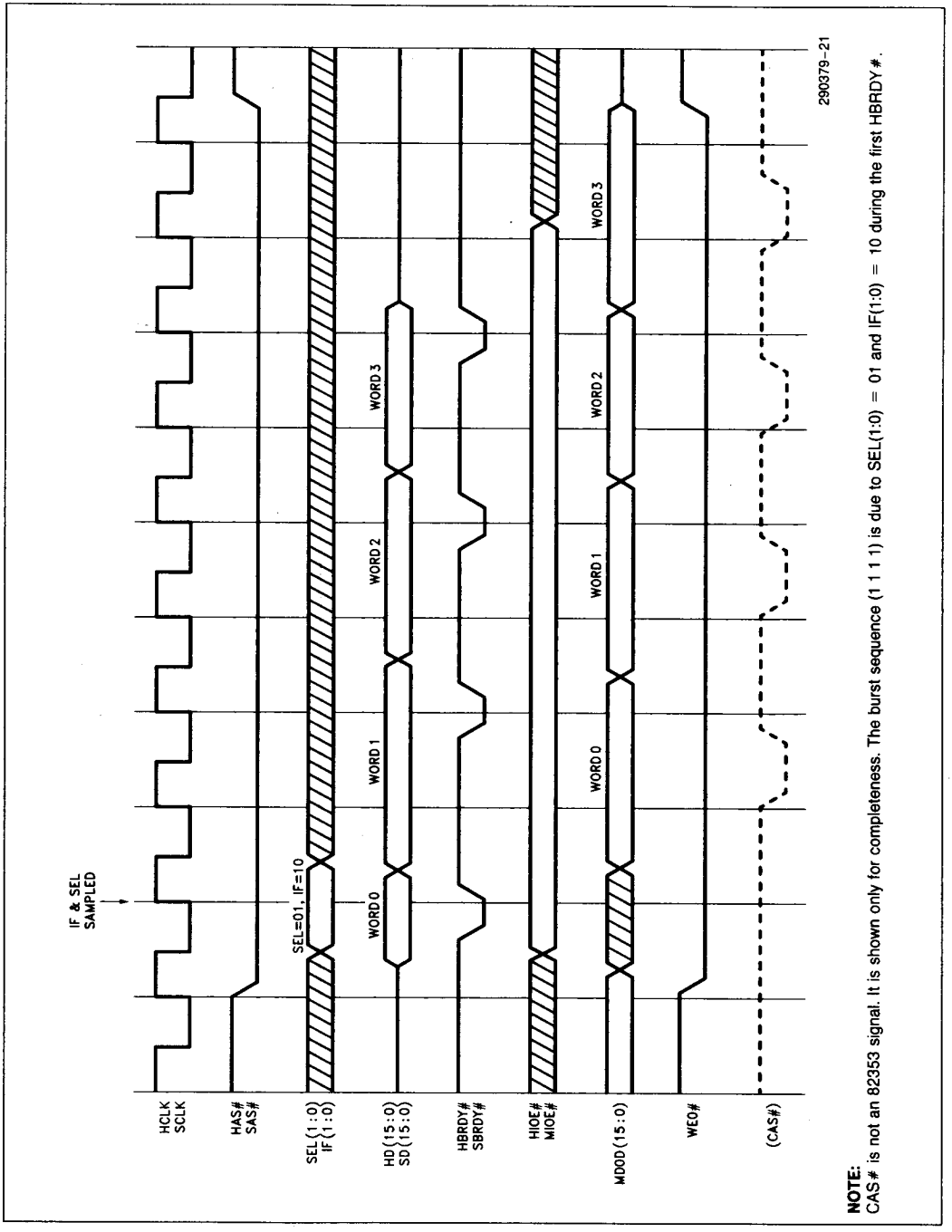


Figure 6.11. Burst Write to Memory (1-Way Interleave)

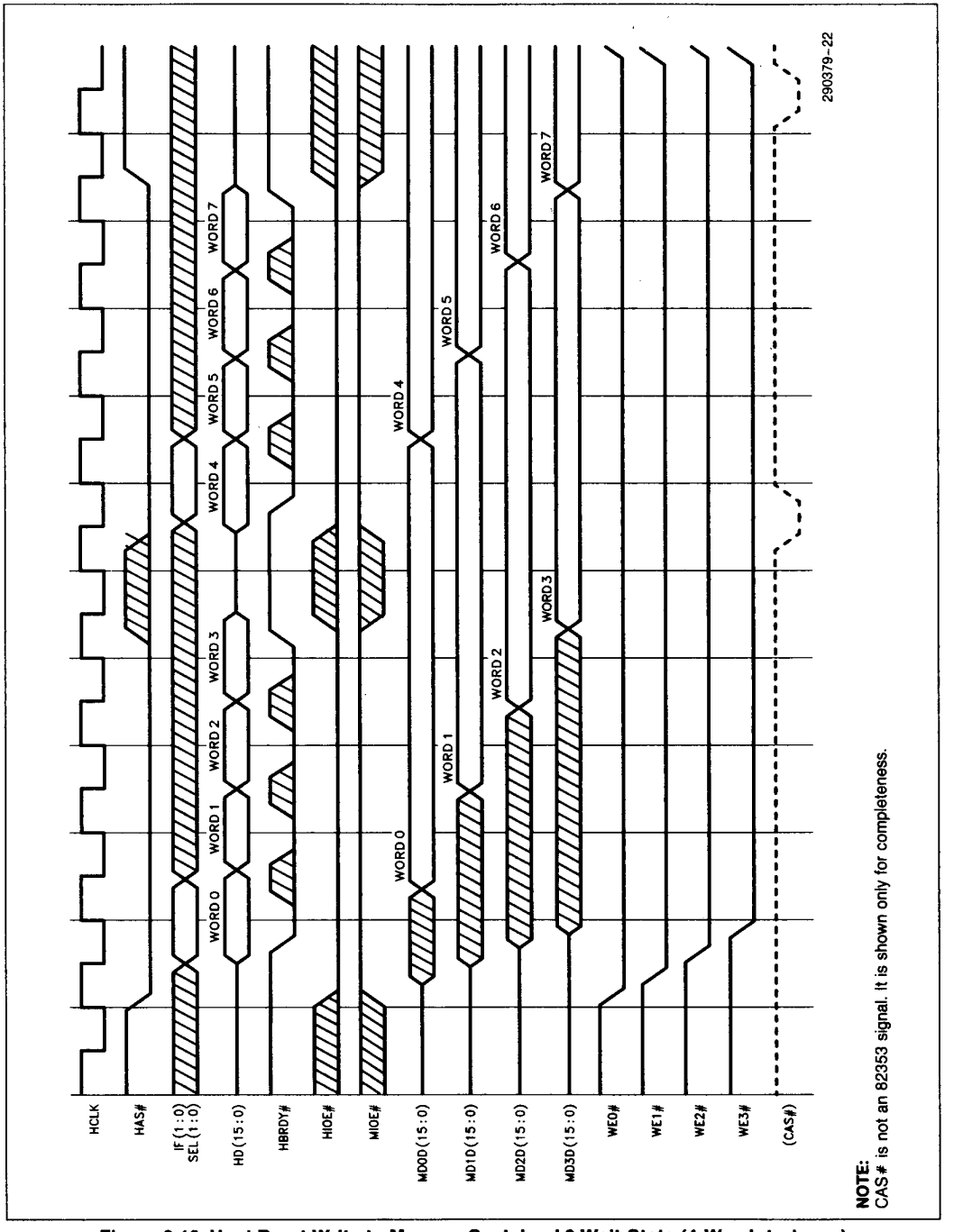


Figure 6.12. Host Burst Write to Memory Sustained 0 Wait-State (4-Way Interleave)

6.5 Host Read of System

A host to system transfer begins with the assertion of HAS#. The DRAM Controller, upon decoding the address, will determine that the transfer is a read from the system port and will de-assert HARDY and activate SAS# to the bus controller. MIOE# and HIOE# are configured for a host read of the system port and HOE# is asserted allowing the data on the internal bus to be driven on the host bus.

Once the system bus request is placed by the 82359, an undetermined amount of time may pass until the requesting master takes ownership. The system cycle begins with the falling edge of START#. Again an undetermined delay may arise before the cycle is ended with rising edge of CMD#. The length of the delay is related to the access times of the slave being addressed. The end of the system cycle is signified by CMD# being de-asserted, at which time the data is valid on the system bus.

The rising edge of CMD# causes the 82358 EISA bus Controller to assert a combination of the byte assembly latch signals IDSDLE (1:0)#, dependent on the size of the slave. IDSDLE (1:0)# latch data from the system port into the 82353 on a byte basis. When the system bus controller has read a word of data from the slave, the EBC asserts SDVLD. The assertion of SDVLD causes the system read latches to become locked, ignoring any further IDSDLE (1:0)# signals until the host has read the latched data, indicated by HBRDY# or the rising edge of HAS#. At this time the latch is re-enabled and ready for further assertions of IDSDLE (1:0)#.

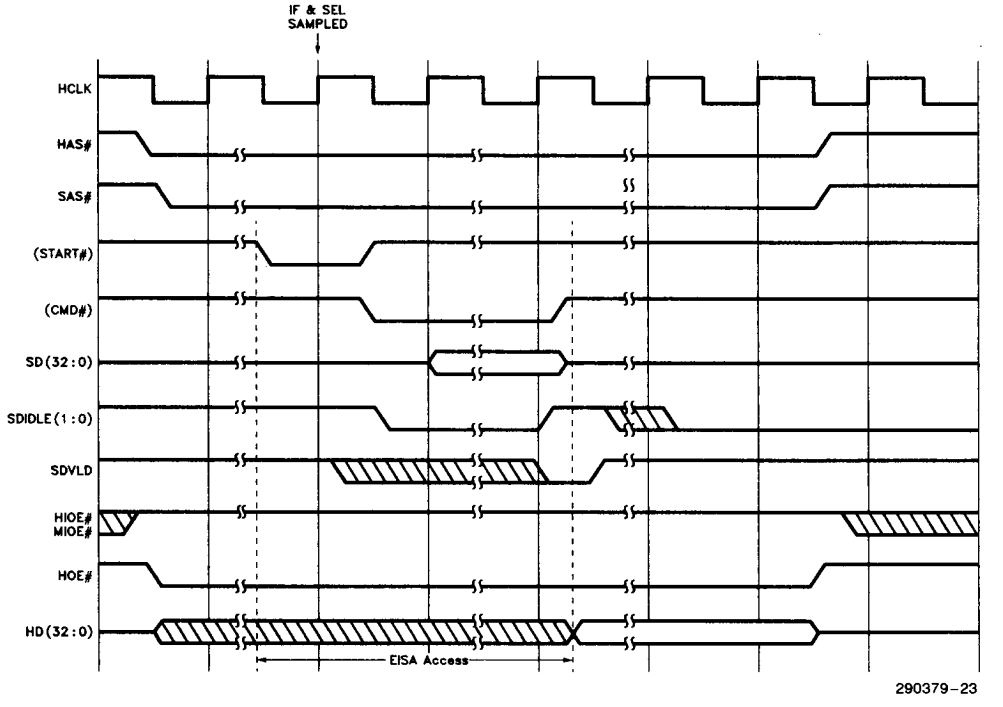
The end of the system cycle causes the assertion of HARDY, indicating to the host master that the data is now ready for reading. The master reads the data and ends the cycle with the de-assertion of HAS#.

Host Single Read of System: 32-Bit Slave (Uses Two 82353s)

Figure 6.13 shows a host read of a 32-bit System slave. Only one system cycle is needed due to the slaves 32-bit size.

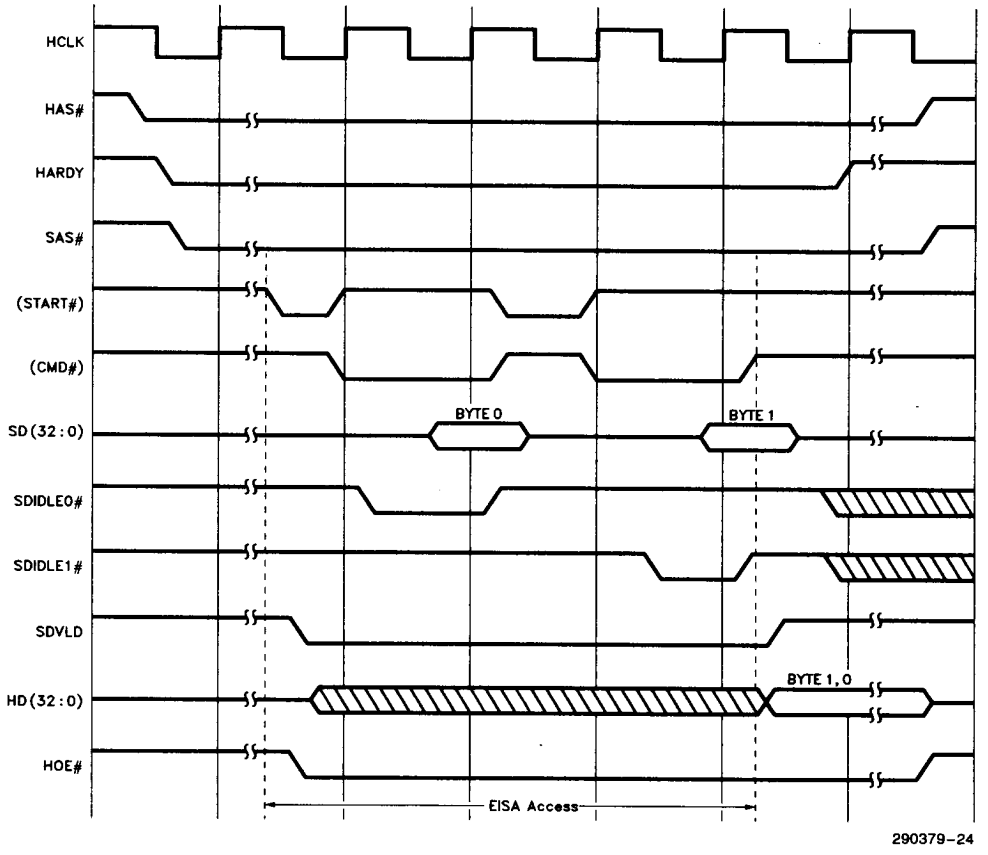
Host Single Read of System: System Access Requires Multiple System Cycles

Figure 6.14 shows a host access to an 16-bit system slave. Two system bus cycles are needed to assemble a 32-bit quantity which is returned to the host. The byte assembly signals SDIDLE (1:0)# are generated by the EBC. For an 8-bit slave, assembling a 32-bit quantity would require four system cycles.



NOTES:
1. START# and CMD# are EISA signals. They are not connected to the 82353, but shown to signify an EISA bus cycle.
2. The EISA Access is in no way related to HCLK.

Figure 6.13. Host Single Read of System (32-Bit Slave)



NOTES:
1. START# and CMD# are EISA signals. They are shown to indicate an EISA access, but are in no way connected to the 82353.
2. The EISA Access is in no way related to HCLK.

Figure 6.14. Host Single Read of System (16-Bit Slave)

6.6 HCLK 1X/2X#

All the previous diagrams show the 82353 strapped for HCLK (1X). The 82353 also is able to work with processors which use two phase clocks such as the 80386. The indication to the 82353 of either 1x or 2x CPU clock frequency is the strapping of the HCLK 1X/2X#.

If HCLK 1X/2X# is sampled low, the HCLK input is expected to be 2x the CPU clock frequency, and the 82353 will internally divide HCLK by 2. Processors like the 80386 use this type of divide by two scheme, each processor T-state having two clock cycles. The first clock cycle is labeled phase-1 and the second is labeled phase-2. The 82353 is also given this phase labeling and must be in phase with the 386. Setting the correct phase relationship is done at 82353 reset time. To start the 82353 and 80386 in the same phase, HRST must be synchronous to the phase 1 clock edge. When HRST is negated, the next clock cycle to appear on HCLK is assumed to be a phase one of the 80386. If HRST in not synchronous, HCLK may be out of phase and the 80386 phase-2 may be assumed to be 82353 phase-1. In 2x mode, all timing relationships are from the phase-1 rising edge, just as if the clock was in 1x mode.

If HCLK 1X/2X# is sampled high, the HCLK input is expected to be 1x the CPU clock frequency, and therefore no phase is implied. In this case HRST may be asynchronous.

See Figure 6.15 for a HCLK 1x and 2x diagram.

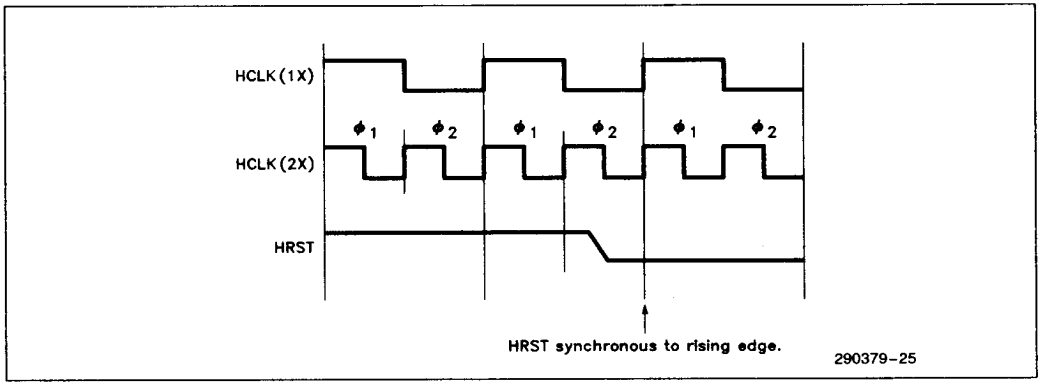


Figure 6.15. HCLK 1X/2X Waveforms

6.7 Host Latch Modes

In the previous diagrams, no mention was given to data latching during host write cycles. Recall that three modes of host operation are available, each differing primarily in the way data is latched off the host bus. Figure 6.16 shows these three modes and how and when the 82353 latches data from the host.

Transparent Mode: In transparent mode, asserting HWLE# causes the host Write Latch to become transparent. The rising edge of HWLE# latches whatever data is currently in the latch.

Clocked Mode: Clocked Mode latches data from the host bus on the rising edge of HCLK qualified by HWCLKEN# asserted. The host Read Latch never becomes transparent, regardless of the state of HWCLKEN#.

82385 Mode: 82385 Mode behaves like an edge-triggered latch. Data from the host bus is clocked-in on the rising edge of HLDSTB. Once data is latched, control of data flow is provided through the use of DOE# and BT/R#.

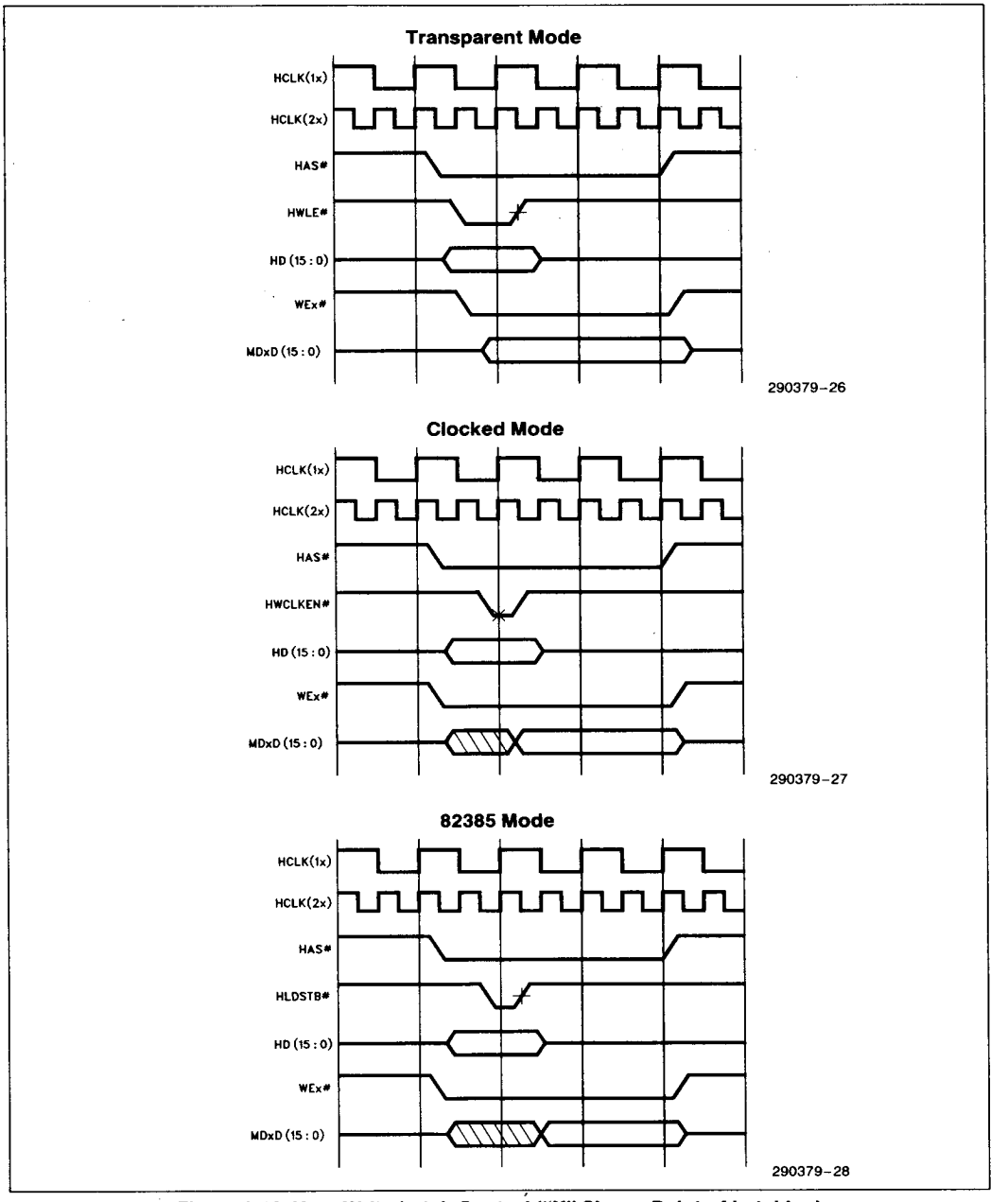


Figure 6.16. Host Write Latch Control ("X" Shows Point of Latching)

6.8 Parity Errors

Figure 6.17 shows a sample cycle in which a parity error occurred. Parity data contained in the host and system memory read latches is compared to parity generated internally. Which set of latches (host memory read latches or system memory read latches) is used is controlled by the setting of the H/S# signal. PER# will be asserted as soon as the error is detected and remain asserted as long as read parity bits and generated parity bits differ. PER# is sampled by the 82359 DRAM Controller for EISA or ISA cycles when the 82353 does not generate PERSTB#.

For masters on either the host or Buffered bus which require a PST (and typically do not generate/check parity), an error pulse is provided by way of the PERSTB# signal. PERSTB# is generated by a state machine one clock after the PER# is sampled asserted. The pulse width of PERSTB# is one SCLK if H/S# = 0, and determined by the strapping of HCLK1/2X# if H/S# = 1. The following table shows the conditions for PERSTB#.

Conditions for PERSTB#	PERSTB# Pulse Width
(H/S# = 1) * (HBRDY# = 0) * (HOE# = 0) * (IF(1:0) < > 11) * (HINTPAR = 1)	1 HCLK (1x) 2 HCLK (2x)
(H/S# = 1) * (HBRDY# = 0) * (DOE# = 0) * (BT/R# = 0) * (IF(1:0) < > 11) * (HINTPAR# = 1)	1 HCLK (1x) 2 HCLK (2x)
(H/S# = 0) * (SBRDY# = 0) * (SOE# = 0) * (IF(1:0) < > 11) * (SINTPAR = 1)	1 SCLK

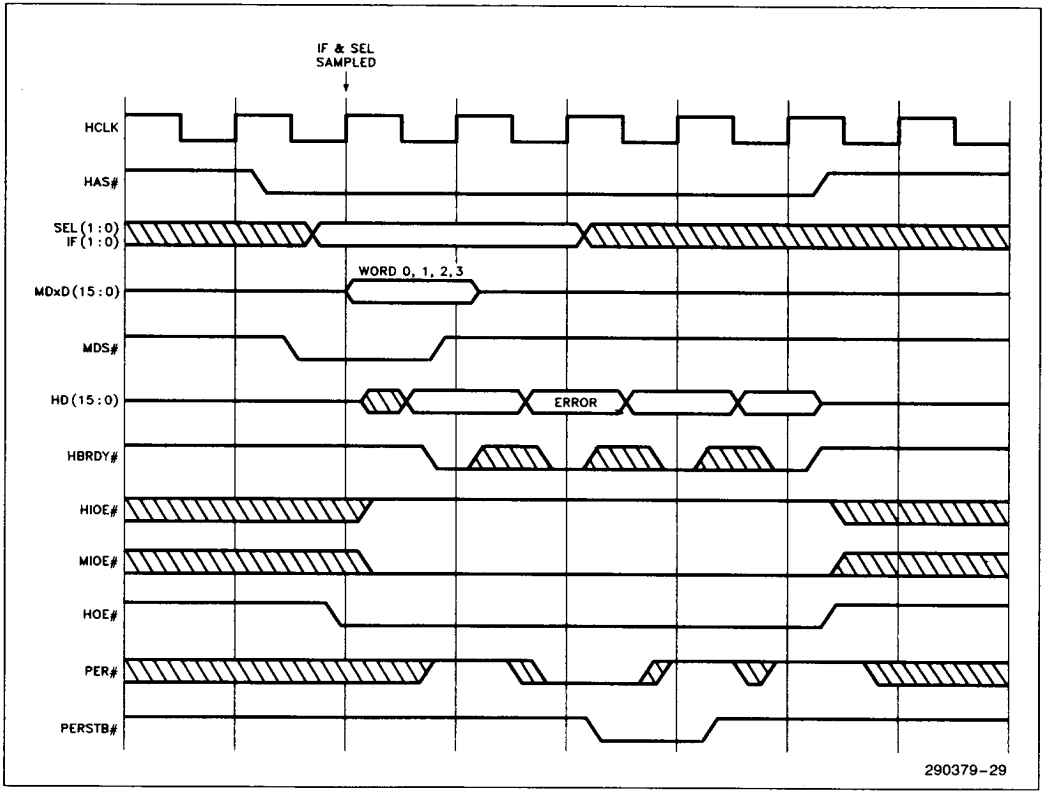


Figure 6.17. Sample Parity Error Occurence (Burst, 4-Way Interleave)

7.0 ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

7.1 D.C. Specifications

7.1.1 ABSOLUTE MAXIMUM RATINGS

Case Temperature Under Bias . . . −65°C to +110°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
with Respect to Ground . . . . . −0.5 to V_{CC} + 0.5

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

7.1.2 D.C. CHARACTERISTICS T_C = 0°C to 85°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	
V_{ILC}	HCLK Input Low	−0.5		0.8	V	(Note 4)
V_{IHC}	HCLK Input High	3.7		V_{CC} + 0.5	V	(Note 4)
V_{OL1}	Output Low Voltage	0.45			V	I_{OL} = 5 mA, (Note 1)
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = −1 mA, (Note 1)
V_{OL2}	Output Low Voltage	0.45			V	I_{OL} = 24 mA, (Note 2)
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = −4 mA, (Note 2)
I_{IL1}	Input Leakage Current			±15	μA	$0 < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current			±15	μA	$0.45 < V_{IN} < V_{CC}$
I_{CC}	Supply Current		110	130	mA	(Note 3)
I_{CC}	Supply Current		125	150	mA	(Note 6)
C_{IN}	Input Capacitance		7	13	pF	F_C = 1 MHz (Note 5)
C_O	I/O or Output Capacitance			15	pF	F_C = 1 MHz (Note 5)

NOTES:
1. V_{OL1} and V_{OH1} apply only to non-system outputs (host data and control, memory data and control).
2. V_{OL2} and V_{OH2} apply only to system port pins that drive the system bus directly.
3. HCLK = 40 MHz, SCLK = 10 MHz. This spec is tested with no external load.
4. Applies to HCLK when 2X clock is used.
5. Not 100% tested.
6. HCLK = 40 MHz, SCLK = 10 MHz. This spec is with external loads. This is not tested.

7.2 A.C. Specifications

The A.C. specifications given in the following tables consist of output delays and input setup requirements. The A.C. diagram's purpose is to illustrate the clock edges from which the timing parameters are measured. The reader should not infer any other timing relationships from them. For specific information on timing relationships between signals, refer to the appropriate functional section. "V" refers to a falling edge. "Λ" refers to a rising edge.

Symbol	Parameter	Min	Max	Notes	Figure #
1X HOST CLOCK					
T1A	HCLK Period (66 MHz max)	15		(Notes 6, 20)	7.2
T2A	HCLK High Time	4		At 2V	7.2
T3A	HCLK Low Time	4		At 0.8V	7.2
T4A	HCLK Fall Time		3	2.0V–0.8V	7.2
T5A	HCLK Rise Time		3	0.8V–2.0V	7.2
1X SYSTEM CLOCK					
T1B	SCLK Period (33 MHz max)	30		(Notes 6, 20)	7.2
T2B	SCLK High Time	10		At 2V	7.2
T3B	SCLK Low Time	10		At 0.8V	7.2
T4B	SCLK Fall Time		4	2.0V–0.8V	7.2
T5B	SCLK Rise Time		4	0.8V–2.0V	7.2
2X HOST CLK					
T1C	HCLK Period (80 MHz max)	12.5		(Note 6)	7.2
T2CA	HCLK High Time	4		At 2V	7.2
T2CB	HCLK High Time	2		At 3.7V	7.2
T3CA	HCLK Low Time	4		At 2V	7.2
T3CB	HCLK Low Time	2		At 0.8V	7.2
T4C	HCLK Full Time		3	3.7V–0.8V	7.2
T5C	HCLK Rise Time		3	0.8V–3.7V	7.2
GENERAL SPECIFICATIONS					
T6	HRST Setup to HCLK (2X)	4		(Note 4)	7.3
T7	HRST Hold from HCLK (2X)	2		(Note 4)	7.3
T8	HRST Min. Pulse Width	50			7.3
T9	Config. Input Setup to HRSTV	15		(Note 5)	7.3
T10	Config. Input Hold from HRSTV	15		(Note 5)	7.3
T11	HDXX Setup to HLDSTBΛ	5			7.4
T12	HDXX Hold from HLDSTBΛ	3			7.4
T13	HLDSTBΛ to MDXX DLY		19	(Note 22)	7.4
T14	HLDSTBΛ to SDXX DLY		35	Both Swap & Non-Swap, (Note 22)	7.4
T15	HLDSTB Min. Pulse Width	6			7.5
T16	HWCLKEN# Setup to HCLK	8		(Note 24)	7.4
T17	HWCKLEN# Hold from HCLK	2		(Note 24)	7.4
T18	HCLK to MDXX DLY		18	Posted Host Write, (Note 22)	7.4
T19	HCLK to SDXX DLY		35	Both Swap & Non-Swap (Note 22)	7.4

7.2 A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Notes	Figure #
GENERAL SPECIFICATIONS (Continued)					
T21	HDXX Setup to HWLE#^	5			7.4
T22	HDXX Hold from HWLE#^	3			7.4
T23	HDXX to MDXX DLY		18	(Note 22)	7.4, 7.7
T24	HDXX to SDXX DLY		35	Both Swap & Non-Swap (Note 22)	7.4, 7.6, 7.7
T25	HWLE#v to MDXX DLY		21	(Note 25)	7.4
T26	HWLE#v to SDXX DLY		35	Both Swap & Non-Swap, (Note 22)	7.4
T27	HWLE# Min. Pulse Width	6			7.4
T30	HRD# to MDXX DLY		35	(Note 22)	7.6
T31	HRD# to SDXX DLY		35	Both Swap & Non-Swap, (Note 22)	7.6
T35	SDXX Setup to SDIDLEx#^	4		Both Swap & Non-Swap, (Note 17)	7.16
T36	SDXX Hold from SDIDLEX#^	3		Both Swap & Non-Swap, (Note 17)	7.16
T37	SDXX to MDXX DLY	7	23	Both Swap & Non-Swap, (Notes 16, 23)	7.7
T38	SDXX to HDXX DLY		30	Both Swap & Non-Swap, (Notes 16, 23)	7.7, 7.16, 7.17
T39	SDIDLEX#v to MDXX DLY		25	(Note 23)	7.7
T40	SDIDLEX#v to HDXX DLY		30	(Note 23)	7.7
T41	SDIDLEX# Min Pulse Width	5			7.7
T42A	HDXX Setup to IDSDLE#^	10		(Note 22)	7.7
T42B	SDXX Setup to IDSDLE#^	7		(Note 17)	7.7
T43A	HDXX Hold from IDSDLE#^	3			7.7
T43B	SDXX Hold from IDSDLE#^	3		(Note 17)	7.7
T45A	IDSDLE#v to SDXX DLY		20	Non-Swap Path	7.7
T45B	IDSDLE#v to SDXX DLY		20	Swap Path	7.7
T46	IDSDLE# Min Pulse Width	5			7.7
T48A	HDXX Setup to HCLK	4		Posted Host Write	7.15
T48B	SDXX Setup to SCLK	8		Burst System Write, (Note 23)	7.15
T48C	HDXX Setup to HCLK	6		Burst Host Write, (Note 22)	7.15

7.2 A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Notes	Figure #
GENERAL SPECIFICATIONS (Continued)					
T49A	HDXX Hold from HCLK	2		Burst/Posted Host Write	7.15
T49B	SDXX Hold from SCLK	2		Burst System Write	7.15
T50A	HCLK to MDXX DLY		17	Burst Host Write	7.15
T50B	SCLK to MDXX DLY		25	Burst System Write	7.15
T51A	IF(1:0),SEL(1:0) Setup to HCLK	7		(Note 3)	7.14, 7.15, 7.17
T51B	IF(1:0),SEL(1:0) Setup to SCLK	7		(Note 3)	7.14, 7.15, 7.17
T51C	SEL(1:0) Setup to MDS#	10			7.14
T52A	IF(1:0),SEL(1:0) Hold from HCLK	10		(Note 3)	7.14, 7.15, 7.17
T52B	IF(1:0),SEL(1:0) Hold from SCLK	10		(Note 3)	7.14, 7.15, 7.17
T53A	HBRDY# Setup to HCLK	4		(Note 1)	7.14, 7.15
T53B	SBRDY# Setup to SCLK	7		(Note 1)	7.14, 7.15
T54A	HBRDY# Hold from HCLK	3		(Note 1)	7.14, 7.15
T54B	SBRDY# Hold from SCLK	3		(Note 1)	7.14, 7.15
T57	MWLS#, H/S# to MDXX DLY		25		7.15
T58A	HAS# Setup to HCLK	5		(Notes 7, 8)	7.4, 7.14, 7.15, 7.17
T58B	SAS# Setup to SCLK	7		(Notes 7, 8)	7.4, 7.14, 7.15, 7.17
T59A	HAS# Hold from HCLK	2		(Notes 7, 8)	7.4, 7.14, 7.15
T59B	SAS# Hold from SCLK	2		(Notes 7, 8)	7.4, 7.14, 7.15
T60A	HAS# Min Pulse Width	10		(Notes 7, 8)	7.4
T60B	SAS# Min Pulse Width	20		(Notes 7, 8)	7.4
T61	HCLK/SCLK to HCLK/SCLK don't care	4		(Note 25)	7.4
T62	MDS# Active Min Pulse Width	10			7.14
T63	MDS# Inactive Min Pulse Width	10			7.14
T64	MDXX Setup to MDS#^	3			7.14
T65	MDXX Hold from MDS#^	5			7.14
T66A	MDXX to HDXX DLY		14	(Note 18)	7.14
T66B	MDXX to SDXX DLY		25	Swap & Non-Swap	7.14
T66C	MDXX to SDXX DLY		20	(Notes 18, 30)	7.14
T67A	HCLK to HDXX DLY	3	14	(Note 18)	7.14
T67B	SCLK to SDXX DLY	3	21	(Notes 18, 30)	7.14
T67C	HAS#/SAS#^ to HDXX/SDXX DLY	3	30	(Notes 18, 30)	7.14
T68A	SEL (1:0) to HDXX DLY		20	Lead Off Mux Select	7.14
T68B	SEL (1:0) to SDXX DLY		30	Lead Off Mux Select, Swap & Non-Swap	7.14

7.2 A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Notes	Figure #
GENERAL SPECIFICATIONS (Continued)					
T69A	MDXX Setup to HCLK/SCLK	12		(Note 29)	7.14
T69B	MDS# Setup to HCLK/SCLK	0		(Note 29)	7.14
T70	SDXX Setup to SDVLD↑	10		(Notes 9, 17); Swap & Non-Swap	7.16, 7.17
T71	SDXX Hold from SDVLD↑	10		(Notes 9, 17); Swap & Non-Swap	7.16, 7.17
T72	SDVLD Min Low Time	10		(Note 9)	7.16
T73	SDVLD Min High Time	10		(Note 9)	7.16
T74	HAS#↑ to HDXX DLY	3	35	(Notes 9, 23)	7.16
T75	SDIDLEX# Inactive Hold from SDVLD↑ for Data Maintenance	10		(Notes 9, 10)	7.16
T76	HCLK to HDXX DLY	3	35	(Note 23)	7.17
T77	HCLK to HARDY↓ DLY		30		7.17
T78	SDVLD↑ to HARDY↑ DLY		30		7.17
T79	HAS#↑ to HARDY↑ DLY		25	(Note 26)	7.17
T80	HOE#↓ to HDXX Valid		22	Non-82385 Mode	7.10
T81	HOE#↑ to HDXX HI-Z	3	10	Non-82385 Mode	7.10
T82	DOE#↓ to HDXX Valid		25	82385 Mode	7.10
T83	DOE#↑ to HDXX HI-Z	3	10	82385 Mode	7.10
T84	BT/R#↓ to HDXX Valid		25	82385 Mode	7.10
T85	BT/R#↑ to HDXX HI-Z	3	10	82385 Mode	7.10
T86	WEX#↓ to MDXX Valid		20	(Note 11)	7.11
T87	WEX#↑ to MDXX HI-Z		10	(Note 11)	7.11
T88	WEX#↓ to WEX#↓ Min Skew	10		(Note 11)	7.11
T90	CPYEN#↓ to SDXX Valid		15	(Note 15)	7.13, 7.14
T91	CPYEN#↑ to SDXX HI-Z		15		7.13
T92	CPYUP to SDXX Valid		15	(Note 15)	7.13
T93	CPYUP to SDXX HI-Z		15		7.13
T94	SOE#↓ to SDXX Valid		25		7.12
T95	SOE#↑ to SDXX HI-Z	3	15		7.12
T96A	SOE (1:0)# to SDXX Valid		15	Non-Swap Path	7.12
T96B	SOE (1:0)# to SDXX Valid		20	Swap Path	7.12
T97	SOE (1:0)# to SDXX HI-Z		15		7.12
T98A	SDXX to SDXX DLY		15	Swap Path	7.13
T98B	SDXX to SDXX DLY		20	Non-Swap Path (Note 21)	
T100	HIOE# to MDXX DLY		20	(Note 12)	7.8
T101	HIOE# to SDXX DLY		35	(Note 12), Swap & Non-Swap	7.8
T102	HIOE# to HDXX DLY		30	(Note 12)	7.8
T103	DOE# to MDXX DLY		20	(Note 12)	7.8
T104	DOE# to SDXX DLY		35	(Note 12), Swap & Non-Swap	7.8

7.2 A.C. Specifications (Continued)

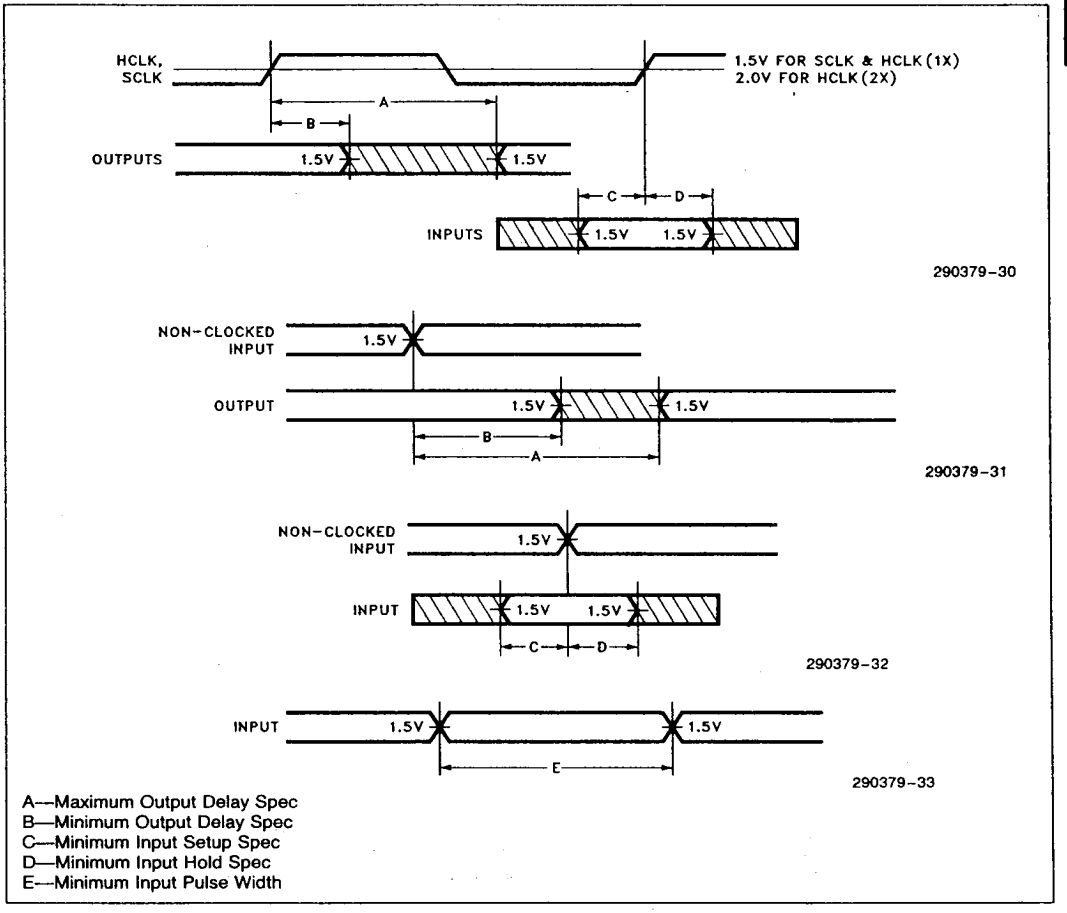
Symbol	Parameter	Min	Max	Notes	Figure #
GENERAL SPECIFICATIONS (Continued)					
T106	BT/R# to MDXX DLY		20	(Note 12)	7.8
T107	BT/R# to SDXX DLY		35	(Note 12), Swap & Non Swap	7.8
T109A	HIOE# Setup to HCLK	6		(Note 13)	7.8
T109B	HIOE# Setup to SCLK	9		(Note 13)	7.8
T110A	HIOE# Hold from HCLK	3		(Note 13)	7.8
T110B	HIOE# Hold from SCLK	3		(Note 13)	7.8
T111	HIOE# Setup to IDSDLE#^	7		(Note 13)	7.8
T112	HIOE# Hold from IDSDLE#^	3		(Note 13)	7.8
T114	MIOE# to HDXX DLY		17	(Note 18)	7.9
T115	MIOE# to SDXX DLY		25	(Notes 14, 18) Swap & Non-Swap	7.9
T116	Valid PER# Lag from Valid HDXX, SDXX during Memory Read		5	(Note 18)	7.18
T117	HOE#, DOE#, BT/R#, SOE# Setup for PERSTB# Generation	7		(Note 19)	7.18
T118	HOE#, DOE#, BT/R#, SOE# Hold for PERSTB# Generation	2		(Note 19)	7.18
T119	PERSTB# DLY	3	30		7.18
T120A	MDXX Setup to HCLK for PERSTB# Generation	17			7.18
T120B	MDXX Setup to SCLK for PERSTB# Generation	25			7.18
T121	HAS#,SAS#,H/S# Setup to First MDS#^	10		(Note 28)	7.14
T122	HAS#,SAS#,H/S# Hold from Last MDS#^	5		(Note 28)	7.14
T123A	MDS#v to HDXX DLY		20	(Notes 28, 18)	7.14
T123B	MDS#v to SDXX DLY		30	(Notes 28, 18)	7.14
T125A	CMOS Input Rise Time		8	0.8–3.0V	
T125B	CMOS Input Fall Time		8	3.0–0.8V	
T126A	TTL Input Rise Time		5	0.8–2.0V	
T126B	TTL Input Fall Time		5	2.0–0.8V	

NOTES:
All units are NS
A.C. TEST LOADS
C_L = 70 pF on HD(15:0).
C_L = 240 pF on SD(15:0).
C_L = 50 pF on all other outputs (except PER# = 25 pF).

1. HBRDY#/SBRDY# synchronous at all rising HCLK(1X)/SCLK edges (or Phase 1 HCLK(2X) edges).
2. Note 2 has been deleted.
3. For Burst Writes, IF(1:0) and SEL(1:0) setup and hold are referenced to clock edge that samples first HBRDY#/SBRDY#. For burst reads of memory, hold is referenced to this edge but setup is referenced to clock edge one period prior to first HBRDY#/SBRDY#.
4. HRST is synchronous to HCLK only when 2X clock is selected and then only for internal phase generation.

NOTES: (Continued)
5. Configuration input sampling assumes HRST is asynchronous and does not assume an active HCLK input to function properly.
6. As long as clock minimum period, high, and low times are met, and all setups/holds referenced to clock edges are met, there are no maximum period or duty cycle restrictions.
7. HAS#/SAS# signals act as asynchronous resets that maintain burst state machines in reset condition as long as they are high. This effectively renders clock a don't care during this interval, allowing smooth transition of state machines from one clock source to another. Note however that doing this when a 2X HCLK is selected will necessitate a new HRST pulse to re-establish phase.
8. HAS#/SAS# need only be active and synchronous to HCLK/SCLK edge that samples first HBRDY#/SBRDY#, and then must remain low until end of burst cycle.
9. SDVLD is explicitly intended to coordinate flow of data during a host read of the system. The system must be careful to never allow a low-to-high transition of SDVLD to occur except within this context. This context insures that when SDVLD^ closes the latch, there is always a subsequent host event, (either HAS#^ or HBRDY# qualified by HCLK^) to re-open the latch.
10. T75 must be met to insure that data latched prior to SDVLD by SDIDLEx# is sustained in the latch until HAS#^ (or HBRDY# qualified by HCLK).
11. In Non-burst writes (MWLS# = 1), only one of the four WEx# signals should be asserted per cycle. In burst writes (MWLS# = 0) however, multiple WEx#'s are allowed to go active in the same cycle. In this case, the system must skew the active transitions of each WE# by T88 to prevent excessive noise. Also, the system timing design should be careful not to allow one 16-bit MDXX word to be turning on simultaneously with the output switching of another already enabled word. Once again, the minimum event skew should be T88. (Note that the burst write latches are such that at any one clock edge, at most only one word is updated.)
12. "A" represents internal system data and "B" internal host data.
13. Although HIOE# is asynchronous, it must be appropriately low or high with enough setup and hold to any event that latches internal write data; specifically IDSDLE#^ during posted system writes, HCLK during host-to-memory burst writes, and SCLK during system-to-memory burst writes. (Of course T109/110 need not be met at all clock edges, but just those that actually latch burst data.)
14. Asserting MIOE# drives internal memory read data to SDXX only if HIOE# = 1. If HIOE# = 0 when MIOE# is asserted, then T115 should be measured not from MIOE#v, but from HIOE#^. (Note this is also true for 82385 mode, assuming the 82385-mode equivalent to HIOE# = 0, namely (DOE# = 0) AND (BT/R# = 1).)
15. Note these specs apply to output buffer turn-on time, to the enabling of swap data from one external byte of the system bus to the other, and to the enabling of internal data onto the system bus, whichever is appropriate.
16. Whether or not a swap path is selected depends on CPYEN# and CPYUP, and T37/T38 assume these signals are resolved prior to SDXX. If SDXX resolves first, T37/T38 should be referenced not to SDXX but to the resolution of CPYEN#/CPYUP.
17. CPYEN# and CPYUP must be resolved and stable around any event that latches SDXX.
18. Assumes HDXX load of 70 pF, SDXX load of 120 pF, and PER# load of 25 pF. Also assumes H/S# resolved prior to HDXX/SDXX.
19. Asynchronous signals.. specs need only be met at HBRDY#/SBRDY# clock edges, and then only when 82353 PERSTB# is used. If for example, HINTPAR = 1 and SINTPAR = 0, then PERSTB# is only generated for host memory reads, and only host signals need obey T117/T118.
20. During burst reads, data muxed from a clock edge internally propagates through the parity detection logic such that on the next edge, a valid PERSTB# pulse can be generated if required. (2 phases if 2X HCLK used.)
21. Applies to the path from an input byte back to the same byte as an output, and is useful only in the case when system data driven into the part is being driven back out on the same pins. To prevent "true" contention, the system must be careful not to enable the output buffer via SOE(1:0)# until T98B nanoseconds after input data on SDXX is guaranteed valid. This spec is guaranteed by design.
22. If parity bits (HPD(1:0)) are supported on the host bus (HINTPAR = 0), then the timing of these bits is in all ways identical to data timing. If HINTPAR = 1, then all Note 22 specs are impacted since time must be allowed for internal parity bit generation. Specifically, if host-originated data is bound for memory, then internally generated parity bits output on MPD(7:0) will lag MDXX by 5 ns. Similarly, SPD (1:0) will lag SD(15:0) by 5 ns. Additionally, if host-originated data is latched internally, then latch setup times must be increased by 5 ns.
23. If parity bits (SPD (1:0)) are supported on the system bus (SINTPAR = 0), then timing of these bits is in all ways identical to data timing. If SINTPAR = 1, or if IBS# = 0 (SPD(1:0) Non-existent), then Note 23 specs are impacted to allow time for internal parity generation. Specifically, if system-originated data is bound for memory, then internally generated parity bits output on MPD(7:0) will lag MDXX by 5 ns. Additionally, if system-originated data is latched internally, then Note 23 latch setup times must be increased by 5 ns.
24. Posting host writes via the clocked posted write latch (HWCLKEN# controlled) is mutually exclusive with burst host writes. I.E., if burst host writes are implemented, the input latch should be configured as transparent (HWLE# controlled).
25. Typically, if HCLK/SCLK is to be switched from one source to another, the soonest the clock of the current cycle would be removed is from the same edge that the bus controller negates HAS#/SAS#. However if either the Host (HINTPAR = 1) or System (SINTPAR = 1) Port is using PERSTB#, then the clock of the current cycle must not be removed until one clock edge after the edge that negates HAS#/SAS#. (Two clock edges for 2x host clock.) This insures a clock edge is available to de-assert PERSTB# in event it had been asserted on the edge HAS#/SAS# had been negated.
26. This is only for the case when at the clock edge, HBRDY# is sampled active indicating that HARDY should be negated. However, subsequent HAS# negation over-rides and brings HARDY back high.

NOTES: (Continued)
27. Note 27 has been deleted.
28. During HAS#/SAS# initiated read cycles to memory, a sequence of from 1 to 4 MDS# rising edges cause the internal burst read latches to sequentially close. These latches then re-open with a rising edge of HAS#/SAS#. (H/S# selects whether the host or system latches are used.) During non HAS#/SAS# initiated cycles to memory, the read latch acts as a simple transparent latch controlled by MDS#. i.e., MDS# low allows data to flow through transparently, and a low-to-high transition of MDS# latches read data and sustains it until MDS# goes low again. T121 and T122 insure that the correct latch scheme is selected.
If HAS# is active and H/S# = 1, then data latched on MDS# edges is sustained until HAS# is de-asserted. If SAS# is active and H/S# = 0, then data latched on MDS# edges is sustained until SAS# is de-asserted. If neither HAS# or SAS# is active, data latched on MDS# rising is sustained until MDS# falling.
29. This applies to the HCLK/SCLK edge that samples the first HBRDY#/SBRDY# active for a burst read cycle.
30. This spec is applicable to buffered mode where the C_L for SDXX is 120 pF.



A—Maximum Output Delay Spec
B—Minimum Output Delay Spec
C—Minimum Input Setup Spec
D—Minimum Input Hold Spec
E—Minimum Input Pulse Width

Figure 7.1. Drive Levels and Measurement Points for A.C. Specifications

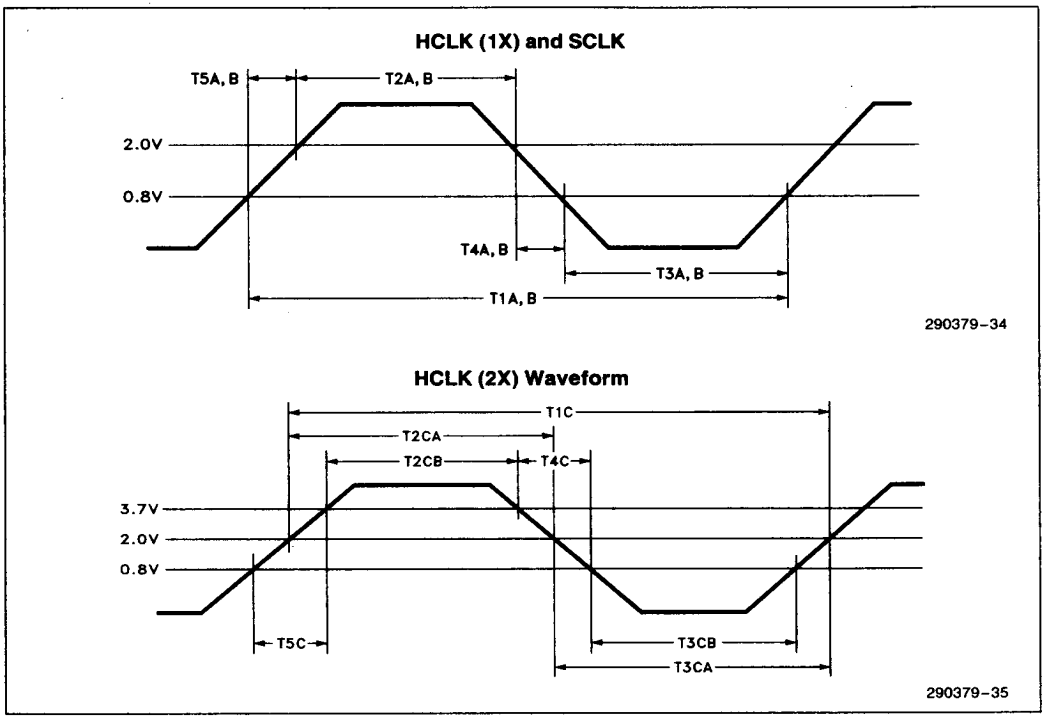


Figure 7.2. HCLK and SCLK Waveforms

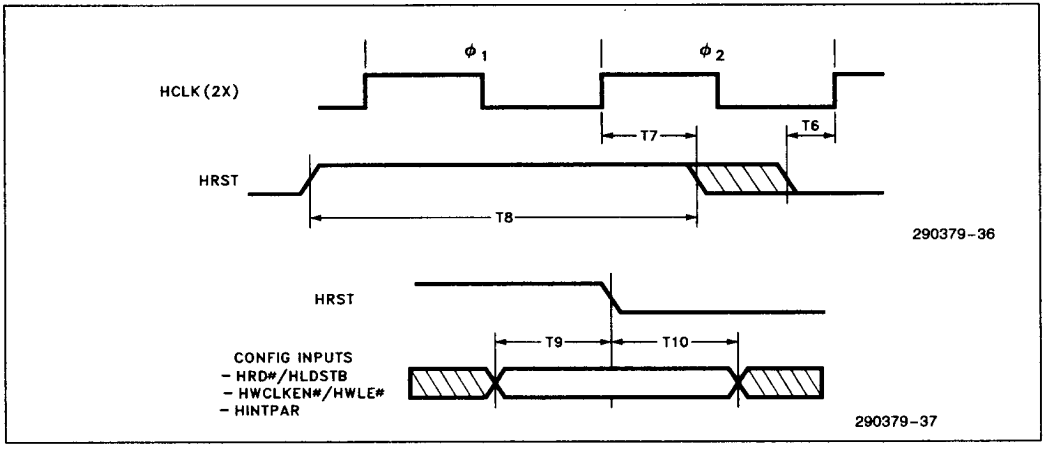


Figure 7.3. Reset Waveforms

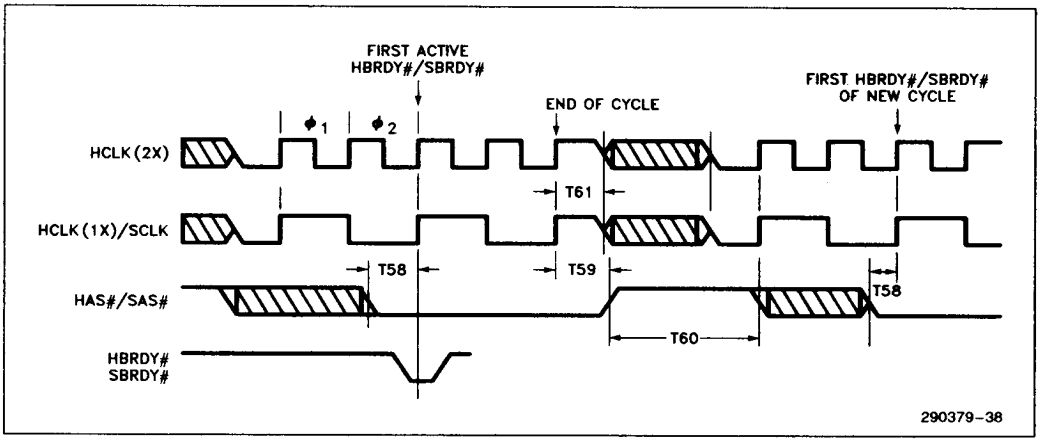


Figure 7.4. HCLK/SCLK Relationship to HAS#/SAS#

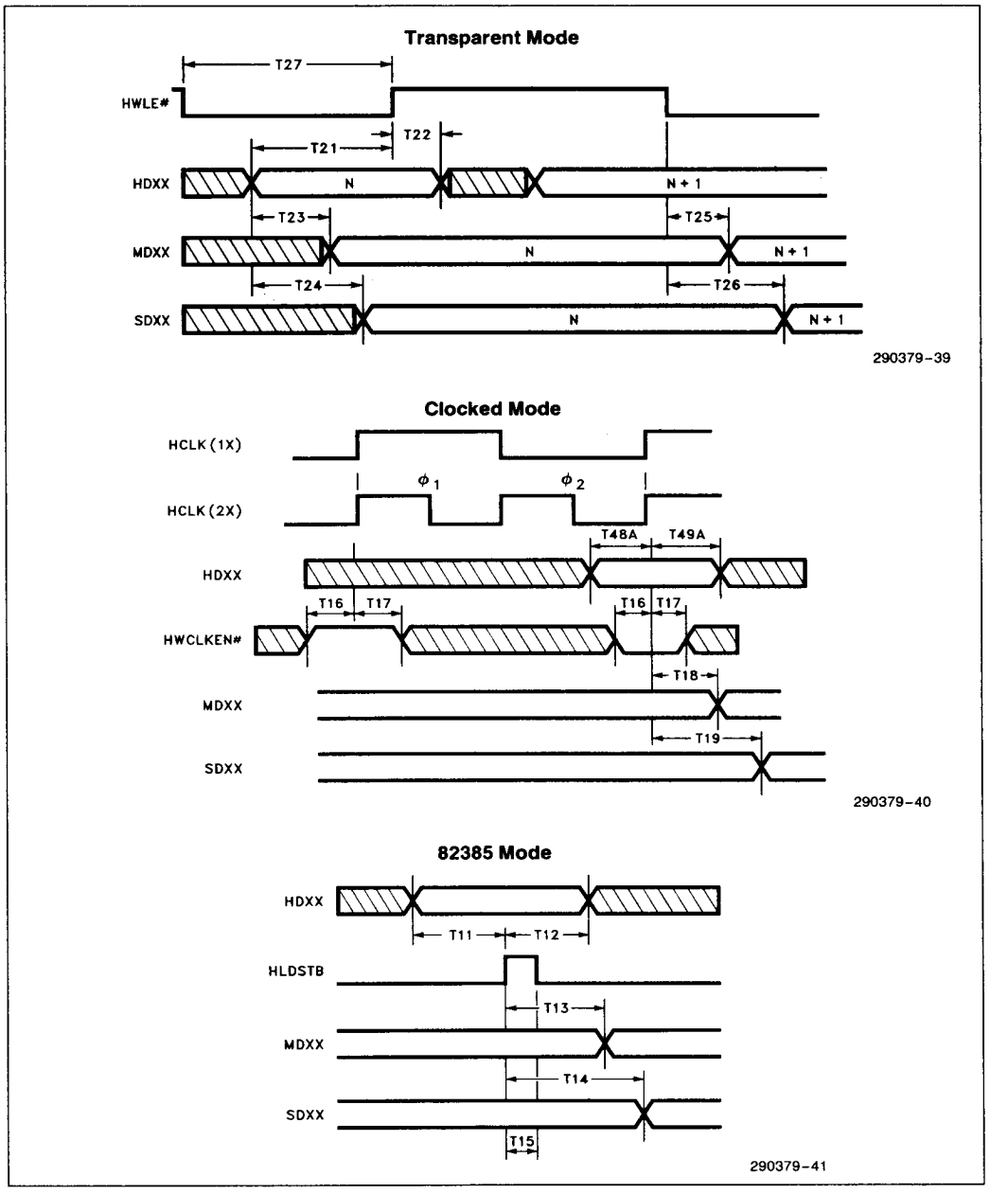


Figure 7.5. Host Latch Control

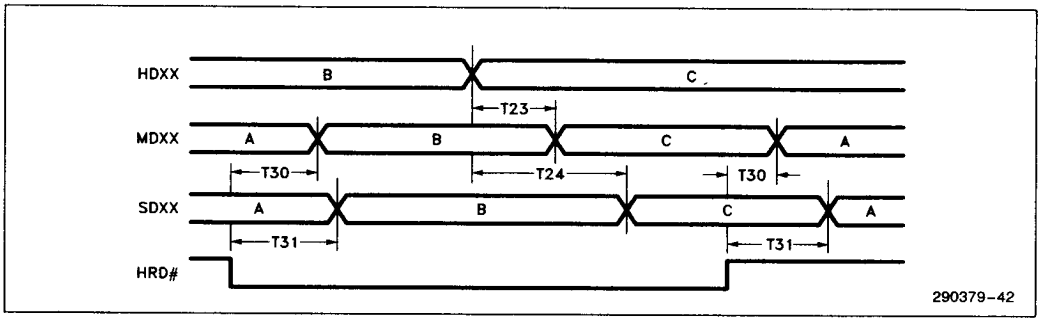


Figure 7.6. Host Read Control

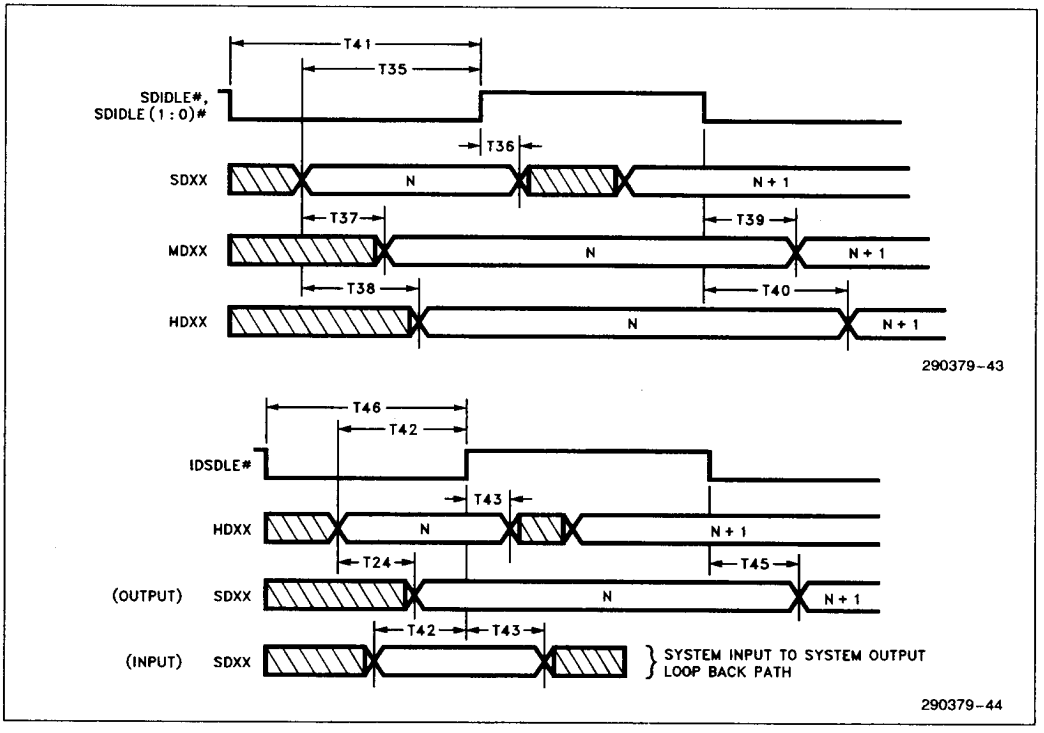


Figure 7.7. System Latch Control

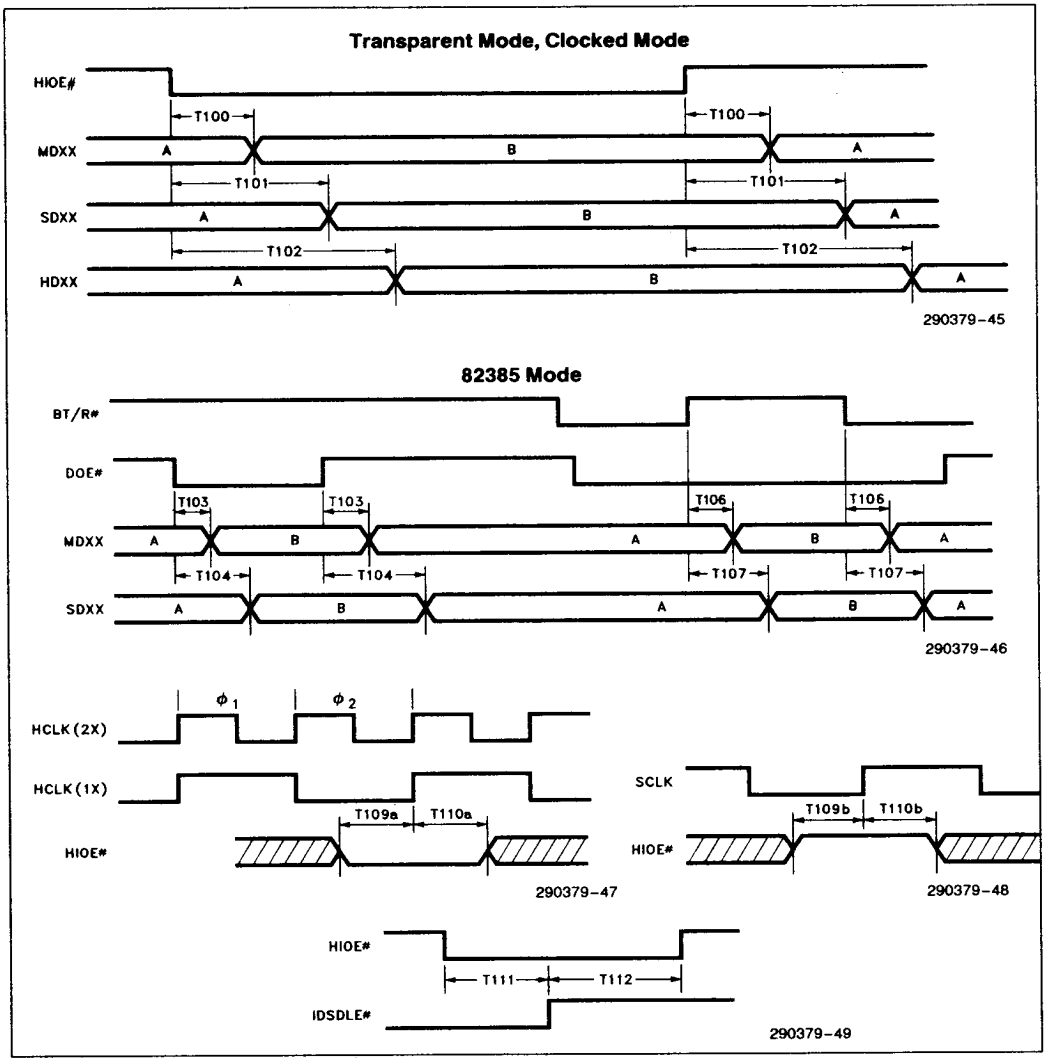


Figure 7.8. Host Internal Enable Control

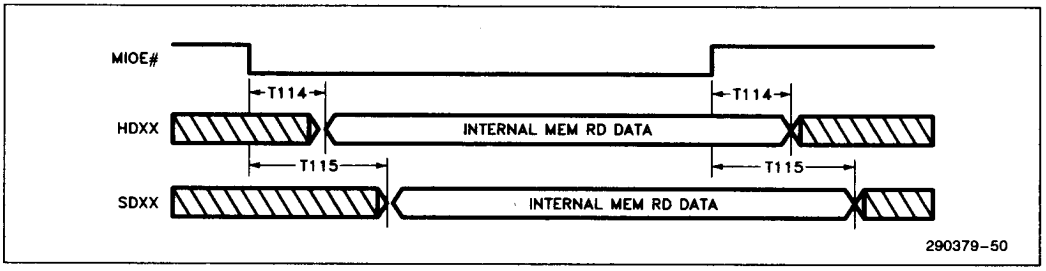


Figure 7.9. Memory Read Internal Enable Control

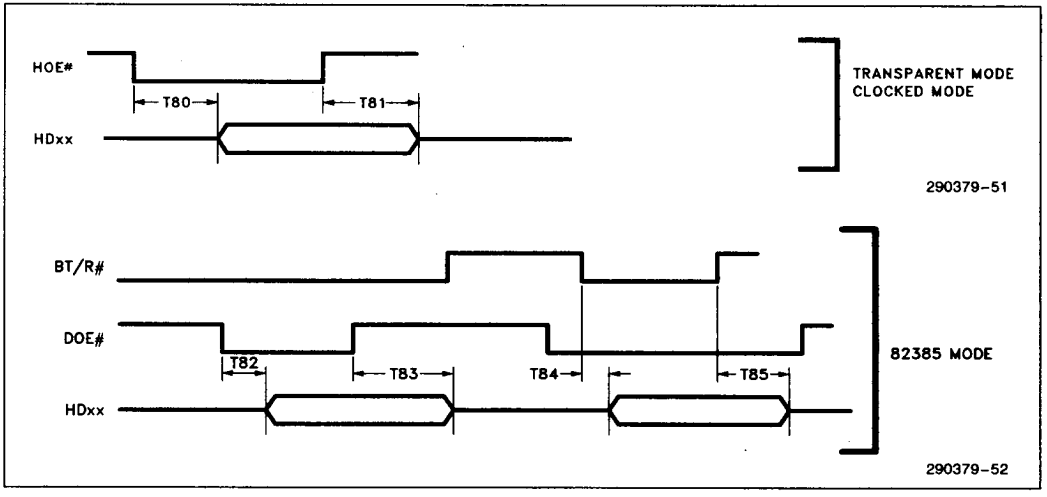


Figure 7.10. Host Output Enable Control

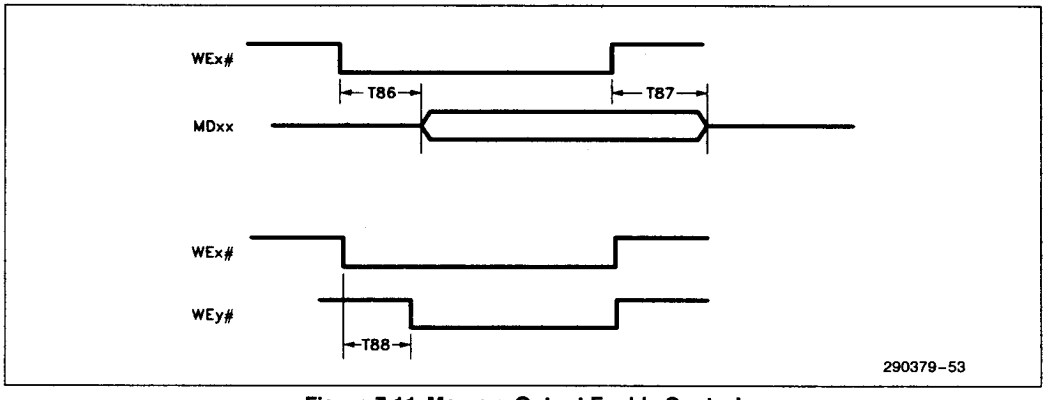


Figure 7.11. Memory Output Enable Control

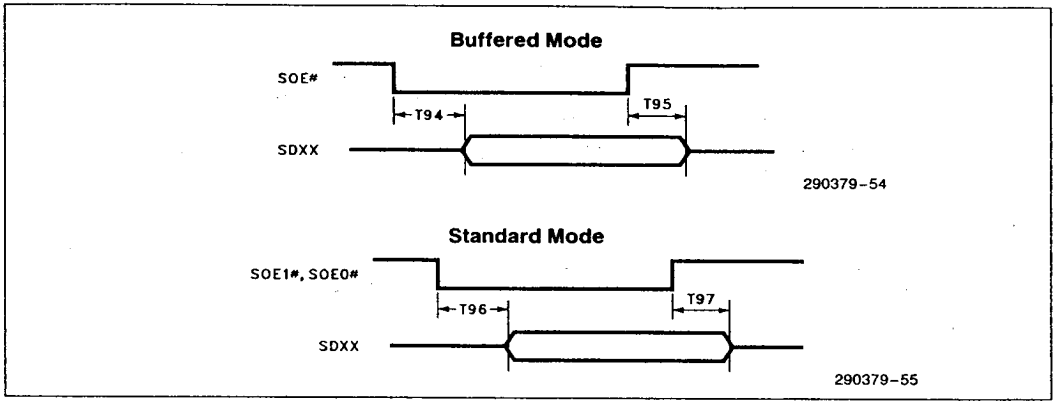


Figure 7.12. Swap Buffer Control

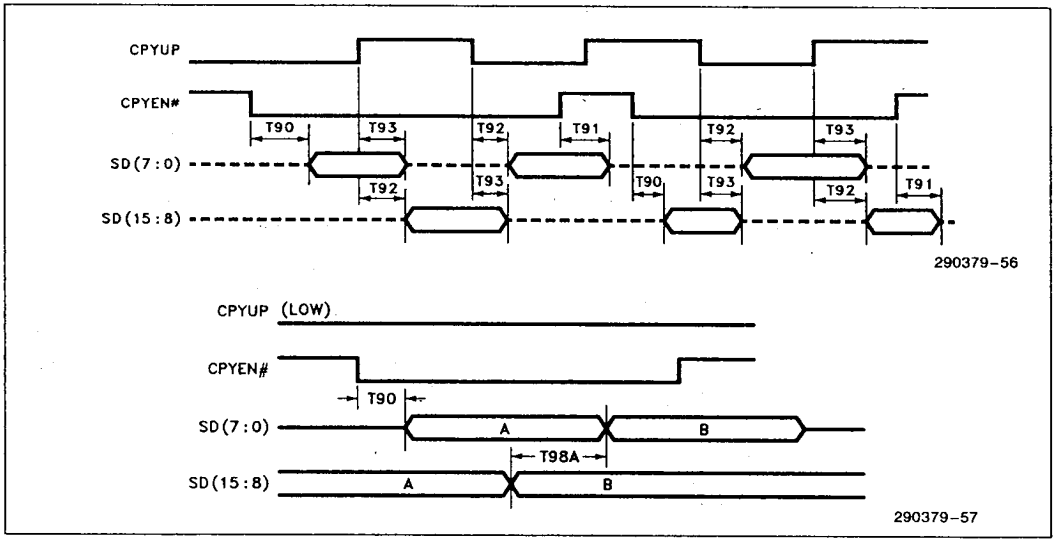


Figure 7.13. System Output Enable Control

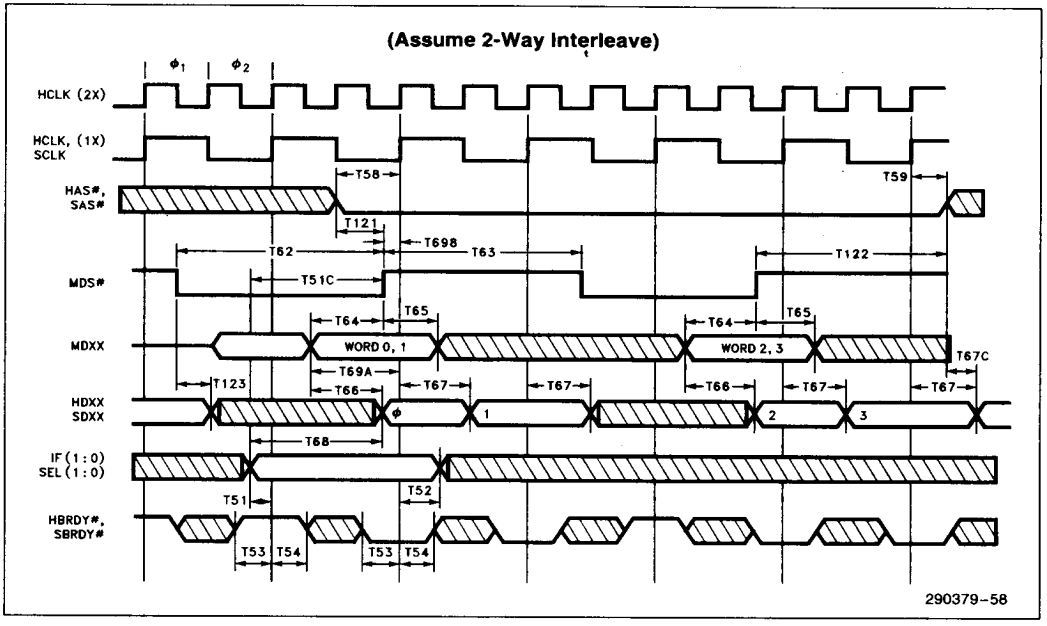


Figure 7.14. Memory Burst Read

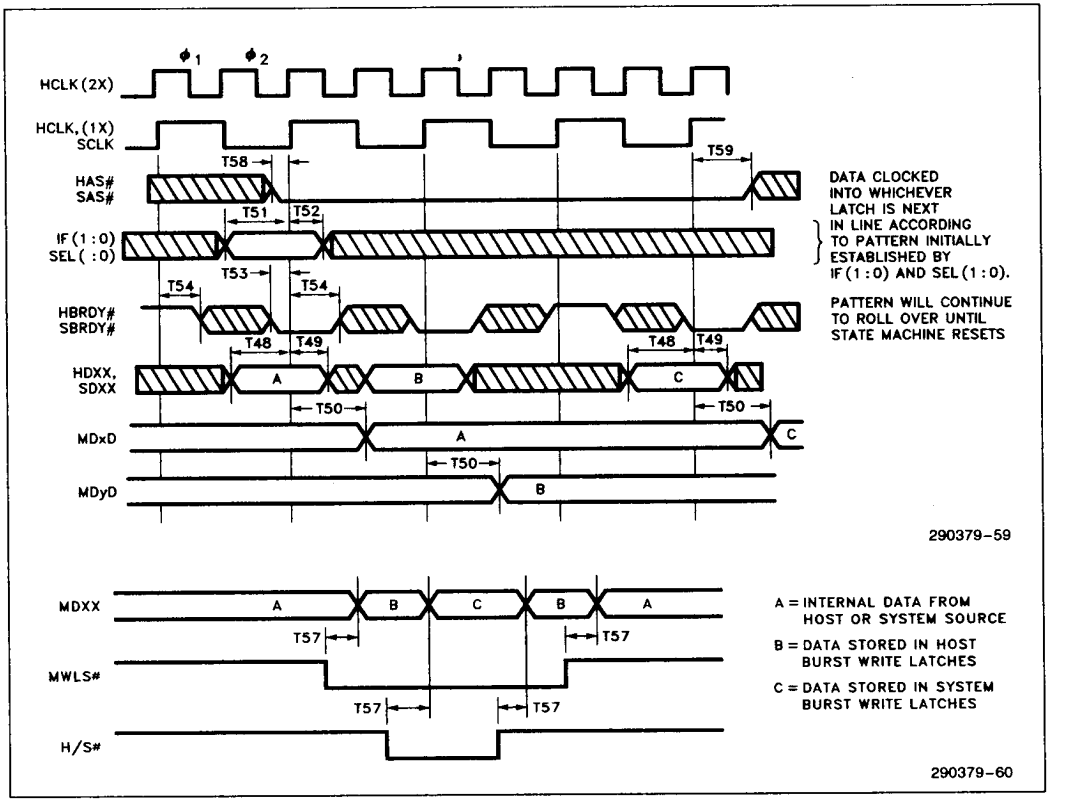


Figure 7.15. Memory Burst Write Latch Control

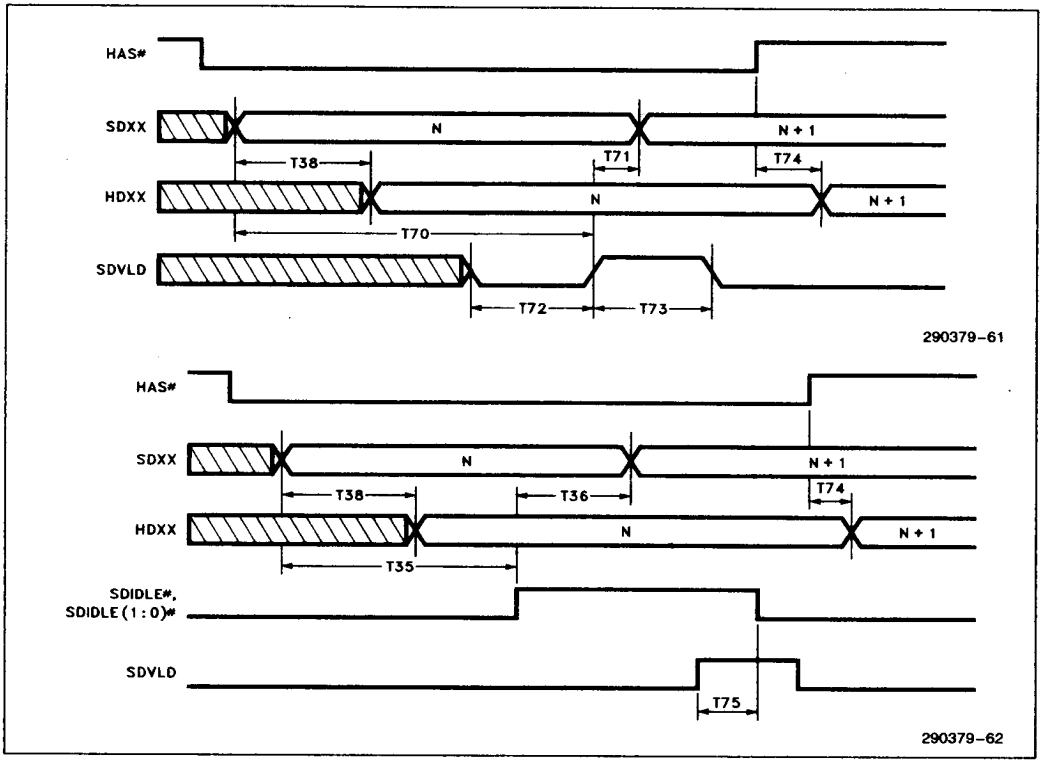


Figure 7.16. Host Single Word Read of System

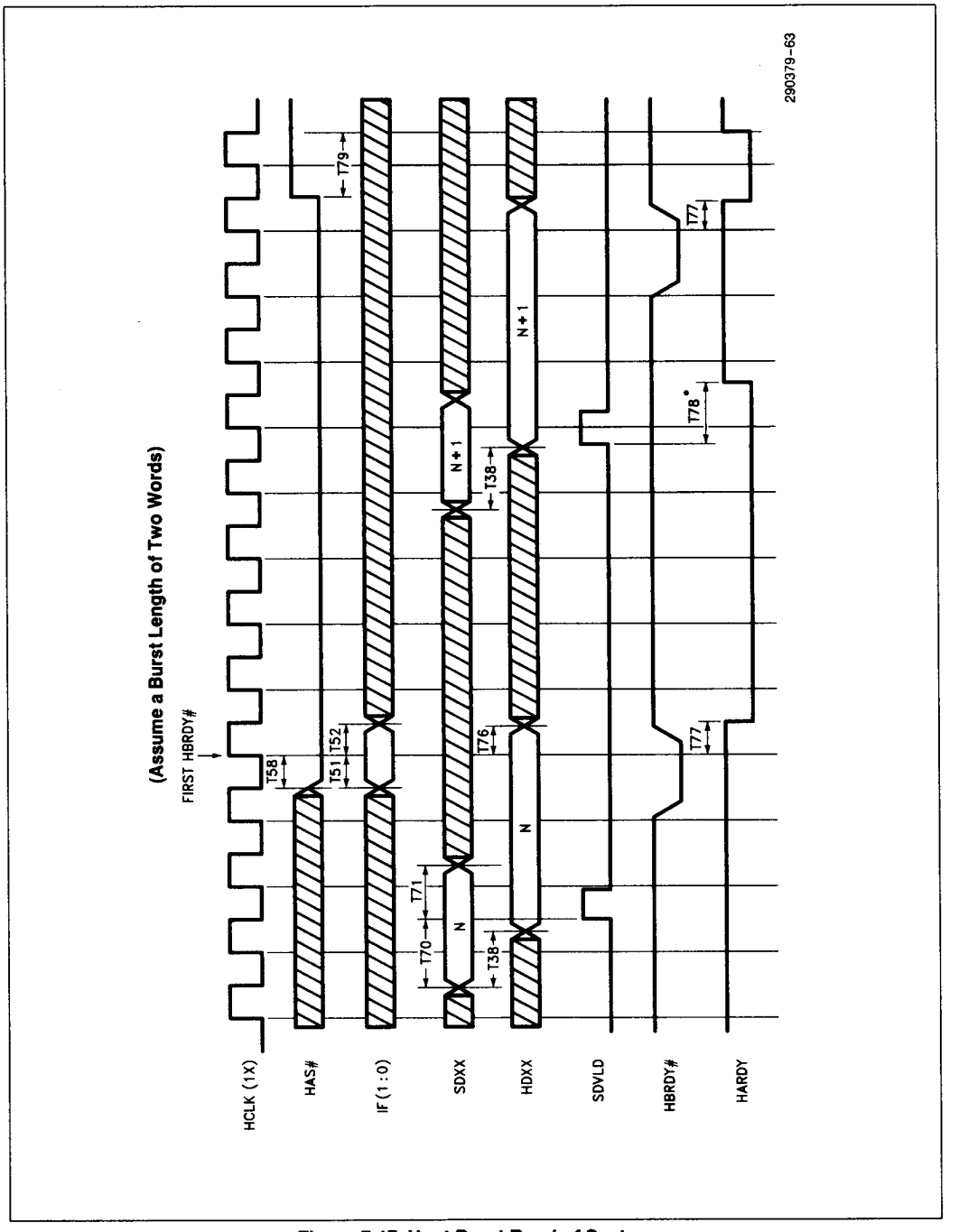


Figure 7.17. Host Burst Read of System

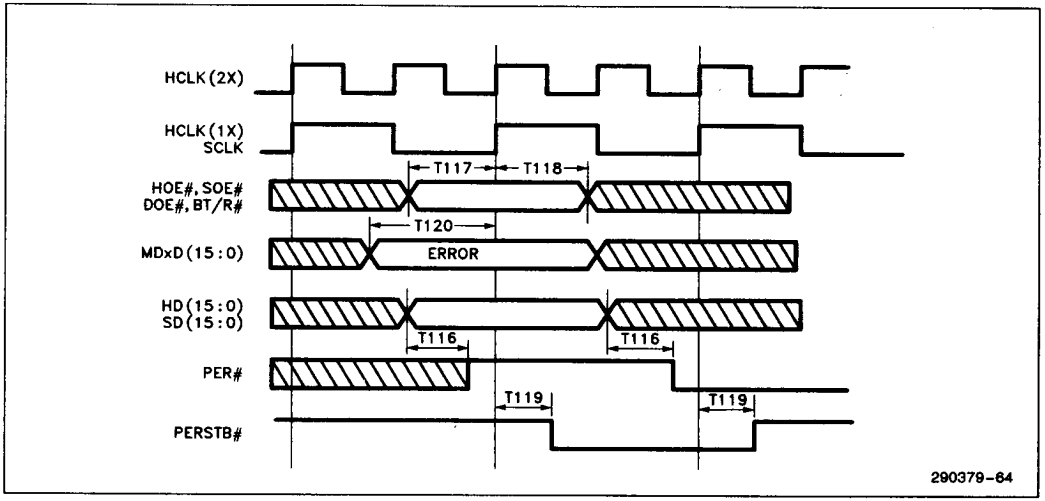


Figure 7.18. Parity Error Timing

7.3 Driver Characterization Data

As systems become more complex, and components operate at higher frequencies, further information on the performance of a component's output drivers becomes helpful or even necessary. This section offers two kinds of data relevent to the A.C. performance of the 82353 drivers:

1. *Capacitive Derating Curves* for quickly adjusting timing delays under simplified loads.
2. *Output V/I Plots* for predicting or modeling an output's performance under more complex loads.

Here, a "simplified load" involves viewing the load driven by an output (traces, inputs, connectors . . .) as a sum of smaller capacitances. This method may often be valid, particularly when the trace driven is short. Longer traces, possibly with numerous stubs, present a more "complex load" to the output driver. Predicting an output's performance under these configurations requires a basic understanding of transmission line phenomena and possibly analog simulation tools.

The 82353 has three different types of outputs, labeled A, B, and C. The following Table associates each 82353 output with its output driver type.

82353 Signals by Output Type

Type	Signal Name
A	HD(15:0), HPD(1:0), SD(15:0), SPD(1:0)
B	MD0D(15:0), MD1D(15:0), MD2D(15:0), MD3D(15:0), MPD(7:0)
C	HARDY, PERSTB#**, PER#

**PERSTB# is an open-drain signal (only drives low), consequently the "Low-to-High Transitions" derate curve and the "Output Driving High" V/I plot do not apply.

To obtain capacitive derating or V/I information for a signal, first find its Type in the above Table and refer to the following sections for the appropriate curves corresponding to that Type.

7.3.1 CAPACITIVE DERATING CURVE

The following information will be useful for adjusting the given A.C. Specifications in the following two cases:

1. The actual capacitive load on a signal trace is *larger* than the specified A.C. test load. In this case, a certain amount of nanoseconds, as derived from the curves, should be *added* to the stated A.C. Specification.

2. The actual capacitive load on a signal trace is *smaller* than the specified A.C. test load. In this case, a certain amount of nanoseconds, as derived from the curves, can be *subtracted* from the stated A.C. Specification.

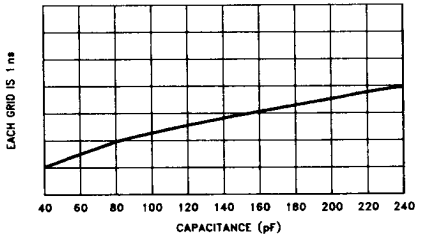
NOTE:
This information is only useful if the actual signal trace is short enough to allow viewing its loading as a lumped capacitor. If the trace is longer, and the loads more distributed, then other methods of analysis must be used to accurately assess the effects of the load.

To assist the user in applying these curves to any specification, the vertical axes show only the change in nanoseconds per gradient. Use the curves to simply determine the amount of nanoseconds to either add to, or subtract from, the given delay.

NOTE:
All derating curves are derived from design and process characteristics, and are not generated by test.

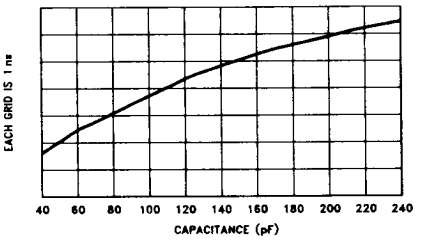
Type A Capacitive Derating Curves

Low-to-High Transitions



290379-66

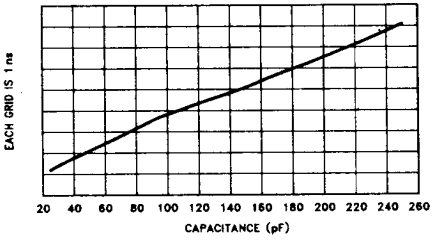
High-to-Low Transitions



290379-67

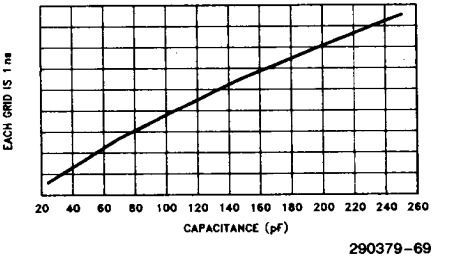
Type B Capacitive Derating Curves

Low-to-High Transitions



290379-68

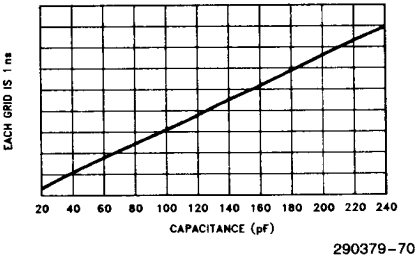
High-to-Low Transitions



290379-69

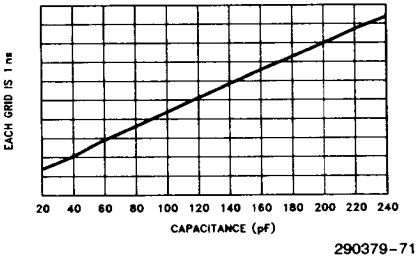
Type C Capacitive Derating Curves

Low-to-High Transitions



290379-70

High-to-Low Transitions



290379-71

7.3.2 OUTPUT V/I PLOTS

Following are V/I plots for each 82353 driver Type (A, B, and C). These plots can be used to obtain:

a) output modeling information

b) a measure of the instantaneous value of the output impedance

c) the magnitude of driven voltage steps through graphical analysis

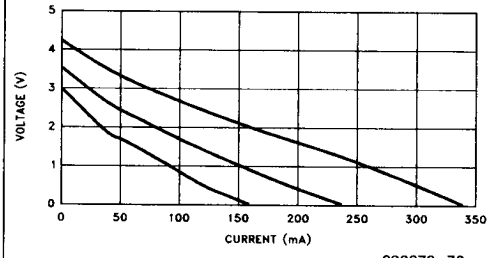
In each set of curves, a range is shown to allow best and worst case analysis over process, temperature (0°C to +85°C), and voltage (5V ±10%)

NOTES:

1. These plots should NOT be used to extract D.C. parameter data.
2. These plots are derived from the process and design characteristics, and are not guaranteed by test.

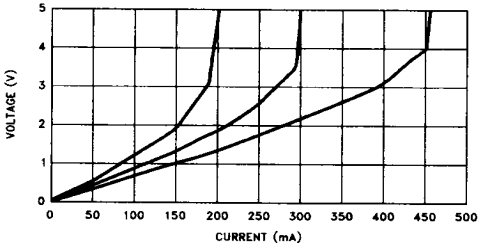
Type A V/I Plots

Output Driving High



290379-72

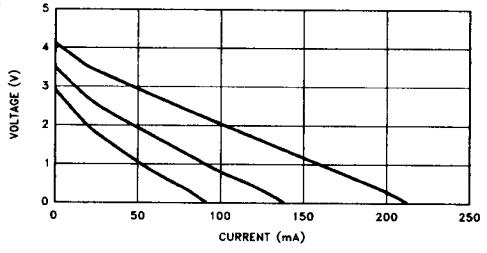
Output Driving Low



290379-73

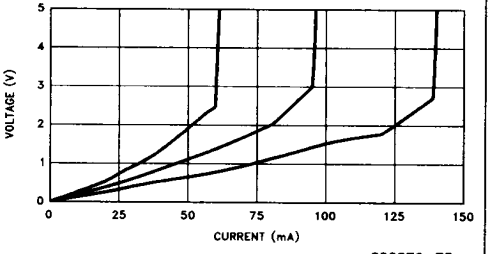
Type B V/I Plots

Output Driving High



290379-74

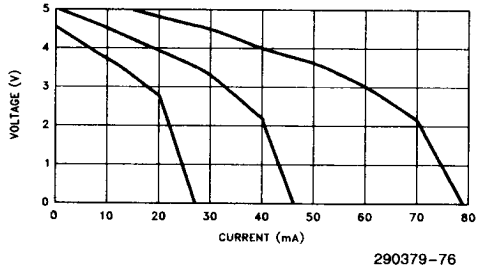
Output Driving Low



290379-75

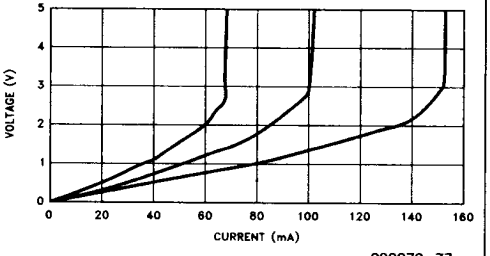
Type C V/I Plots

Output Driving High



290379-76

Output Driving Low



290379-77

8.0 DEVICE PINOUT INFORMATION

8.1 Pin Listing (Numerical Order)

Pin No.	Description
1	MIOE#
2	H/S#
3	PER#
4	Reserved//SAS#
5	IDSDLE#
6	RESIST
7	V_{DD}
8	SIOE#//SOE#
9	CPYUP//SDIDLE#
10	CPYEN#//SBRDY#
11	SOE1#//SCLK
12	SOE0#//SINTPAR
13	SDVLD
14	SDIDLE1#//SPD1
15	SDIDLE0#//SPD0
16	SD15
17	SD7
18	V_{SS}
19	SD14
20	SD6
21	V_{DD}
22	V_{SS}
23	SD13
24	SD5
25	SD12
26	V_{SS}
27	SD4
28	V_{DD}
29	SD11
30	SD3
31	V_{SS}
32	SD10
33	SD2
34	V_{DD}
35	SD9
36	V_{SS}
37	SD1
38	SD8
39	SD0
40	HPD1
41	HPD0

Pin No.	Description
42	HD15
43	HD7
44	V_{SS}
45	V_{DD}
46	HD14
47	HD6
48	HD13
49	HD5
50	HD12
51	HD4
52	HD11
53	HD3
54	HD10
55	HD2
56	V_{SS}
57	V_{DD}
58	HD9
59	HD1
60	HD8
61	HD0
62	V_{SS}
63	HRD#//HLDSTB
64	HRST
65	HWLE#//HWCLKEN#
66	HINTPAR
67	HBRDY#
68	HCLK
69	HCLK1/2X#
70	HOE#//DOE#
71	HIOE#//B/TR#
72	V_{DD}
73	HAS#
74	PERSTB#
75	HARDY
76	MDS#
77	SEL0
78	SEL1
79	IF0
80	IF1
81	V_{SS}
82	MD0D0

Pin No.	Description
83	MD1D0
84	MD2D0
85	MD3D0
86	MD0D8
87	MD1D8
88	MD2D8
89	MD3D8
90	V_{DD}
91	MD0D1
92	MD1D1
93	MD2D1
94	MD3D1
95	MD0D9
96	MD1D9
97	MD2D9
98	MD3D9
99	MD0D2
100	MD1D2
101	MD2D2
102	MD3D2
103	WE0#
104	WE1#
105	MD0D10
106	MD1D10
107	MD2D10
108	MD3D10
109	MD0D3
110	MD1D3
111	MD2D3
112	MD3D3
113	MD0D11
114	MD1D11
115	MD2D11
116	MD3D11
117	V_{SS}
118	MD0D4
119	MD1D4
120	MD2D4
121	MD3D4
122	V_{DD}
123	MD0D12

8.1 Pin Listing (Numerical Order)
(Continued)

Pin No.	Description
124	MD1D12
125	MD2D12
126	MD3D12
127	MD0D5
128	MD1D5
129	MD2D5
130	MD3D5
131	V_{SS}
132	MD0D13
133	MD1D13
134	MD2D13
135	MD3D13
136	MD0D6
137	MD1D6
138	MD2D6
139	MD3D6
140	MD0D14
141	MD1D14
142	MD2D14
143	MD3D14
144	WE2#
145	WE3#
146	MD0D7
147	MD1D7
148	MD2D7
149	MD3D7
150	MD0D15
151	MD1D15
152	MD2D15
153	MD3D15
154	V_{DD}
155	MPD0
156	MPD2
157	MPD4
158	MPD6
159	MPD1
160	MPD3
161	MPD5
162	MPD7
163	V_{SS}
164	MWLS#

8.2 Pin Listing (Alphabetical Order)

Pin No.	Description
10	CPYEN#//SBRDY#
9	CPYUP//SDIDLE#
2	H/S#
75	HARDY
73	HAS#
67	HBRDY#
68	HCLK
69	HCLK1/2X#
61	HD0
59	HD1
54	HD10
52	HD11
50	HD12
48	HD13
46	HD14
42	HD15
55	HD2
53	HD3
51	HD4
49	HD5
47	HD6
43	HD7
60	HD8
58	HD9
66	HINTPAR
71	HIOE#//BT/R#
70	HOE#//DOE#
41	HPD0
40	HPD1
63	HRD#//HLDSTB
64	HRST
65	HWLE#//HWCLKEN#
5	IDSDLE#
79	IF0
80	IF1
82	MD0D0
91	MD0D1
105	MD0D10
113	MD0D11
123	MD0D12
132	MD0D13

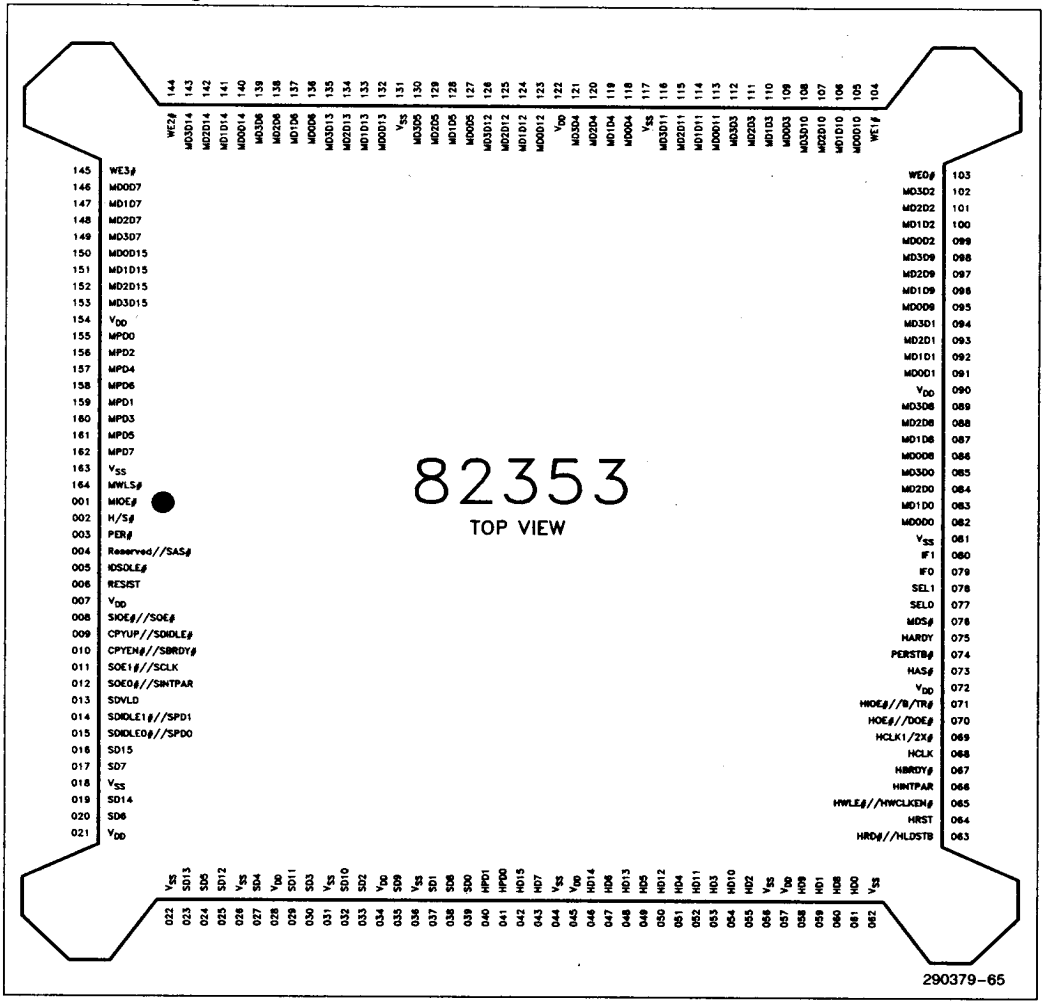
Pin No.	Description
140	MD0D14
150	MD0D15
99	MD0D2
109	MD0D3
118	MD0D4
127	MD0D5
136	MD0D6
146	MD0D7
86	MD0D8
95	MD0D9
83	MD1D0
92	MD1D1
106	MD1D10
114	MD1D11
124	MD1D12
133	MD1D13
141	MD1D14
151	MD1D15
100	MD1D2
110	MD1D3
119	MD1D4
128	MD1D5
137	MD1D6
147	MD1D7
87	MD1D8
96	MD1D9
84	MD2D0
93	MD2D1
107	MD2D10
115	MD2D11
125	MD2D12
134	MD2D13
142	MD2D14
152	MD2D15
101	MD2D2
111	MD2D3
120	MD2D4
129	MD2D5
138	MD2D6
148	MD2D7
88	MD2D8

8.2 Pin Listing (Alphabetical Order) (Continued)

Pin No.	Description
97	MD2D9
85	MD3D0
94	MD3D1
108	MD3D10
116	MD3D11
126	MD3D12
135	MD3D13
143	MD3D14
153	MD3D15
102	MD3D2
112	MD3D3
121	MD3D4
130	MD3D5
139	MD3D6
149	MD3D7
89	MD3D8
98	MD3D9
76	MDS#
1	MIOE#
155	MPD0
159	MPD1
156	MPD2
160	MPD3
157	MPD4
161	MPD5
158	MPD6
162	MPD7
164	MWLS#
3	PER#
74	PERSTB#
4	Reserved//SAS#
6	RESIST
39	SD0
37	SD1
32	SD10
29	SD11
25	SD12
23	SD13
19	SD14
16	SD15
33	SD2

Pin No.	Description
30	SD3
27	SD4
24	SD5
20	SD6
17	SD7
38	SD8
35	SD9
15	SDIDLE0#//SPD0
14	SDIDLE1#//SPD1
13	SDVLD
77	SEL0
78	SEL1
8	SIOE#//SOE#
12	SOE0#//SINTPAR
11	SOE1#//SCLK
7	V_{DD}
57	V_{DD}
21	V_{DD}
72	V_{DD}
154	V_{DD}
28	V_{DD}
45	V_{DD}
122	V_{DD}
90	V_{DD}
34	V_{DD}
26	V_{SS}
56	V_{SS}
22	V_{SS}
163	V_{SS}
18	V_{SS}
31	V_{SS}
117	V_{SS}
62	V_{SS}
81	V_{SS}
44	V_{SS}
131	V_{SS}
36	V_{SS}
103	WE0#
104	WE1#
144	WE2#
145	WE3#

8.3 Pinout Diagram



9.0 THERMAL SPECIFICATIONS

Air Flow Rate	
0 (ft/min)	
θ_{JA} (°C/W)	θ_{JC} (°C/W)
45	20

10.0 REVISION SUMMARY

This data sheet contains updates and improvements between version 001 and 002. A revision summary is listed here for your convenience.

82353 Advanced Data Path

Highlights — Added Footnote.

Section 4.3.2 — Corrected device name in Figure 4.9.

Section 5.1 — Changed reference to the 82359 to 82353 in the second paragraph of the HARDY pin description.

Section 5.1.1 — Added IF(1:0) values to HBRDY description.

Section 5.3 — Added non-burst cycle description to SEL(1:0) description.

Section 6.6 — Corrected HCLK 1X/2X# typos.

Section 6.7 — Corrected signal names in Figure 6.16.

Section 7.2 — t37 minimum specification is 7 ns. t52A and t52B minimum specifications are 10 ns for each. Note 3 has been revised. t65 is 5 ns. Note 29 and Note 30 have been added. PERSTB# was inverted in Figure 7.18. Note 18 has been revised. Added t125A, t125B, t126A, t126B.

82353 Revision Summary

Revisions from versions 002 to 003.

Section 5.1.1 — Added resist pin descriptions: This is used to control current for the output drivers. This should be connected through a 900Ω (±5%) resistor to GND.

Section 5.2.3 — In the pin description of SINTPAR deleted the sentences in the pin description which read: "If SINTPAR is asserted . . . any parity errors." It has been replaced with "if SINTPAR is low, it is the system PST master's responsibility to generate and test system bus data parity and the PERSTB# signal will not respond to system cycle. If SINTPAR is high, parity on the SP(1:0) is ignored, the 82353 will generate and check system bus data parity, and PERSTB# will respond to indicate any system bus parity errors."

Section 7.1.2 — Added C_{IN} typical value of 5 ns. Changed I_{IL1} and I_{LO} to ±15 μA. Changed I_{CC} Supply Current from 125 mA to 130 mA (tested with no external loads), and added I_{CC} Supply Current typical value of 110 mA. Added "tested with no external loads" to Note 3. Added I_{CC} Supply Current typical value of 125 mA, maximum value of 150 mA, and Note 6 "HCLK = 40 MHz, SCLK = 10 MHz. This specification is with external loads. This specification is not tested."

Section 7.2 — In t66C and t67B deleted "120 pF" and "(vs 240 pF)". t67A changed from 12 ns to 14 ns max. t67B changed from 20 ns to 21 ns max.

t109A changed from 5 ns to 6 ns. t120 changed to t120A MDXX Setup to HCLK for PERSTB# Generation (17 ns min). Added t120B MDXX Setup to SCLK for PERSTB# Generation (25 ns min).

Clarified Note 18 to read "Assumes HDXX load of 70 pF, SDXX load of 120 pF, and PER# load of 25 pF. Deleted the sentence "This spec applies . . . that opens memory read latches".

t67C was added to Figure 7.14. t27 was clarified in Figure 7.5. t41 and t46 were clarified in Figure 7.7.

Section 7.3 — Added new Driver Characterization Data section including Capacitive Derating Curves and Output V/I Plots.

Section 9.0 — Added Thermal specifications.