Intel® IXP2400 Network Processor

Datasheet

Product Features

The Intel® IXP2400 Network Processor enables faster deployment of intelligent network services by providing high programming flexibility, code re-use, and high-performance processing. IXP2400 Network Processor supports a wide variety of WAN and LAN applications requiring support for a broad range of speeds, currently ranging from OC-3 to OC-48. High performance and scalability is achieved through an innovative Microengine architecture that includes a multi-threaded distribution cache architecture that enables pipeline features in software. The Microengines feature innovative inter-thread communication capabilities for efficient processing at high line rates, and general-purpose hardware elements that support advanced networking algorithms. The Microengines play a key role in the Intel® Exchange Architecture (IXA) store and forward architecture, providing flexible, rich network processing in converged communications environments.

- Eight integrated Microengine Version 2 Processors
  - Operating frequencies of 400 and 600 MHz
  - Configurable to four or eight threads per Microengine
  - 640 x 32-bit local memory per Microengine
  - Sixteen-entry CAM per Microengine with single cycle lookup
  - Next Neighbor bus: A dedicated datapath between adjacent Microengines
  - CRC unit per Microengine supporting CRC-16 (CCITT) and CRC-32
  - 4K-instruction control store per Microengine
  - Support for Generalized Thread Signaling
  - Reflector access to read or write data between any Microengines
- Integrated Intel XScale core
  - Operating frequencies of 400 and 600 MHz
  - High-performance, low-power, 32-bit embedded RISC processor
  - 32-Kbyte instruction cache
  - 32-Kbyte data cache
  - 2-Kbyte mini data cache
- Two uni-directional 32-bit low-voltage transistor-transistor logic (LVTTL) data interfaces
  - Speeds from 25 to 133 MHz supported
  - Separately configurable for POS-PHY, UTOPIA 1/2/3, or CSIX-L1-B Protocol support
  - Interprocessor “Cbus” communication
- Industry-standard PCI Bus Version 2.2 interface for 64-bit, 66-MHz I/O
- Industry-standard double-data-rate (DDR) SDRAM memory interface
  - Peak bandwidth of 2.4 GB/s
  - Clock speeds of 100, 150 MHz supported when IXP2400 is running at 600 MHz; 100 MHz when IXP2400 is running at 400 MHz
  - Error correction code (ECC)
  - Addressable from the Intel XScale core, MEs, and PCI
- Two industry-standard 32-bit quad-data-rate (QDR) SRAM interfaces
  - Peak bandwidth of 1.6 GB/s per channel
  - 100- or 133-MHz SRAM when IXP2400 is running at 400 MHz; 100-, 150- or 200-MHz SRAM when IXP2400 is running at 600 MHz
  - Hardware support for Linked List and Ring operations
  - Atomic bit operations
  - Atomic arithmetic support
  - Addressable from the Intel XScale core, MEs, and PCI
- Additional integrated features
  - Hardware hash unit (48, 64 and 128 bit)
  - 16-Kbyte scratchpad memory
  - Serial port for debug
  - Eight general-purpose I/O pins
  - Four 32-bit timers
- 1356-Ball FCBGA2 package
  - Dimensions of 37.5 mm x 37.5 mm
  - 1 mm solder ball pitch

Notice: Please verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

February 2004

Document Number: 301164-011

Revision History

Date	Revision	Description
January 2002	001	Release for the Customer Information Book V0.3.
March 2002	002	Initial release of Advance Information for Intel® Field Personnel and customers under NDA.
June 2002	003	Release for the Customer Information Book V0.4.
July 2002	004	Update to best-known Advance information for Intel® Field Personnel and customers under NDA.
September 2002	005	Further updates (primarily to Electrical Specifications) to Advance information for Intel® Field Personnel and customers under NDA.
November 2002	006	Further updates to signal and electrical information; Advance information for Intel® Field Personnel and customers under NDA.
December 2002	007	Further updates, mostly to electrical information; Advance information for Intel® Field Personnel and customers under NDA.
March 2003	008	Updated Electrical Specifications with B stepping information; Advance information for Intel® Field Personnel and customers under NDA.
April 2003	009	Added Media Switch Fabric mode signal-usage tables, ball map; updated Electrical Specifications.
October 2003	010	Minor modifications to Figures 10, 11, and 45.
February 2004	011	Further modifications to Figures 10 and 11; changes to Tables 6, 30, and 53.

Contents

Figures

Tables

1.0 Product Description

The Intel® IXP2400 Network Processor is a second-generation high-performance device. The IXP2400 is a highly integrated, programmable data processor that provides high-performance parallel processing power and flexibility to a wide variety of OC-48 (2.5 Gb/s) networking, communications, and data-intensive applications.

The IXP2400 has a store and forward architecture that combines a state-of-the-art Intel XScale core with eight multithreaded, independent 32-bit RISC data engines that, when combined, can provide a total of 5.4 giga-operations per second.

Figure 1 shows two IXP2400 network processors in a typical 2.5 Gb/s full-duplex line rate application.

Figure 1. IXP2400 Network Processor OC-48 Line Card

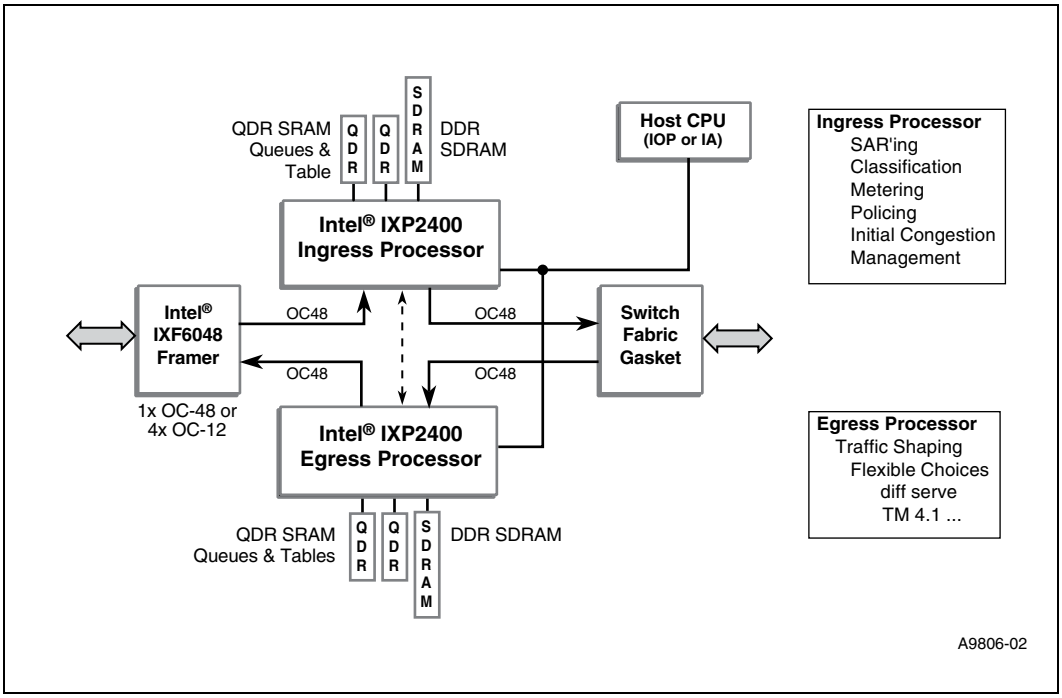


Figure 2 and Figure 3 illustrate the functional signal groups within the IXP2400.

Figure 2. IXP2400 Network Processor Functional Signal Groups Diagram 1

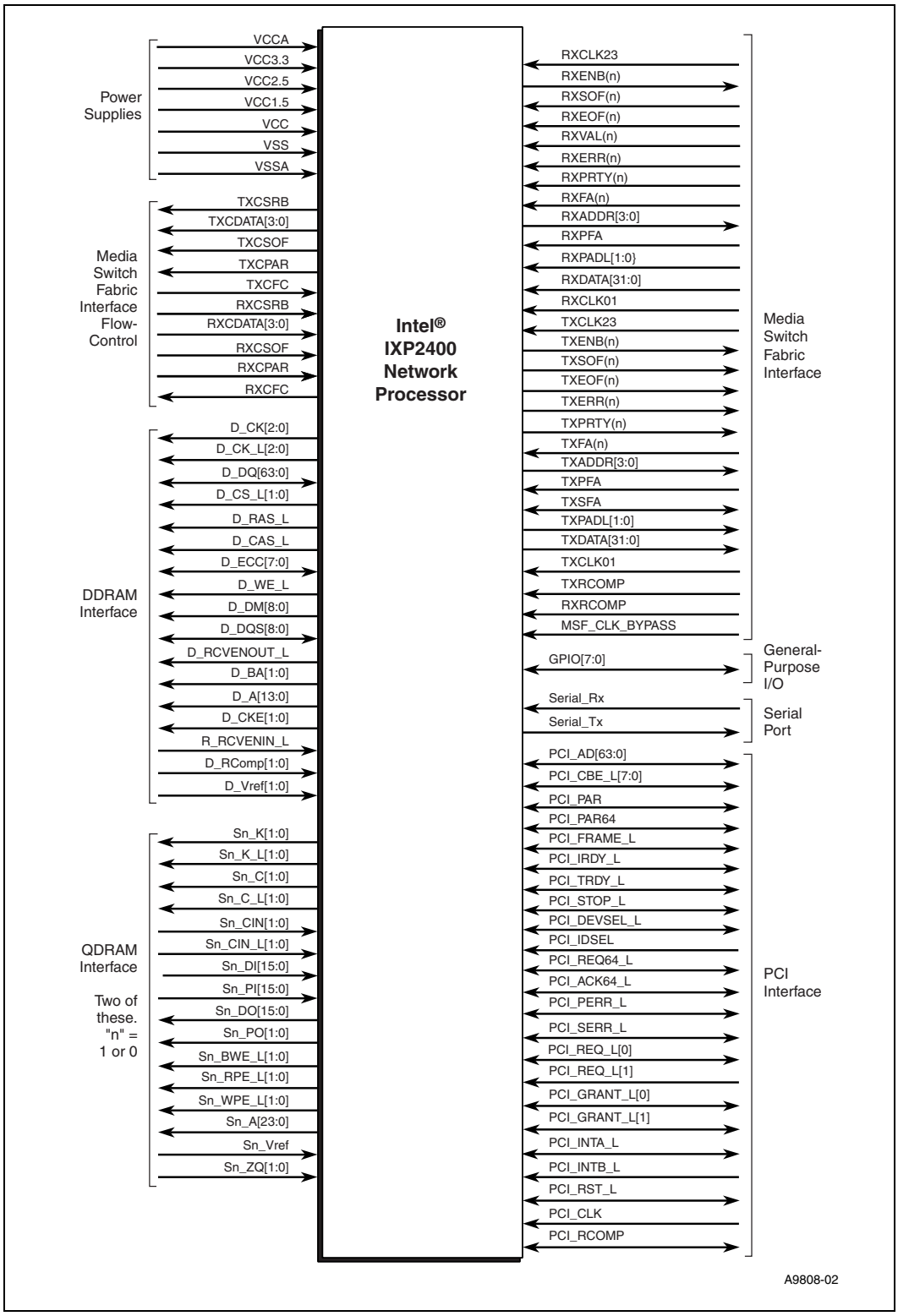
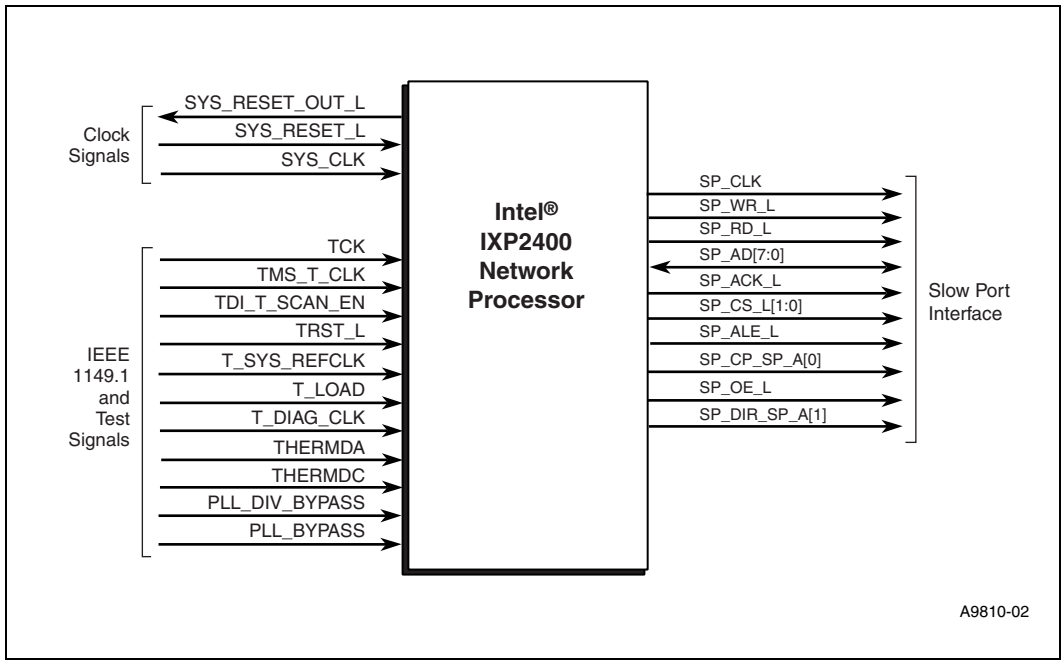


Figure 3. IXP2400 Network Processor Functional Signal Groups Diagram 2

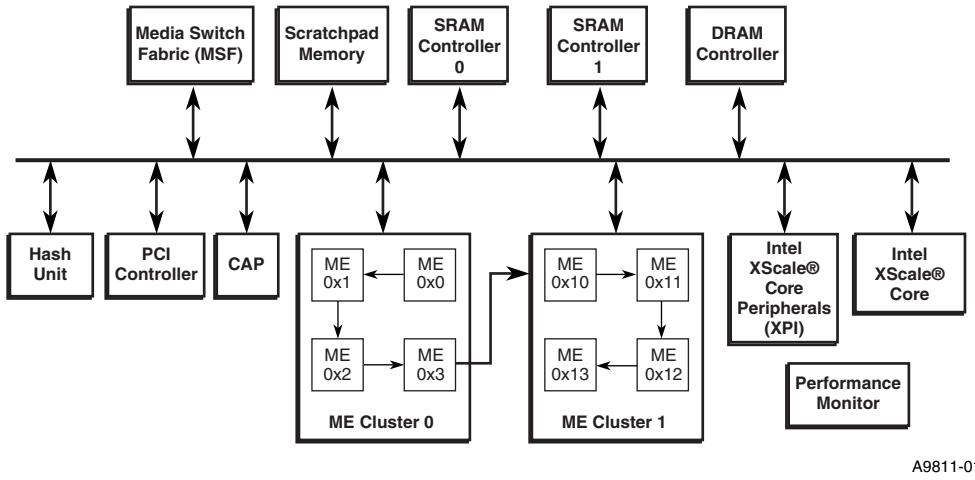


2.0 Functional Units

2.1 Functional Overview

This section provides a brief overview of the IXP2400 Network Processor internal hardware. Figure 4 is a simple block diagram that shows the device's major internal blocks.

Figure 4. IXP2400 Network Processor Chassis Concept Block Diagram



The major blocks are:

- Intel XScale core — General-purpose 32-bit RISC processor compatible to ARM Version 5 Architecture. The Intel XScale core is used to initialize and manage the chip, and can be used for higher layer network processing tasks.
- Microengines (MEs) — 8 32-bit programmable engines specialized for network processing. Microengines do the main data plane processing per packet.
- DRAM Controller — 1 DDR SDRAM controller. Typically DRAM is used for data buffer storage.
- SRAM Controller — 2 independent controllers for QDR SRAM. Typically SRAM is used for control information storage.
- Scratchpad Memory — 16 Kbytes of storage for general-purpose use.
- Media and Switch Fabric Interface (MSF) — Interface for network framers and/or Switch Fabric. Contains receive and transmit buffers.
- Hash Unit — Polynomial hash accelerator. The Intel XScale core and Microengines can use it to offload hash calculations.
- PCI Controller — 64-bit PCI Rev 2.2 compliant IO bus. PCI can be used to either connect to a Host processor, or to attach PCI-compliant peripheral devices.

- CAP — Chip-wide Control and status registers. These provide special inter-processor communication features to allow flexible and efficient inter-Microengine and Microengine-to-Intel-XScale-core communication.
- Intel XScale® Core Peripherals (XPI) — Interrupt Controller, Timers, UART, General-Purpose IO (GPIO) and interface to low-speed off chip peripherals (such as maintenance port of network devices) and Flash memory.
- Performance Monitor — Counters that can be programmed to count selected internal chip hardware events; can be used to analyze and tune performance.

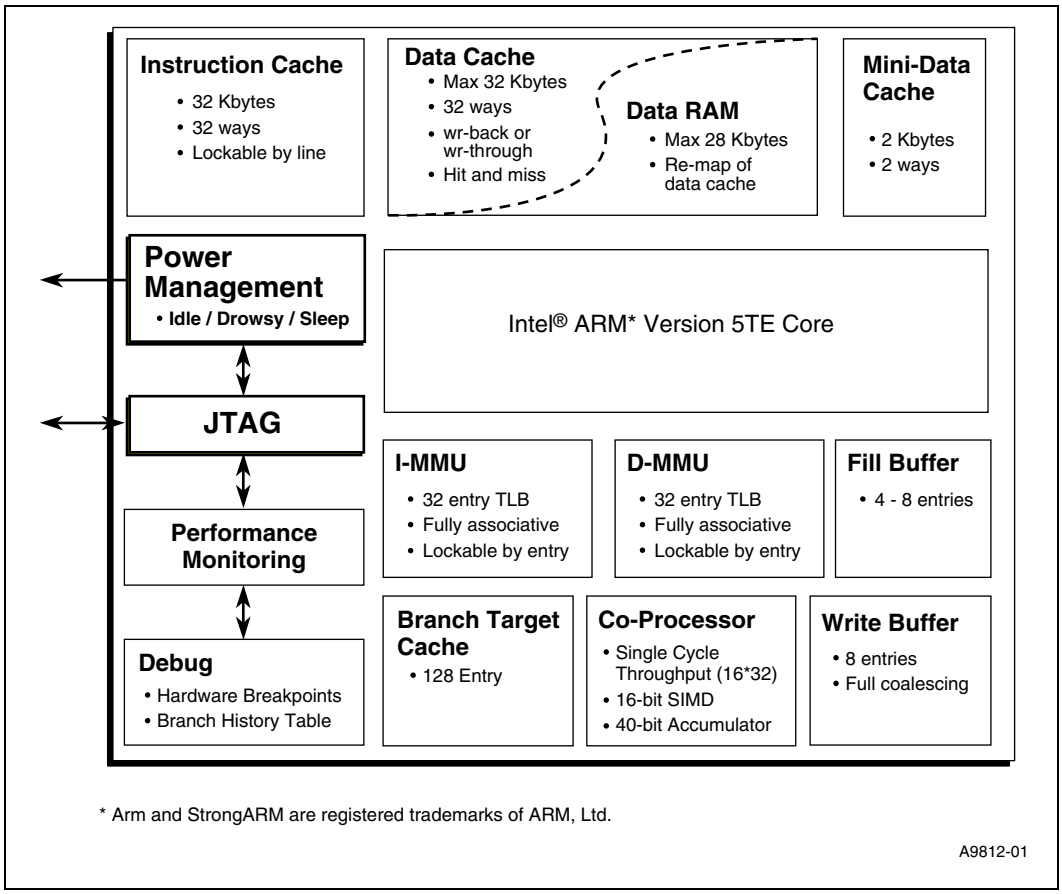
2.2 Intel XScale® Core

The Intel XScale core is a 32-bit general-purpose RISC processor. It incorporates an extensive list of architecture features that allows it to achieve high performance. The Intel XScale core is compatible to ARM* Version 5 (V5) Architecture. It implements the integer instruction set of ARM V5, but does not provide hardware support of the floating point instructions.

The Intel XScale core provides the Thumb instruction set (ARM V5T) and the ARM V5E DSP extensions. Backward compatibility with the first generation of StrongARM* products is maintained for user-mode applications. Operating systems may require modifications to match the specific hardware features of the Intel XScale core and to take advantage of the performance enhancements to the core.

Figure 5 shows the major functional Intel XScale core blocks that surround the ARM* V5TE core. The following sections give a brief, high-level overview of these blocks.

Figure 5. Intel XScale® Core Internal Block Diagram



2.2.1 Instruction Cache

The Intel XScale core implements a 32-Kbyte, 32-way set associative instruction cache with a line size of 32 bytes. All requests that “miss” the instruction cache generate a 32-byte read request to external memory. A mechanism to lock critical code within the cache is also provided.

2.2.2 Data Cache

The Intel XScale core implements a 32-Kbyte 32-way set-associative data cache, and a 2-Kbyte 2-way set-associative mini-data cache. Each cache has a line size of 32 bytes and supports write-through or write-back caching. The data/mini-data cache is controlled by the page attributes defined in the Memory Management Unit (MMU) Architecture.

2.2.3 Debug

The Intel XScale core supports software debugging, via the JTAG Port, through two instruction address breakpoint registers, one data-address breakpoint register, one data-address/mask breakpoint register, and a trace buffer.

2.2.4 Memory Management

The Intel XScale core implements the Memory Management Unit (MMU) Architecture specified in the ARM Architecture Reference Manual. The MMU provides access protection and virtual to physical address translation. The MMU Architecture also specifies the caching policies for the instruction cache and data memory. These policies are specified as page attributes and include:

- Identifying code as cacheable or non-cacheable
- Selecting between the mini-data cache or data cache
- Write-back or write-through data caching
- Enabling data write allocation policy
- Enabling the write buffer to coalesce stores to external memory

2.2.5 Branch Target Buffer

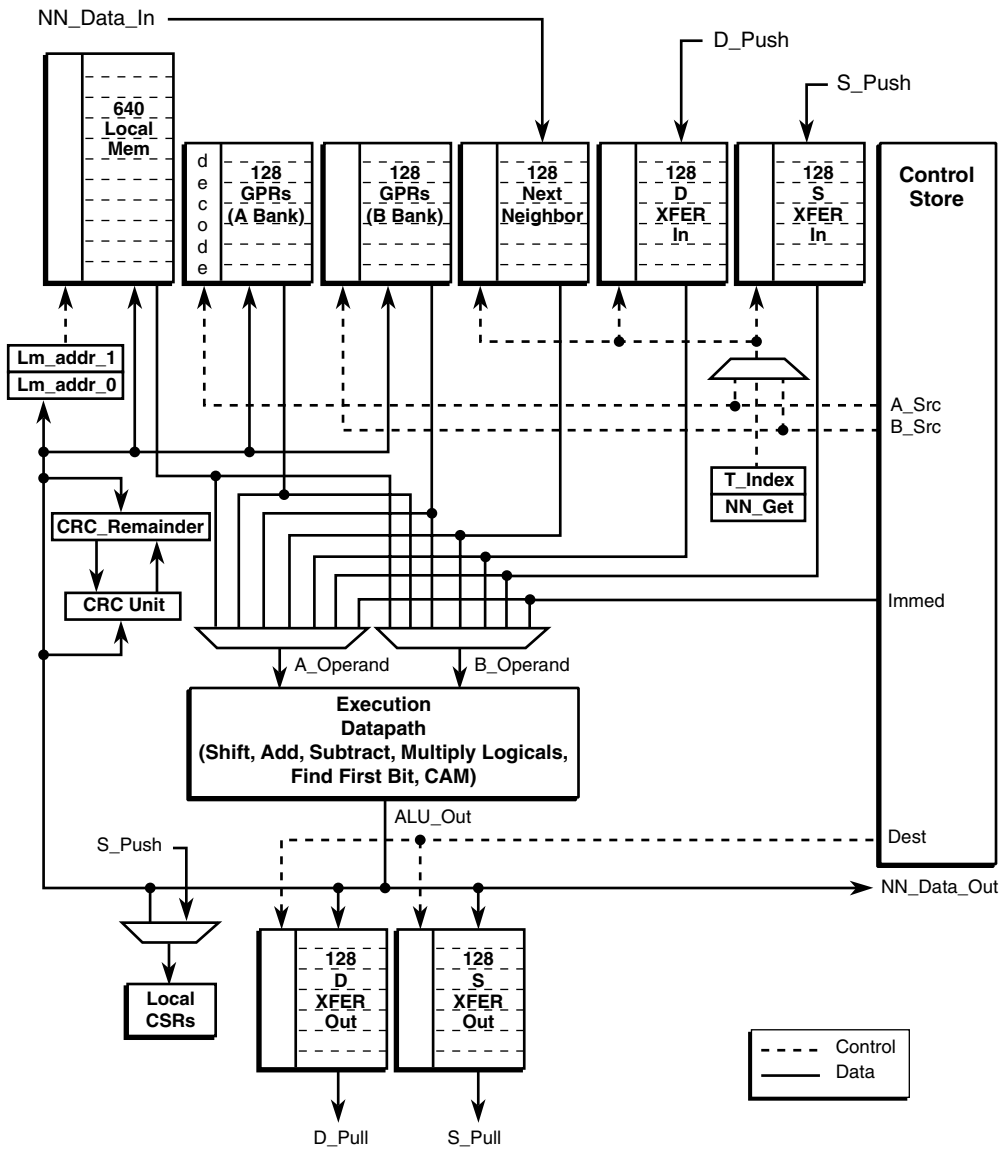
The Intel XScale core provides a Branch Target Buffer (BTB) to predict the outcome of branch-type instructions. It provides storage for the target address of branch-type instructions and predicts the next address to present to the instruction cache when the current instruction address is that of a branch. The BTB holds 128 entries.

2.3 Microengines

The Microengines (MEs) do most of the programmable per-packet processing in the IXP2400. There are eight MEs, connected as shown in Figure 4. The MEs have access to all shared resources (SRAM, DRAM, MSF, etc.) as well as private connections between adjacent MEs.

The MEs provide support for software-controlled multi-threaded operation. Given the disparity in processor cycle times versus external memory times, a single thread of execution will often block, waiting for external memory operations to complete. Having multiple threads available allows for threads to interleave operation; there is often at least one thread ready to run while others are blocked.

Figure 6. Microengine Block Diagram



2.3.1 Control Store

The Control Store is a RAM, which holds the program that the ME executes. It holds 4096 instructions, each of which is 40 bits wide. It is initialized by an external device (for example, the internal Intel XScale core.) The Control Store can optionally be protected by parity against soft errors.

2.3.1.1 Microengine Contexts

There are eight hardware Contexts available in the ME. To allow for efficient context swapping, each Context has its own register set, Program Counter, and context-specific local registers. Having a copy per Context eliminates the need to move Context-specific information to/from shared memory and ME registers for each Context swap. Fast context swapping allows a Context to do computation while other Contexts wait for IO (typically external memory accesses) to complete or for a signal from another Context or hardware unit.

2.3.2 General-Purpose Registers (GPRs)

The GPRs are used for general programming purposes. They are read and written exclusively under program control. GPRs, when used as a source in an instruction, supply operands to the execution datapath. When used as a destination in an instruction, they are written with the result of the execution datapath. The specific GPRs selected are encoded in the instruction. The GPRs are physically and logically contained in two banks, GPR A and GPR B.

2.3.3 Transfer Registers

Transfer Registers (Xfer Registers) are used for transferring data to and from the ME and locations external to the ME, (for example DRAMs, SRAMs etc). There are four types of transfer registers:

1. S_Transfer_In
2. S_Transfer_Out
3. D_Transfer_In
4. D_Transfer_Out

Transfer_In Registers, when used as a source in an instruction, supply operands to the execution datapath. The specific register selected is either encoded in the instruction, or selected indirectly via indexing. Transfer_In Registers are written by external units based on the ME requesting data from a resource outside of itself.

Transfer_Out Registers, when used as a destination in an instruction, are written with the result from the execution datapath. The specific register selected is encoded in the instruction, or selected indirectly via indexing. These registers in turn supply data to external units when selected by that unit.

2.3.4 Next Neighbor Registers

Next Neighbor Registers, when used as a source in an instruction, supply operands to the execution datapath. They are written either by the adjacent ME or by the same ME they are in. When Next Neighbor is used as a destination in an instruction; the instruction result data is sent out of the ME to the adjacent ME.

2.3.5 Local Memory (LM)

Local Memory is addressable storage located in the ME. LM is read and written exclusively under program control. LM supplies operands to the execution datapath as a source, and receives results as a destination. The specific LM location selected is based on the value in one of the LM_Addr Registers which are written by local_CSR_wr instructions. There are two LM_Addr Registers per

Context and a working copy of each. When a Context goes to Sleep state, the value of the working copies is put into the Context's copy of LM_Addr. When the Context returns to the Executing state, the value in its copy of LM_Addr are put into the working copies. The choice of LM_Addr_0 or LM_Addr_1 is selected in the instruction.

2.3.6 CRC Unit

The CRC Unit operates in parallel with the Execution Datapath. It takes two operands, performs a CRC operation, and writes back a result. CRC-16 and CRC-32 are supported. One of the operands is the CRC_Remainder Local CSR, and the other is a GPR, Transfer In Register, Next Neighbor, or LM, specified in the instruction and passed through the Execution Datapath to the CRC Unit. The instruction specifies the CRC operation type.

2.3.7 Event Signals

Event Signals are used to coordinate a program with completion of external events. For example, when a ME issues a command to an external unit to read data (which will be written into a Transfer_In register), the program must ensure that it does not try to use the data until the external unit has written it. There is no hardware mechanism to flag that a register write is pending, and then prevent the program from using it. Instead the coordination is under software control, with hardware support.

When the program issues the command to the external event, it can request that the external unit supply an indication (called an Event Signal) that the command has been completed. There are 15 Event Signals per Context that can be used, and Local CSRs per Context to track which Event Signals are pending and which have been returned. The Event Signals can be used to move a Context from Sleep state to Ready state, or alternatively, the program can test and branch on the status of Event Signals. Event Signals can be set in nine different ways:

1. When data is written into S_Transfer_In Registers (part of S_Push_ID input)
2. When data is written into D_Transfer_In Registers (part of D_Push_ID input)
3. When data is taken from S_Transfer_Out Registers (part of S_Pull_ID input)
4. When data is taken from D_Transfer_Out Registers (part of D_Pull_ID input)
5. On InterThread_Sig_In input
6. On NN_Sig_In input
7. On Prev_Sig_In input
8. On write to Same_ME_Signal Local CSR
9. By Internal Timer

2.4 DDR SDRAM

The DDR Memory Controller controls the off-chip DRAM. The DDR Controller contains the mechanism that allows the other functional units to access the single channel of DRAM present in the IXP2400. DRAM sizes of 64 MB, 128 MB, 512 MB and 1 GB are supported. Single-sided or double-sided DIMMs are supported. The IXP2400 only supports 4-bank DDR devices. Table 1 shows the supported configurations. The addressing capability of the DDR Controller is 2 GB. The address space always appears contiguous to software executing on the IXP2400. If less than 2 GB

of physical memory is present, the upper part of the address space is not utilized. Read and writes to DRAM generated by the MEs, the Intel XScale core, and PCI units, are presented as requests to the DDR controller, which enqueues them to their respective bank(s).

Error Correction Code (ECC) is supported. Each 64 bits (8 bytes) has an 8-bit ECC associated with it, thus all single bit errors are corrected while multiple bit errors are detected and optionally reported. The ECC operation can be disabled. When ECC is enabled, partial writes (writes of less than 8 bytes) will be performed as read-modify-write by the DDR controller.

Table 1. DDR Supported Configurations

Memory Capacity	DRAM Density	Part Width	Total Number of SDRAMs	Number of DIMMs	Number of Sides	Comments (sample DIMM vendors shown)
64 MB	64 Mbit	x8	9	1	1	
	128 Mbit	x16	5	1	1	
128 MB	64 Mbit	x8	18	1	2	
	128 Mbit	x8	9	1	1	Samsung*, Micron*
	128 Mbit	x16	10	1	2	
	256 Mbit	x16	5	1	1	
256 MB	128 Mbit	x8	18	1	2	Samsung*, Micron*
	256 Mbit	x16	10	1	2	Samsung*
	256 Mbit	x16	10	1	2	
	512 Mbit	x16	5	1	1	
512 MB	256 Mbit	x8	18	1	2	Samsung*, Micron*
	512 Mbit	x8	9	1	1	
	512 Mbit	x16	10	1	2	
	1.0 Gbit	x16	5	1	1	
1.0 GB	512 Mbit	x 8	18	1	2	
	1.0 Gbit	x 8	9	1	1	
	1.0 Gbit	x16	10	1	2	
2.0 GB	1.0 Gbit	x8	18	1	2	

2.5 SRAM

The IXP2400 has two independent SRAM controllers, each of which supports pipelined QDR synchronous static RAM (SRAM) and/or a coprocessor that adheres to QDR signaling. Either controller can be left unused if the application does not need to use its SRAM channels, which are accessible by the Microengines, the Intel XScale core, and the PCI Unit (external bus masters).

The memory is logically four bytes (32 bits) wide; physically the data pins are two bytes wide and are double clocked. Byte parity is supported. Each of the four bytes has a parity bit, which is generated when the byte is written and checked when the data is read. There are byte enables that select which bytes to write for writes of less than 32 bits.

Examples of supported SRAMs are:

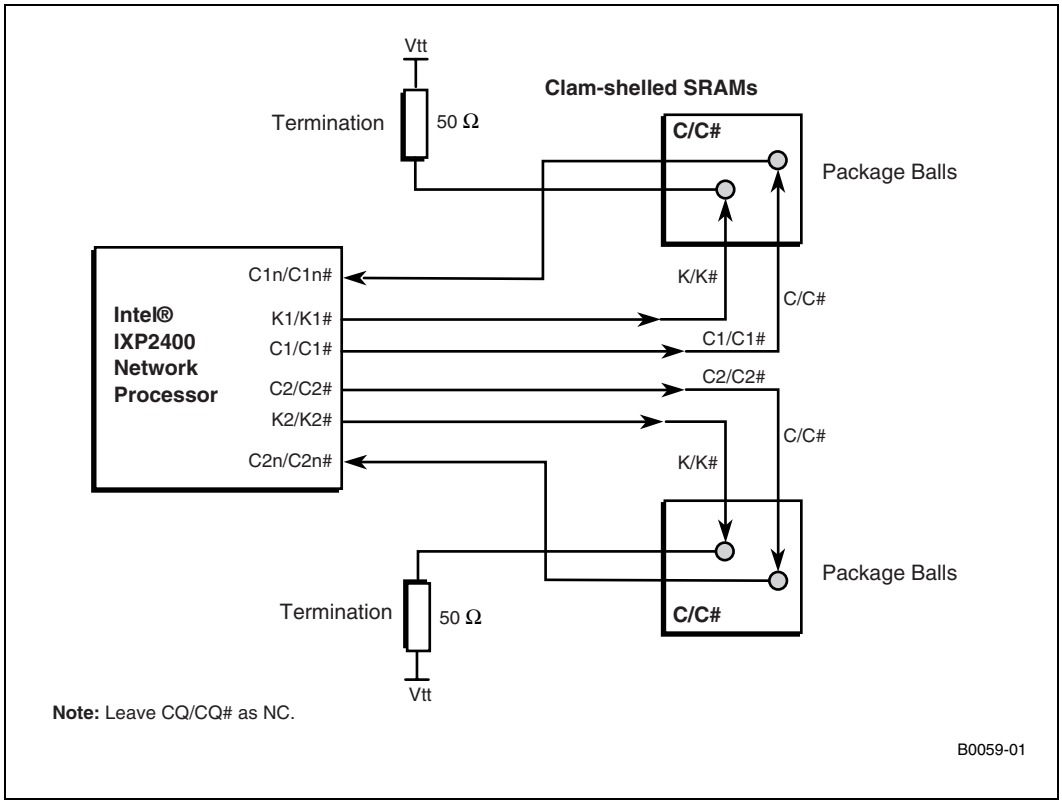
- Samsung* 36-Mb QDRII x9 K7R320982M-FC20 or 36-Mb QDRII x18 K7R321882M-FC20 SRAM
- IDT* IDT71T6280H 9-Mb pipelined QDR SRAM burst of 2 (512K x 18)
- Cypress* CY7C1302V25 9-Mb pipelined SRAM with QDR architecture (512K x 18)

Each of the two QDR ports are QDR- and QDRII-compatible. Each port implements the "_K" and "_C" output clocks as an input and their inversions. The "_C" clocks are used for reading SRAM data and the "_K" clocks are used for writing SRAM data. Extensive work has been performed to control the impedance within the IXP2400 for IXP2400-initiated signals that drive QDR parts. The receivers of IXP2400 QDR have on-die termination.

The IXP2400 IO driver/receiver can drive up to four QDR device loads. The IXP2400 supports bursts of two SRAM devices. The IXP2400 uses one pair of the Cn/Cn# clocks for read data; the other pair is terminated on the die.

The SRAM controller can also be configured to interface to an external coprocessor that adheres to the QDR electricals and protocol.

Figure 7. Clock Configuration



2.5.1 SRAM Controller Configurations

Each channel has enough address pins (24) to support up to 64 MB of SRAM. The SRAM controllers can directly generate multiple port enables (up to four pairs) to allow for depth expansion. Two pairs of pins are dedicated for port enables. Smaller RAMs use fewer address

signals than the number provided to accommodate the largest RAMs, so some address pins (23:20) are configurable as either address- or port-enable based on CSR setting as shown in Table 2. Note that all of the SRAMs on a given channel must be the same size.

Table 2. SRAM Controller Configurations

SRAM Configuration	SRAM Size	Addresses Needed to Index SRAM	Addresses Used as Port Enables	Total Number of Port Select Pairs Available
512K x 18	1 MB	17:0	23:22, 21:20	4
1M x 18	2 MB	18:0	23:22, 21:20	4
2M x 18	4 MB	19:0	23:22, 21:20	4
4M x 18	8 MB	20:0	23:22	3
8M x 18	16 MB	21:0	23:22	3
16M x 18	32 MB	22:0	None	2
32M x 18	64 MB	23:0	None	1

Each channel can be expanded by depth according to the number of port enables available. If external decoding is used, then the number of SRAMs used is not limited by the number of port enables generated by the SRAM controller.

Note: External decoding may require external pipeline registers to account for the decode time, depending on the desired frequency.

Maximum SRAM system sizes are shown in Table 3. Shaded entries require external decoding, because they use more port enables than the SRAM controller can supply directly.

Table 3. Total Memory per Channel

SRAM Size	Number of SRAMs on Channel							
	1	2	3	4	5	6	7	8
512K x 18	1 MB	2 MB	3 MB	4 MB	5 MB	6 MB	7 MB	8 MB
1M x 18	2 MB	4 MB	6 MB	8 MB	10 MB	12 MB	14 MB	16 MB
2M x 18	4 MB	8 MB	12 MB	16 MB	20 MB	24 MB	28 MB	32 MB
4M x 18	8 MB	16 MB	24 MB	32 MB	64 MB	NA	NA	NA
8M x 18	16 MB	32 MB	48 MB	64 MB	NA	NA	NA	NA
16M x 18	32 MB	64 MB	NA	NA	NA	NA	NA	NA
32M x 18	64 MB	NA	NA	NA	NA	NA	NA	NA

2.6 Media and Switch Fabric Interface

2.6.1 PHY Modes Supported

The Media and Switch Fabric (MSF) Interface connects the IXP2400 to a physical layer device (PHY) and/or a Switch Fabric Interface. MSF consists of the following external interfaces:

- Receive and transmit interfaces, each of which can be individually configured for either UTOPIA (Level 1, 2, and 3), POS-PHY (Level 2 and 3) or CSIX protocols.

- A Flow Control Interface, which provides a point-to-point connection used to pass CSIX-L1-B flow control C-Frames either between two IXP2400 network processors or between a IXP2400 and a CSIX-L1-B switch fabric.
- Each 32-bit interface can be subdivided into 8- or 16-bit channel combinations. The MSF interface uses 3.3V LVTTL (low-voltage transistor-transistor logic) signaling. While the CSIX standard is a source-synchronous bus, the IXP2400 uses a common-clocking scheme for compatibility with the other protocols.

In UTOPIA and POS-PHY modes, each port can function as a single 32-bit interface, or can be subdivided into a combination of 8- or 16-bit channels. Each channel is a point-to-point connection to a single physical layer device. Each Channel operates independently when subdivided. In addition to single-PHY mode, the IXP2400 supports multi-PHY (MPHY) mode. In MPHY mode, the 32-bit bus is shared by up to 16 ports in accordance with the UTOPIA Level 3 and POS PHY Level 3 Specifications. Master Mode only is supported in UTOPIA and POS-PHY modes.

Note: SPI3 is the name associated with POS-PHY Level 3.

The Optical Inter-networking Forum (OIF) controls the SPI3 Implementation Agreement document (available at http://www.oiforum.com).

2.6.2 CSIX

The IXP2400 implements CSIX_L1 (Common Switch Interface) for signalling and clocks. CSIX_L1 defines an interface between a Traffic Manager (TM) and a Switch Fabric (SF) for ATM, IP, MPLS, Ethernet, and similar data communications applications. The basic unit of information transferred between TMs and SFs is called a CFrame. There are a number of CFrame types defined, but they can be basically categorized as either Data, Control, or Flow Control. Associated with each CFrame is information such as length, type, address. This information is collected by the MSF and passed to Microengines.

The Network Processor Forum (NPF) controls the CSIX_L1 specification (available at http://www.npforum.org).

2.7 PCI Controller

The PCI Controller provides 64-bit, 66-MHz-capable PCI Rev. 2.2 interface. It is also compatible to 32-bit and/or 33-MHz PCI devices. The PCI controller provides the following functions:

- Target access (external bus master access to SRAM, DRAM, and CSRs)
- Master access (Intel XScale core or Microengine access to PCI target devices)
- Three DMA channels
- Mailbox and Doorbell Registers for Intel XScale core-to-host communication
- PCI arbiter

The IXP2400 can be configured to act as PCI central function, or can own the arbitration.

2.8 XPI Unit

2.8.1 GPIO

The IXP2400 contains eight General-Purpose IO (GPIO) pins. These can be programmed as either input or output, and can be used for slow-speed IO, such as LEDs or input switches. They can also be used as interrupts to the Intel XScale core, or to clock the programmable timers.

2.8.2 Serial Port

The IXP2400 contains a standard RS-232–compatible universal asynchronous receiver/transmitter (UART), which can be used for communication with a debugger or maintenance console. Modem controls are not supported; if they are needed, GPIO pins can be used for that purpose.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the processor. The processor can read the complete status of the UART at any time during operation. Available status information includes the type and condition of the transfer operations being performed by the UART and any error conditions (parity, overrun, framing or break interrupt).

The serial ports can operate in either FIFO or non-FIFO mode. In FIFO mode, a 64-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 64-byte receive FIFO buffers data from the serial link until read by the processor.

The UART includes a programmable baud rate generator that is capable of dividing the internal clock input (APB_CLK, running at 50 MHz) by divisors of 1 to 2^{16} - 1, and produces a 16x clock to drive the internal transmitter logic. It also drives the receive logic. The UART can be operated in polled or in interrupt-driven mode as selected by software.

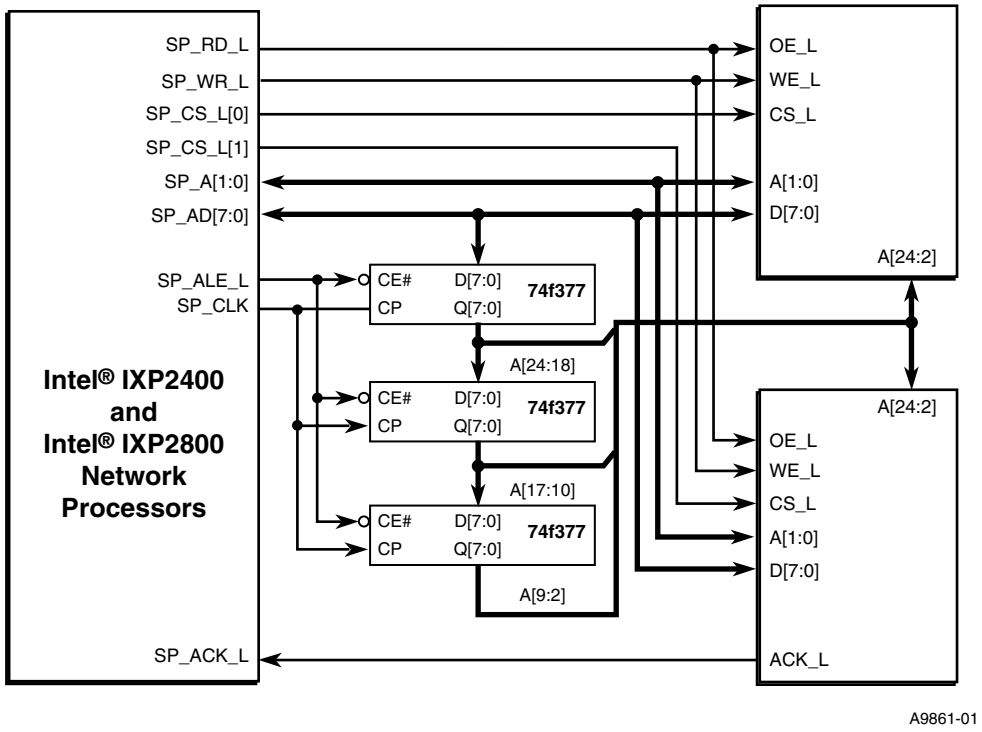
The UART has two clocks: The clock from the baud rate generator for transmit and receive operation, and the clock from the XPI unit for register reads and writes.

2.8.3 SlowPort

The SlowPort is an external interface to the IXP2400 and is used for Flash memory access and 8-, 16-, or 32-bit asynchronous device access. It allows the Intel XScale core to do read/ write data transfers to these slave devices.

The address bus and data bus are multiplexed to reduce the pin count. In addition, the address bus is also compressed from A[24:0] down to A[7:0] and shifted out with three clock cycles in Mode 0, and four clock cycles in Mode 1–4. Therefore, an external set of buffers is needed to latch the address. Two chip selects are provided. Several modes of configurations are supported to connect with the microprocessor control port of various framers or MAC devices. See Figure 8 for an example configuration (note that the ACK signal is optional).

Figure 8. Example SlowPort Connection

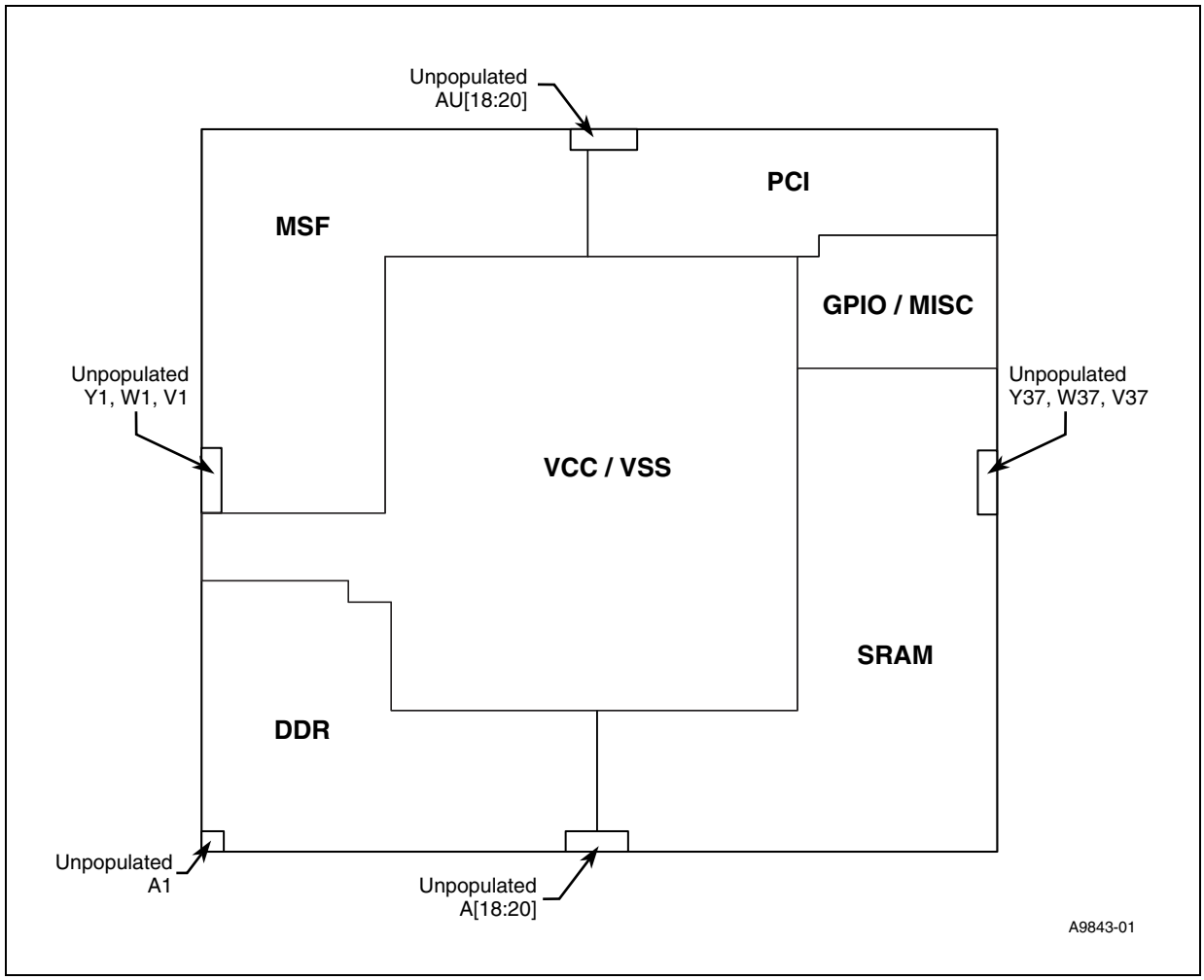


3.0 Signal Description

3.1 Ballout Functional Groupings Diagram

Figure 9 provides a high-level overview of the general groupings of the balls by function. Note that the following ball locations are unpopulated: A1, Y1, W1, V1, Y37, W37, V37, AU[18:20], and A[18:20].

Figure 9. High-Level Overview of Ballout Functional Groupings Diagram (Ball Side)



3.2 Ball Descriptions Grouped by Function

This section gives an overview of the IXP2400 IO signals. Detailed definitions and description of the use of signals can be found in chapters of the specification specific to each interface.

IXP2400 signals are categorized into one of several groups: DRAM, SRAM, Media and Switch Fabric Interface, PCI, GPIO, SlowPort (Serial ROM), Serial Port, Clocks, and JTAG and Test.

3.2.1 DDR SDRAM

There is one double-data-rate (DDR) DRAM channel, having the signals found in Table 4. The DDR SDRAM interface is clocked at 100 or 150 MHz with data transfers on both edges of the clock. The SDRAMs use SSTL_2 signaling levels per the JEDEC JESD79 specification.

Table 4. DDR SDRAM Signals

Signal Name	I/O	Description	Number
D_CK[2:0]	O	Positive master clock	3
D_CK_L[2:0]	O	Negative master clock	3
D_CS_L[1:0]	O	Chip selects	2
D_RAS_L	O	Row address strobe	1
D_CAS_L	O	Column address strobe	1
D_WE_L	O	Write enable	1
D_DM[8:0]	O	Data mask (write data)	9
D_BA[1:0]	O	Bank address selects	2
D_A[13:0]	O	Address	14
D_DQ[63:0]	I/O	Data	64
D_ECC[7:0]	I/O	Error Correction Code bits	8
D_DQS[8:0]	I/O	Data strobes	9
D_RCVENOUT_L	O	Output clock for source synchronous reads	1
D_RCVENIN_L	I	Input clock for source synchronous reads	1
D_RCOMP[1:0]	I	Buffer compensation[1]	2
D_VREF[1:0]	I	Voltage reference	2
D_CKE[1:0]	O	Clock enables used by controller during initialization	2
Total (per channel)			125

1. The IXP2400 uses a compensation signal to adjust the system memory buffer characteristics over temperature, process, and voltage variations. The DDR pins D_RCOMP[1] and D_RCOMP[0] should be connected to the DDR termination voltage (1.25V) through a 30Ω ±1% resistor and one 0603 0.1 µF decoupling capacitor to ground. Place the resistor and capacitor as close to the IXP2400 as possible, within 1.0” of the package. The compensation signal and the VTT trace should be routed with as wide a trace as possible, minimum of 12 mils wide and isolated from other signals with a minimum of 10-mil spacing.

3.2.2 SRAM

There are two SRAM interfaces to quad-data-rate (QDR) SRAMs. Each interface has the signals found in Table 5. The SRAMs use HSTL signaling levels.

QDR SRAM datasheets typically document the data and parity signals as D[17:0]. The IXP2400 signal documentation splits up the data and parity signals, in terms of data[7:0], data[15:8], parity[0], and parity[1]. The data[7:0] signals should be connected to QDR SRAM D[7:0]. The data[15:8] signals should be connected to QDR SRAM D[16:9]. The parity[0] signal should be connected to QDR SRAM D[8]. The parity[1] signal should be connected to QDR SRAM D[17].

Table 5. SRAM Signals

Signal Name	I/O	Description	Number
Sn_K[1:0]	O	Positive and negative output clocks. Address, Port Enable, Data Out are referenced to these clocks.	2
Sn_K_L[1:0]	O		2
Sn_C[1:0]	O	Positive and negative output clocks used to generate Sn_CIN[1:0] and Sn_CIN_L[1:0]	2
Sn_C_L[1:0]	O		2
Sn_CIN[1:0]	I	Positive and negative clock inputs. They are the feedback of Sn_C[1:0] and Sn_C_L[1:0].	2
Sn_CIN_L[1:0]	I		2
Sn_DI[15:0]	I	Data Input bus	16
Sn_PI[1:0]	I	Byte parity for data in; PI[1] for DI[15:8], and PI[0] for DI[7:0]	2
Sn_DO[15:0]	O	Data Output bus	16
Sn_PO[1:0]	O	Byte parity for data out; PO[1] for DO[15:8], and PO[0] for DO[7:0]	2
Sn_BWE_L[1:0]	O	Byte write enables; asserted to enable writing each byte during writes.	2
Sn_RPE_L[1:0]	O	Read Port enable; asserted to start a read.	2
Sn_WPE_L[1:0]	O	Write Port enable; asserted to start a write.	
Sn_A[23:0]	O	Address to SRAMs. Some addresses signals can be programmed to act as additional port enables (via CSR control).	24
Sn_Vref		HSTL reference voltage	1
Sn_ZQ[1:0]	I	Impedance match[1]	2
Total (per channel)			81

1. QDR uses a similar compensation scheme as DDR. However, the voltage references are different. The pins S0_ZQ[0] and S1_ZQ[0] must each be separately connected to ground through a high precision 50Ω resistor and one 0603 0.1 µF decoupling capacitor. The pins S0_ZQ[1] and S1_ZQ[1] should each be separately connected to QDR IO voltage (1.5V) thorough a high precision 50Ω resistor and one 0603 0.1 µF decoupling capacitor. Place the resistor and capacitor as close to the IXP2400 as possible, within 1.0" of the package. The compensation signal and the VTT trace should be routed with as wide a trace as possible, minimum of 12 mils wide and isolated from other signals with a minimum of 10-mil spacing.

3.2.3 Media and Switch Fabric (MSF) Interface

In Table 6, the use of the pins is based on whether or not the port is in UTOPIA, POS-PHY, or CSIX mode. Table 6 shows how the external pin names map to the signal names referenced in the UTOPIA, POS-PHY, and CSIX specifications. The table shows all the possible signals that could be used for a particular standard. However, a particular mode within a standard, such as MPHY or SPHY, will not necessarily use all the signals shown in a column.

Note: The Media bus is 3.3V LVTTL using globally synchronous (common) clocking. Thus the bus does not have electrical or clocking compatibility with the CSIX-L1 specification, which is 2.5V LVCMOS with source synchronous clocking.

Each interface has two clocks; RXCLK01/TXCLK01 is used by the ports associated with bits [15:0]; RXCLK23/TXCLK23 is used by the ports associated with bits[31:16]. This applies only to the 4 x 8, 2 x 16, and 1 x 16 + 2 x 8 SPHY modes, and allows each half of the bus to be clocked independently. In 1 x 32 SPHY, MPHY, or CSIX modes, only RXCLK01/TXCLK01 is used and is internally routed to all the logic; RXCLK23 and TXCLK23 are tied to ground.

Table 6. MSF Data Signals

Pin Name	I/O	Type	Description	Number
RXCLK23	I	LVTTL	Receive clock for Channel 2 and 3	1
RXCLK01	I	LVTTL	Receive clock for Channel 0 and 1	1
RXENB[3:0]	O	LVTTL	Receive enable	4
RXSOF[3:0]	I	LVTTL	Receive start of frame	4
RXEOF[3:0]	I	LVTTL	Receive end of frame	4
RXVAL[3:0]	I	LVTTL	Receive data valid	4
RXERR[3:0]	I	LVTTL	Receive data error	4
RXPRTY[3:0]	I	LVTTL	Receive data parity	4
RXFA[3:0]	I	LVTTL	Received cell/frame available	4
RXADDR[3:0]	O	LVTTL	Receive PHY address	4
RXPFA	I	LVTTL	Receive (polled) frame available	1
RXPADL[1:0]	I	LVTTL	These are the same signals as RMOD[1:0] in SPI3 and POS PHY L2.	2
RXDATA[31:0]	I	LVTTL	Receive data	32
TXCLK23	I	LVTTL	Transmit clock for Channel 2 and 3	1
TXCLK01	I	LVTTL	Transmit clock for Channel 0 and 1	1
TXENB[3:0]	O	LVTTL	Transmit enable	4
TXSOF[3:0]	O	LVTTL	Transmit start of frame	4
TXEOF[3:0]	O	LVTTL	Transmit end of frame	4
TXERR[3:0]	O	LVTTL	Transmit error indicator	4
TXPRTY[3:0]	O	LVTTL	Transmit bus parity	4
TXFA[3:0]	I	LVTTL	Transmit cell buffer available	4
TXADDR[3:0]	O	LVTTL	Transmit address of PHY	4
TXPFA	I	LVTTL	Transmit polled PHY frame available	1
TXSFA	I	LVTTL	Transmit selected PHY frame available	1
TXPADL[1:0]	O	LVTTL	Transmit modulo. They are the same signals as TMOD[1:0] in SPI3 and POS PHY L2.	2
TXDATA[31:0]	O	LVTTL	Transmit data	32
TXRCOMP[1]	I	LVTTL	Transmitter compensation resistor	1

Table 6. MSF Data Signals (Continued)

Pin Name	I/O	Type	Description	Number
RXRCOMP[1]	I	LVTTL	Receiver compensation resistor	1
MSF_CLK_BYPASS[2]	I	LVTTL	Media switch fabric PLL bypass	1
RSVD[3:0]			Reserved pins. These pins should be No Connect.	4
Total (per channel)				142

NOTES:
1. The MSF TXRCOMP and RXRCOMP pins should be separately connected to ground through external 45Ω±1% resistor and one 0603 0.1 µF decoupling capacitor. Place the resistor and capacitor as close to the IXP2400 as possible, within 1.0" of the package. The compensation signal should be routed with as wide a trace as possible, minimum of 12 mils wide and isolated from other signals with a minimum of 10-mil spacing.
2. MSF_CLK_BYPASS is used for debug only. If the MSF PLL fails to work, asserting this signal enables the buffered external clock to bypass the PLL to connect to the internal MSF clock trees. In normal operation, it should be tied to low.

See Table 22 "CBus Pinout" on page 62 for information regarding signals used to communicate flow control information between two IXP2400 network processors.

3.2.3.1 MSF Mode Signal Usage

The following tables specify the signal usage for each mode supported by the MSF and the mapping of these signals to the MSF pinout.

1. Table 7, Table 8, Table 9, and Table 10 describe the UTOPIA and POS-PHY SPHY modes. In these modes, the bus is configured as 1x32, 2x16, 4x8, or 1x16+2x8, and the ports may be any combination of UTOPIA or POS-PHY SPHY ports, master or slave.
2. Table 11 describes x32 UTOPIA Level 3 MPHY mode pinout.
3. Table 12 describes x32 POS-PHY Level 3 MPHY mode pinout.
4. Table 13 describes CSIX/CBus mode pinout.
5. Table 14 and Table 15 describe x16 UTOPIA Level 2 MPHY mode with one x16 or two x8 SPHY ports. The SPHY ports may be any combination of UTOPIA or POS-PHY, master or slave.
6. Table 16 and Table 17 describe x16 POS-PHY Level 2 MPHY mode with one x16 or two x8 SPHY ports. The SPHY ports may be any combination of UTOPIA or POS-PHY, master or slave.
7. The pin names assume master mode operation. In slave mode operation, the pins have a different meaning. Table 18, Table 19, Table 20, and Table 21 describe the master pin name to slave function mapping for various bus widths.
8. Table 22 describes the CBus pinout.

Table 7. 1x32 SPHY UTOPIA/POS-PHY Master Mode

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground
Port 2 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[2]	Output	unused; no connect
	RXSOF[2]	Input	unused; tie to ground
	RXEOF[2]	Input	unused; tie to ground
	RXVAL[2]	Input	unused; tie to ground
	RXERR[2]	Input	unused; tie to ground
	RXPRTY[2]	Input	unused; tie to ground
	RXFA[2]	Input	unused; tie to ground
Port 1 (unused)	RXCLK01	Input	
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0	RXCLK01	Input	
	RXENB[0]	Output	
	RXSOF[0]	Input	
	RXEOF[0]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[0]	Input	not used in UTOPIA mode, tie to ground
	RXERR[0]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[0]	Input	
	RXFA[0]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXDATA[31:0]	Input	
	RXPADL[1:0]	Input	not used in UTOPIA mode, tie to ground
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground

Table 7. 1x32 SPHY UTOPIA/POS-PHY Master Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	unused; tie to ground
Port 2 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[2]	Output	unused; no connect
	TXSOF[2]	Output	unused; no connect
	TXEOF[2]	Output	unused; no connect
	TXERR[2]	Output	unused; no connect
	TXPRTY[2]	Output	unused; no connect
	TXFA[2]	Input	unused; tie to ground
Port 1 (unused)	TXCLK01	Input	
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	unused; tie to ground
Port 0	TXCLK01	Input	
	TXENB[0]	Output	
	TXSOF[0]	Output	
	TXEOF[0]	Output	not used in UTOPIA mode, no connect
	TXERR[0]	Output	not used in UTOPIA mode, no connect
	TXPRTY[0]	Output	
	TXFA[0]	Input	
	TXPADL[1:0]	Output	not used in UTOPIA mode, no connect
	TXDATA[31:0]	Output	
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 8. 2x16 SPHY UTOPIA/POS Master Mode

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	RXCLK23	Input	
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground
Port 2	RXCLK23	Input	
	RXENB[2]	Output	
	RXSOF[2]	Input	
	RXEOF[2]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[2]	Input	not used in UTOPIA mode, tie to ground
	RXERR[2]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[2]	Input	
	RXFA[2]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXPADL[1]	Input	not used in UTOPIA mode, tie to ground
	RXDATA[31:16]	Input	
Port 1	RXCLK01	Input	
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0	RXCLK01	Input	
	RXENB[0]	Output	
	RXSOF[0]	Input	
	RXEOF[0]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[0]	Input	not used in UTOPIA mode, tie to ground
	RXERR[0]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[0]	Input	
	RXFA[0]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXPADL[0]	Input	not used in UTOPIA mode, tie to ground
	RXDATA[15:0]	Input	

Table 8. 2x16 SPHY UTOPIA/POS Master Mode (Continued)

Port	Master Pin Name	Direction	Notes
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground
Port 3 (unused)	TXCLK23	Input	
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	unused; tie to ground
Port 2	TXCLK23	Input	
	TXENB[2]	Output	
	TXSOF[2]	Output	
	TXEOF[2]	Output	not used in UTOPIA mode, no connect
	TXERR[2]	Output	not used in UTOPIA mode, no connect
	TXPRTY[2]	Output	
	TXFA[2]	Input	
	TXPADL[1]	Output	not used in UTOPIA mode, no connect
	TXDATA[31:16]	Output	
Port 1 (unused)	TXCLK01	Input	
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	unused; tie to ground
Port 0	TXCLK01	Input	
	TXENB[0]	Output	
	TXSOF[0]	Output	
	TXEOF[0]	Output	not used in UTOPIA mode, no connect
	TXERR[0]	Output	not used in UTOPIA mode, no connect
	TXPRTY[0]	Output	
	TXFA[0]	Input	
	TXPADL[0]	Output	not used in UTOPIA mode, no connect
	TXDATA[15:0]	Output	
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 9. 4x8 SPHY UTOPIA/POS-PHY Master Mode

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3	RXCLK23	Input	
	RXENB[3]	Output	
	RXSOF[3]	Input	
	RXEOF[3]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[3]	Input	not used in UTOPIA mode, tie to ground
	RXERR[3]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[3]	Input	
	RXFA[3]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXDATA[31:24]	Input	
Port 2	RXCLK23	Input	
	RXENB[2]	Output	
	RXSOF[2]	Input	
	RXEOF[2]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[2]	Input	not used in UTOPIA mode, tie to ground
	RXERR[2]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[2]	Input	
	RXFA[2]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXPADL[1]	Input	not used in UTOPIA mode, tie to ground; not used in POS-PHY x8 mode, tie to ground
	RXDATA[23:16]	Input	
Port 1	RXCLK01	Input	
	RXENB[1]	Output	
	RXSOF[1]	Input	
	RXEOF[1]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[1]	Input	not used in UTOPIA mode, tie to ground
	RXERR[1]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[1]	Input	
	RXFA[1]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXDATA[15:8]	Input	

Table 9. 4x8 SPHY UTOPIA/POS-PHY Master Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 0	RXCLK01	Input	
	RXENB[0]	Output	
	RXSOF[0]	Input	
	RXEOF[0]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[0]	Input	not used in UTOPIA mode, tie to ground
	RXERR[0]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[0]	Input	
	RXFA[0]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXPADL[0]	Input	not used in UTOPIA mode, tie to ground; not used in POS-PHY x8 mode, tie to ground
	RXDATA[7:0]	Input	
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground
Port 3	TXCLK23	Input	
	TXENB[3]	Output	
	TXSOF[3]	Output	
	TXEOF[3]	Output	not used in UTOPIA mode, no connect
	TXERR[3]	Output	not used in UTOPIA mode, no connect
	TXPRTY[3]	Output	
	TXFA[3]	Input	
	TXDATA[31:24]	Output	
Port 2	TXCLK23	Input	
	TXENB[2]	Output	
	TXSOF[2]	Output	
	TXEOF[2]	Output	not used in UTOPIA mode, no connect
	TXERR[2]	Output	not used in UTOPIA mode, no connect
	TXPRTY[2]	Output	
	TXFA[2]	Input	
	TXPADL[0]	Output	not used in UTOPIA mode, no connect; not used in POS-PHY x8 mode, no connect
	TXDATA[23:16]	Output	

Table 9. 4x8 SPHY UTOPIA/POS-PHY Master Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 1	TXCLK01	Input	
	TXENB[1]	Output	
	TXSOF[1]	Output	
	TXEOF[1]	Output	not used in UTOPIA mode, no connect
	TXERR[1]	Output	not used in UTOPIA mode, no connect
	TXPRTY[1]	Output	
	TXFA[1]	Input	
	TXDATA[15:8]	Output	
Port 0	TXCLK01	Input	
	TXENB[0]	Output	
	TXSOF[0]	Output	
	TXEOF[0]	Output	not used in UTOPIA mode, no connect
	TXERR[0]	Output	not used in UTOPIA mode, no connect
	TXPRTY[0]	Output	
	TXFA[0]	Input	
	TXPADL[0]	Output	not used in UTOPIA mode, no connect; not used in POS-PHY x8 mode, no connect
	TXDATA[7:0]	Output	
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 10. 1x16+2x8 SPHY UTOPIA/POS Master Mode

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3	RXCLK23	Input	
	RXENB[3]	Output	
	RXSOF[3]	Input	
	RXEOF[3]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[3]	Input	not used in UTOPIA mode, tie to ground
	RXERR[3]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[3]	Input	
	RXFA[3]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXDATA[31:24]	Input	

Table 10. 1x16+2x8 SPHY UTOPIA/POS Master Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 2	RXCLK23	Input	
	RXENB[2]	Output	
	RXSOF[2]	Input	
	RXEOF[2]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[2]	Input	not used in UTOPIA mode, tie to ground
	RXERR[2]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[2]	Input	
	RXFA[2]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXPADL[1]	Input	not used in UTOPIA mode, tie to ground; not used in POS-PHY x8 mode, tie to ground
	RXDATA[23:16]	Input	
Port 1 (unused)	RXCLK01	Input	
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0	RXCLK01	Input	
	RXENB[0]	Output	
	RXSOF[0]	Input	
	RXEOF[0]	Input	not used in UTOPIA mode, tie to ground
	RXVAL[0]	Input	not used in UTOPIA mode, tie to ground
	RXERR[0]	Input	not used in UTOPIA mode, tie to ground
	RXPRTY[0]	Input	
	RXFA[0]	Input	not used in POS-PHY Level 3 SPHY mode, tie to ground
	RXPADL[0]	Input	not used in UTOPIA mode, tie to ground
	RXDATA[15:0]	Input	
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground

Table 10. 1x16+2x8 SPHY UTOPIA/POS Master Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3	TXCLK23	Input	
	TXENB[3]	Output	
	TXSOF[3]	Output	
	TXEOF[3]	Output	not used in UTOPIA mode, no connect
	TXERR[3]	Output	not used in UTOPIA mode, no connect
	TXPRTY[3]	Output	
	TXFA[3]	Input	
	TXDATA[31:24]	Output	
Port 2	TXCLK23	Input	
	TXENB[2]	Output	
	TXSOF[2]	Output	
	TXEOF[2]	Output	not used in UTOPIA mode, no connect
	TXERR[2]	Output	not used in UTOPIA mode, no connect
	TXPRTY[2]	Output	
	TXFA[2]	Input	
	TXPADL[1]	Output	not used in UTOPIA mode, no connect; not used in POS-PHY x8 mode, no connect
	TXDATA[23:16]	Output	
Port 1 (unused)	TXCLK01	Input	
	TXENB[1]	Output	
	TXSOF[1]	Output	
	TXEOF[1]	Output	not used in UTOPIA mode, no connect
	TXERR[1]	Output	not used in UTOPIA mode, no connect
	TXPRTY[1]	Output	
	TXFA[1]	Input	
Port 0	TXCLK01	Input	
	TXENB[0]	Output	
	TXSOF[0]	Output	
	TXEOF[0]	Output	not used in UTOPIA mode, no connect
	TXERR[0]	Output	not used in UTOPIA mode, no connect
	TXPRTY[0]	Output	
	TXFA[0]	Input	
	TXPADL[0]	Output	not used in UTOPIA mode, no connect
	TXDATA[15:0]	Output	
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 11. x32 UTOPIA Level 3 MPHY Mode

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	used only in MPHY-4 direct status mode
Port 2 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[2]	Output	unused; no connect
	RXSOF[2]	Input	unused; tie to ground
	RXEOF[2]	Input	unused; tie to ground
	RXVAL[2]	Input	unused; tie to ground
	RXERR[2]	Input	unused; tie to ground
	RXPRTY[2]	Input	unused; tie to ground
	RXFA[2]	Input	used only in MPHY-4 direct status mode
Port 1 (unused)	RXCLK01	Input	
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	used only in MPHY-4 direct status mode

Table 11. x32 UTOPIA Level 3 MPHY Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 0 (MPHY)	RXCLK01	Input	
	RXENB[0]	Output	
	RXSOF[0]	Input	
	RXEOF[0]	Input	unused; tie to ground
	RXVAL[0]	Input	unused; tie to ground
	RXERR[0]	Input	unused; tie to ground
	RXPRTY[0]	Input	
	RXFA[0]	Input	used only in MPHY-4 direct status mode
	RXDATA[31:0]	Input	
	RXPADL[1:0]	Input	unused; tie to ground
	TXCSRB	Output	RXADDR[4]
	RXADDR[3:0]	Output	
	RXPFA	Input	used only in MPHY-4/MPHY-32 polled status mode
Port 3 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	used only in MPHY-4 direct status mode
Port 2 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[2]	Output	unused; no connect
	TXSOF[2]	Output	unused; no connect
	TXEOF[2]	Output	unused; no connect
	TXERR[2]	Output	unused; no connect
	TXPRTY[2]	Output	unused; no connect
	TXFA[2]	Input	used only in MPHY-4 direct status mode
Port 1 (unused)	TXCLK01	Input	
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	used only in MPHY-4 direct status mode

Table 11. x32 UTOPIA Level 3 MPHY Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 0 (MPHY)	TXCLK01	Input	
	TXENB[0]	Output	
	TXSOF[0]	Output	
	TXEOF[0]	Output	unused in UTOPIA mode, no connect
	TXERR[0]	Output	unused in UTOPIA mode, no connect
	TXPRTY[0]	Output	
	TXFA[0]	Input	used only in MPHY-4 direct status mode
	TXPADL[1:0]	Output	unused in UTOPIA mode, no connect
	TXDATA[31:0]	Output	
	TXPFA	Input	used only in MPHY-4/MPHY-32 polled status mode
	TXSFA	Input	unused in UTOPIA mode, tie to ground
	TXENB[1]	Output	TXADDR[4]
	TXADDR[3:0]	Output	

Table 12. x32 POS-PHY Level 3 MPHY Mode

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground
Port 2 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[2]	Output	unused; no connect
	RXSOF[2]	Input	unused; tie to ground
	RXEOF[2]	Input	unused; tie to ground
	RXVAL[2]	Input	unused; tie to ground
	RXERR[2]	Input	unused; tie to ground
	RXPRTY[2]	Input	unused; tie to ground
	RXFA[2]	Input	unused; tie to ground

Table 12. x32 POS-PHY Level 3 MPHY Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 1 (unused)	RXCLK01	Input	
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0 (MPHY)	RXCLK01	Input	
	RXENB[0]	Output	
	RXSOF[0]	Input	
	RXEOF[0]	Input	
	RXVAL[0]	Input	
	RXERR[0]	Input	
	RXPRTY[0]	Input	
	RXFA[0]	Input	unused; tie to ground
	RXDATA[31:0]	Input	
	RXPADL[1:0]	Input	
	TXCSRB	Output	unused; no connect
	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	
Port 3 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	used only in MPHY-4 direct status mode
Port 2 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[2]	Output	unused; no connect
	TXSOF[2]	Output	unused; no connect
	TXEOF[2]	Output	unused; no connect
	TXERR[2]	Output	unused; no connect
	TXPRTY[2]	Output	unused; no connect
	TXFA[2]	Input	used only in MPHY-4 direct status mode

Table 12. x32 POS-PHY Level 3 MPHY Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 1 (unused)	TXCLK01	Input	
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	used only in MPHY-4 direct status mode
Port 0 (MPHY)	TXCLK01	Input	
	TXENB[0]	Output	
	TXSOF[0]	Output	
	TXEOF[0]	Output	
	TXERR[0]	Output	
	TXPRTY[0]	Output	
	TXFA[0]	Input	used only in MPHY-4 direct status mode
	TXPADL[1:0]	Output	
	TXDATA[31:0]	Output	
	TXPFA	Input	used only in MPHY-4/MPHY-32 polled status mode
	TXSFA	Input	unused, tie to ground
	TXENB[1]	Output	TXADDR[4]
	TXADDR[3:0]	Output	

Table 13. 1x32 CSIX Mode

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground

Table 13. 1x32 CSIX Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 2 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[2]	Output	unused; no connect
	RXSOF[2]	Input	unused; tie to ground
	RXEOF[2]	Input	unused; tie to ground
	RXVAL[2]	Input	unused; tie to ground
	RXERR[2]	Input	unused; tie to ground
	RXPRTY[2]	Input	unused; tie to ground
	RXFA[2]	Input	unused; tie to ground
Port 1 (unused)	RXCLK01	Input	
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0 (CSIX Rx)	RXCLK01	Input	
	RXENB[0]	Output	unused; no connect
	RXSOF[0]	Input	
	RXEOF[0]	Input	unused; tie to ground
	RXVAL[0]	Input	unused; tie to ground
	RXERR[0]	Input	unused; tie to ground
	RXPRTY[0]	Input	
	RXFA[0]	Input	unused; tie to ground
	RXDATA[31:0]	Input	
	RXPADL[1:0]	Input	unused; tie to ground
	RXADDR[3:0]	Output	TXCDAT[7:4]; used only in x8 CBus mode
	RXPFA	Input	unused; tie to ground
CBus Tx	RXCLK01	Input	
	TXCSOF	Output	
	TXCDAT[3:0]	Output	
	TXCPAR	Output	
	TXCSRB	Output	
	TXCFC	Output	

Table 13. 1x32 CSIX Mode (Continued)

Port	Master Pin Name	Direction	Notes
Port 3 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	unused; tie to ground
Port 2 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[2]	Output	unused; no connect
	TXSOF[2]	Output	unused; no connect
	TXEOF[2]	Output	unused; no connect
	TXERR[2]	Output	unused; no connect
	TXPRTY[2]	Output	unused; no connect
	TXFA[2]	Input	unused; tie to ground
Port 1 (unused)	TXCLK01	Input	
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	RXCDAT[7]; used only in x8 CBus mode
Port 0 (CSix Tx)	TXCLK01	Input	RXCDAT[6]; used only in x8 CBus mode
	TXENB[0]	Output	unused; no connect
	TXSOF[0]	Output	
	TXEOF[0]	Output	unused; no connect
	TXERR[0]	Output	unused; no connect
	TXPRTY[0]	Output	
	TXFA[0]	Input	unused; tie to ground
	TXPADL[1:0]	Output	unused; no connect
	TXDATA[31:0]	Output	
	TXPFA	Input	RXCDAT[5]; used only in x8 CBus mode
	TXSFA	Input	RXCDAT[4]; used only in x8 CBus mode
	TXADDR[3:0]	Output	unused; no connect

Table 13. 1x32 CSIX Mode (Continued)

Port	Master Pin Name	Direction	Notes
CBus Rx	RXCSOF	Input	
	RXCDAT[3:0]	Input	
	RXCPAR	Input	
	RXCSRB	Input	
	RXCFC	Output	

Table 14. x16 UTOPIA Level 2 MPHY-32 + x16 SPHY (UTOPIA or POS-PHY) Mode

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 3 (unused)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[3]	Output	unused; no connect	unused, no connect
	RXSOF[3]	Input	unused; tie to ground	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground	unused; tie to ground
Port 2 (SPHY)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[2]	Output	RXENB[2]	TXFA[2]
	RXSOF[2]	Input	RXSOF[2]	TXSOF[2]
	RXEOF[2]	Input	RXEOF[2]	TXEOF[2]
	RXVAL[2]	Input	RXVAL[2]	TXENB[2]
	RXERR[2]	Input	RXERR[2]	TXERR[2]
	RXPRTY[2]	Input	RXPRTY[2]	TXPRTY[2]
	RXFA[2]	Input	RXFA[2]	unused; tie to ground
	RXPADL[1]	Input	RXPADL[1]	TXPADL[1]
	RXDATA[31:16]	Input	RXDATA[31:16]	TXDATA[31:16]
Port 1 (unused)	RXCLK01	Input	RXCLK01	TXCLK01
	RXSOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground	unused; tie to ground

Table 14. x16 UTOPIA Level 2 MPHY-32 + x16 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 0 (MPHY)	RXCLK01	Input	RXCLK01	MPHY slave mode is not supported
	RXENB[0]	Output	RXENB[0]	
	RXSOF[0]	Input	RXSOF[0]	
	RXEOF[0]	Input	unused, tie to ground	
	RXVAL[0]	Input	unused; tie to ground	
	RXERR[0]	Input	unused, tie to ground	
	RXPRTY[0]	Input	RXPRTY[0]	
	RXFA[0]	Input	unused, tie to ground	
	RXPADL[0]	Input	unused, tie to ground	
	RXDATA[15:0]	Input	RXDATA[15:0]	
	TXCSRB	Output	RXADDR[4]	
	RXADDR[3:0]	Output	RXADDR[3:0]	
	RXPFA	Input	RXPFA	
Port 3 (unused)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[3]	Output	unused; no connect	unused; no connect
	TXSOF[3]	Output	unused; no connect	unused; no connect
	TXEOF[3]	Output	unused; no connect	unused; no connect
	TXERR[3]	Output	unused; no connect	unused; no connect
	TXPRTY[3]	Output	unused; no connect	unused; no connect
	TXFA[3]	Input	unused; tie to ground	unused; tie to ground
Port 2 (SPHY)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[2]	Output	TXENB[2]	RXVAL[2]
	TXSOF[2]	Output	TXSOF[2]	RXSOF[2]
	TXEOF[2]	Output	TXEOF[2]	RXEOF[2]
	TXERR[2]	Output	TXERR[2]	RXERR[2]
	TXPRTY[2]	Output	TXPRTY[2]	RXPRTY[2]
	TXFA[2]	Input	TXFA[2]	RXENB[2]
	TXPADL[1]	Output	TXPADL[1]	RXPADL[1]
	TXDATA[31:16]	Output	TXDATA[31:16]	RXDATA[31:16]
Port 1 (unused)	TXCLK01	Input	TXCLK01	RXCLK01
	TXSOF[1]	Output	unused; no connect	unused; no connect
	TXEOF[1]	Output	unused; no connect	unused; no connect
	TXERR[1]	Output	unused; no connect	unused; no connect
	TXPRTY[1]	Output	unused; no connect	unused; no connect
	TXFA[1]	Input	unused; tie to ground	unused; tie to ground

Table 14. x16 UTOPIA Level 2 MPHY-32 + x16 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 0 (MPHY)	TXCLK01	Input	TXCLK01	MPHY slave mode is not supported
	TXENB[0]	Output	TXENB[0]	
	TXSOF[0]	Output	TXSOF[0]	
	TXEOF[0]	Output	unused; no connect	
	TXERR[0]	Output	unused; no connect	
	TXPRTY[0]	Output	TXPRTY[0]	
	TXFA[0]	Input	unused; tie to ground	
	TXPADL[0]	Output	unused; no connect	
	TXDATA[15:0]	Output	TXDATA[15:0]	
	TXPFA	Input	TXPFA	
	TXSFA	Input	unused; no connect	
	TXENB[1]	Output	TXADDR[4]	
	TXADDR[3:0]	Output	TXADDR[3:0]	

Table 15. x16 UTOPIA Level 2 MPHY-32 + 2x8 SPHY (UTOPIA or POS-PHY) Mode

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 3 (SPHY)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[3]	Output	RXENB[3]	TXFA[3]
	RXSOF[3]	Input	RXSOF[3]	TXSOF[3]
	RXEOF[3]	Input	RXEOF[3]	TXEOF[3]
	RXVAL[3]	Input	RXVAL[3]	TXENB[3]
	RXERR[3]	Input	RXERR[3]	TXERR[3]
	RXPRTY[3]	Input	RXPRTY[3]	TXPRTY[3]
	RXFA[3]	Input	RXFA[3]	unused; tie to ground
	RXDATA[31:24]	Input	RXDATA[31:24]	TXDATA[31:24]

Table 15. x16 UTOPIA Level 2 MPHY-32 + 2x8 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 2 (SPHY)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[2]	Output	RXENB[2]	TXFA[2]
	RXSOF[2]	Input	RXSOF[2]	TXSOF[2]
	RXEOF[2]	Input	RXEOF[2]	TXEOF[2]
	RXVAL[2]	Input	RXVAL[2]	TXENB[2]
	RXERR[2]	Input	RXERR[2]	TXERR[2]
	RXPRTY[2]	Input	RXPRTY[2]	TXPRTY[2]
	RXFA[2]	Input	RXFA[2]	unused; tie to ground
	RXPADL[1]	Input	unused; tie to ground	unused; tie to ground
	RXDATA[23:16]	Input	RXDATA[23:16]	TXDATA[23:16]
Port 1 (unused)	RXCLK01	Input	RXCLK01	TXCLK01
	RXSOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground	unused; tie to ground
Port 0 (MPHY)	RXCLK01	Input	RXCLK01	MPHY slave mode is not supported
	RXENB[0]	Output	RXENB[0]	
	RXSOF[0]	Input	RXSOF[0]	
	RXEOF[0]	Input	unused, tie to ground	
	RXVAL[0]	Input	unused; tie to ground	
	RXERR[0]	Input	unused, tie to ground	
	RXPRTY[0]	Input	RXPRTY[0]	
	RXFA[0]	Input	unused, tie to ground	
	RXPADL[0]	Input	unused, tie to ground	
	RXDATA[15:0]	Input	RXDATA[15:0]	
	TXCSRB	Output	RXADDR[4]	
	RXADDR[3:0]	Output	RXADDR[3:0]	
	RXPFA	Input	RXPFA	

Table 15. x16 UTOPIA Level 2 MPHY-32 + 2x8 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 3 (SPHY)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[3]	Output	TXENB[3]	RXVAL[3]
	TXSOF[3]	Output	TXSOF[3]	RXSOF[3]
	TXEOF[3]	Output	TXEOF[3]	RXEOF[3]
	TXERR[3]	Output	TXERR[3]	RXERR[3]
	TXPRTY[3]	Output	TXPRTY[3]	RXPRTY[3]
	TXFA[3]	Input	TXFA[3]	RXENB[3]
	TXDATA[31:24]	Output	TXDATA[31:24]	RXDATA[31:24]
Port 2 (SPHY)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[2]	Output	TXENB[2]	RXVAL[2]
	TXSOF[2]	Output	TXSOF[2]	RXSOF[2]
	TXEOF[2]	Output	TXEOF[2]	RXEOF[2]
	TXERR[2]	Output	TXERR[2]	RXERR[2]
	TXPRTY[2]	Output	TXPRTY[2]	RXPRTY[2]
	TXFA[2]	Input	TXFA[2]	RXENB[2]
	TXPADL[1]	Output	unused; tie to ground	unused; tie to ground
	TXDATA[23:16]	Output	TXDATA[23:16]	RXDATA[23:16]
Port 1 (unused)	TXCLK01	Input	TXCLK01	RXCLK01
	TXSOF[1]	Output	unused; no connect	unused; no connect
	TXEOF[1]	Output	unused; no connect	unused; no connect
	TXERR[1]	Output	unused; no connect	unused; no connect
	TXPRTY[1]	Output	unused; no connect	unused; no connect
	TXFA[1]	Input	unused; tie to ground	unused; tie to ground
Port 0 (MPHY)	TXCLK01	Input	TXCLK01	MPHY slave mode is not supported
	TXENB[0]	Output	TXENB[0]	
	TXSOF[0]	Output	TXSOF[0]	
	TXEOF[0]	Output	unused; no connect	
	TXERR[0]	Output	unused; no connect	
	TXPRTY[0]	Output	TXPRTY[0]	
	TXFA[0]	Input	unused; tie to ground	
	TXPADL[0]	Output	unused; no connect	
	TXDATA[15:0]	Output	TXDATA[15:0]	
	TXPFA	Input	TXPFA	
	TXSFA	Input	unused; no connect	
	TXENB[1]	Output	TXADDR[4]	
	TXADDR[3:0]	Output	TXADDR[3:0]	

Table 16. x16 POS-PHY Level 2 MPHY-32 + x16 SPHY (UTOPIA or POS-PHY) Mode

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 3 (unused)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[3]	Output	unused; no connect	unused, no connect
	RXSOF[3]	Input	unused; tie to ground	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground	unused; tie to ground
Port 2 (SPHY)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[2]	Output	RXENB[2]	TXFA[2]
	RXSOF[2]	Input	RXSOF[2]	TXSOF[2]
	RXEOF[2]	Input	RXEOF[2]	TXEOF[2]
	RXVAL[2]	Input	RXVAL[2]	TXENB[2]
	RXERR[2]	Input	RXERR[2]	TXERR[2]
	RXPRTY[2]	Input	RXPRTY[2]	TXPRTY[2]
	RXFA[2]	Input	RXFA[2]	unused; tie to ground
	RXPADL[1]	Input	RXPADL[1]	TXPADL[1]
	RXDATA[31:16]	Input	RXDATA[31:16]	TXDATA[31:16]
Port 1 (unused)	RXCLK01	Input	RXCLK01	TXCLK01
	RXSOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground	unused; tie to ground

Table 16. x16 POS-PHY Level 2 MPHY-32 + x16 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 0 (MPHY)	RXCLK01	Input	RXCLK01	MPHY slave mode is not supported
	RXENB[0]	Output	RXENB[0]	
	RXSOF[0]	Input	RXSOF[0]	
	RXEOF[0]	Input	RXEOF[0]	
	RXVAL[0]	Input	RXVAL[0]	
	RXERR[0]	Input	RXERR[0]	
	RXPRTY[0]	Input	RXPRTY[0]	
	RXFA[0]	Input	unused, tie to ground	
	RXPADL[0]	Input	RXPADL[0]	
	RXDATA[15:0]	Input	RXDATA[15:0]	
	TXCSRB	Output	RXADDR[4]	
	RXADDR[3:0]	Output	RXADDR[3:0]	
	RXPFA	Input	RXPFA	
Port 3 (unused)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[3]	Output	unused; no connect	unused; no connect
	TXSOF[3]	Output	unused; no connect	unused; no connect
	TXEOF[3]	Output	unused; no connect	unused; no connect
	TXERR[3]	Output	unused; no connect	unused; no connect
	TXPRTY[3]	Output	unused; no connect	unused; no connect
	TXFA[3]	Input	unused; tie to ground	unused; tie to ground
Port 2 (SPHY)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[2]	Output	TXENB[2]	RXVAL[2]
	TXSOF[2]	Output	TXSOF[2]	RXSOF[2]
	TXEOF[2]	Output	TXEOF[2]	RXEOF[2]
	TXERR[2]	Output	TXERR[2]	RXERR[2]
	TXPRTY[2]	Output	TXPRTY[2]	RXPRTY[2]
	TXFA[2]	Input	TXFA[2]	RXENB[2]
	TXPADL[1]	Output	TXPADL[1]	RXPADL[1]
	TXDATA[31:16]	Output	TXDATA[31:16]	RXDATA[31:16]
Port 1 (unused)	TXCLK01	Input	TXCLK01	RXCLK01
	TXSOF[1]	Output	unused; no connect	unused; no connect
	TXEOF[1]	Output	unused; no connect	unused; no connect
	TXERR[1]	Output	unused; no connect	unused; no connect
	TXPRTY[1]	Output	unused; no connect	unused; no connect
	TXFA[1]	Input	unused; tie to ground	unused; tie to ground

Table 16. x16 POS-PHY Level 2 MPHY-32 + x16 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 0 (MPHY)	TXCLK01	Input	TXCLK01	MPHY slave mode is not supported
	TXENB[0]	Output	TXENB[0]	
	TXSOF[0]	Output	TXSOF[0]	
	TXEOF[0]	Output	TXEOF[0]	
	TXERR[0]	Output	TXERR[0]	
	TXPRTY[0]	Output	TXPRTY[0]	
	TXFA[0]	Input	unused; tie to ground	
	TXPADL[0]	Output	TXPADL[0]	
	TXDATA[15:0]	Output	TXDATA[15:0]	
	TXPFA	Input	TXPFA	
	TXSFA	Input	TXSFA	
	TXENB[1]	Output	TXADDR[4]	
	TXADDR[3:0]	Output	TXADDR[3:0]	

Table 17. x16 POS-PHY Level 2 MPHY-32 + 2x8 SPHY (UTOPIA or POS-PHY) Mode

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 3 (SPHY)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[3]	Output	RXENB[3]	TXFA[3]
	RXSOF[3]	Input	RXSOF[3]	TXSOF[3]
	RXEOF[3]	Input	RXEOF[3]	TXEOF[3]
	RXVAL[3]	Input	RXVAL[3]	TXENB[3]
	RXERR[3]	Input	RXERR[3]	TXERR[3]
	RXPRTY[3]	Input	RXPRTY[3]	TXPRTY[3]
	RXFA[3]	Input	RXFA[3]	unused; tie to ground
	RXDATA[31:24]	Input	RXDATA[31:24]	TXDATA[31:24]

Table 17. x16 POS-PHY Level 2 MPHY-32 + 2x8 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 2 (SPHY)	RXCLK23	Input	RXCLK23	TXCLK23
	RXENB[2]	Output	RXENB[2]	TXFA[2]
	RXSOF[2]	Input	RXSOF[2]	TXSOF[2]
	RXEOF[2]	Input	RXEOF[2]	TXEOF[2]
	RXVAL[2]	Input	RXVAL[2]	TXENB[2]
	RXERR[2]	Input	RXERR[2]	TXERR[2]
	RXPRTY[2]	Input	RXPRTY[2]	TXPRTY[2]
	RXFA[2]	Input	RXFA[2]	unused; tie to ground
	RXPADL[1]	Input	unused; tie to ground	unused; tie to ground
	RXDATA[23:16]	Input	RXDATA[23:16]	TXDATA[23:16]
Port 1 (unused)	RXCLK01	Input	RXCLK01	TXCLK01
	RXSOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground	unused; tie to ground
Port 0 (MPHY)	RXCLK01	Input	RXCLK01	MPHY slave mode is not supported
	RXENB[0]	Output	RXENB[0]	
	RXSOF[0]	Input	RXSOF[0]	
	RXEOF[0]	Input	RXEOF[0]	
	RXVAL[0]	Input	RXVAL[0]	
	RXERR[0]	Input	RXERR[0]	
	RXPRTY[0]	Input	RXPRTY[0]	
	RXFA[0]	Input	unused, tie to ground	
	RXPADL[0]	Input	RXPADL[0]	
	RXDATA[15:0]	Input	RXDATA[15:0]	
	TXCSRB	Output	RXADDR[4]	
	RXADDR[3:0]	Output	RXADDR[3:0]	
	RXPFA	Input	RXPFA	

Table 17. x16 POS-PHY Level 2 MPHY-32 + 2x8 SPHY (UTOPIA or POS-PHY) Mode (Continued)

Port	Pin Name	Direction	Master Mode Function and Description	Slave Mode Function and Description
Port 3 (SPHY)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[3]	Output	TXENB[3]	RXVAL[3]
	TXSOF[3]	Output	TXSOF[3]	RXSOF[3]
	TXEOF[3]	Output	TXEOF[3]	RXEOF[3]
	TXERR[3]	Output	TXERR[3]	RXERR[3]
	TXPRTY[3]	Output	TXPRTY[3]	RXPRTY[3]
	TXFA[3]	Input	TXFA[3]	RXENB[3]
	TXDATA[31:24]	Output	TXDATA[31:24]	RXDATA[31:24]
Port 2 (SPHY)	TXCLK23	Input	TXCLK23	RXCLK23
	TXENB[2]	Output	TXENB[2]	RXVAL[2]
	TXSOF[2]	Output	TXSOF[2]	RXSOF[2]
	TXEOF[2]	Output	TXEOF[2]	RXEOF[2]
	TXERR[2]	Output	TXERR[2]	RXERR[2]
	TXPRTY[2]	Output	TXPRTY[2]	RXPRTY[2]
	TXFA[2]	Input	TXFA[2]	RXENB[2]
	TXPADL[1]	Output	unused; tie to ground	unused; tie to ground
	TXDATA[23:16]	Output	TXDATA[23:16]	RXDATA[23:16]
Port 1 (unused)	TXCLK01	Input	TXCLK01	RXCLK01
	TXSOF[1]	Output	unused; no connect	unused; no connect
	TXEOF[1]	Output	unused; no connect	unused; no connect
	TXERR[1]	Output	unused; no connect	unused; no connect
	TXPRTY[1]	Output	unused; no connect	unused; no connect
	TXFA[1]	Input	unused; tie to ground	unused; tie to ground
Port 0 (MPHY)	TXCLK01	Input	TXCLK01	MPHY slave mode is not supported
	TXENB[0]	Output	TXENB[0]	
	TXSOF[0]	Output	TXSOF[0]	
	TXEOF[0]	Output	TXEOF[0]	
	TXERR[0]	Output	TXERR[0]	
	TXPRTY[0]	Output	TXPRTY[0]	
	TXFA[0]	Input	unused; tie to ground	
	TXPADL[0]	Output	TXPADL[0]	
	TXDATA[15:0]	Output	TXDATA[15:0]	
	TXPFA	Input	TXPFA	
	TXSFA	Input	TXSFA	
	TXENB[1]	Output	TXADDR[4]	
	TXADDR[3:0]	Output	TXADDR[3:0]	

Table 18. 1x32 SPHY Slave Mode

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground
Port 2 (unused)	RXCLK23	Input	unused; tie to ground
	RXENB[2]	Output	unused; no connect
	RXSOF[2]	Input	unused; tie to ground
	RXEOF[2]	Input	unused; tie to ground
	RXVAL[2]	Input	unused; tie to ground
	RXERR[2]	Input	unused; tie to ground
	RXPRTY[2]	Input	unused; tie to ground
	RXFA[2]	Input	unused; tie to ground
Port 1 (unused)	RXCLK01	Input	TXCLK01
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0	RXCLK01	Input	TXCLK01
	RXENB[0]	Output	TXFA[0]
	RXSOF[0]	Input	TXSOF[0]
	RXEOF[0]	Input	TXEOF[0]
	RXVAL[0]	Input	TXENB[0]
	RXERR[0]	Input	TXERR[0]
	RXPRTY[0]	Input	TXPRTY[0]
	RXFA[0]	Input	unused; tie to ground
	RXDATA[31:0]	Input	TXDATA[31:0]
	RXPADL[1:0]	Input	TXPADL[1:0]
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground

Table 18. 1x32 SPHY Slave Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	unused; tie to ground
Port 2 (unused)	TXCLK23	Input	unused; tie to ground
	TXENB[2]	Output	unused; no connect
	TXSOF[2]	Output	unused; no connect
	TXEOF[2]	Output	unused; no connect
	TXERR[2]	Output	unused; no connect
	TXPRTY[2]	Output	unused; no connect
	TXFA[2]	Input	unused; tie to ground
Port 1 (unused)	TXCLK01	Input	RXCLK01
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	unused; tie to ground
Port 0	TXCLK01	Input	RXCLK01
	TXENB[0]	Output	RXVAL[0]
	TXSOF[0]	Output	RXSOF[0]
	TXEOF[0]	Output	RXEOF[0]
	TXERR[0]	Output	RXERR[0]
	TXPRTY[0]	Output	RXPRTY[0]
	TXFA[0]	Input	RXENB[0]
	TXPADL[1:0]	Output	RXPADL[1:0]
	TXDATA[31:0]	Output	RXDATA[31:0]
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 19. 2x16 SPHY Slave Mode

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3 (unused)	RXCLK23	Input	TXCLK23
	RXENB[3]	Output	unused; no connect
	RXSOF[3]	Input	unused; tie to ground
	RXEOF[3]	Input	unused; tie to ground
	RXVAL[3]	Input	unused; tie to ground
	RXERR[3]	Input	unused; tie to ground
	RXPRTY[3]	Input	unused; tie to ground
	RXFA[3]	Input	unused; tie to ground
Port 2	RXCLK23	Input	TXCLK23
	RXENB[2]	Output	TXFA[2]
	RXSOF[2]	Input	TXSOF[2]
	RXEOF[2]	Input	TXEOF[2]
	RXVAL[2]	Input	TXENB[2]
	RXERR[2]	Input	TXERR[2]
	RXPRTY[2]	Input	TXPRTY[2]
	RXFA[2]	Input	unused; tie to ground
	RXPADL[1]	Input	TXPADL[1]; Port 2
	RXDATA[31:16]	Input	TXDATA[31:16]; Port 2 transmit data
Port 1	RXCLK01	Input	TXCLK01
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0	RXCLK01	Input	TXCLK01
	RXENB[0]	Output	TXFA[0]
	RXSOF[0]	Input	TXSOF[0]
	RXEOF[0]	Input	TXEOF[0]
	RXVAL[0]	Input	TXENB[0]
	RXERR[0]	Input	TXERR[0]
	RXPRTY[0]	Input	TXPRTY[0]
	RXFA[0]	Input	unused; tie to ground
	RXPADL[0]	Input	TXPADL[0]; Port 0
	RXDATA[15:0]	Input	TXDATA[15:0]; Port 0 transmit data

Table 19. 2x16 SPHY Slave Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground
Port 3 (unused)	TXCLK23	Input	RXCLK23
	TXENB[3]	Output	unused; no connect
	TXSOF[3]	Output	unused; no connect
	TXEOF[3]	Output	unused; no connect
	TXERR[3]	Output	unused; no connect
	TXPRTY[3]	Output	unused; no connect
	TXFA[3]	Input	unused; tie to ground
Port 2	TXCLK23	Input	RXCLK23
	TXENB[2]	Output	RXVAL[2]
	TXSOF[2]	Output	RXSOF[2]
	TXEOF[2]	Output	RXEOF[2]
	TXERR[2]	Output	RXERR[2]
	TXPRTY[2]	Output	RXPRTY[2]
	TXFA[2]	Input	RXENB[2]
	TXPADL[1]	Output	RXPADL[1]; Port 2
	TXDATA[31:16]	Output	RXDATA[31:16]; Port 2 receive data
Port 1 (unused)	TXCLK01	Input	RXCLK01
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	unused; tie to ground
Port 0	TXCLK01	Input	RXCLK01
	TXENB[0]	Output	RXVAL[0]
	TXSOF[0]	Output	RXSOF[0]
	TXEOF[0]	Output	RXEOF[0]
	TXERR[0]	Output	RXERR[0]
	TXPRTY[0]	Output	RXPRTY[0]
	TXFA[0]	Input	RXENB[0]
	TXPADL[0]	Output	RXPADL[0]; Port 0
	TXDATA[15:0]	Output	RXDATA[15:0]; Port 0 receive data
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 20. 4x8 SPHY Slave Mode

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3	RXCLK23	Input	TXCLK23
	RXENB[3]	Output	TXFA[3]
	RXSOF[3]	Input	TXSOF[3]
	RXEOF[3]	Input	TXEOF[3]
	RXVAL[3]	Input	TXENB[3]
	RXERR[3]	Input	TXERR[3]
	RXPRTY[3]	Input	TXPRTY[3]
	RXFA[3]	Input	unused; tie to ground
	RXDATA[31:24]	Input	TXDATA[31:24]; Port 3 transmit data
Port 2	RXCLK23	Input	TXCLK23
	RXENB[2]	Output	TXFA[2]
	RXSOF[2]	Input	TXSOF[2]
	RXEOF[2]	Input	TXEOF[2]
	RXVAL[2]	Input	TXENB[2]
	RXERR[2]	Input	TXERR[2]
	RXPRTY[2]	Input	TXPRTY[2]
	RXFA[2]	Input	unused; tie to ground
	RXPADL[1]	Input	unused; tie to ground
	RXDATA[23:16]	Input	TXDATA[23:16]; Port 2 transmit data
Port 1	RXCLK01	Input	TXCLK01
	RXENB[1]	Output	TXFA[3]
	RXSOF[1]	Input	TXSOF[1]
	RXEOF[1]	Input	TXEOF[1]
	RXVAL[1]	Input	TXENB[1]
	RXERR[1]	Input	TXERR[1]
	RXPRTY[1]	Input	TXPRTY[1]
	RXFA[1]	Input	unused; tie to ground
	RXDATA[15:8]	Input	TXDATA[15:8]; Port 1 transmit data

Table 20. 4x8 SPHY Slave Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 0	RXCLK01	Input	TXCLK01
	RXENB[0]	Output	TXFA[0]
	RXSOF[0]	Input	TXSOF[0]
	RXEOF[0]	Input	TXEOF[0]
	RXVAL[0]	Input	TXENB[0]
	RXERR[0]	Input	TXERR[0]
	RXPRTY[0]	Input	TXPRTY[0]
	RXFA[0]	Input	unused; tie to ground
	RXPADL[0]	Input	unused; tie to ground
	RXDATA[7:0]	Input	TXDATA[7:0]; Port 0 transmit data
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground
Port 3	TXCLK23	Input	RXCLK23
	TXENB[3]	Output	RXVAL[3]
	TXSOF[3]	Output	RXSOF[3]
	TXEOF[3]	Output	RXEOF[3]
	TXERR[3]	Output	RXERR[3]
	TXPRTY[3]	Output	RXPRTY[3]
	TXFA[3]	Input	RXENB[3]
	TXDATA[31:24]	Output	RXDATA[31:24]; Port 3 receive data
Port 2	TXCLK23	Input	RXCLK23
	TXENB[2]	Output	RXVAL[2]
	TXSOF[2]	Output	RXSOF[2]
	TXEOF[2]	Output	RXEOF[2]
	TXERR[2]	Output	RXERR[2]
	TXPRTY[2]	Output	RXPRTY[2]
	TXFA[2]	Input	RXENB[2]
	TXPADL[0]	Output	unused; no connect
	TXDATA[23:16]	Output	RXDATA[23:16]; Port 2 receive data
Port 1	TXCLK01	Input	RXCLK01
	TXENB[1]	Output	RXVAL[1]
	TXSOF[1]	Output	RXSOF[1]
	TXEOF[1]	Output	RXEOF[1]
	TXERR[1]	Output	RXERR[1]
	TXPRTY[1]	Output	RXPRTY[1]
	TXFA[1]	Input	RXENB[1]
	TXDATA[15:8]	Output	RXDATA[15:8]; Port 1 receive data

Table 20. 4x8 SPHY Slave Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 0	TXCLK01	Input	RXCLK01
	TXENB[0]	Output	RXVAL[0]
	TXSOF[0]	Output	RXSOF[0]
	TXEOF[0]	Output	RXEOF[0]
	TXERR[0]	Output	RXERR[0]
	TXPRTY[0]	Output	RXPRTY[0]
	TXFA[0]	Input	RXENB[0]
	TXPADL[0]	Output	unused; no connect
	TXDATA[7:0]	Output	RXDATA[7:0]; Port 0 receive data
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 21. 1x16+2x8 SPHY Slave Mode

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 3	RXCLK23	Input	TXCLK23
	RXENB[3]	Output	TXFA[3]
	RXSOF[3]	Input	TXSOF[3]
	RXEOF[3]	Input	TXEOF[3]
	RXVAL[3]	Input	TXENB[3]
	RXERR[3]	Input	TXERR[3]
	RXPRTY[3]	Input	TXPRTY[3]
	RXFA[3]	Input	unused; tie to ground
	RXDATA[31:24]	Input	TXDATA[31:24]; Port 3 transmit data
Port 2	RXCLK23	Input	TXCLK23
	RXENB[2]	Output	TXFA[2]
	RXSOF[2]	Input	TXSOF[2]
	RXEOF[2]	Input	TXEOF[2]
	RXVAL[2]	Input	TXENB[2]
	RXERR[2]	Input	TXERR[2]
	RXPRTY[2]	Input	TXPRTY[2]
	RXFA[2]	Input	unused; tie to ground
	RXPADL[1]	Input	unused; tie to ground
	RXDATA[23:16]	Input	TXDATA[23:16]; Port 2 transmit data

Table 21. 1x16+2x8 SPHY Slave Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 1 (unused)	RXCLK01	Input	TXCLK01
	RXENB[1]	Output	unused; no connect
	RXSOF[1]	Input	unused; tie to ground
	RXEOF[1]	Input	unused; tie to ground
	RXVAL[1]	Input	unused; tie to ground
	RXERR[1]	Input	unused; tie to ground
	RXPRTY[1]	Input	unused; tie to ground
	RXFA[1]	Input	unused; tie to ground
Port 0	RXCLK01	Input	TXCLK01
	RXENB[0]	Output	TXFA[0]
	RXSOF[0]	Input	TXSOF[0]
	RXEOF[0]	Input	TXEOF[0]
	RXVAL[0]	Input	TXENB[0]
	RXERR[0]	Input	TXERR[0]
	RXPRTY[0]	Input	TXPRTY[0]
	RXFA[0]	Input	unused; tie to ground
	RXPADL[0]	Input	TXPADL[0]; Port 0
	RXDATA[15:0]	Input	TXDATA[15:0]; Port 0 transmit data
MPHY (unused)	RXADDR[3:0]	Output	unused; no connect
	RXPFA	Input	unused; tie to ground
Port 3	TXCLK23	Input	RXCLK23
	TXENB[3]	Output	RXVAL[3]
	TXSOF[3]	Output	RXSOF[3]
	TXEOF[3]	Output	RXEOF[3]
	TXERR[3]	Output	RXERR[3]
	TXPRTY[3]	Output	RXPRTY[3]
	TXFA[3]	Input	RXENB[3]
	TXDATA[31:24]	Output	RXDATA[31:24]; Port 3 receive data
Port 2	TXCLK23	Input	RXCLK23
	TXENB[2]	Output	RXVAL[2]
	TXSOF[2]	Output	RXSOF[2]
	TXEOF[2]	Output	RXEOF[2]
	TXERR[2]	Output	RXERR[2]
	TXPRTY[2]	Output	RXPRTY[2]
	TXFA[2]	Input	RXENB[2]
	TXPADL[1]	Output	unused; no connect
	TXDATA[23:16]	Output	RXDATA[23:16]; Port 2 receive data

Table 21. 1x16+2x8 SPHY Slave Mode (Continued)

Port	Master Pin Name	Direction	Slave Mode Function and Description
Port 1 (unused)	TXCLK01	Input	RXCLK01
	TXENB[1]	Output	unused; no connect
	TXSOF[1]	Output	unused; no connect
	TXEOF[1]	Output	unused; no connect
	TXERR[1]	Output	unused; no connect
	TXPRTY[1]	Output	unused; no connect
	TXFA[1]	Input	unused; tie to ground
Port 0	TXCLK01	Input	RXCLK01
	TXENB[0]	Output	RXVAL[0]
	TXSOF[0]	Output	RXSOF[0]
	TXEOF[0]	Output	RXEOF[0]
	TXERR[0]	Output	RXERR[0]
	TXPRTY[0]	Output	RXPRTY[0]
	TXFA[0]	Input	RXENB[0]
	TXPADL[0]	Output	RXPADL[0]; Port 0
	TXDATA[15:0]	Output	RXDATA[31:0]; Port 0 receive data
MPHY (unused)	TXPFA	Input	unused; tie to ground
	TXSFA	Input	unused; tie to ground
	TXADDR[3:0]	Output	unused; no connect

Table 22. CBus Pinout

Pin Name	Direction	Description
TXCDATA[3:0]	Output	Transmit data
TXCDATA[7:4]	Output	Additonal 4 bits to double the CBUS width, these pins are muxed on RXADDR[3:0] as shown in Table 13.
TXCSOF	Output	Transmit Start Of Frame
TXCSRB	Output	Transmit Serialized Ready Bits
TXCFC	Input	Transmit Flow Control FIFO Full
TXCPAR	Output	Transmit parity for TXCDATA[3:0]
RXCDATA[3:0]	Input	Receive data
RXCDATA[7:4]	Input	Additonal 4 bits to double the CBUS width, these pins are muxed on TXFA[1], TXFA[0], TXPFA, TXSFA respectively as shown in Table 13.
RXCSOF	Input	Receive Start Of Frame
RXCSRB	Input	Receive Serialized Ready Bits
RXCFC	Output	Receive Flow Control FIFO Full
RXCPAR	Input	Receive parity

3.2.4 PCI

PCI Bus can be used to interface to industry-standard IO devices, or to a host processor. See Table 23 for a list of signals. PCI signaling levels are defined in PCI Rev. 2.2 specification.

Table 23. PCI Signals

Signal Name	I/O	Description	Number
PCI_CLK	I	Clock input for the PCI core clock domain (0 to 66 MHz)	1
PCI_AD[63:0]	IO	Multiplexed address/data bus	64
PCI_CBE_L[7:0]	IO	Command and byte enable bus	8
PCI_RST_L	IO	Active-low PCI reset signal. This is an output if IXP2400 is the bus host. It is an input if IXP2400 is not the bus host. The direction of this pin is controlled by the CFG_RSTDIR pin.	1
PCI_INTA_L	IO	Receives interrupt from another PCI device if the IXP2400 is the bus host; otherwise used as an interrupt to the host processor.	1
PCI_INTB_L	I	Receives interrupt from another PCI device if the IXP2400 is the bus host.	1
PCI_FRAME_L	IO	Transaction in progress indication	1
PCI_STOP_L	IO	Termination with retry or disconnect-with-data	1
PCI_IRDY_L	IO	Initiator ready on data phase	1
PCI_TRDY_L	IO	Target ready on data phase	1
PCI_DEVSEL_L	IO	Device select indication	1
PCI_IDSEL	I	IdSel signal to the IXP2400; used during the configuration cycle	1
PCI_REQ_L[0]	IO	Bus requests from external master 0, used when the IXP2400 is arbiter/host; the IXP2400's request output to external arbiter when not a host.	1
PCI_REQ_L[1]	I	Bus requests from external master 1, used when the IXP2400 is arbiter/host.	1
PCI_GNT_L[0]	IO	Bus grant output to external master 0 when this chip is arbiter/host; grant input to the IXP2400 from external arbiter when not a host.	1
PCI_GNT_L[1]	O	Bus grants to external master 1, used when the IXP2400 is arbiter/host	1
PCI_REQ64_L	IO	Indication that a 64-bit data phase is desired. During reset, driven low by the system to indicate 64-bit capability.	1
PCI_ACK64_L	IO	Indicates that a 64-bit data phase is accepted.	1
PCI_PAR	IO	Parity on AD[31:0]	1
PCI_PAR64	IO	Parity on AD[63:32]	1
PCI_PERR_L	IO	Parity error detected on incoming data	1
PCI_SERR_L	IO	Parity error on address phase, illegal command, etc. When this chip is the host SERR is an input; when using with an external host, SERR is an output.	1
PCI_RCOMP	I	Buffer Compensation[1]	1
Total (per channel)			93

1. The PCI_RCOMP pin should be connected to ground through external a 24Ω ±1% resistor and one 0603 0.1 µF decoupling capacitor. Place the resistor and capacitor as close to the IXP2400 as possible, within 1.0" of the package. The compensation signal should be routed with as wide a trace as possible, minimum of 12 mils wide and isolated from other signals with a minimum of 10-mil spacing.

3.2.5 SlowPort Signals

The SlowPort is used to interface to asynchronous devices. Typically this will be a Flash ROM (Boot ROM) and maintenance port of MAC devices. See Table 24.

Table 24. SlowPort Signals

Signal Name	I/O	Description	Number
SP_CLK[1]	O	This clock is used to time all the external SlowPort transfers. It can be adjusted by the CCR register. The CCR contains the clock divisor information. This clock is generated by dividing the SHXP_APB_CLK.	1
SP_WR_L	O	Write strobe to indicate the write access to the PROM bus.	1
SP_RD_L	O	Read strobe to indicate the read access from the PROM Bus.	1
SP_AD[7:0]	IO	Address and data multiplexed bidirectional tri-state bus.	8
SP_ACK_L	I	Acknowledge signal responded by the PROM devices when the transaction is complete.For special application, this pin acts as interrupt input from the external device.	1
SP_CS_L[1:0]	O	Device select signals to indicate which device will be addressed.	2
SP_ALE_L	O	Address latch enable signal to indicate the address is placed in the PROM Bus.	1
SP_CP_SP_A[0]	O	Latches consecutive bytes onto external buffers. Used for 16,32-bit data bus device only. Also acts as an address [0] signal during the mode 0 set in the protocol control register for 8-bit device transaction.	1
SP_OE_L	O	Shifts the bytes out of the external buffers.	1
SP_DIR_SP_A[1]	O	Controls the direction of the data transaction. For read, it is asserted low; For write, it is asserted high. Also acts as an address [1] signal during the mode 0 set in the protocol control register for the 8-bit device transaction.	1
Total (per channel)			18

1. SP_CLK can drive a maximum of two loads, 10 pF each.

3.2.6 GPIO Signals

GPIO are general-purpose IO signals. They can be used for slow-speed, software-controlled IO such as LEDs and input switches. They are also tri-stated during reset to bring configuration information into the IXP2400; this information is latched at the deassertion of reset. GPIOs use LVTTL signalling (3.3V); see Table 25.

Table 25. GPIO Signals

Signal Name	I/O	Description	Number
GPIO[7:0]	IO	General-purpose IO	8
Total (per channel)			8

3.2.7 Serial Port Signals

Serial port is the RS-232–compatible UART used for debug and diagnostics. See Table 26.

Table 26. Serial Port Signals

Signal Name	I/O	Description	Number
SERIAL_RX	I	Receive data into the UART	1
SERIAL_TX	O	Transmit data from the UART	1
Total (per channel)			2

3.2.8 Clock Signals

Table 27 lists the clock and reset signals.

Table 27. Clock Signals

Signal Name	I/O	Description	Number
SYS_CLK	I	System Clock This is the core PLL reference clock; nominally 100 MHz	1
SYS_RESET_L	I	System reset input If the IXP2400 is on an externally hosted PCI system this is connected to PCI_RST_L	1
SYS_RESET_OUT_L	O	Reset out IXP2400 output to reset the other board devices	1
Total (per channel)			3

3.2.9 Test, JTAG, and Miscellaneous Signals

JTAG is the IEEE 1149.1 test access port. The JTAG input signals have a weak pull-up resistor internal to the chip, so that any input not terminated will be interpreted as a high. Other test signals are IXP2400–specific for manufacturing use only. See Table 28.

Table 28. Test, JTAG, and Miscellaneous Signals

Signal Name	I/O	Description	Number
TCK	I	Test interface reference clock. This clock times all the transfers on the JTAG test interface.	1
TMS_T_CLK	I	When T_Load = 0 this pin functions as the JTAG Test Mode Select pin. When T_Load = 1 this pin functions as the test logic Test Clock, used to capture test mode data from GPIO and SlowPort pins into the Test Box.	1
TDI_T_SCAN_EN	I	When T_Load = 0 this pin functions as the JTAG Test Data In pin. When T_Load = 1 this pin functions as the test logic Scan Enable, configuring the internal flip-flops into scan chains.	1
TDO	O	Test interface data output. TDO is the serial output through which test instructions and data from the test logic leave the IXP2400.	1
TRST_L	I	Test interface reset. When asserted low, the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. This pin must be driven or held low to achieve normal device operation.	1
T_SYS_REFCLK	I	Test System Reference Clock (for debug only) This input is XOR'ed with SYS_CLK so that a 2x clock can be generated when the PLL is bypassed; for normal operation tie to GND.	1
T_LOAD	I	Test Load 1- Selects signals from the GPIO and SlowPort pins to be routed to the Test Box instead of the GPIO and SlowPort ports, and sets the TMS/T_CLK and TDI/T_SCAN_EN pins to operate in their test mode. 0 - These pins have their normal function.	1
T_DIAG_CLK	I	Memory BIST Diagnostic Clock This clock is used to shift out failing data from the memory BIST controllers during the debug mode.	1
THERMDA[1]	I	Thermal Diode Anode. If unused, this pin does not need to be connected.	1
THERMDC[1]	I	Thermal Diode Cathode. If unused, this pin does not need to be connected.	1
PLL_BYPASS	I	System PLL Bypass Select 0 - Use core PLL output as core clock 1 - Use SYS_CLK as core clock For normal operation, connect to 0.	1
PLL_DIV_BYPASS	I	PLL Divider Bypass 0 - Core PLL divider block is not bypassed In a system board this pin should be held low. If set high, the IXP2400 may not operate properly.	1
TST_RESET_L	I	Indicates that power has reached a certain level. Keep pulled-up for normal operation.	1
VCCA		Analog clock power	1
VSSA			1
VCC3_3		3.3 V I/O power	1

Table 28. Test, JTAG, and Miscellaneous Signals (Continued)

Signal Name	I/O	Description	Number
VCC2_5		2.5 V DDR I/O power	1
VCC1_5		1_5 V QDR I/O power	1
Total (per channel)			18

1. For these signals, the thermal equation used to convert voltage to temperature is:
   y = -551.225x + 410.694

For example, if the voltage is 0.53, then y = -551.225 * .53 + 410.694 = 118°C

3.2.10 Configuration Pins

These pins are tied statically high or low through a resistor to provide configuration information into the IXP2400 at reset. For all but CFG_RST_DIR, these pins are used for other purposes after reset. For those pins the configuration information is sampled at the deassertion edge of reset. The values sampled can be read in the Strap_Options Register.

Table 29. Configuration/GPIO Pins (Sheet 1 of 2)

Signal Name	I/O	Configuration Function	Description	Number
CFG_RSTDIR	IO	CFG_RST_DIR	• 1—IXP2400 is the host supporting central functions IXP2400 will drive PCI_RST_L (output). IXP2400 will drive PCI_REQ64_L low during PCI reset. IXP2400 will drive PCI_AD[31:0], PCI_BE[3:0] and PAR low during PCI reset • 0—There is an external PCI host supporting the central functions. PCI_RST_L is an input PCI_REQ64_L is an input during reset. PCI_AD[31:0], PCI_BE[3:0] and PCI_PAR are tristated during PCI reset.	1
GPIO[0]	IO	CFG_PROM_ BOOT	Indicates if Boot ROM is present • 0—No Boot ROM; host must download Boot image into DRAM • 1—Boot ROM is present	1
GPIO[1]	IO	CFG_PCI_BOOT_ HOST	Indicates if host or the Intel XScale core will configure PCI devices • 0— External Host • 1—IXP2400 Network Processor	1
GPIO[2]	IO	CFG_PCI_ARB	PCI Arbiter Used • 0—external arbiter • 1—internal arbiter	1
GPIO[4:3]	IO	CFG_PCI_ DWIN[1:0]	Select DRAM BAR Window Size • 11—1024 Mbyte • 10—512 Mbyte • 01—256 Mbyte • 00—128 Mbyte	2

Table 29. Configuration/GPIO Pins (Sheet 2 of 2)

Signal Name	I/O	Configuration Function	Description	Number
GPIO[6:5]	IO	CFG_PCI_ SWIN[1:0]	Select SRAM BAR Window Size • 11—64 Mbyte • 10—32 Mbyte • 01—16 Mbyte • 00— 8 Mbyte	2
GPIO[7]			Not Used	
Total (per channel)				8

3.2.11 Pin State During Reset

In addition to the configuration pins listed in Table 29, at the deassertion edge of the reset TST_RESET_L must always be tied high.

3.3 Power Supply Sequencing

3.3.1 Power-Up Sequence

The IXP2400 has the following power supplies:

1. VCC3.3 — 3.3V power supply for the Media Switch Fabric interface, PCI, GPIO, SlowPort and Misc.
2. VCC and VCCA — 1.3V power supply for the Core and for the PLL
3. VCC2.5 — 2.5V power supply for the DDR DRAM
4. VCC1.5 — 1.5V power supply for the QDR SRAM
5. D_Vref — 1.25V for the DDR DRAM
6. Sn_Vref — 0.75V for QDR SRAM channel 0, and channel 1

The power supplies for the IXP2400 should be brought up in a controlled sequence. The delay between the power-up of the power supplies should be 5 ms or less (min is 50 µs); there is no dependency between the sequence of the 1.5V and 2.5V power-on.

1. The 3.3V must be brought up before the1.3V
2. The 1.3V must be brought up before the 1.5V and 2.5V
3. The 1.5V must be brought up before or at the same time as the 0.75V
4. The 2.5V must be brought up before or at the same time as the 1.25V

3.3.2 Power-Down Sequence

All the power supplies should be brought down simultaneously. If the user cannot power down all the supplies simultaneously, the Power-down sequence is recommended to be the reverse order of the Power-up sequence shown in Section 3.3.1.

3.3.3 SlowPort Clock Behavior During Reset

In IXP2400 A0 silicon, when the SYS_RESET_L or the PCI_RST_L is asserted, the SP_CLK drives out the clock signal at the same frequency as the SYS_CLK, but 180 degrees out of phase with the SYS_CLK. After the de-assertion of both SYS_RESET_L (and PCI_RST_L if CFG_RSTDIR = 1), the SP_CLK will drive out the clock signal at half of the SYS_CLK frequency after approximately three SYS_CLK cycles, or at the programmed frequency.

3.3.4 Pullup/Pulldown and Unused Pin Guidelines

For normal (i.e., non-test mode) operation, terminate signals as follows:

Typical pullup/pulldown resistor values are in the range of 5-10 Kohms.

For unused QDR SRAM channels, the output pins can be left unconnected (no connect). The input pins need to be tied to ground with a 100-Kohm resistor. Similarly, for unused MSF channels, the output pins can be left unconnected (no connect); the input pins need to be tied to ground with a 100-Kohm resistor.

3.4 Ball Information

Figure 10. IXP2400 Network Processor Ball Map (bottom left side)

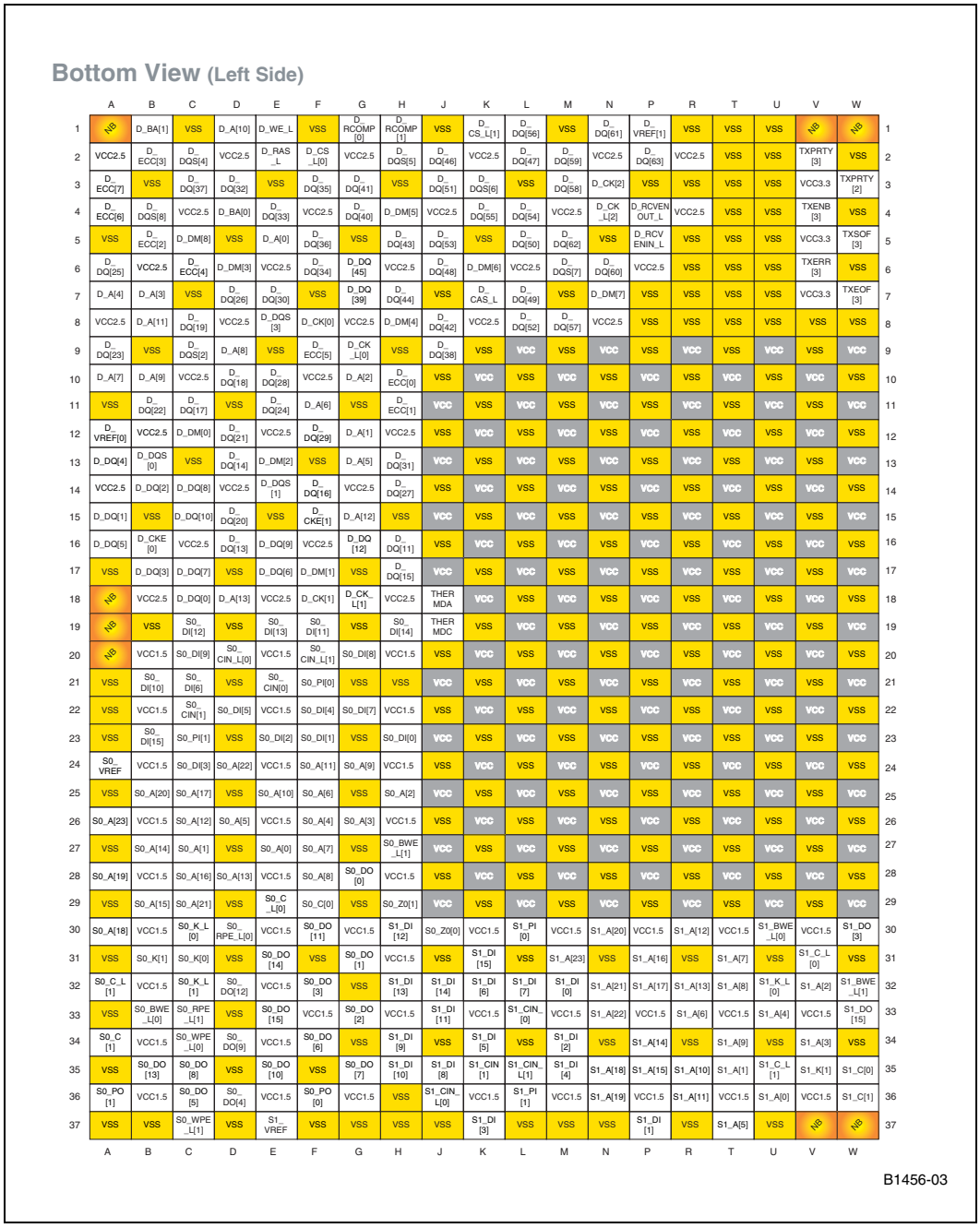
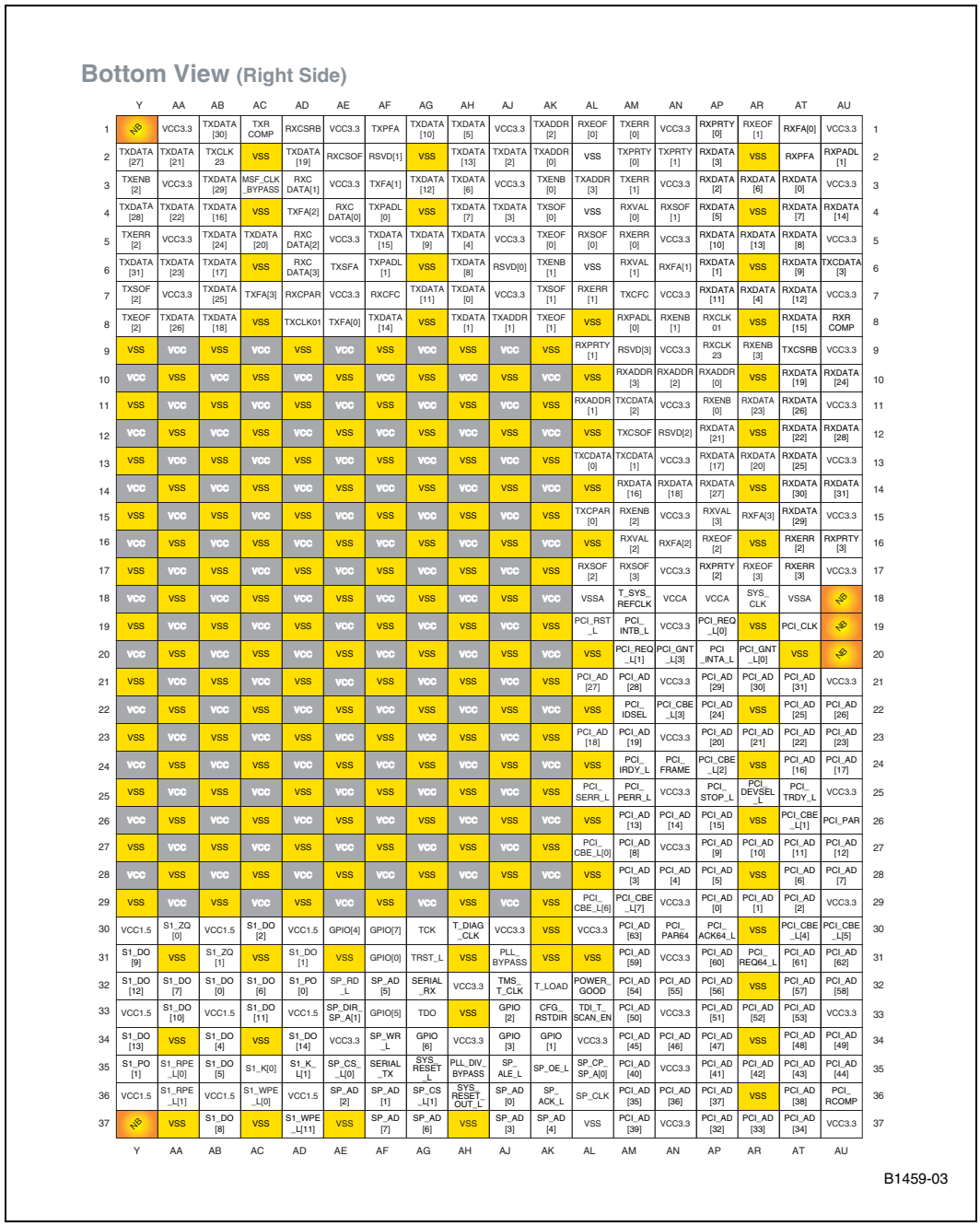


Figure 11. IXP2400 Network Processor Ball Map (bottom right side)



3.5 Ball List Tables

Table 30 defines the signal types on the ball list.

Table 30. IXP2400 Network Processor Signal-Type Abbreviations

Ball Abbreviation	Electrical	Description
VCC3.3	3.3Vdc	Power 3.3-volt supply for MSF, PCI and misc.
VCC2.5	2.5Vdc	Power 2.5-volt supply for DDR
VCC1.5	1.5Vdc	Power 1.5-volt supply for QDR
VCC	1.3Vdc	Power 1.3-volt supply for core
VSS	GND	Return for 3.3, 2.5, 1.5 and core supplies
VCCA	1.3Vdc	PLL power supply 1.3 volt
VSSA		See Figure 12 for connections.
	Three-state	Logic high, logic low or high impedance
PD		Pull-down required
OD	Open Drain	Pull-up required
DNC	None	Do not connect

3.5.1 Balls Listed in Alphanumeric Order by Signal Name

The following ball locations are not associated with a signal, therefore are not listed in Table 31: A1, Y1, W1, V1, Y37, W37, V37, AU[18:20], and A[18:20].

Table 31 shows the ball locations and signal names arranged in alphanumeric order by the signal name.

Table 31. Ball List in Alphanumeric Order by Signal Location

Signal Name	Ball Location
CFG_RSTDIR	AK33
D_A[0]	E5
D_A[1]	G12
D_A[10]	D1
D_A[11]	B8
D_A[12]	G15
D_A[13]	D18
D_A[2]	G10
D_A[3]	B7
D_A[4]	A7
D_A[5]	G13
D_A[6]	F11
D_A[7]	A10

Signal Name	Ball Location
D_A[8]	D9
D_A[9]	B10
D_BA[0]	D4
D_BA[1]	B1
D_CAS_L	K7
D_CK[0]	F8
D_CK[1]	F18
D_CK[2]	N3
D_CK_L[0]	G9
D_CK_L[1]	G18
D_CK_L[2]	N4
D_CKE[0]	B16
D_CKE[1]	F15

Signal Name	Ball Location
D_CS_L[0]	F2
D_CS_L[1]	K1
D_DM[0]	C12
D_DM[1]	F17
D_DM[2]	E13
D_DM[3]	D6
D_DM[4]	H8
D_DM[5]	H4
D_DM[6]	K6
D_DM[7]	N7
D_DM[8]	C5
D_DQ[0]	C18
D_DQ[1]	A15

Signal Name	Ball Location
D_DQ[10]	C15
D_DQ[11]	H16
D_DQ[12]	G16
D_DQ[13]	D16
D_DQ[14]	D13
D_DQ[15]	H17
D_DQ[16]	F14
D_DQ[17]	C11
D_DQ[18]	D10
D_DQ[19]	C8
D_DQ[2]	B14
D_DQ[20]	D15
D_DQ[21]	D12
D_DQ[22]	B11
D_DQ[23]	A9
D_DQ[24]	E11
D_DQ[25]	A6
D_DQ[26]	D7
D_DQ[27]	H14
D_DQ[28]	E10
D_DQ[29]	F12
D_DQ[3]	B17
D_DQ[30]	E7
D_DQ[31]	H13
D_DQ[32]	D3
D_DQ[33]	E4
D_DQ[34]	F6
D_DQ[35]	F3
D_DQ[36]	F5
D_DQ[37]	C3
D_DQ[38]	J9
D_DQ[39]	G7
D_DQ[4]	A13
D_DQ[40]	G4
D_DQ[41]	G3
D_DQ[42]	J8
D_DQ[43]	H5
D_DQ[44]	H7

Signal Name	Ball Location
D_DQ[45]	G6
D_DQ[46]	J2
D_DQ[47]	L2
D_DQ[48]	J6
D_DQ[49]	L7
D_DQ[5]	A16
D_DQ[50]	L5
D_DQ[51]	J3
D_DQ[52]	L8
D_DQ[53]	J5
D_DQ[54]	L4
D_DQ[55]	K4
D_DQ[56]	L1
D_DQ[57]	M8
D_DQ[58]	M3
D_DQ[59]	M2
D_DQ[6]	E17
D_DQ[60]	N6
D_DQ[61]	N1
D_DQ[62]	M5
D_DQ[63]	P2
D_DQ[7]	C17
D_DQ[8]	C14
D_DQ[9]	E16
D_DQS[0]	B13
D_DQS[1]	E14
D_DQS[2]	C9
D_DQS[3]	E8
D_DQS[4]	C2
D_DQS[5]	H2
D_DQS[6]	K3
D_DQS[7]	M6
D_DQS[8]	B4
D_ECC[0]	H10
D_ECC[1]	H11
D_ECC[2]	B5
D_ECC[3]	B2
D_ECC[4]	C6

Signal Name	Ball Location
D_ECC[5]	F9
D_ECC[6]	A4
D_ECC[7]	A3
D_RAS_L	E2
D_RCOMP[0]	G1
D_RCOMP[1]	H1
D_RCVENIN_L	P5
D_RCVENOUT_L	P4
D_VREF[0]	A12
D_VREF[1]	P1
D_WE_L	E1
GPIO[0]	AF31
GPIO[1]	AK34
GPIO[2]	AJ33
GPIO[3]	AJ34
GPIO[4]	AE30
GPIO[5]	AF33
GPIO[6]	AG34
GPIO[7]	AF30
MSF_CLK_BYPASS	AC3
PCI_ACK64_L	AP30
PCI_AD[0]	AP29
PCI_AD[1]	AR29
PCI_AD[10]	AR27
PCI_AD[11]	AT27
PCI_AD[12]	AU27
PCI_AD[13]	AM26
PCI_AD[14]	AN26
PCI_AD[15]	AP26
PCI_AD[16]	AT24
PCI_AD[17]	AU24
PCI_AD[18]	AL23
PCI_AD[19]	AM23
PCI_AD[2]	AT29
PCI_AD[20]	AP23
PCI_AD[21]	AR23
PCI_AD[22]	AT23
PCI_AD[23]	AU23

Signal Name	Ball Location
PCI_AD[24]	AP22
PCI_AD[25]	AT22
PCI_AD[26]	AU22
PCI_AD[27]	AL21
PCI_AD[28]	AM21
PCI_AD[29]	AP21
PCI_AD[3]	AM28
PCI_AD[30]	AR21
PCI_AD[31]	AT21
PCI_AD[32]	AP37
PCI_AD[33]	AR37
PCI_AD[34]	AT37
PCI_AD[35]	AM36
PCI_AD[36]	AN36
PCI_AD[37]	AP36
PCI_AD[38]	AT36
PCI_AD[39]	AM37
PCI_AD[4]	AN28
PCI_AD[40]	AM35
PCI_AD[41]	AP35
PCI_AD[42]	AR35
PCI_AD[43]	AT35
PCI_AD[44]	AU35
PCI_AD[45]	AM34
PCI_AD[46]	AN34
PCI_AD[47]	AP34
PCI_AD[48]	AT34
PCI_AD[49]	AU34
PCI_AD[5]	AP28
PCI_AD[50]	AM33
PCI_AD[51]	AP33
PCI_AD[52]	AR33
PCI_AD[53]	AT33
PCI_AD[54]	AM32
PCI_AD[55]	AN32
PCI_AD[56]	AP32
PCI_AD[57]	AT32
PCI_AD[58]	AU32

Signal Name	Ball Location
PCI_AD[59]	AM31
PCI_AD[6]	AT28
PCI_AD[60]	AP31
PCI_AD[61]	AT31
PCI_AD[62]	AU31
PCI_AD[63]	AM30
PCI_AD[7]	AU28
PCI_AD[8]	AM27
PCI_AD[9]	AP27
PCI_CBE_L[0]	AL27
PCI_CBE_L[1]	AT26
PCI_CBE_L[2]	AP24
PCI_CBE_L[3]	AN22
PCI_CBE_L[4]	AT30
PCI_CBE_L[5]	AU30
PCI_CBE_L[6]	AL29
PCI_CBE_L[7]	AM29
PCI_CLK	AT19
PCI_DEVSEL_L	AR25
PCI_FRAME_L	AN24
PCI_GNT_L[0]	AR20
PCI_GNT_L[1]	AN20
PCI_IDSEL	AM22
PCI_INTA_L	AP20
PCI_INTB_L	AM19
PCI_IRDY_L	AM24
PCI_PAR	AU26
PCI_PAR64	AN30
PCI_PERR_L	AM25
PCI_RCOMP	AU36
PCI_REQ_L[0]	AP19
PCI_REQ_L[1]	AM20
PCI_REQ64_L	AR31
PCI_RST_L	AL19
PCI_SERR_L	AL25
PCI_STOP_L	AP25
PCI_TRDY_L	AT25
PLL_BYPASS	AJ31

Signal Name	Ball Location
PLL_DIV_BYPASS	AH35
RSVD[0]	AJ6
RSVD[1]	AF2
RSVD[2]	AN12
RSVD[3]	AM9
RXADDR[0]	AP10
RXADDR[1]	AL11
RXADDR[2]	AN10
RXADDR[3]	AM10
RXCDATA[0]	AE4
RXCDATA[1]	AD3
RXCDATA[2]	AD5
RXCDATA[3]	AD6
RXCFC	AF7
RXCLK01	AP8
RXCLK23	AP9
RXCPAR	AD7
RXCSOF	AE2
RXCSRB	AD1
RXDATA[0]	AT3
RXDATA[1]	AP6
RXDATA[10]	AP5
RXDATA[11]	AP7
RXDATA[12]	AT7
RXDATA[13]	AR5
RXDATA[14]	AU4
RXDATA[15]	AT8
RXDATA[16]	AM14
RXDATA[17]	AP13
RXDATA[18]	AN14
RXDATA[19]	AT10
RXDATA[2]	AP3
RXDATA[20]	AR13
RXDATA[21]	AP12
RXDATA[22]	AT12
RXDATA[23]	AR11
RXDATA[24]	AU10
RXDATA[25]	AT13

Signal Name	Ball Location
RXDATA[26]	AT11
RXDATA[27]	AP14
RXDATA[28]	AU12
RXDATA[29]	AT15
RXDATA[3]	AP2
RXDATA[30]	AT14
RXDATA[31]	AU14
RXDATA[4]	AR7
RXDATA[5]	AP4
RXDATA[6]	AR3
RXDATA[7]	AT4
RXDATA[8]	AT5
RXDATA[9]	AT6
RXENB[0]	AP11
RXENB[1]	AN8
RXENB[2]	AM15
RXENB[3]	AR9
RXEOF[0]	AL1
RXEOF[1]	AR1
RXEOF[2]	AP16
RXEOF[3]	AR17
RXERR[0]	AM5
RXERR[1]	AL7
RXERR[2]	AT16
RXERR[3]	AT17
RXFA[0]	AT1
RXFA[1]	AN6
RXFA[2]	AN16
RXFA[3]	AR15
RXPADL[0]	AM8
RXPADL[1]	AU2
RXPFA	AT2
RXPRTY[0]	AP1
RXPRTY[1]	AL9
RXPRTY[2]	AP17
RXPRTY[3]	AU16
RXRCOMP	AU8
RXSOF[0]	AL5

Signal Name	Ball Location
RXSOF[1]	AN4
RXSOF[2]	AL17
RXSOF[3]	AM17
RXVAL[0]	AM4
RXVAL[1]	AM6
RXVAL[2]	AM16
RXVAL[3]	AP15
S0_A[0]	E27
S0_A[1]	C27
S0_A[10]	E25
S0_A[11]	F24
S0_A[12]	C26
S0_A[13]	D28
S0_A[14]	B27
S0_A[15]	B29
S0_A[16]	C28
S0_A[17]	C25
S0_A[18]	A30
S0_A[19]	A28
S0_A[2]	H25
S0_A[20]	B25
S0_A[21]	C29
S0_A[22]	D24
S0_A[23]	A26
S0_A[3]	G26
S0_A[4]	F26
S0_A[5]	D26
S0_A[6]	F25
S0_A[7]	F27
S0_A[8]	F28
S0_A[9]	G24
S0_BWE_L[0]	B33
S0_BWE_L[1]	H27
S0_C[0]	F29
S0_C[1]	A34
S0_C_L[0]	E29
S0_C_L[1]	A32
S0_CIN[0]	E21

Signal Name	Ball Location
S0_CIN[1]	C22
S0_CIN_L[0]	D20
S0_CIN_L[1]	F20
S0_DI[0]	H23
S0_DI[1]	F23
S0_DI[10]	B21
S0_DI[11]	F19
S0_DI[12]	C19
S0_DI[13]	E19
S0_DI[14]	H19
S0_DI[15]	B23
S0_DI[2]	E23
S0_DI[3]	C24
S0_DI[4]	F22
S0_DI[5]	D22
S0_DI[6]	C21
S0_DI[7]	G22
S0_DI[8]	G20
S0_DI[9]	C20
S0_DO[0]	G28
S0_DO[1]	G31
S0_DO[10]	E35
S0_DO[11]	F30
S0_DO[12]	D32
S0_DO[13]	B35
S0_DO[14]	E31
S0_DO[15]	E33
S0_DO[2]	G33
S0_DO[3]	F32
S0_DO[4]	D36
S0_DO[5]	C36
S0_DO[6]	F34
S0_DO[7]	G35
S0_DO[8]	C35
S0_DO[9]	D34
S0_K[0]	C31
S0_K[1]	B31
S0_K_L[0]	C30

Signal Name	Ball Location
S0_K_L[1]	C32
S0_PI[0]	F21
S0_PI[1]	C23
S0_PO[0]	F36
S0_PO[1]	A36
S0_RPE_L[0]	D30
S0_RPE_L[1]	C33
S0_VREF	A24
S0_WPE_L[0]	C34
S0_WPE_L[1]	C37
S0_ZQ[0]	J30
S0_ZQ[1]	H29
S1_A[0]	U36
S1_A[1]	T35
S1_A[10]	R35
S1_A[11]	R36
S1_A[12]	R30
S1_A[13]	R32
S1_A[14]	P34
S1_A[15]	P35
S1_A[16]	P31
S1_A[17]	P32
S1_A[18]	N35
S1_A[19]	N36
S1_A[2]	V32
S1_A[20]	N30
S1_A[21]	N32
S1_A[22]	N33
S1_A[23]	M31
S1_A[3]	V34
S1_A[4]	U33
S1_A[5]	T37
S1_A[6]	R33
S1_A[7]	T31
S1_A[8]	T32
S1_A[9]	T34
S1_BWE_L[0]	U30
S1_BWE_L[1]	W32

Signal Name	Ball Location
S1_C[0]	W35
S1_C[1]	W36
S1_C_L[0]	V31
S1_C_L[1]	U35
S1_CIN[0]	L33
S1_CIN[1]	K35
S1_CIN_L[0]	J36
S1_CIN_L[1]	L35
S1_DI[0]	M32
S1_DI[1]	P37
S1_DI[10]	H35
S1_DI[11]	J33
S1_DI[12]	H30
S1_DI[13]	H32
S1_DI[14]	J32
S1_DI[15]	K31
S1_DI[2]	M34
S1_DI[3]	K37
S1_DI[4]	M35
S1_DI[5]	K34
S1_DI[6]	K32
S1_DI[7]	L32
S1_DI[8]	J35
S1_DI[9]	H34
S1_DO[0]	AB32
S1_DO[1]	AD31
S1_DO[10]	AA33
S1_DO[11]	AC33
S1_DO[12]	Y32
S1_DO[13]	Y34
S1_DO[14]	AD34
S1_DO[15]	W33
S1_DO[2]	AC30
S1_DO[3]	W30
S1_DO[4]	AB34
S1_DO[5]	AB35
S1_DO[6]	AC32
S1_DO[7]	AA32

Signal Name	Ball Location
S1_DO[8]	AB37
S1_DO[9]	Y31
S1_K[0]	AC35
S1_K[1]	V35
S1_K_L[0]	U32
S1_K_L[1]	AD35
S1_PI[0]	L30
S1_PI[1]	L36
S1_PO[0]	AD32
S1_PO[1]	Y35
S1_RPE_L[0]	AA35
S1_RPE_L[1]	AA36
S1_VREF	E37
S1_WPE_L[0]	AC36
S1_WPE_L[1]	AD37
S1_ZQ[0]	AA30
S1_ZQ[1]	AB31
SERIAL_RX	AG32
SERIAL_TX	AF35
SP_ACK_L	AK36
SP_AD[0]	AJ36
SP_AD[1]	AF36
SP_AD[2]	AE36
SP_AD[3]	AJ37
SP_AD[4]	AK37
SP_AD[5]	AF32
SP_AD[6]	AG37
SP_AD[7]	AF37
SP_ALE_L	AJ35
SP_CLK	AL36
SP_CP_SP_A[0]	AL35
SP_CS_L[0]	AE35
SP_CS_L[1]	AG36
SP_DIR_SP_A[1]	AE33
SP_OE_L	AK35
SP_RD_L	AE32
SP_WR_L	AF34
SYS_CLK	AR18

Signal Name	Ball Location
SYS_RESET_L	AG35
SYS_RESET_OUT_L	AH36
T_DIAG_CLK	AH30
T_LOAD	AK32
T_SYS_REFCLK	AM18
TCK	AG30
TDI_T_SCAN_EN	AL33
TDO	AG33
THERMDA	J18
THERMDC	J19
TMS_T_CLK	AJ32
TRST_L	AG31
TST_RESET_L	AL32
TXADDR[0]	AK2
TXADDR[1]	AJ8
TXADDR[2]	AK1
TXADDR[3]	AL3
TXCDATA[0]	AL13
TXCDATA[1]	AM13
TXCDATA[2]	AM11
TXCDATA[3]	AU6
TXCFC	AM7
TXCLK01	AD8
TXCLK23	AB2
TXCPAR	AL15
TXCSOF	AM12
TXCSRB	AT9
TXDATA[0]	AH7
TXDATA[1]	AH8
TXDATA[10]	AG1
TXDATA[11]	AG7
TXDATA[12]	AG3
TXDATA[13]	AH2
TXDATA[14]	AF8
TXDATA[15]	AF5
TXDATA[16]	AB4
TXDATA[17]	AB6
TXDATA[18]	AB8

Signal Name	Ball Location
TXDATA[19]	AD2
TXDATA[2]	AJ2
TXDATA[20]	AC5
TXDATA[21]	AA2
TXDATA[22]	AA4
TXDATA[23]	AA6
TXDATA[24]	AB5
TXDATA[25]	AB7
TXDATA[26]	AA8
TXDATA[27]	Y2
TXDATA[28]	Y4
TXDATA[29]	AB3
TXDATA[3]	AJ4
TXDATA[30]	AB1
TXDATA[31]	Y6
TXDATA[4]	AH5
TXDATA[5]	AH1
TXDATA[6]	AH3
TXDATA[7]	AH4
TXDATA[8]	AH6
TXDATA[9]	AG5
TXENB[0]	AK3
TXENB[1]	AK6
TXENB[2]	Y3
TXENB[3]	V4
TXEOF[0]	AK5
TXEOF[1]	AK8
TXEOF[2]	Y8
TXEOF[3]	W7
TXERR[0]	AM1
TXERR[1]	AM3
TXERR[2]	Y5
TXERR[3]	V6
TXFA[0]	AE8
TXFA[1]	AF3
TXFA[2]	AD4
TXFA[3]	AC7
TXPADL[0]	AF4

Signal Name	Ball Location
TXPADL[1]	AF6
TXPFA	AF1
TXPRTY[0]	AM2
TXPRTY[1]	AN2
TXPRTY[2]	W3
TXPRTY[3]	V2
TXRCOMP	AC1
TXSFA	AE6
TXSOF[0]	AK4
TXSOF[1]	AK7
TXSOF[2]	Y7
TXSOF[3]	W5
VCC	AJ29
VCC	AG29
VCC	AE29
VCC	AC29
VCC	AA29
VCC	W29
VCC	U29
VCC	R29
VCC	N29
VCC	L29
VCC	J29
VCC	AK28
VCC	AH28
VCC	AF28
VCC	AD28
VCC	AB28
VCC	Y28
VCC	V28
VCC	T28
VCC	P28
VCC	M28
VCC	K28
VCC	AJ27
VCC	AG27
VCC	AE27
VCC	AC27

Signal Name	Ball Location
VCC	AA27
VCC	W27
VCC	U27
VCC	R27
VCC	N27
VCC	L27
VCC	J27
VCC	AK26
VCC	AH26
VCC	AF26
VCC	AD26
VCC	AB26
VCC	Y26
VCC	V26
VCC	T26
VCC	P26
VCC	M26
VCC	K26
VCC	AJ25
VCC	AG25
VCC	AE25
VCC	AC25
VCC	AA25
VCC	W25
VCC	U25
VCC	R25
VCC	N25
VCC	L25
VCC	J25
VCC	AK24
VCC	AH24
VCC	AF24
VCC	AD24
VCC	AB24
VCC	Y24
VCC	V24
VCC	T24
VCC	P24

Signal Name	Ball Location
VCC	M24
VCC	K24
VCC	AJ23
VCC	AG23
VCC	AE23
VCC	AC23
VCC	AA23
VCC	W23
VCC	U23
VCC	R23
VCC	N23
VCC	L23
VCC	J23
VCC	AK22
VCC	AH22
VCC	AF22
VCC	AD22
VCC	AB22
VCC	Y22
VCC	V22
VCC	T22
VCC	P22
VCC	M22
VCC	K22
VCC	AJ21
VCC	AG21
VCC	AE21
VCC	AC21
VCC	AA21
VCC	W21
VCC	U21
VCC	R21
VCC	N21
VCC	L21
VCC	J21
VCC	AK20
VCC	AH20
VCC	AF20

Signal Name	Ball Location
VCC	AD20
VCC	AB20
VCC	Y20
VCC	V20
VCC	T20
VCC	P20
VCC	M20
VCC	K20
VCC	AJ19
VCC	AG19
VCC	AE19
VCC	AC19
VCC	AA19
VCC	W19
VCC	U19
VCC	R19
VCC	N19
VCC	L19
VCC	AK18
VCC	AH18
VCC	AF18
VCC	AD18
VCC	AB18
VCC	Y18
VCC	V18
VCC	T18
VCC	P18
VCC	M18
VCC	K18
VCC	AJ17
VCC	AG17
VCC	AE17
VCC	AC17
VCC	AA17
VCC	W17
VCC	U17
VCC	R17
VCC	N17

Signal Name	Ball Location
VCC	L17
VCC	J17
VCC	AK16
VCC	AH16
VCC	AF16
VCC	AD16
VCC	AB16
VCC	Y16
VCC	V16
VCC	T16
VCC	P16
VCC	M16
VCC	K16
VCC	AJ15
VCC	AG15
VCC	AE15
VCC	AC15
VCC	AA15
VCC	W15
VCC	U15
VCC	R15
VCC	N15
VCC	L15
VCC	J15
VCC	AK14
VCC	AH14
VCC	AF14
VCC	AD14
VCC	AB14
VCC	Y14
VCC	V14
VCC	T14
VCC	P14
VCC	M14
VCC	K14
VCC	AJ13
VCC	AG13
VCC	AE13

Signal Name	Ball Location
VCC	AC13
VCC	AA13
VCC	W13
VCC	U13
VCC	R13
VCC	N13
VCC	L13
VCC	J13
VCC	AK12
VCC	AH12
VCC	AF12
VCC	AD12
VCC	AB12
VCC	Y12
VCC	V12
VCC	T12
VCC	P12
VCC	M12
VCC	K12
VCC	AJ11
VCC	AG11
VCC	AE11
VCC	AC11
VCC	AA11
VCC	W11
VCC	U11
VCC	R11
VCC	N11
VCC	L11
VCC	J11
VCC	AK10
VCC	AH10
VCC	AF10
VCC	AD10
VCC	AB10
VCC	Y10
VCC	V10
VCC	T10

Signal Name	Ball Location
VCC	P10
VCC	M10
VCC	K10
VCC	AJ9
VCC	AG9
VCC	AE9
VCC	AC9
VCC	AA9
VCC	W9
VCC	U9
VCC	R9
VCC	N9
VCC	L9
VCC1.5	AD36
VCC1.5	AB36
VCC1.5	Y36
VCC1.5	V36
VCC1.5	T36
VCC1.5	P36
VCC1.5	M36
VCC1.5	K36
VCC1.5	G36
VCC1.5	E36
VCC1.5	B36
VCC1.5	E34
VCC1.5	B34
VCC1.5	AD33
VCC1.5	AB33
VCC1.5	Y33
VCC1.5	V33
VCC1.5	T33
VCC1.5	P33
VCC1.5	M33
VCC1.5	K33
VCC1.5	H33
VCC1.5	F33
VCC1.5	E32
VCC1.5	B32

Signal Name	Ball Location
VCC1.5	H31
VCC1.5	AD30
VCC1.5	AB30
VCC1.5	Y30
VCC1.5	V30
VCC1.5	T30
VCC1.5	P30
VCC1.5	M30
VCC1.5	K30
VCC1.5	G30
VCC1.5	E30
VCC1.5	B30
VCC1.5	H28
VCC1.5	E28
VCC1.5	B28
VCC1.5	H26
VCC1.5	E26
VCC1.5	B26
VCC1.5	H24
VCC1.5	E24
VCC1.5	B24
VCC1.5	H22
VCC1.5	E22
VCC1.5	B22
VCC1.5	H20
VCC1.5	E20
VCC1.5	B20
VCC2.5	H18
VCC2.5	E18
VCC2.5	B18
VCC2.5	F16
VCC2.5	C16
VCC2.5	G14
VCC2.5	D14
VCC2.5	A14
VCC2.5	H12
VCC2.5	E12
VCC2.5	B12

Signal Name	Ball Location
VCC2.5	F10
VCC2.5	C10
VCC2.5	N8
VCC2.5	K8
VCC2.5	G8
VCC2.5	D8
VCC2.5	A8
VCC2.5	P6
VCC2.5	L6
VCC2.5	H6
VCC2.5	E6
VCC2.5	B6
VCC2.5	R4
VCC2.5	M4
VCC2.5	J4
VCC2.5	F4
VCC2.5	C4
VCC2.5	R2
VCC2.5	N2
VCC2.5	K2
VCC2.5	G2
VCC2.5	D2
VCC2.5	A2
VCC3.3	AU37
VCC3.3	AN37
VCC3.3	AN35
VCC3.3	AL34
VCC3.3	AH34
VCC3.3	AE34
VCC3.3	AU33
VCC3.3	AN33
VCC3.3	AH32
VCC3.3	AN31
VCC3.3	AL30
VCC3.3	AJ30
VCC3.3	AU29
VCC3.3	AN29
VCC3.3	AN27

Signal Name	Ball Location
VCC3.3	AU25
VCC3.3	AN25
VCC3.3	AN23
VCC3.3	AU21
VCC3.3	AN21
VCC3.3	AN19
VCC3.3	AU17
VCC3.3	AN17
VCC3.3	AU15
VCC3.3	AN15
VCC3.3	AU13
VCC3.3	AN13
VCC3.3	AU11
VCC3.3	AN11
VCC3.3	AU9
VCC3.3	AN9
VCC3.3	AU7
VCC3.3	AN7
VCC3.3	AJ7
VCC3.3	AE7
VCC3.3	AA7
VCC3.3	V7
VCC3.3	AU5
VCC3.3	AN5
VCC3.3	AJ5
VCC3.3	AE5
VCC3.3	AA5
VCC3.3	V5
VCC3.3	AU3
VCC3.3	AN3
VCC3.3	AJ3
VCC3.3	AE3
VCC3.3	AA3
VCC3.3	V3
VCC3.3	AU1
VCC3.3	AN1
VCC3.3	AJ1
VCC3.3	AE1

Signal Name	Ball Location
VCC3.3	AA1
VCCA	AP18
VCCA	AN18
VSS	AL37
VSS	AH37
VSS	AE37
VSS	AC37
VSS	AA37
VSS	U37
VSS	R37
VSS	N37
VSS	M37
VSS	L37
VSS	J37
VSS	H37
VSS	G37
VSS	F37
VSS	D37
VSS	B37
VSS	A37
VSS	AR36
VSS	H36
VSS	F35
VSS	D35
VSS	A35
VSS	AR34
VSS	AC34
VSS	AA34
VSS	W34
VSS	U34
VSS	R34
VSS	N34
VSS	L34
VSS	J34
VSS	G34
VSS	AH33
VSS	D33
VSS	A33

Signal Name	Ball Location
VSS	AR32
VSS	G32
VSS	AL31
VSS	AK31
VSS	AH31
VSS	AE31
VSS	AC31
VSS	AA31
VSS	W31
VSS	U31
VSS	R31
VSS	N31
VSS	L31
VSS	J31
VSS	F31
VSS	D31
VSS	A31
VSS	AR30
VSS	AK30
VSS	AK29
VSS	AH29
VSS	AF29
VSS	AD29
VSS	AB29
VSS	Y29
VSS	V29
VSS	T29
VSS	P29
VSS	M29
VSS	K29
VSS	G29
VSS	D29
VSS	A29
VSS	AR28
VSS	AL28
VSS	AJ28
VSS	AG28
VSS	AE28

Signal Name	Ball Location
VSS	AC28
VSS	AA28
VSS	W28
VSS	U28
VSS	R28
VSS	N28
VSS	L28
VSS	J28
VSS	AK27
VSS	AH27
VSS	AF27
VSS	AD27
VSS	AB27
VSS	Y27
VSS	V27
VSS	T27
VSS	P27
VSS	M27
VSS	K27
VSS	G27
VSS	D27
VSS	A27
VSS	AR26
VSS	AL26
VSS	AJ26
VSS	AG26
VSS	AE26
VSS	AC26
VSS	AA26
VSS	W26
VSS	U26
VSS	R26
VSS	N26
VSS	L26
VSS	J26
VSS	AK25
VSS	AH25
VSS	AF25

Signal Name	Ball Location
VSS	AD25
VSS	AB25
VSS	Y25
VSS	V25
VSS	T25
VSS	P25
VSS	M25
VSS	K25
VSS	G25
VSS	D25
VSS	A25
VSS	AR24
VSS	AL24
VSS	AJ24
VSS	AG24
VSS	AE24
VSS	AC24
VSS	AA24
VSS	W24
VSS	U24
VSS	R24
VSS	N24
VSS	L24
VSS	J24
VSS	AK23
VSS	AH23
VSS	AF23
VSS	AD23
VSS	AB23
VSS	Y23
VSS	V23
VSS	T23
VSS	P23
VSS	M23
VSS	K23
VSS	G23
VSS	D23
VSS	A23

Signal Name	Ball Location
VSS	AR22
VSS	AL22
VSS	AJ22
VSS	AG22
VSS	AE22
VSS	AC22
VSS	AA22
VSS	W22
VSS	U22
VSS	R22
VSS	N22
VSS	L22
VSS	J22
VSS	A22
VSS	AK21
VSS	AH21
VSS	AF21
VSS	AD21
VSS	AB21
VSS	Y21
VSS	V21
VSS	T21
VSS	P21
VSS	M21
VSS	K21
VSS	H21
VSS	G21
VSS	D21
VSS	A21
VSS	AT20
VSS	AL20
VSS	AJ20
VSS	AG20
VSS	AE20
VSS	AC20
VSS	AA20
VSS	W20
VSS	U20

Signal Name	Ball Location
VSS	R20
VSS	N20
VSS	L20
VSS	J20
VSS	AR19
VSS	AK19
VSS	AH19
VSS	AF19
VSS	AD19
VSS	AB19
VSS	Y19
VSS	V19
VSS	T19
VSS	P19
VSS	M19
VSS	K19
VSS	G19
VSS	D19
VSS	B19
VSS	AJ18
VSS	AG18
VSS	AE18
VSS	AC18
VSS	AA18
VSS	W18
VSS	U18
VSS	R18
VSS	N18
VSS	L18
VSS	AK17
VSS	AH17
VSS	AF17
VSS	AD17
VSS	AB17
VSS	Y17
VSS	V17
VSS	T17
VSS	P17

Signal Name	Ball Location
VSS	M17
VSS	K17
VSS	G17
VSS	D17
VSS	A17
VSS	AR16
VSS	AL16
VSS	AJ16
VSS	AG16
VSS	AE16
VSS	AC16
VSS	AA16
VSS	W16
VSS	U16
VSS	R16
VSS	N16
VSS	L16
VSS	J16
VSS	AK15
VSS	AH15
VSS	AF15
VSS	AD15
VSS	AB15
VSS	Y15
VSS	V15
VSS	T15
VSS	P15
VSS	M15
VSS	K15
VSS	H15
VSS	E15
VSS	B15
VSS	AR14
VSS	AL14
VSS	AJ14
VSS	AG14
VSS	AE14
VSS	AC14

Signal Name	Ball Location
VSS	AA14
VSS	W14
VSS	U14
VSS	R14
VSS	N14
VSS	L14
VSS	J14
VSS	AK13
VSS	AH13
VSS	AF13
VSS	AD13
VSS	AB13
VSS	Y13
VSS	V13
VSS	T13
VSS	P13
VSS	M13
VSS	K13
VSS	F13
VSS	C13
VSS	AR12
VSS	AL12
VSS	AJ12
VSS	AG12
VSS	AE12
VSS	AC12
VSS	AA12
VSS	W12
VSS	U12
VSS	R12
VSS	N12
VSS	L12
VSS	J12
VSS	AK11
VSS	AH11
VSS	AF11
VSS	AD11
VSS	AB11

Signal Name	Ball Location
VSS	Y11
VSS	V11
VSS	T11
VSS	P11
VSS	M11
VSS	K11
VSS	G11
VSS	D11
VSS	A11
VSS	AR10
VSS	AL10
VSS	AJ10
VSS	AG10
VSS	AE10
VSS	AC10
VSS	AA10
VSS	W10
VSS	U10
VSS	R10
VSS	N10
VSS	L10
VSS	J10
VSS	AK9
VSS	AH9
VSS	AF9
VSS	AD9
VSS	AB9
VSS	Y9
VSS	V9
VSS	T9
VSS	P9
VSS	M9
VSS	K9
VSS	H9
VSS	E9
VSS	B9
VSS	AR8
VSS	AL8

Signal Name	Ball Location
VSS	AG8
VSS	AC8
VSS	W8
VSS	V8
VSS	U8
VSS	T8
VSS	R8
VSS	P8
VSS	U7
VSS	T7
VSS	R7
VSS	P7
VSS	M7
VSS	J7
VSS	F7
VSS	C7
VSS	AR6
VSS	AL6
VSS	AG6
VSS	AC6
VSS	W6
VSS	U6
VSS	T6
VSS	R6
VSS	U5
VSS	T5
VSS	R5
VSS	N5
VSS	K5
VSS	G5
VSS	D5
VSS	A5
VSS	AR4
VSS	AL4
VSS	AG4
VSS	AC4
VSS	W4
VSS	U4

Signal Name	Ball Location
VSS	T4
VSS	U3
VSS	T3
VSS	R3
VSS	P3
VSS	L3
VSS	H3
VSS	E3
VSS	B3
VSS	AR2
VSS	AL2
VSS	AG2
VSS	AC2
VSS	W2
VSS	U2
VSS	T2
VSS	U1
VSS	T1
VSS	R1
VSS	M1
VSS	J1
VSS	F1
VSS	C1
VSSA	AT18
VSSA	AL18

3.5.2 Balls Listed in Alphanumeric Order by Ball Location

The following ball locations are not associated with a signal, therefore are not listed in Table 32: A1, Y1, W1, V1, Y37, W37, V37, AU[18:20], and A[18:20].

Table 32 shows the ball locations and signal names arranged in alphanumeric order by ball location.

Table 32. Ball List in Alphanumeric Order by Ball Location

Ball Location	Signal Name
A2	VCC2.5
A3	D_ECC[7]
A4	D_ECC[6]
A5	VSS
A6	D_DQ[25]
A7	D_A[4]
A8	VCC2.5
A9	D_DQ[23]
A10	D_A[7]
A11	VSS
A12	D_VREF[0]
A13	D_DQ[4]
A14	VCC2.5
A15	D_DQ[1]
A16	D_DQ[5]
A17	VSS
A21	VSS
A22	VSS
A23	VSS
A24	S0_VREF
A25	VSS
A26	S0_A[23]
A27	VSS
A28	S0_A[19]
A29	VSS
A30	S0_A[18]
A31	VSS
A32	S0_C_L[1]
A33	VSS
A34	S0_C[1]
A35	VSS
A36	S0_PO[1]
A37	VSS
AA1	VCC3.3
AA2	TXDATA[21]
AA3	VCC3.3
AA4	TXDATA[22]
AA5	VCC3.3
AA6	TXDATA[23]
AA7	VCC3.3
AA8	TXDATA[26]
AA9	VCC
AA10	VSS
AA11	VCC
AA12	VSS
AA13	VCC
AA14	VSS
AA15	VCC
AA16	VSS
AA17	VCC
AA18	VSS
AA19	VCC
AA20	VSS
AA21	VCC
AA22	VSS
AA23	VCC
AA24	VSS
AA25	VCC
AA26	VSS
AA27	VCC
AA28	VSS
AA29	VCC
AA30	S1_ZQ[0]
AA31	VSS
AA32	S1_DO[7]
AA33	S1_DO[10]
AA34	VSS
AA35	S1_RPE_L[0]
AA36	S1_RPE_L[1]
AA37	VSS
AB1	TXDATA[30]
AB2	TXCLK23
AB3	TXDATA[29]
AB4	TXDATA[16]
AB5	TXDATA[24]
AB6	TXDATA[17]
AB7	TXDATA[25]
AB8	TXDATA[18]
AB9	VSS
AB10	VCC
AB11	VSS
AB12	VCC
AB13	VSS
AB14	VCC
AB15	VSS
AB16	VCC
AB17	VSS
AB18	VCC
AB19	VSS
AB20	VCC
AB21	VSS
AB22	VCC
AB23	VSS

Ball Location	Signal Name
AB24	VCC
AB25	VSS
AB26	VCC
AB27	VSS
AB28	VCC
AB29	VSS
AB30	VCC1.5
AB31	S1_ZQ[1]
AB32	S1_DO[0]
AB33	VCC1.5
AB34	S1_DO[4]
AB35	S1_DO[5]
AB36	VCC1.5
AB37	S1_DO[8]
AC1	TXRCOMP
AC2	VSS
AC3	MSF_CLK_BYPASS
AC4	VSS
AC5	TXDATA[20]
AC6	VSS
AC7	TXFA[3]
AC8	VSS
AC9	VCC
AC10	VSS
AC11	VCC
AC12	VSS
AC13	VCC
AC14	VSS
AC15	VCC
AC16	VSS
AC17	VCC
AC18	VSS
AC19	VCC
AC20	VSS
AC21	VCC
AC22	VSS
AC23	VCC
AC24	VSS

Ball Location	Signal Name
AC25	VCC
AC26	VSS
AC27	VCC
AC28	VSS
AC29	VCC
AC30	S1_DO[2]
AC31	VSS
AC32	S1_DO[6]
AC33	S1_DO[11]
AC34	VSS
AC35	S1_K[0]
AC36	S1_WPE_L[0]
AC37	VSS
AD1	RXCSRB
AD2	TXDATA[19]
AD3	RXCDATA[1]
AD4	TXFA[2]
AD5	RXCDATA[2]
AD6	RXCDATA[3]
AD7	RXCPAR
AD8	TXCLK01
AD9	VSS
AD10	VCC
AD11	VSS
AD12	VCC
AD13	VSS
AD14	VCC
AD15	VSS
AD16	VCC
AD17	VSS
AD18	VCC
AD19	VSS
AD20	VCC
AD21	VSS
AD22	VCC
AD23	VSS
AD24	VCC
AD25	VSS

Ball Location	Signal Name
AD26	VCC
AD27	VSS
AD28	VCC
AD29	VSS
AD30	VCC1.5
AD31	S1_DO[1]
AD32	S1_PO[0]
AD33	VCC1.5
AD34	S1_DO[14]
AD35	S1_K_L[1]
AD36	VCC1.5
AD37	S1_WPE_L[1]
AE1	VCC3.3
AE2	RXCSOF
AE3	VCC3.3
AE4	RXCDATA[0]
AE5	VCC3.3
AE6	TXSFA
AE7	VCC3.3
AE8	TXFA[0]
AE9	VCC
AE10	VSS
AE11	VCC
AE12	VSS
AE13	VCC
AE14	VSS
AE15	VCC
AE16	VSS
AE17	VCC
AE18	VSS
AE19	VCC
AE20	VSS
AE21	VCC
AE22	VSS
AE23	VCC
AE24	VSS
AE25	VCC
AE26	VSS

Ball Location	Signal Name
AE27	VCC
AE28	VSS
AE29	VCC
AE30	GPIO[4]
AE31	VSS
AE32	SP_RD_L
AE33	SP_DIR_SP_A[1]
AE34	VCC3.3
AE35	SP_CS_L[0]
AE36	SP_AD[2]
AE37	VSS
AF1	TXPFA
AF2	RSVD[1]
AF3	TXFA[1]
AF4	TXPADL[0]
AF5	TXDATA[15]
AF6	TXPADL[1]
AF7	RXCFC
AF8	TXDATA[14]
AF9	VSS
AF10	VCC
AF11	VSS
AF12	VCC
AF13	VSS
AF14	VCC
AF15	VSS
AF16	VCC
AF17	VSS
AF18	VCC
AF19	VSS
AF20	VCC
AF21	VSS
AF22	VCC
AF23	VSS
AF24	VCC
AF25	VSS
AF26	VCC
AF27	VSS

Ball Location	Signal Name
AF28	VCC
AF29	VSS
AF30	GPIO[7]
AF31	GPIO[0]
AF32	SP_AD[5]
AF33	GPIO[5]
AF34	SP_WR_L
AF35	SERIAL_TX
AF36	SP_AD[1]
AF37	SP_AD[7]
AG1	TXDATA[10]
AG2	VSS
AG3	TXDATA[12]
AG4	VSS
AG5	TXDATA[9]
AG6	VSS
AG7	TXDATA[11]
AG8	VSS
AG9	VCC
AG10	VSS
AG11	VCC
AG12	VSS
AG13	VCC
AG14	VSS
AG15	VCC
AG16	VSS
AG17	VCC
AG18	VSS
AG19	VCC
AG20	VSS
AG21	VCC
AG22	VSS
AG23	VCC
AG24	VSS
AG25	VCC
AG26	VSS
AG27	VCC
AG28	VSS

Ball Location	Signal Name
AG29	VCC
AG30	TCK
AG31	TRST_L
AG32	SERIAL_RX
AG33	TDO
AG34	GPIO[6]
AG35	SYS_RESET_L
AG36	SP_CS_L[1]
AG37	SP_AD[6]
AH1	TXDATA[5]
AH2	TXDATA[13]
AH3	TXDATA[6]
AH4	TXDATA[7]
AH5	TXDATA[4]
AH6	TXDATA[8]
AH7	TXDATA[0]
AH8	TXDATA[1]
AH9	VSS
AH10	VCC
AH11	VSS
AH12	VCC
AH13	VSS
AH14	VCC
AH15	VSS
AH16	VCC
AH17	VSS
AH18	VCC
AH19	VSS
AH20	VCC
AH21	VSS
AH22	VCC
AH23	VSS
AH24	VCC
AH25	VSS
AH26	VCC
AH27	VSS
AH28	VCC
AH29	VSS

Ball Location	Signal Name
AH30	T_DIAG_CLK
AH31	VSS
AH32	VCC3.3
AH33	VSS
AH34	VCC3.3
AH35	PLL_DIV_BYPASS
AH36	SYS_RESET_OUT_L
AH37	VSS
AJ1	VCC3.3
AJ2	TXDATA[2]
AJ3	VCC3.3
AJ4	TXDATA[3]
AJ5	VCC3.3
AJ6	RSVD[0]
AJ7	VCC3.3
AJ8	TXADDR[1]
AJ9	VCC
AJ10	VSS
AJ11	VCC
AJ12	VSS
AJ13	VCC
AJ14	VSS
AJ15	VCC
AJ16	VSS
AJ17	VCC
AJ18	VSS
AJ19	VCC
AJ20	VSS
AJ21	VCC
AJ22	VSS
AJ23	VCC
AJ24	VSS
AJ25	VCC
AJ26	VSS
AJ27	VCC
AJ28	VSS
AJ29	VCC
AJ30	VCC3.3

Ball Location	Signal Name
AJ31	PLL_BYPASS
AJ32	TMS_T_CLK
AJ33	GPIO[2]
AJ34	GPIO[3]
AJ35	SP_ALE_L
AJ36	SP_AD[0]
AJ37	SP_AD[3]
AK1	TXADDR[2]
AK2	TXADDR[0]
AK3	TXENB[0]
AK4	TXSOF[0]
AK5	TXEOF[0]
AK6	TXENB[1]
AK7	TXSOF[1]
AK8	TXEOF[1]
AK9	VSS
AK10	VCC
AK11	VSS
AK12	VCC
AK13	VSS
AK14	VCC
AK15	VSS
AK16	VCC
AK17	VSS
AK18	VCC
AK19	VSS
AK20	VCC
AK21	VSS
AK22	VCC
AK23	VSS
AK24	VCC
AK25	VSS
AK26	VCC
AK27	VSS
AK28	VCC
AK29	VSS
AK30	VSS
AK31	VSS

Ball Location	Signal Name
AK32	T_LOAD
AK33	CFG_RSTDIR
AK34	GPIO[1]
AK35	SP_OE_L
AK36	SP_ACK_L
AK37	SP_AD[4]
AL1	RXEOF[0]
AL2	VSS
AL3	TXADDR[3]
AL4	VSS
AL5	RXSOF[0]
AL6	VSS
AL7	RXERR[1]
AL8	VSS
AL9	RXPRTY[1]
AL10	VSS
AL11	RXADDR[1]
AL12	VSS
AL13	TXCDATA[0]
AL14	VSS
AL15	TXCPAR
AL16	VSS
AL17	RXSOF[2]
AL18	VSSA
AL19	PCI_RST_L
AL20	VSS
AL21	PCI_AD[27]
AL22	VSS
AL23	PCI_AD[18]
AL24	VSS
AL25	PCI_SERR_L
AL26	VSS
AL27	PCI_CBE_L[0]
AL28	VSS
AL29	PCI_CBE_L[6]
AL30	VCC3.3
AL31	VSS
AL32	TST_RESET_L

Ball Location	Signal Name
AL33	TDI_T_SCAN_EN
AL34	VCC3.3
AL35	SP_CP_SP_A[0]
AL36	SP_CLK
AL37	VSS
AM1	TXERR[0]
AM2	TXPRTY[0]
AM3	TXERR[1]
AM4	RXVAL[0]
AM5	RXERR[0]
AM6	RXVAL[1]
AM7	TXCFC
AM8	RXPADL[0]
AM9	RSVD[3]
AM10	RXADDR[3]
AM11	TXCDATA[2]
AM12	TXCSOF
AM13	TXCDATA[1]
AM14	RXDATA[16]
AM15	RXENB[2]
AM16	RXVAL[2]
AM17	RXSOF[3]
AM18	T_SYS_REFCLK
AM19	PCI_INTB_L
AM20	PCI_REQ_L[1]
AM21	PCI_AD[28]
AM22	PCI_IDSEL
AM23	PCI_AD[19]
AM24	PCI_IRDY_L
AM25	PCI_PERR_L
AM26	PCI_AD[13]
AM27	PCI_AD[8]
AM28	PCI_AD[3]
AM29	PCI_CBE_L[7]
AM30	PCI_AD[63]
AM31	PCI_AD[59]
AM32	PCI_AD[54]
AM33	PCI_AD[50]

Ball Location	Signal Name
AM34	PCI_AD[45]
AM35	PCI_AD[40]
AM36	PCI_AD[35]
AM37	PCI_AD[39]
AN1	VCC3.3
AN2	TXPRTY[1]
AN3	VCC3.3
AN4	RXSOF[1]
AN5	VCC3.3
AN6	RXFA[1]
AN7	VCC3.3
AN8	RXENB[1]
AN9	VCC3.3
AN10	RXADDR[2]
AN11	VCC3.3
AN12	RSVD[2]
AN13	VCC3.3
AN14	RXDATA[18]
AN15	VCC3.3
AN16	RXFA[2]
AN17	VCC3.3
AN18	VCCA
AN19	VCC3.3
AN20	PCI_GNT_L[1]
AN21	VCC3.3
AN22	PCI_CBE_L[3]
AN23	VCC3.3
AN24	PCI_FRAME_L
AN25	VCC3.3
AN26	PCI_AD[14]
AN27	VCC3.3
AN28	PCI_AD[4]
AN29	VCC3.3
AN30	PCI_PAR64
AN31	VCC3.3
AN32	PCI_AD[55]
AN33	VCC3.3
AN34	PCI_AD[46]

Ball Location	Signal Name
AN35	VCC3.3
AN36	PCI_AD[36]
AN37	VCC3.3
AP1	RXPRTY[0]
AP2	RXDATA[3]
AP3	RXDATA[2]
AP4	RXDATA[5]
AP5	RXDATA[10]
AP6	RXDATA[1]
AP7	RXDATA[11]
AP8	RXCLK01
AP9	RXCLK23
AP10	RXADDR[0]
AP11	RXENB[0]
AP12	RXDATA[21]
AP13	RXDATA[17]
AP14	RXDATA[27]
AP15	RXVAL[3]
AP16	RXEOF[2]
AP17	RXPRTY[2]
AP18	VCCA
AP19	PCI_REQ_L[0]
AP20	PCI_INTA_L
AP21	PCI_AD[29]
AP22	PCI_AD[24]
AP23	PCI_AD[20]
AP24	PCI_CBE_L[2]
AP25	PCI_STOP_L
AP26	PCI_AD[15]
AP27	PCI_AD[9]
AP28	PCI_AD[5]
AP29	PCI_AD[0]
AP30	PCI_ACK64_L
AP31	PCI_AD[60]
AP32	PCI_AD[56]
AP33	PCI_AD[51]
AP34	PCI_AD[47]
AP35	PCI_AD[41]

Ball Location	Signal Name
AP36	PCI_AD[37]
AP37	PCI_AD[32]
AR1	RXEOF[1]
AR2	VSS
AR3	RXDATA[6]
AR4	VSS
AR5	RXDATA[13]
AR6	VSS
AR7	RXDATA[4]
AR8	VSS
AR9	RXENB[3]
AR10	VSS
AR11	RXDATA[23]
AR12	VSS
AR13	RXDATA[20]
AR14	VSS
AR15	RXFA[3]
AR16	VSS
AR17	RXEOF[3]
AR18	SYS_CLK
AR19	VSS
AR20	PCI_GNT_L[0]
AR21	PCI_AD[30]
AR22	VSS
AR23	PCI_AD[21]
AR24	VSS
AR25	PCI_DEVSEL_L
AR26	VSS
AR27	PCI_AD[10]
AR28	VSS
AR29	PCI_AD[1]
AR30	VSS
AR31	PCI_REQ64_L
AR32	VSS
AR33	PCI_AD[52]
AR34	VSS
AR35	PCI_AD[42]
AR36	VSS

Ball Location	Signal Name
AR37	PCI_AD[33]
AT1	RXFA[0]
AT2	RXPFA
AT3	RXDATA[0]
AT4	RXDATA[7]
AT5	RXDATA[8]
AT6	RXDATA[9]
AT7	RXDATA[12]
AT8	RXDATA[15]
AT9	TXCSRB
AT10	RXDATA[19]
AT11	RXDATA[26]
AT12	RXDATA[22]
AT13	RXDATA[25]
AT14	RXDATA[30]
AT15	RXDATA[29]
AT16	RXERR[2]
AT17	RXERR[3]
AT18	VSSA
AT19	PCI_CLK
AT20	VSS
AT21	PCI_AD[31]
AT22	PCI_AD[25]
AT23	PCI_AD[22]
AT24	PCI_AD[16]
AT25	PCI_TRDY_L
AT26	PCI_CBE_L[1]
AT27	PCI_AD[11]
AT28	PCI_AD[6]
AT29	PCI_AD[2]
AT30	PCI_CBE_L[4]
AT31	PCI_AD[61]
AT32	PCI_AD[57]
AT33	PCI_AD[53]
AT34	PCI_AD[48]
AT35	PCI_AD[43]
AT36	PCI_AD[38]
AT37	PCI_AD[34]

Ball Location	Signal Name
AU1	VCC3.3
AU2	RXPADL[1]
AU3	VCC3.3
AU4	RXDATA[14]
AU5	VCC3.3
AU6	TXCDATA[3]
AU7	VCC3.3
AU8	RXRCOMP
AU9	VCC3.3
AU10	RXDATA[24]
AU11	VCC3.3
AU12	RXDATA[28]
AU13	VCC3.3
AU14	RXDATA[31]
AU15	VCC3.3
AU16	RXPRTY[3]
AU17	VCC3.3
AU21	VCC3.3
AU22	PCI_AD[26]
AU23	PCI_AD[23]
AU24	PCI_AD[17]
AU25	VCC3.3
AU26	PCI_PAR
AU27	PCI_AD[12]
AU28	PCI_AD[7]
AU29	VCC3.3
AU30	PCI_CBE_L[5]
AU31	PCI_AD[62]
AU32	PCI_AD[58]
AU33	VCC3.3
AU34	PCI_AD[49]
AU35	PCI_AD[44]
AU36	PCI_RCOMP
AU37	VCC3.3
B1	D_BA[1]
B2	D_ECC[3]
B3	VSS
B4	D_DQS[8]

Ball Location	Signal Name
B5	D_ECC[2]
B6	VCC2.5
B7	D_A[3]
B8	D_A[11]
B9	VSS
B10	D_A[9]
B11	D_DQ[22]
B12	VCC2.5
B13	D_DQS[0]
B14	D_DQ[2]
B15	VSS
B16	D_CKE[0]
B17	D_DQ[3]
B18	VCC2.5
B19	VSS
B20	VCC1.5
B21	S0_DI[10]
B22	VCC1.5
B23	S0_DI[15]
B24	VCC1.5
B25	S0_A[20]
B26	VCC1.5
B27	S0_A[14]
B28	VCC1.5
B29	S0_A[15]
B30	VCC1.5
B31	S0_K[1]
B32	VCC1.5
B33	S0_BWE_L[0]
B34	VCC1.5
B35	S0_DO[13]
B36	VCC1.5
B37	VSS
C1	VSS
C2	D_DQS[4]
C3	D_DQ[37]
C4	VCC2.5
C5	D_DM[8]

Ball Location	Signal Name
C6	D_ECC[4]
C7	VSS
C8	D_DQ[19]
C9	D_DQS[2]
C10	VCC2.5
C11	D_DQ[17]
C12	D_DM[0]
C13	VSS
C14	D_DQ[8]
C15	D_DQ[10]
C16	VCC2.5
C17	D_DQ[7]
C18	D_DQ[0]
C19	S0_DI[12]
C20	S0_DI[9]
C21	S0_DI[6]
C22	S0_CIN[1]
C23	S0_PI[1]
C24	S0_DI[3]
C25	S0_A[17]
C26	S0_A[12]
C27	S0_A[1]
C28	S0_A[16]
C29	S0_A[21]
C30	S0_K_L[0]
C31	S0_K[0]
C32	S0_K_L[1]
C33	S0_RPE_L[1]
C34	S0_WPE_L[0]
C35	S0_DO[8]
C36	S0_DO[5]
C37	S0_WPE_L[1]
D1	D_A[10]
D2	VCC2.5
D3	D_DQ[32]
D4	D_BA[0]
D5	VSS
D6	D_DM[3]

Ball Location	Signal Name
D7	D_DQ[26]
D8	VCC2.5
D9	D_A[8]
D10	D_DQ[18]
D11	VSS
D12	D_DQ[21]
D13	D_DQ[14]
D14	VCC2.5
D15	D_DQ[20]
D16	D_DQ[13]
D17	VSS
D18	D_A[13]
D19	VSS
D20	S0_CIN_L[0]
D21	VSS
D22	S0_DI[5]
D23	VSS
D24	S0_A[22]
D25	VSS
D26	S0_A[5]
D27	VSS
D28	S0_A[13]
D29	VSS
D30	S0_RPE_L[0]
D31	VSS
D32	S0_DO[12]
D33	VSS
D34	S0_DO[9]
D35	VSS
D36	S0_DO[4]
D37	VSS
E1	D_WE_L
E2	D_RAS_L
E3	VSS
E4	D_DQ[33]
E5	D_A[0]
E6	VCC2.5
E7	D_DQ[30]

Ball Location	Signal Name
E8	D_DQS[3]
E9	VSS
E10	D_DQ[28]
E11	D_DQ[24]
E12	VCC2.5
E13	D_DM[2]
E14	D_DQS[1]
E15	VSS
E16	D_DQ[9]
E17	D_DQ[6]
E18	VCC2.5
E19	S0_DI[13]
E20	VCC1.5
E21	S0_CIN[0]
E22	VCC1.5
E23	S0_DI[2]
E24	VCC1.5
E25	S0_A[10]
E26	VCC1.5
E27	S0_A[0]
E28	VCC1.5
E29	S0_C_L[0]
E30	VCC1.5
E31	S0_DO[14]
E32	VCC1.5
E33	S0_DO[15]
E34	VCC1.5
E35	S0_DO[10]
E36	VCC1.5
E37	S1_VREF
F1	VSS
F2	D_CS_L[0]
F3	D_DQ[35]
F4	VCC2.5
F5	D_DQ[36]
F6	D_DQ[34]
F7	VSS
F8	D_CK[0]

Ball Location	Signal Name
F9	D_ECC[5]
F10	VCC2.5
F11	D_A[6]
F12	D_DQ[29]
F13	VSS
F14	D_DQ[16]
F15	D_CKE[1]
F16	VCC2.5
F17	D_DM[1]
F18	D_CK[1]
F19	S0_DI[11]
F20	S0_CIN_L[1]
F21	S0_PI[0]
F22	S0_DI[4]
F23	S0_DI[1]
F24	S0_A[11]
F25	S0_A[6]
F26	S0_A[4]
F27	S0_A[7]
F28	S0_A[8]
F29	S0_C[0]
F30	S0_DO[11]
F31	VSS
F32	S0_DO[3]
F33	VCC1.5
F34	S0_DO[6]
F35	VSS
F36	S0_PO[0]
F37	VSS
G1	D_RCOMP[0]
G2	VCC2.5
G3	D_DQ[41]
G4	D_DQ[40]
G5	VSS
G6	D_DQ[45]
G7	D_DQ[39]
G8	VCC2.5
G9	D_CK_L[0]

Ball Location	Signal Name
G10	D_A[2]
G11	VSS
G12	D_A[1]
G13	D_A[5]
G14	VCC2.5
G15	D_A[12]
G16	D_DQ[12]
G17	VSS
G18	D_CK_L[1]
G19	VSS
G20	S0_DI[8]
G21	VSS
G22	S0_DI[7]
G23	VSS
G24	S0_A[9]
G25	VSS
G26	S0_A[3]
G27	VSS
G28	S0_DO[0]
G29	VSS
G30	VCC1.5
G31	S0_DO[1]
G32	VSS
G33	S0_DO[2]
G34	VSS
G35	S0_DO[7]
G36	VCC1.5
G37	VSS
H1	D_RCOMP[1]
H2	D_DQS[5]
H3	VSS
H4	D_DM[5]
H5	D_DQ[43]
H6	VCC2.5
H7	D_DQ[44]
H8	D_DM[4]
H9	VSS
H10	D_ECC[0]

Ball Location	Signal Name
H11	D_ECC[1]
H12	VCC2.5
H13	D_DQ[31]
H14	D_DQ[27]
H15	VSS
H16	D_DQ[11]
H17	D_DQ[15]
H18	VCC2.5
H19	S0_DI[14]
H20	VCC1.5
H21	VSS
H22	VCC1.5
H23	S0_DI[0]
H24	VCC1.5
H25	S0_A[2]
H26	VCC1.5
H27	S0_BWE_L[1]
H28	VCC1.5
H29	S0_ZQ[1]
H30	S1_DI[12]
H31	VCC1.5
H32	S1_DI[13]
H33	VCC1.5
H34	S1_DI[9]
H35	S1_DI[10]
H36	VSS
H37	VSS
J1	VSS
J2	D_DQ[46]
J3	D_DQ[51]
J4	VCC2.5
J5	D_DQ[53]
J6	D_DQ[48]
J7	VSS
J8	D_DQ[42]
J9	D_DQ[38]
J10	VSS
J11	VCC

Ball Location	Signal Name
J12	VSS
J13	VCC
J14	VSS
J15	VCC
J16	VSS
J17	VCC
J18	THERMDA
J19	THERMDC
J20	VSS
J21	VCC
J22	VSS
J23	VCC
J24	VSS
J25	VCC
J26	VSS
J27	VCC
J28	VSS
J29	VCC
J30	S0_ZQ[0]
J31	VSS
J32	S1_DI[14]
J33	S1_DI[11]
J34	VSS
J35	S1_DI[8]
J36	S1_CIN_L[0]
J37	VSS
K1	D_CS_L[1]
K2	VCC2.5
K3	D_DQS[6]
K4	D_DQ[55]
K5	VSS
K6	D_DM[6]
K7	D_CAS_L
K8	VCC2.5
K9	VSS
K10	VCC
K11	VSS
K12	VCC

Ball Location	Signal Name
K13	VSS
K14	VCC
K15	VSS
K16	VCC
K17	VSS
K18	VCC
K19	VSS
K20	VCC
K21	VSS
K22	VCC
K23	VSS
K24	VCC
K25	VSS
K26	VCC
K27	VSS
K28	VCC
K29	VSS
K30	VCC1.5
K31	S1_DI[15]
K32	S1_DI[6]
K33	VCC1.5
K34	S1_DI[5]
K35	S1_CIN[1]
K36	VCC1.5
K37	S1_DI[3]
L1	D_DQ[56]
L2	D_DQ[47]
L3	VSS
L4	D_DQ[54]
L5	D_DQ[50]
L6	VCC2.5
L7	D_DQ[49]
L8	D_DQ[52]
L9	VCC
L10	VSS
L11	VCC
L12	VSS
L13	VCC

Ball Location	Signal Name
L14	VSS
L15	VCC
L16	VSS
L17	VCC
L18	VSS
L19	VCC
L20	VSS
L21	VCC
L22	VSS
L23	VCC
L24	VSS
L25	VCC
L26	VSS
L27	VCC
L28	VSS
L29	VCC
L30	S1_PI[0]
L31	VSS
L32	S1_DI[7]
L33	S1_CIN[0]
L34	VSS
L35	S1_CIN_L[1]
L36	S1_PI[1]
L37	VSS
M1	VSS
M2	D_DQ[59]
M3	D_DQ[58]
M4	VCC2.5
M5	D_DQ[62]
M6	D_DQS[7]
M7	VSS
M8	D_DQ[57]
M9	VSS
M10	VCC
M11	VSS
M12	VCC
M13	VSS
M14	VCC

Ball Location	Signal Name
M15	VSS
M16	VCC
M17	VSS
M18	VCC
M19	VSS
M20	VCC
M21	VSS
M22	VCC
M23	VSS
M24	VCC
M25	VSS
M26	VCC
M27	VSS
M28	VCC
M29	VSS
M30	VCC1.5
M31	S1_A[23]
M32	S1_DI[0]
M33	VCC1.5
M34	S1_DI[2]
M35	S1_DI[4]
M36	VCC1.5
M37	VSS
N1	D_DQ[61]
N2	VCC2.5
N3	D_CK[2]
N4	D_CK_L[2]
N5	VSS
N6	D_DQ[60]
N7	D_DM[7]
N8	VCC2.5
N9	VCC
N10	VSS
N11	VCC
N12	VSS
N13	VCC
N14	VSS
N15	VCC

Ball Location	Signal Name
N16	VSS
N17	VCC
N18	VSS
N19	VCC
N20	VSS
N21	VCC
N22	VSS
N23	VCC
N24	VSS
N25	VCC
N26	VSS
N27	VCC
N28	VSS
N29	VCC
N30	S1_A[20]
N31	VSS
N32	S1_A[21]
N33	S1_A[22]
N34	VSS
N35	S1_A[18]
N36	S1_A[19]
N37	VSS
P1	D_VREF[1]
P2	D_DQ[63]
P3	VSS
P4	D_RCVENOUT_L
P5	D_RCVENIN_L
P6	VCC2.5
P7	VSS
P8	VSS
P9	VSS
P10	VCC
P11	VSS
P12	VCC
P13	VSS
P14	VCC
P15	VSS
P16	VCC

Ball Location	Signal Name
P17	VSS
P18	VCC
P19	VSS
P20	VCC
P21	VSS
P22	VCC
P23	VSS
P24	VCC
P25	VSS
P26	VCC
P27	VSS
P28	VCC
P29	VSS
P30	VCC1.5
P31	S1_A[16]
P32	S1_A[17]
P33	VCC1.5
P34	S1_A[14]
P35	S1_A[15]
P36	VCC1.5
P37	S1_DI[1]
R1	VSS
R2	VCC2.5
R3	VSS
R4	VCC2.5
R5	VSS
R6	VSS
R7	VSS
R8	VSS
R9	VCC
R10	VSS
R11	VCC
R12	VSS
R13	VCC
R14	VSS
R15	VCC
R16	VSS
R17	VCC

Ball Location	Signal Name
R18	VSS
R19	VCC
R20	VSS
R21	VCC
R22	VSS
R23	VCC
R24	VSS
R25	VCC
R26	VSS
R27	VCC
R28	VSS
R29	VCC
R30	S1_A[12]
R31	VSS
R32	S1_A[13]
R33	S1_A[6]
R34	VSS
R35	S1_A[10]
R36	S1_A[11]
R37	VSS
T1	VSS
T2	VSS
T3	VSS
T4	VSS
T5	VSS
T6	VSS
T7	VSS
T8	VSS
T9	VSS
T10	VCC
T11	VSS
T12	VCC
T13	VSS
T14	VCC
T15	VSS
T16	VCC
T17	VSS
T18	VCC

Ball Location	Signal Name
T19	VSS
T20	VCC
T21	VSS
T22	VCC
T23	VSS
T24	VCC
T25	VSS
T26	VCC
T27	VSS
T28	VCC
T29	VSS
T30	VCC1.5
T31	S1_A[7]
T32	S1_A[8]
T33	VCC1.5
T34	S1_A[9]
T35	S1_A[1]
T36	VCC1.5
T37	S1_A[5]
U1	VSS
U2	VSS
U3	VSS
U4	VSS
U5	VSS
U6	VSS
U7	VSS
U8	VSS
U9	VCC
U10	VSS
U11	VCC
U12	VSS
U13	VCC
U14	VSS
U15	VCC
U16	VSS
U17	VCC
U18	VSS
U19	VCC

Ball Location	Signal Name
U20	VSS
U21	VCC
U22	VSS
U23	VCC
U24	VSS
U25	VCC
U26	VSS
U27	VCC
U28	VSS
U29	VCC
U30	S1_BWE_L[0]
U31	VSS
U32	S1_K_L[0]
U33	S1_A[4]
U34	VSS
U35	S1_C_L[1]
U36	S1_A[0]
U37	VSS
V2	TXPRTY[3]
V3	VCC3.3
V4	TXENB[3]
V5	VCC3.3
V6	TXERR[3]
V7	VCC3.3
V8	VSS
V9	VSS
V10	VCC
V11	VSS
V12	VCC
V13	VSS
V14	VCC
V15	VSS
V16	VCC
V17	VSS
V18	VCC
V19	VSS
V20	VCC
V21	VSS

Ball Location	Signal Name
V22	VCC
V23	VSS
V24	VCC
V25	VSS
V26	VCC
V27	VSS
V28	VCC
V29	VSS
V30	VCC1.5
V31	S1_C_L[0]
V32	S1_A[2]
V33	VCC1.5
V34	S1_A[3]
V35	S1_K[1]
V36	VCC1.5
W2	VSS
W3	TXPRTY[2]
W4	VSS
W5	TXSOF[3]
W6	VSS
W7	TXEOF[3]
W8	VSS
W9	VCC
W10	VSS
W11	VCC
W12	VSS
W13	VCC
W14	VSS
W15	VCC
W16	VSS
W17	VCC
W18	VSS
W19	VCC
W20	VSS
W21	VCC
W22	VSS
W23	VCC
W24	VSS

Ball Location	Signal Name
W25	VCC
W26	VSS
W27	VCC
W28	VSS
W29	VCC
W30	S1_DO[3]
W31	VSS
W32	S1_BWE_L[1]
W33	S1_DO[15]
W34	VSS
W35	S1_C[0]
W36	S1_C[1]
Y2	TXDATA[27]
Y3	TXENB[2]
Y4	TXDATA[28]
Y5	TXERR[2]
Y6	TXDATA[31]
Y7	TXSOF[2]
Y8	TXEOF[2]
Y9	VSS
Y10	VCC
Y11	VSS
Y12	VCC
Y13	VSS
Y14	VCC
Y15	VSS
Y16	VCC
Y17	VSS
Y18	VCC
Y19	VSS
Y20	VCC
Y21	VSS
Y22	VCC
Y23	VSS
Y24	VCC
Y25	VSS
Y26	VCC
Y27	VSS

Ball Location	Signal Name
Y28	VCC
Y29	VSS
Y30	VCC1.5
Y31	S1_DO[9]
Y32	S1_DO[12]
Y33	VCC1.5
Y34	S1_DO[13]
Y35	S1_PO[1]
Y36	VCC1.5

4.0 Electrical Specifications

This chapter specifies the following electrical behavior of the IXP2400:

- Absolute maximum ratings
- DC values and AC timing specifications for the following:
  - PCI I/O Unit
  - QDR
  - DDR SDRAM
  - C Bus
  - POS-PHY and CSIX
  - SlowPort I/O Buffer
  - GPIO
  - JTAG
  - Serial Port

4.1 Absolute Maximum Ratings

Operating beyond the functional operating temperature ranges shown in Table 33 is not recommended and extended exposure beyond the functional operating temperature range may affect reliability. Table 34 lists the functional operating voltage range.

Table 33. Functional Operating Temperature Range

Parameter	Minimum	Maximum	Maximum Junction Temperature	Comment
Commercial temperature operating range	0°C	70°C	120°C	Refer to the IXP2400 *Network Processor Thermal Design Considerations Application Note*.
Extended temperature operating range	-40°C	85°C		Refer to the IXP2400 *Network Processor Thermal Design Considerations Application Note*.

Table 34. Functional Operating Voltage Range

Supply Name	Voltage (V) 400 MHz (B Stepping)	Voltage (V) 600 MHz (A and B Stepping)	Tolerance	Comments
VCC1.3	1.1[1]	1.30	±5%	Core supply for the IXP2400
VCCA1.3	1.1[1]	1.30	±5%	PLL supply: isolated from core. Low current.
VCC2.5	2.5	2.5	±5%	DDR SDRAM interface supply
VCC1.5	1.50	1.50	±3%	QDR SRAM interface supply
VCC3.3	3.3	3.3	±5%	Media Switch Fabric, PCI and misc.

1. For A-stepping (400-MHz) IXP2400, VCC1.3 and VCCA1.3 is 1.3V.

Table 35. Power Totals for B Stepping

Operating Frequency	Typical[1]	Maximum	Units
400 MHz	9.3	11.52	W
600 MHz	12.85	16.05	W

1. Typical values are based on a full-duplex 2G Ethernet design with one QDR channel used.

The measurements shown in Table 36 were taken by running a reference application (IPv4 forwarding + QoS) at OC-48 line rate with worst-case minimum size 48-byte packets.

Table 36. Maximum Power for Thermal Solution[1]

Supply Name	A Stepping		B Stepping		Units
	400 MHz (1.3V)	600 MHz (1.3V)	400 MHz (1.1V)[2]	600 MHz (1.3V)	
VCC1.3	7.41	11.05	4.4	8.26	W
VCCA1.3					
VCC1.5[3]	2.03	2.03	2.25	2.25	W
VCC2.5[3]	2.30	2.30	1.75	1.75	W
VCC3.3	2.45	2.45	2.45	2.45	W
Totals	**14.19**	**17.83**	**10.85**	**14.71**	**W**

1. Values presented include core and I/O.
2. 400-MHz (B Stepping) IXP2400 devices should use a 1.1V core power supply; 600-MHz IXP2400 devices can only use a 1.3V core power supply.
3. QDR and DDR I/O values include power consumption from termination.

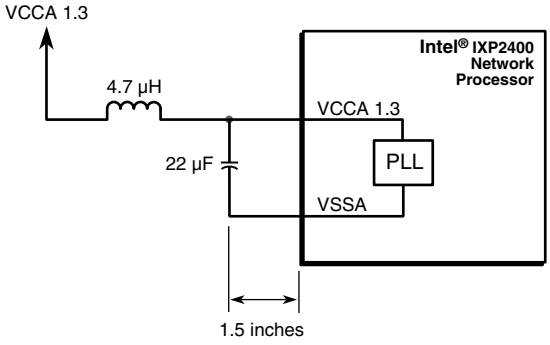
The values in Table 37 are used for the board design on each power rail. The measurements were taken by running synthetic tests that maximize the activity factors for a particular power supply rail, one rail at a time, and are expected to reflect the worst-case power consumption for each power supply rail under artificial conditions.

Table 37. Maximum Power Consumption by Power Supply[1]

Supply Name	A Stepping		B Stepping		Units
	400 MHz (1.3V)	600 MHz (1.3V)	400 MHz (1.1V)[2]	600 MHz (1.3V)	
VCC1.3	8.92	13.62	4.46	8.59	W
VCCA1.3					
VCC1.5[3]	2.67	2.67	2.34	2.49	W
VCC2.5[3]	3.15	3.15	1.75	2.00	W
VCC3.3	2.97	2.97	2.97	2.97	W
Totals	**17.71**	**22.41**	**11.52**	**16.05**	**W**

1. Values presented include core and I/O.
2. 400-MHz (B Stepping) IXP2400 devices should use a 1.1V core power supply; 600-MHz IXP2400 devices can only use a 1.3V core power supply.
3. QDR and DDR I/O values include power consumption from termination.

Figure 12. PLL Power Supply Connection



4.1.1 Reducing Power Consumption

The following are recommendations to help reduce power consumption:

- Don't connect unused QDR channels (remove any termination for the channel; do not connect anything to it).
- If only one or two SRAM chips suffice for an application and the board design allows the IXP2400 and the SRAM chips to be close to each other, termination can be removed or termination resistance can be increased. For instance, on boards that demonstrate good signal integrity and have the IXP2400 and SRAM chips placed within two inches of each other, there may be no need for termination.
- Use only as much of the 32-bit MSF interface as needed; this minimizes the power consumption at the unused sub-channels.

- Use only 32-bit and/or 33-MHz PCI if it is adequate for the application. Power consumption in such cases is lower than PCI 64-bit/66-MHz.

4.2 AC/DC Specifications

4.2.1 Clock Timing Specifications

Figure 13. SYS_CLK Timing

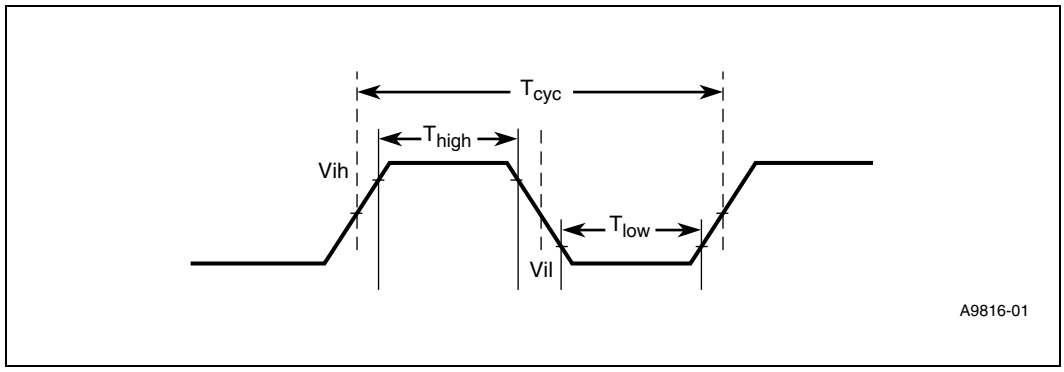


Table 38. SYS_CLK DC Specification

Symbol	Parameter	Minimum	Maximum	Maximum Duration	Unit
V_{il}	Input low voltage	0	0.5	—	V
V_{ih}	Input high voltage	2.4	3.3	—	V
VOV	Overshoot	0	0.2	3% of SYS_CLK cycle	V
VUS	Undershoot	-0.2	0		V

Table 39. SYS_CLK AC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
SYS_CLK[1]	Reference clock frequency	66	—	100	MHz
T_{cyc}	SYS_CLK cycle time	10	—	16.6	ns
T_{high}	SYS_CLK high time	4.2	—	—	ns
T_{low}	SYS_CLK low time	4.2	—	—	ns
—	SYS_CLK slew rate[2]	2	—	4	V/ns

1. These specifications apply only to SYS_CLK and are very preliminary estimates.
2. 0.2 x VCC3.3 to 0.6 x VCC3.3.
3. When the IXP2400 powers up, the reference clock should start running as soon as possible.

4.2.2 PCI I/O Unit

This section specifies the following electrical behavior for the PCI I/O Unit.

- Absolute maximum ratings
- DC specifications
- AC timing specifications

4.2.2.1 PCI Absolute Maximum Ratings

Table 40. Absolute Maximum PCI Ratings

Parameter	Minimum	Maximum	Comment
Maximum voltage applied to signal pins	-0.3 V	3.6 V	
Supply voltage (I/O), VCC3.3	3.0 V	3.6 V	3.3 V supply

The power specifications listed in Table 41 are based on the following assumption:

- PCI Bus Frequency (PCI_CLK) = 66 MHz.

Table 41. PCI Typical and Maximum Power

Parameter	Typical[1]	Maximum	Comment
VCC3.3	0.37 W	0.92 W	3.3 V supply

1. Typical power measured at nominal supply voltages. The power consumption from the 1.3V supply is very low and will be ignored.

4.2.2.2 PCI DC Specifications

In Table 42, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (-) current. Input leakage currents include high-Z output leakage for all bidirectional buffers with tri-state outputs. These electrical specifications are preliminary and subject to change.

Table 42. PCI DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	0.5 x VCC3.3	VCC3.3 + 0.5 V
V_{il}	Input low voltage	—	—	0.3 x VCC3.3
V_{oh}	Output high voltage	Ioh = -0.5 mA	0.9 x VCC3.3	—
V_{ol}	Output low voltage	Iol = 1.5 mA	—	0.1 x VCC3.3
I_i	Input leakage current[1]	0 <Vin< VCC3.3	—	± 10 µA
C_{load}	Pin capacitance	—	5 pF	10 pF

1. Input leakage currents include high-impedance output leakage for all bidirectional buffers with tri-state outputs.

4.2.2.3 PCI Overshoot/Undershoot Specifications

The PCI I/Os are designed to tolerate overshoot and undershoot associated with normal I/O switching. However, excessive overshoot or undershoot of I/O signals can cause the device to latchup. Table 43 specifies limits on I/O overshoot and undershoot that should never be exceeded.

Table 43. Overshoot/Undershoot Specifications

Pin Type	Undershoot	Overshoot	Maximum Duration
Input	VSS – 1V	VCC3.3 + 1V	6 ns
Output	VSS – 0.74V	VCC3.3 + 0.74V	4 ns
Bidirectional	VSS – 0.74V	VCC3.3 + 0.74V	4 ns

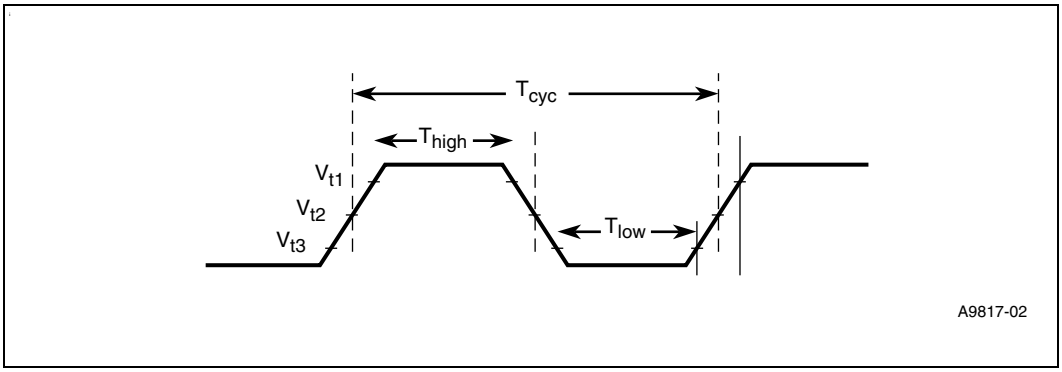
4.2.2.4 PCI AC Specifications

The AC specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal.

The PCI pins support the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.2*. See that document for a complete description of the PCI I/O protocol and pin AC specifications.

4.2.2.5 PCI Clock Signal AC Parameter Measurements

Figure 14. PCI Clock Signal AC Parameter Measurements



Vt1 = 0.5*VCC3.3
Vt2 = 0.4*VCC3.3
Vt3 = 0.3*VCC3.3

Table 44. 66-MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	PCI_CLK cycle time	15		ns
T_{high}	PCI_CLK high time	6	—	ns
T_{low}	PCI_CLK low time	6	—	ns
—	PCI_CLK slew rate[1]	1.5	4	V/ns

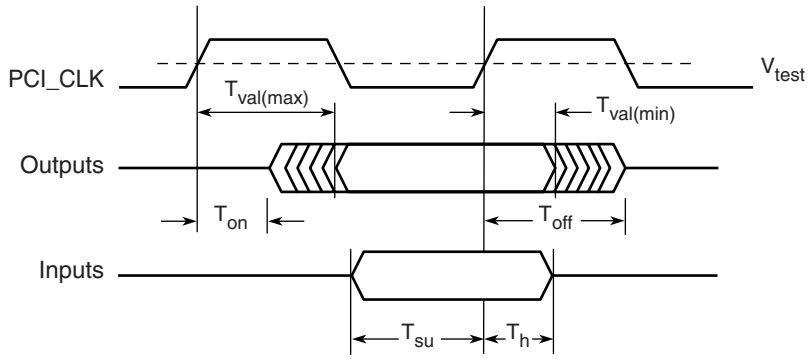
1. 0.3 VCC3.3 to 0.6 VCC3.3

Table 45. 33-MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	PCI_CLK cycle time	30	—	ns
T_{high}	PCI_CLK high time	11	—	ns
T_{low}	PCI_CLK low time	11	—	ns
—	PCI_CLK slew rate[1]	1	4	V/ns

1. 0.3 VCC3.3 to 0.6 VCC3.3.

Figure 15. PCI Bus Signals



Note: V_{test} = 0.4 VCC3.3 for 3.3 volt PCI signals

A9393-01

4.2.2.6 PCI Bus Signals Timing

Table 46. 33-MHz PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay, bused signals	2	11	ns
T_{val} (point-to-point)	CLK to signal valid delay, point-to-point signals[1]	2	12	ns
T_{on}	Float to active delay	2	—	ns
T_{off}	Active to float delay	—	28	ns
T_{su}[2]	Input setup time to CLK, bused signals[3]	7	—	ns
T_{su} (point-to-point)	Input setup time to CLK, point-to-point signals (GNT_L)[1]	10	—	ns
T_{su} (point-to-point)	Input setup time to CLK, point-to-point signals (REQ_L)[1]	12	—	ns
T_h[4]	Input signal hold time from CLK	0.5	—	ns

1. Point-to-point signals are REQ_L, GNT_L.
2. The setup time is measured with a 1–4V/ns input slew rate.

3. Bused signals are AD, CBE_L, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, DEVSEL_L, STOP_L
4. These parameters are at variance with those in the *PCI Local Bus Specification, Revision 2.2*.

Table 47. 66-MHz PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay, bused signals	2	6	ns
T_{val} (point-to-point)	CLK to signal valid delay, point-to-point signals[1]	2	6	ns
T_{on}	Float to active delay	2	—	ns
T_{off}	Active to float delay	—	—	ns
T_{su}[2]	Input setup time to CLK, bused signals[3]	3	—	ns
T_{su} (point-to-point)	Input setup time to CLK, point-to-point signals[1]	5	—	ns
T_h[4]	Input signal hold time from CLK	0.5	—	ns

1. Point-to-point signals are REQ_L, GNT_L.
2. The setup time is measured with a 1–4V/ns input slew rate.
3. Bused signals are AD, CBE_L, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, DEVSEL_L, STOP_L.
4. These parameters are at variance with those in the *PCI Local Bus Specification, Revision 2.2*.

4.2.3 SRAM

Please note that the data presented in Table 48 was gathered using a load circuit with attributes as shown in Figure 16.

Table 48. QDR DC Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit	Notes
V_{IH}	Input high voltage (Logic 1)	—	VREF + 0.1	VCC1.5 + 0.1	V	3
V_{IL}	Input low voltage (Logic 0)	—	-0.1	VREF - 0.1	V	3
I_{LI}	Input leakage current	0V ≤VIN≤ VCC1.5	0	20	µA	
I_{LO}	Output leakage current	Output(s) disabled, 0V≤ VIN≤ VCC1.5	0	20	µA	
V_{OH} (Low current)	Output high voltage	|IOH| ≤ 0.1 mA (when the I/O is tristated)	VCC1.5/2 - 0.2	VCC1.5/2 + 0.2	V	3, 5
V_{OH}		Note 1	VCC1.5 x .75 - 0.1	VCC1.5 x .75 - 0.1	V	3, 5
V_{OL} (Low current)	Output low voltage	|IOL| ≤ 0.1 mA (when the I/O is tristated)	VCC1.5/2 - 0.2	VCC1.5/2 + 0.2	V	3, 5
V_{OL}		Note 2	VCC1.5/4 - 0.1	VCC1.5/4 + 0.1	V	3, 5
VCC1.5	Isolated output buffer supply	—	1.4	1.6	V	3
V_{REF}	Reference voltage	—	0.7	0.8	V	3

NOTES:
1. Outputs are impedance-controlled. | IOH | = (VCC1.5/2)/(Rz) for values of Rz = 50 ohms.
2. Outputs are impedance-controlled. IOL = (VCC1.5/2)/((Rz) for values of Rz = 50 ohms.
3. All voltages referenced to VSS (GND).
4. AC load current is higher than the shown DC values. AC I/O (IBIS model) curves are available in the IXA HDK2400.
5. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

Figure 16. QDR Load Circuit

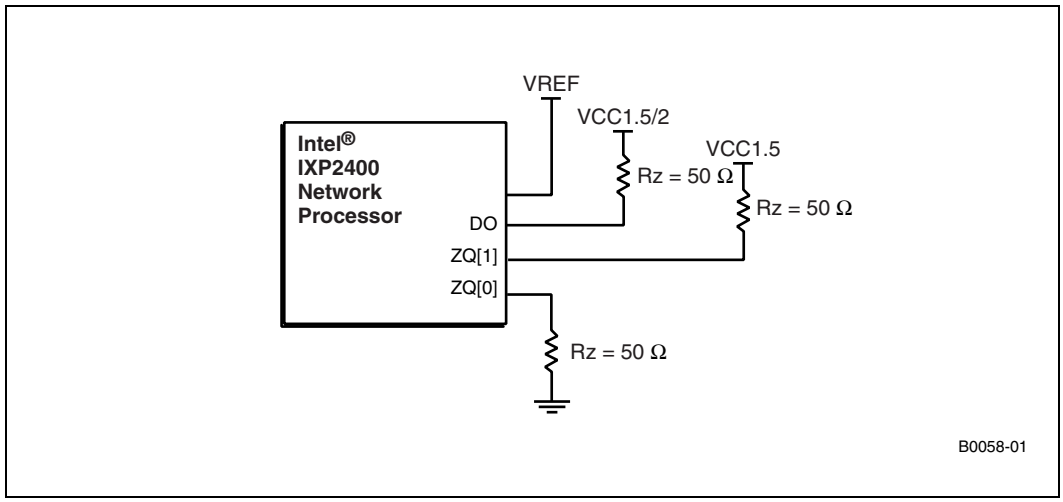


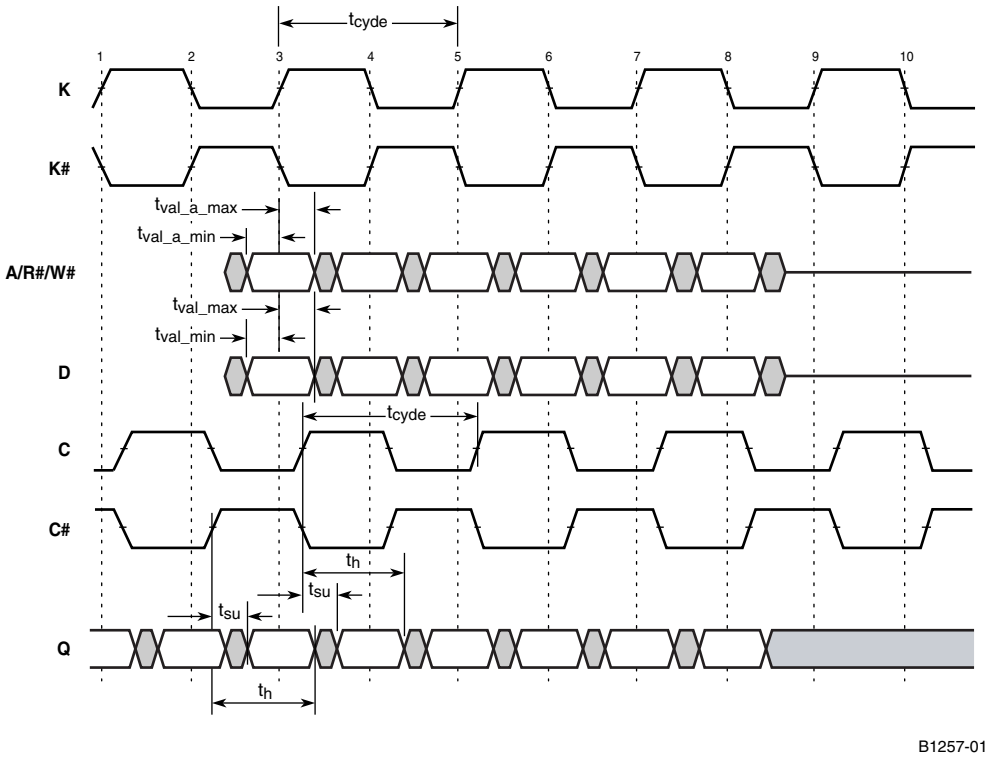
Table 49. QDR and QDRII Signal Timing Parameters

Symbol	Parameter	QDRII (200 MHz)		QDR/QDRII (150 MHz)		QDR/QDRII (133 MHz)		QDR/QDRII (100 MHz)	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Tcycle	Clock cycle time	5.0	—	6.6	—	7.5	—	10.0	—
Tvalmin	Tval clock to data output valid (K/K#)	0.85	—	1.25	—	1.25	—	1.95	—
Tvalmax		—	0.85	—	1.25	—	1.25	—	1.95
Tval_a_min	Clock to R/W control output valid and address[1]	0.85	—	1.25	—	1.25	—	1.95	—
Tval_a_max		—	0.85	—	1.25	—	1.25	—	1.95
Tsu	Tsu[2] (setup time)	—	-0.60	—	-0.95	—	-1.0	—	-1.7
Th	Th (hold time)	1.80	—	2.35	—	2.5	—	2.8	—
Tjt	Clock cycle-to-cycle jitter	100 psec	—	150 psec	—	150 psec	—	200 psec	—
—	C/C# duty cycle	2.4	2.6	3.2	3.4	3.65	3.85	4.9	5.1
—	K/K# duty cycle	2.4	2.6	3.2	3.4	3.65	3.85	4.9	5.1

1. If reference K clock any given pins, including data and controls, the maximum skew is ±300 psec.
2. The setup time is measured before the rising edge of the clock; when the measurements for Tsu are prefaced by a minus symbol (“-”), the data is actually after the rising edge of the clock. When the measurements for Tsu are prefaced by a plus symbol (“+”), the data is actually before the rising edge of the clock.
   The setup time is measured with 1V/ns input slew rate.

Figure 17 illustrates the timing goals for the IXP2400 QDRII interface. For QDR, it is necessary to delay the input clock appropriately to acheive the required setup and hold time. For example, for QDR at 100 MHz, delay the input clock by 2.1 ns compared to data. The clock will be shifted by 2.5 ns by internal DLL and hence strobe for the data at 4.6 ns.

Figure 17. QDRII Timing Reference



4.2.4 DDR SDRAM

Table 50 lists the DDR SDRAM DC parameters. Table 51 lists the AC parameters.

Table 50. DDR SDRAM DC Parameters for 100/150 MHz

Symbol	Parameter	Minimum	Maximum	Unit
V_{DREF}	DDR reference voltage	0.48 x VCC2.5	0.52 x VCC2.5	—
V_{OH}	Output high voltage	VCC2.5 x .75 - 0.15	VCC2.5 x .75 + 0.15	V
V_{OL}	Output low voltage	VCC2.5/4 - 0.15	VCC2.5/4 + 0.15	V
I_{OH}	Output high current	18	22	mA
I_{OL}	Output low current	18	22	mA
I_{Leak}	Input leakage current	-10	+10	µA
VIL (DC)	input low voltage, DC	—	VDREF - 0.15	V
VIH (DC)	DDR input high voltage, DC	VDREF + 0.15	—	V

Table 50. DDR SDRAM DC Parameters for 100/150 MHz (Continued)

Symbol	Parameter	Minimum	Maximum	Unit
VIL (AC)	DDR input low voltage, AC	—	VDREF - 0.31	V
VIH (AC)	DDR input high voltage, AC	VDREF + 0.31	—	V
CIO	DDR input/output pin capacitance	4.690	5.370	pF

Table 51. DDR SDRAM AC Parameters for 100/150 MHz

Symbol	Parameter	150 MHz		100 MHz		Unit
		Min	Max	Min	Max	
Tck	D_CK period	6.6	—	10	—	ns
Tck (high)	D_CK high time	3.11	—	4.67	—	ns
Tck (low)	D_CK low time	3.19	—	4.79	—	ns
Tjt (jitter time)	D_CK cycle to cycle	—	132	—	198	psec
TSKEW tDQSCK	Skew between any system memory differential clock pair	—	+ or - 170 (340 total)	—	+ or - 255 (510 total)	psec
TCKVB	D_RAS_L, D_CAS_L, D_WE_L, D_A[12:0], D_BA[1:0]. Valid Before CK rising Edge	2.50	—	3.99	—	ns
TCKVA	D_RAS_L, D_CAS_L, D_WE_L, D_A[12:0], D_BA[1:0]. Valid	3.10	—	3.49	—	ns
TCKE_VB	D_CKE_[1:0]. Valid Before D_CK Rising Edge	2.50	—	3.99	—	ns
TCKE_VA	D_CKE_[1:0]. Valid After D_CK Rising Edge	3.10	—	3.49	—	ns
TCS_VB	D_DM_[8:0], D_UNUSED_CS_L_2, D_CS_L[1:0]. Valid Before D_DQS Rising Edge	2.50	—	3.99	—	ns
TCS_VA	D_DM_[8:0], D_UNUSED_CS_L_2, D_CS_L[1:0]. Valid After D_DQS Rising Edge	3.10	—	3.49	—	ns
TDVB	D_DQ[63:0], D_ECC[7:0] Valid Before D_DQS[1:0] Rising or Falling Edge	0.95	—	1.25	—	ns
TDVA	D_DQ[63:0], D_ECC[7:0] valid After D_DQS[1:0] rising or falling edge	0.95	—	1.25	—	ns
TSU	D_DQ and D_ECC Input Setup Time to D_DQS Rising or Falling Edge		-0.9		-0.7	ns
THD	D_DQ and D_ECC Input Hold Time to D_DQS Rising or Falling Edge	2.5	—	3.5	—	ns
TDSS	D_DQS Falling Edge Output Access Time to D_CK Rising Edge	2.77	—	4.16	—	ns
TDSH	D_DQS Falling Edge Output Access Time from D_CK Rising Edge	2.80	—	4.21	—	ns
TWPRE	D_DQS Write Preamble Duration	4.65	—	6.98	—	ns

Table 51. DDR SDRAM AC Parameters for 100/150 MHz (Continued)

Symbol	Parameter	150 MHz		100 MHz		Unit
		Min	Max	Min	Max	
TWPST	D_DQS Write Postamble Duration	3.19	—	4.78	—	ns
TDQSS	D_CK Rising Edge Output Access Time, Where a Write Command is Referenced, to the First D_DQS Rising Edge	5.99	7.08	8.99	10.61	ns
TPOE	D_CK Rising Edge Output Access Time, Where a Write Command is Referenced, to the D_DQS Preamble Falling Edge	—	1.96	—	2.94	ns
TRCVENOUT	D_CK Rising Edge Output Access Time: A Read Command is Referenced, to the D_RCVENOUT_L Falling Edge	9.45 (tCKlow= 2.0) 12.78 (tCKlow= 2.5)	10.31 (tCKlow= 2.0) 13.64 (tCKlow= 2.5)	14.17 (tCKlow= 2.0) 19.17 (tCKlow= 2.5)	15.47 (tCKlow= 2.0) 20.47 (tCKlow= 2.5)	ns
TSurcv	D_RCVENIN_L Falling Edge Setup Time to the First D_DQS Rising Edge	3.13	—	4.7	—	ns
THDrcv	D_RCVENIN_L Falling Edge Hold Time to the First D_DQS Rising Edge	-0.87	—	-1.30	—	ns
TpreHDrev	D_RCVENIN_L Falling Edge Hold Time to the First D_DQS Preamble Falling Edge	-0.87	—	-1.30	—	ns

4.2.4.1 AC Timing Diagrams

This section provides the AC timing diagrams for the DDR SDRAM interface.

Figure 18. Data and Error Correction Setup/Hold Relationship to/from Data Strobe (Read Operation)

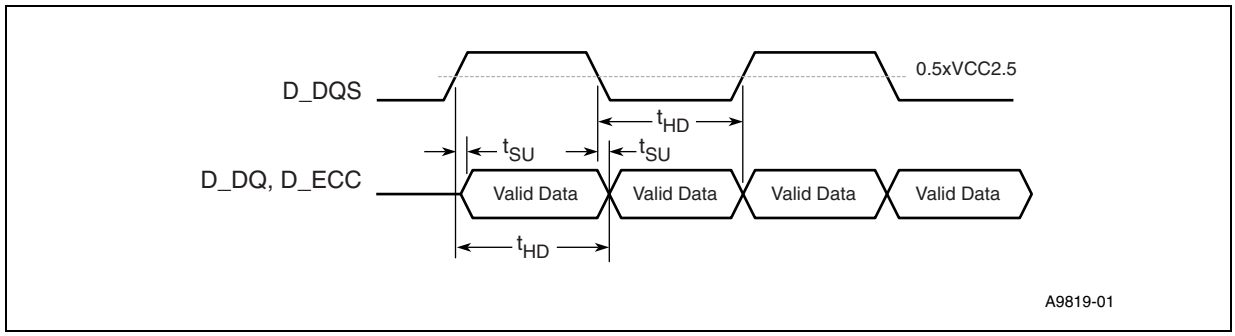


Figure 19. Data and Error Correction Valid Before and After Data Strobe (Write Operation)

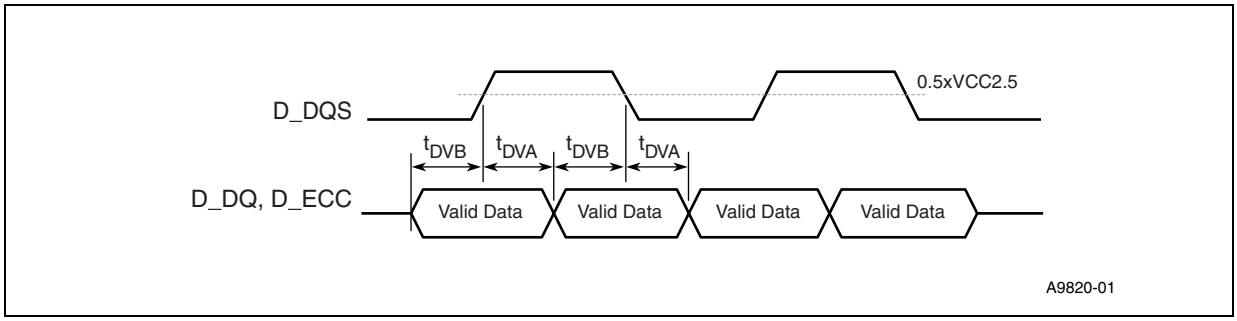


Figure 20. Write Preamble Duration

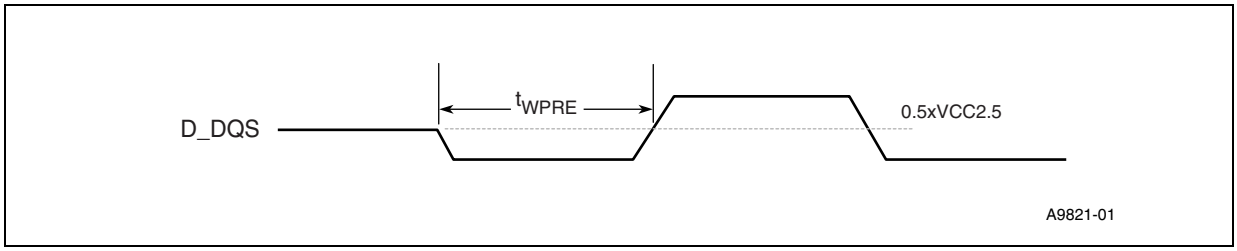


Figure 21. Write Postamble Duration

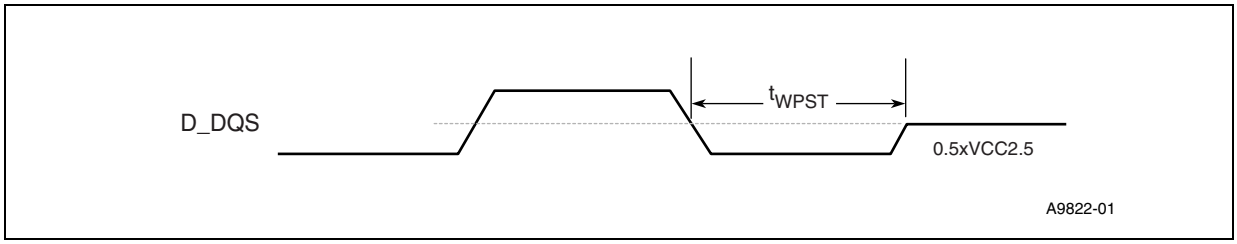


Figure 22. Command Signals Valid Before and After Clock Rising Edge

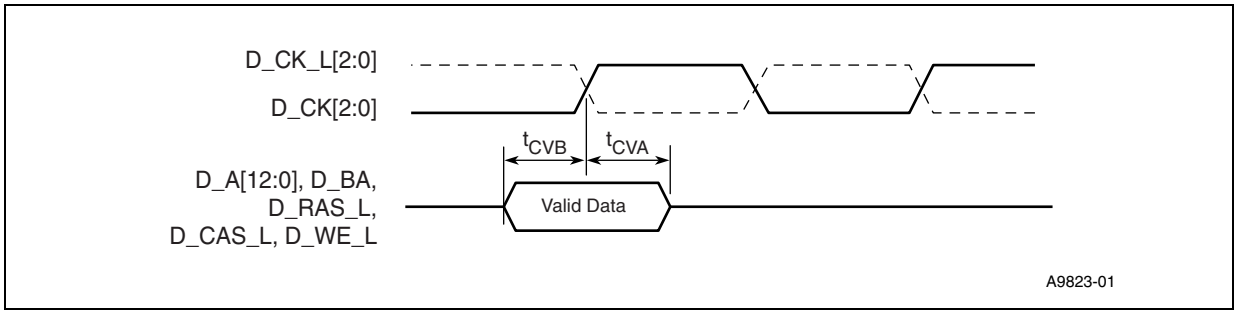


Figure 23. Clock Enable Valid Before and After Clock Rising Edge

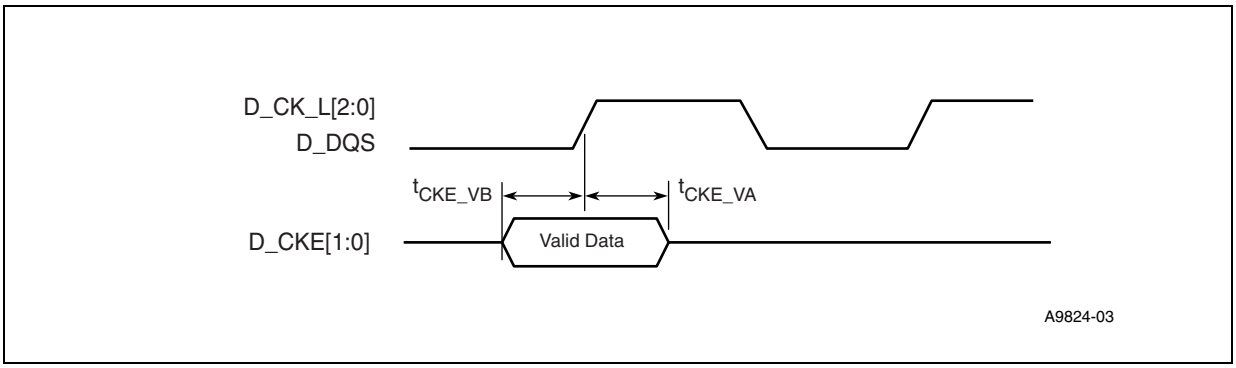


Figure 24. Chip Select Valid Before and After Clock Rising Edge

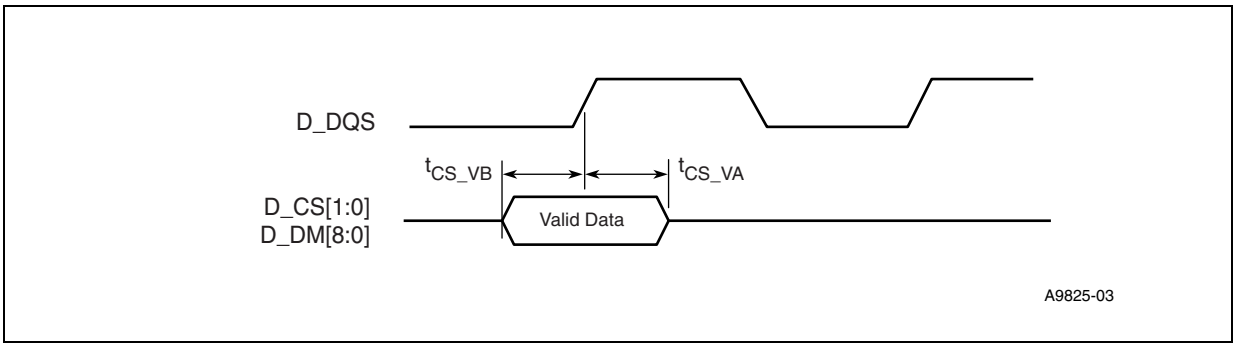


Figure 25. Clock Cycle Time

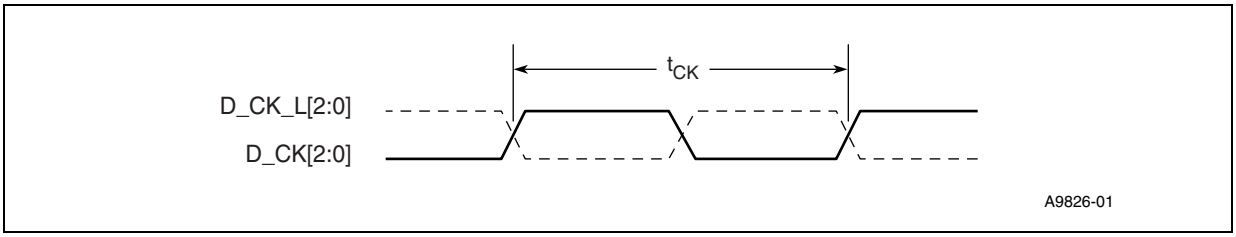


Figure 26. Skew Between Any System Memory Differential Clock Pair

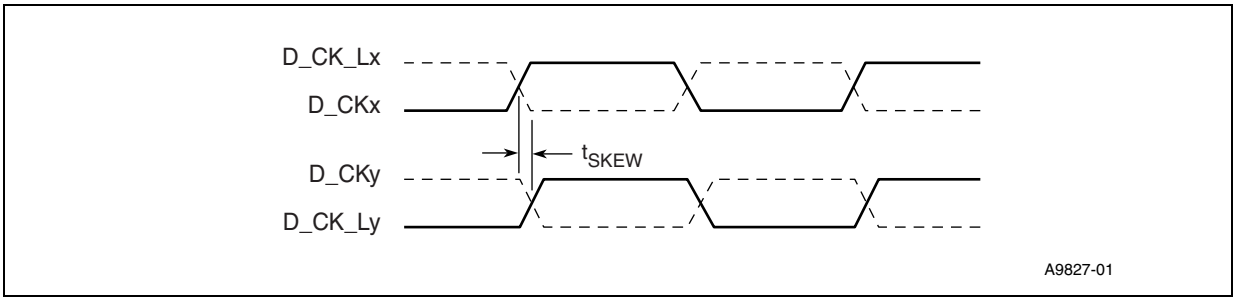


Figure 27. Clock High Time

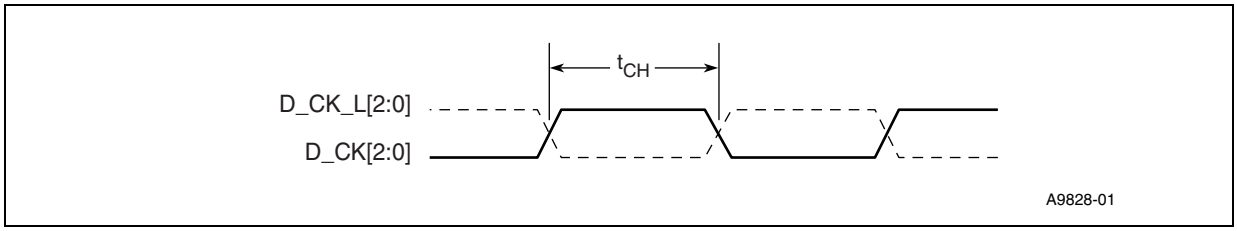


Figure 28. Clock Low Time

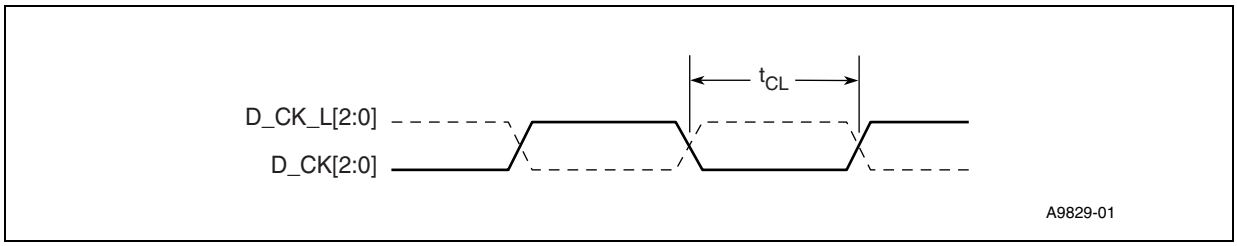


Figure 29. Data Strobe Falling Edge Output Access Time to Clock Rising Edge

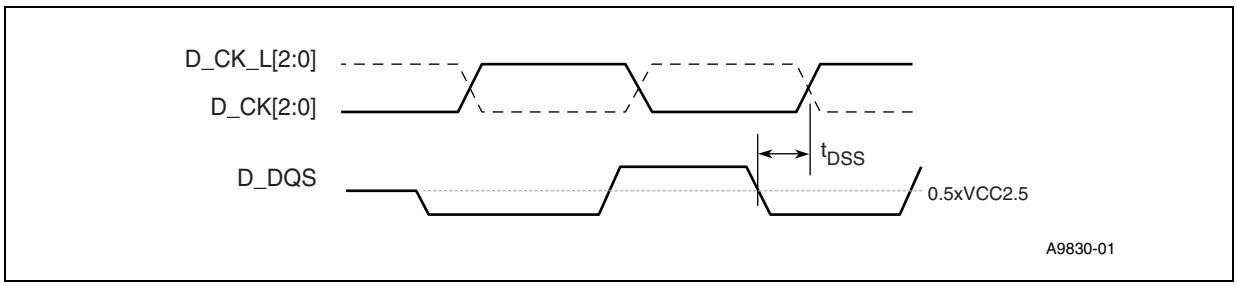


Figure 30. Data Strobe Falling Edge Output Access Time from Clock Rising Edge

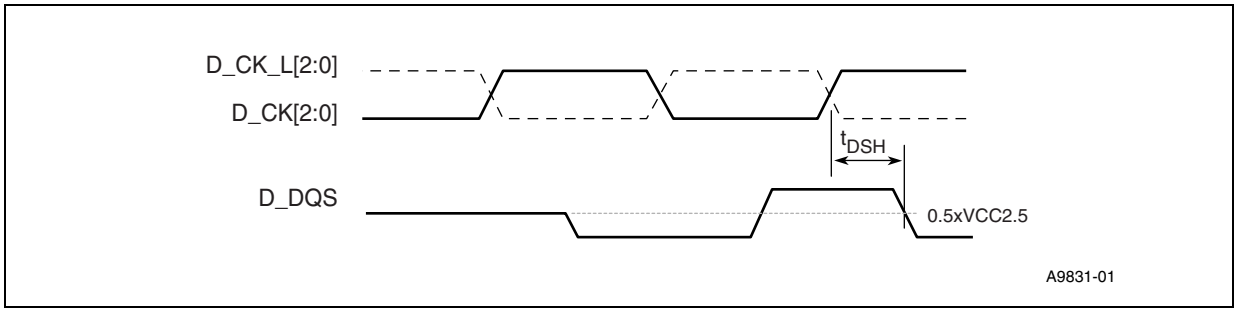


Figure 31. Clock Rising Edge Output Access Time to the First Data Strobe Rising Edge

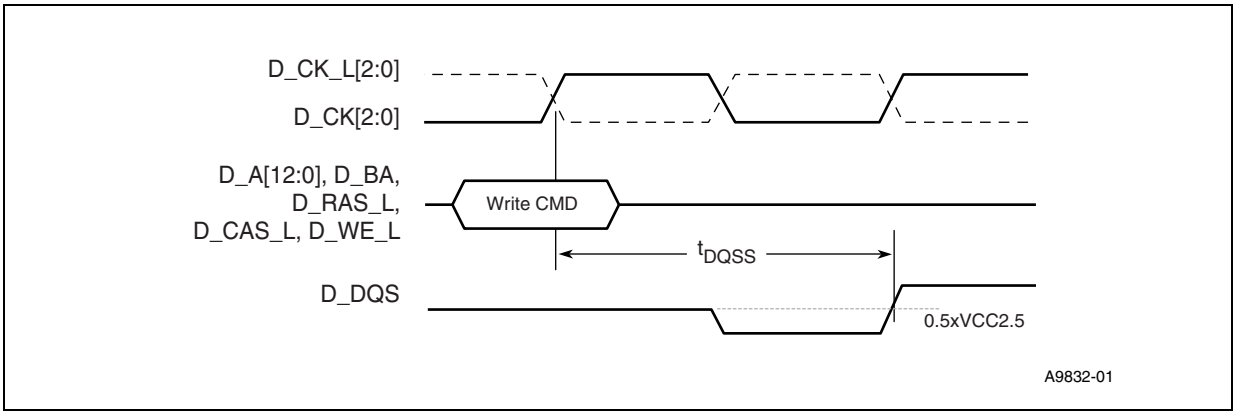


Figure 32. Clock Rising Edge Output Access Time to the Data Strobe Preamble Falling Edge

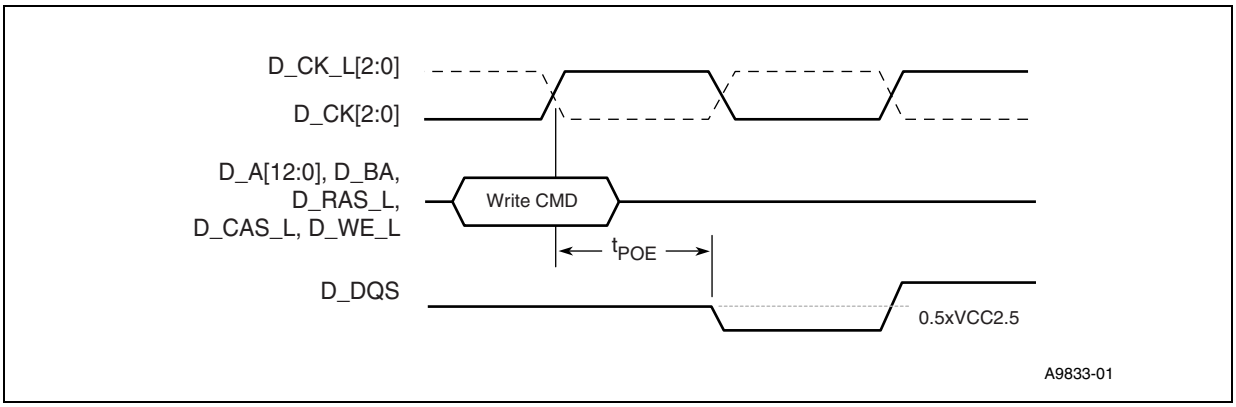


Figure 33. Clock Rising Edge Output Access Time to Output Clock Falling Edge

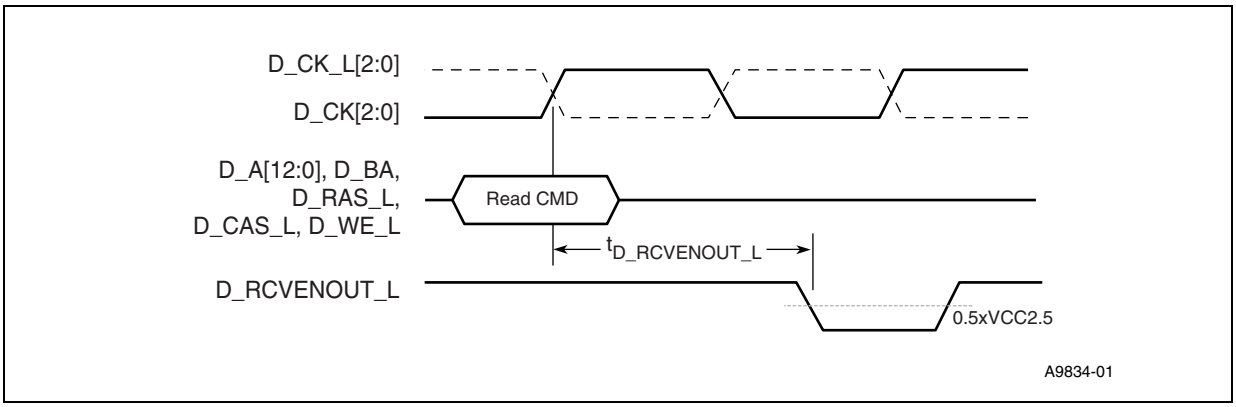


Figure 34. Input Clock Falling Edge Setup Time to the First Data Strobe Rising Edge

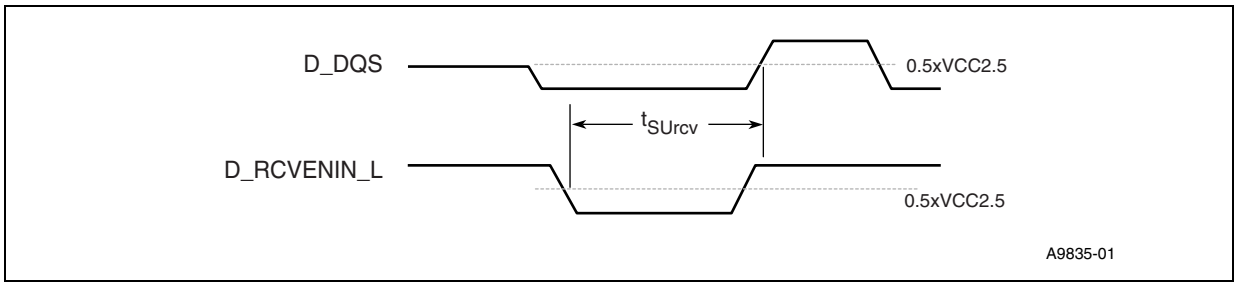


Figure 35. Input Clock Rising Edge Hold Time from the First Data Strobe Rising Edge

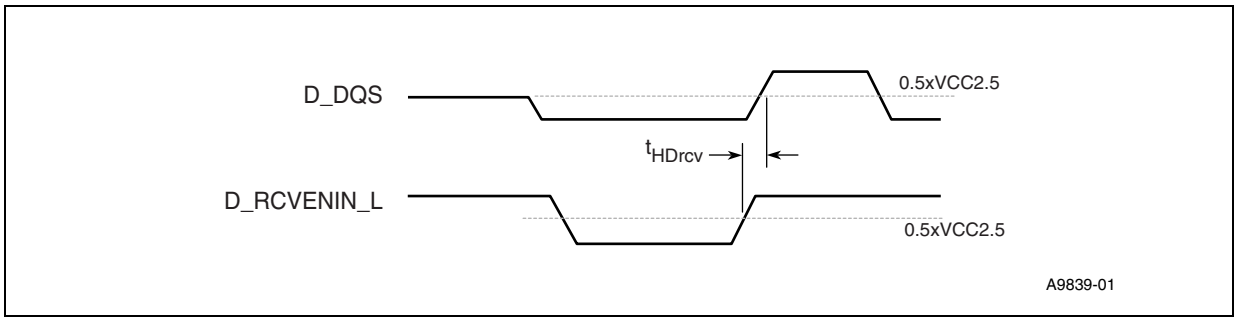
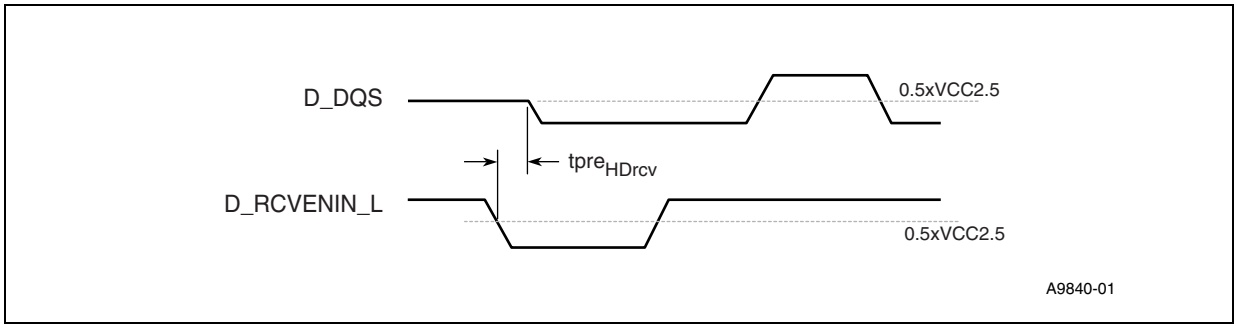


Figure 36. Input Clock Falling Edge Hold Time from the Data Strobe Preamble Falling Edge



4.2.5 Media and Switch Fabric (MSF) Interface

This section describes the parameters for the MSF Interface. These parameters apply whether the bus is configured to carry either POS Level 2/SPI-3 packets/cells or UTOPIA 1/2/3 CSIX C-Frames.

The MSF Interface can operate at a maximum of 133 MHz with a 600-MHz IXP2400, and at a maximum of 104 MHz with a 400-MHz IXP2400.

4.2.5.1 DC Parameters

Table 52 lists applicable DC thresholds for the MSF.

Table 52. MSF (LVTTL) DC Thresholds

Symbol	Parameter	Condition	Min	Max
Vih	Input high	—	2.0V	—
Vil	Input low	—	—	0.8V
Voh	Output	Ioh = -8 mA	2.4V	—
Vol	Output low	Iol = 8 mA	—	0.5V
I_{Leak}	Input leakage current	—	-10 µA	+10 µA
Cload	Pin capacitance	—	—	10 pF

Table 53. MSF Overshoot/Undershoot Specifications

Pin Type	Undershoot	Overshoot	Maximum Duration
Input	VSS – 1V	VCC3.3 + 1V	6 ns
Output	VSS – 0.74V	VCC3.3 + 0.74V	4 ns

4.2.5.2 Media Clocks

Figure 37. Media Clock Timing

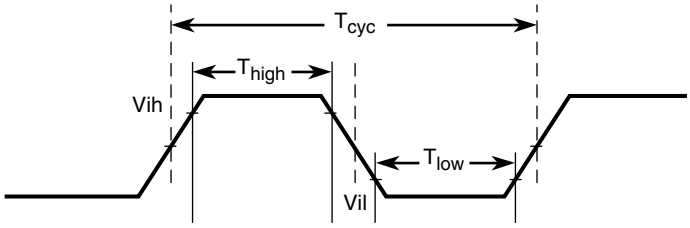


Table 54. Media Clock DC Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VL	Input low voltage	0	—	0.8	V
VH	Input high voltage	2.4	—	3.3	V
VOV	Overshoot	0	—	0.2	V
VUS	Undershoot	-0.2	—	0	V

Table 55. Media Clock AC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
T_{cyc}	CLK cycle time	8	—	40	ns
T_{high}	CLK high time	3.4	—	—	ns
T_{low}	CLK low time[2]	3.4	—	—	ns
—	CLK slew rate[1, 2]	2	—	4	V/ns

1. 0.3 VCC3.3 to 0.6 VCC3.3
2. Includes RXCLK01, RXCLK23, and TXCLK01, TXCLK23.

4.2.5.3 AC Parameters

Table 56. Media Interface Signal AC Parameters

Symbol	Parameter	600-MHz IXP2400 (Max of 150-MHz MSF)		400-MHz IXP2400 (Max of 104-MHz MSF)		Unit
		Min	Max	Min	Max	Unit
$T_{RXval01}$	Output valid delay from RXCLK01	1.2	3.4	1.2	3.6	ns
T_{RXsu01}	Input setup time to RXCLK01	1.0	—	1.5	—	ns
T_{RXh01}	Input hold time from RXCLK01	0.3	—	0.15	—	ns
$T_{RXval23}$	Output valid delay from RXCLK23	1.2	3.4	1.2	3.6	ns
T_{RXsu23}	Input setup time to RXCLK23	1.0	—	1.5	—	ns
T_{RXh23}	Input hold time from RXCLK23	0.3	—	0.15	—	ns
$T_{TXval01}$	Output valid delay from RXCLK01	1.2	3.4	1.2	3.6	ns
T_{TXsu01}	Input setup time to RXCLK01	1.0	—	1.5	—	ns
T_{TXh01}	Input hold time from RXCLK01	0.3	—	0.15	—	ns
$T_{TXval23}$	Output valid delay from RXCLK23	1.2	3.4	1.2	3.6	ns
T_{TXsu23}	Input setup time to RXCLK23	1.0	—	1.5	—	ns
T_{TXh23}	Input hold time from RXCLK23	0.3	—	0.15	—	ns

The IXP2400 supports the IXF6048 UTOPIA Level 3 (single 64-bit, 32-bit, or quad 8-bit), Level 2 (single 8/16-bit), and Level 1 (quad 8/16-bit) interface modes.

Figure 38 and Figure 39 illustrate receive and transmit, respectively, UTOPIA/POS/CSIX single interface, 32/16/8-bit databus, two clock cycle decode-response delay and no high-impedance outputs.

Figure 38. Receive UTOPIA/POS/CSIX

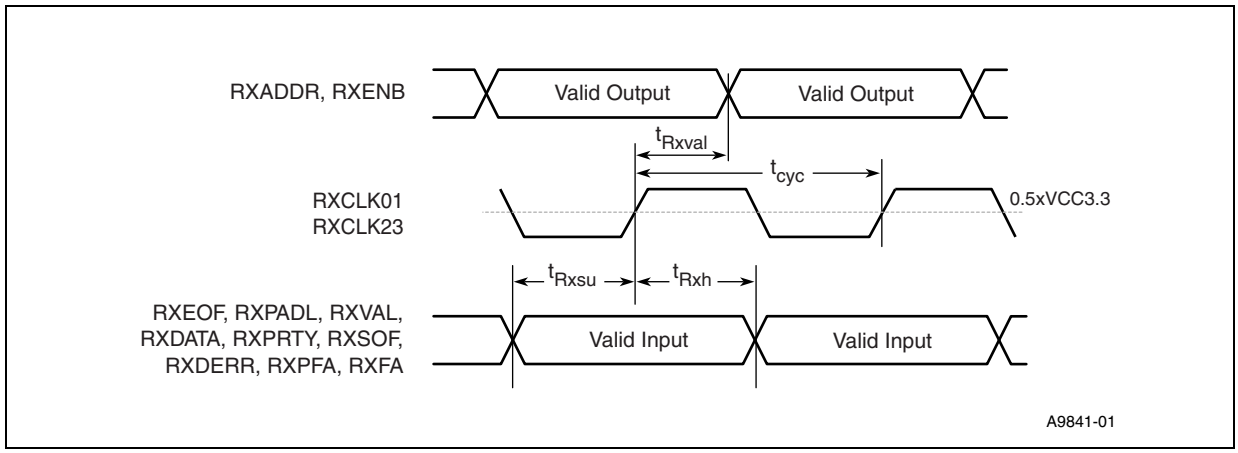
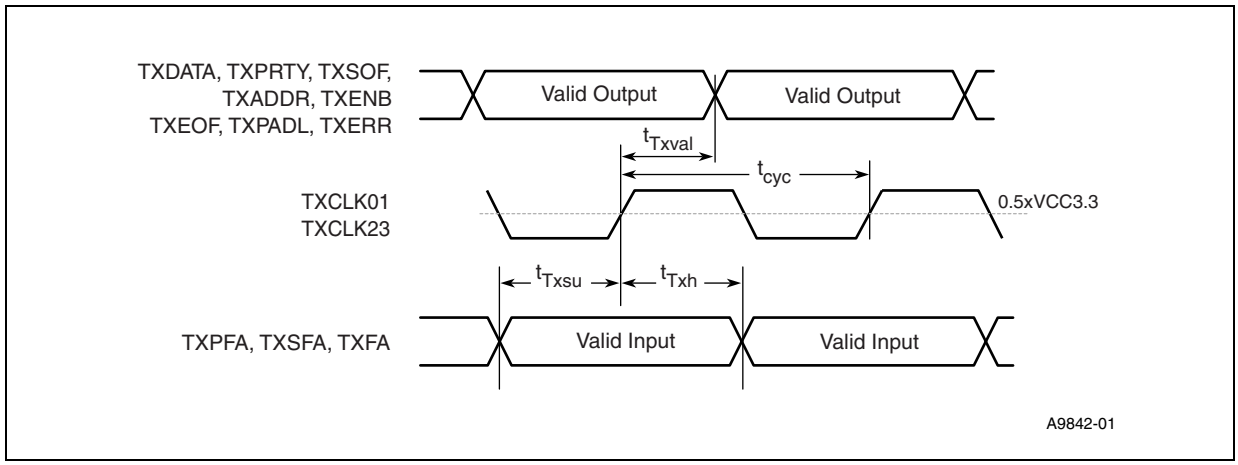


Figure 39. Transmit UTOPIA/POS/CSIX



4.2.6 CBus

Table 57 lists applicable driver DC thresholds for the CBus.

Table 57. CBus (LVTTL) Driver DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input High	—	2.0V	—
Vil	Input Low	—	—	0.8V
Voh	Output	Ioh = -8 mA	2.4V	—
Vol	Output Low	Iol = 8 mA		0.4V
I_{Leak}	Input Leakage Current	0<Vin<VCC3.3	-10 µA	+10 µA
C_{load}	Pin Capacitance	—	—	10 pF

4.2.7 SlowPort, GPIO, and Serial I/O Buffer

Table 58 lists the AC and DC parameters for the SlowPort and GPIO. The GPIO can be used with appropriate software in I^2C application. Refer to the Philips Semiconductor* I^2C bus specification for the DC and AC characteristics. The serial port consists of TXD, RXD, which are asynchronous relative to any device outside the IXP2400.

Table 58. SlowPort, GPIO, and Serial I/O Buffer AC/DC Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit	Notes
VIH	Input high (Logic 1) voltage	—	2.0	VCC3.3 + 0.3	V	—
VIL	Input low (Logic 0) voltage	—	-0.3	0.8	V	—
ILI	Input leakage current	—	-10.0	+10.0	µA	—
VOH	Output high voltage	IOH = -2.0 mA	2.4	—	V	1, 2
VOL	Output low voltage	IOL = 2.0 mA	—	0.4	V	1, 2
tr	Slew rate rising	Cload = 10 pF	1.3	5.1	V/ns	3
tf	Slew rate falling	Cload = 10 pF	0.9	4.7	V/ns	3
tr	Slew rate rising	Cload = 20 pF	1.1	3.4	V/ns	3
tf	Slew rate falling	Cload = 20 pF	0.7	3.4	V/ns	3
Cload	Pin capacitance	—	5	20	pF	3

1. All voltages referenced to Vss (GND).
2. AC load current is higher than the shown DC values.
3. For Cload greater than 20 pF or three or more devices, transceivers or clock buffers need to be used.

Table 59 timing applies to Mode 0, 1, 2, 3, and 4. Logic diagrams for these modes are presented in the *Intel* IXP2400 *Hardware Reference Manual*.

Figure 40. Mode 0 Single Write Transfer for Self-Timing Device — SlowPort

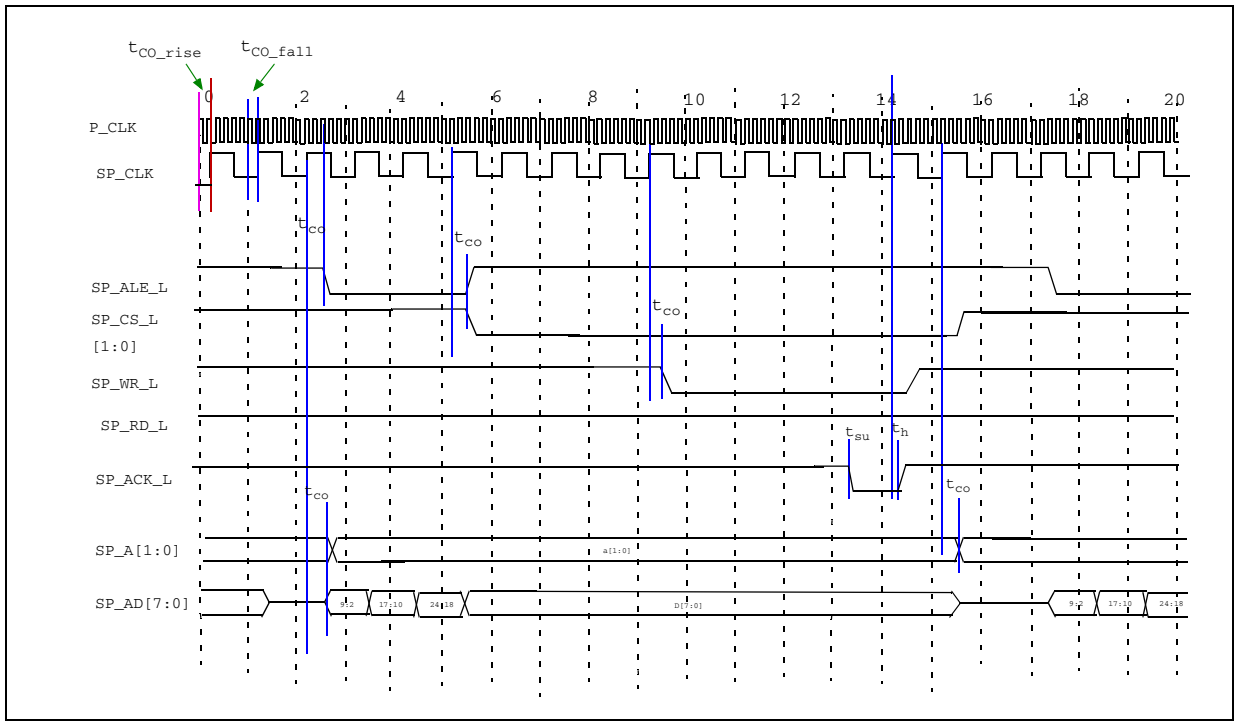


Table 59. SlowPort Write Timing

External Signals	tco rise (default[1]) (ns)		tco fall (default[2]) (ns)		th (ns)		tsu (ns)		tpw (ns)	
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
SP_CLK	3.0	1.4	3.7	3.3	—	—	—	—	—	—
SP_ALE	8.5	5.3	9.0	5.4	—	—	—	—	—	—
SP_CS[0]	8.4	5.3	9.0	5.4	—	—	—	—	—	—
SP_CS[1]	8.4	5.3	9.0	5.4	—	—	—	—	—	—
SP_WR	9.1	5.5	9.2	5.6	—	—	—	—	—	—
SP_RD	—	—	—	—	—	—	—	—	—	—
SP_ACK	—	—	—	—	0	0	6.8	4.5	—	—
SP_A[1:0]	8.4	5.3	9.0	5.4	—	—	—	—	—	—
SP_AD[7:0] output to external device	9.0	5.5	9.2	5.6	9.2	5.5	—	—	—	—

1. Default out timing delay is controlled by the TXE register. By default, this register is set to 1, i.e., two P clock cycles delay or 6666.66 psec. Minimum delay can be set to 0.
2. Default out timing delay is controlled by the TXE register. By default, this register is set to 1, i.e., two P clock cycles delay or 6666.66 psec. Minimum delay can be set to 0.

Table 60 timing applies to Mode 0, 1, 2, 3, and 4.

Figure 41. Mode 0 Single Read Transfer for Self-Timing Device — SlowPort

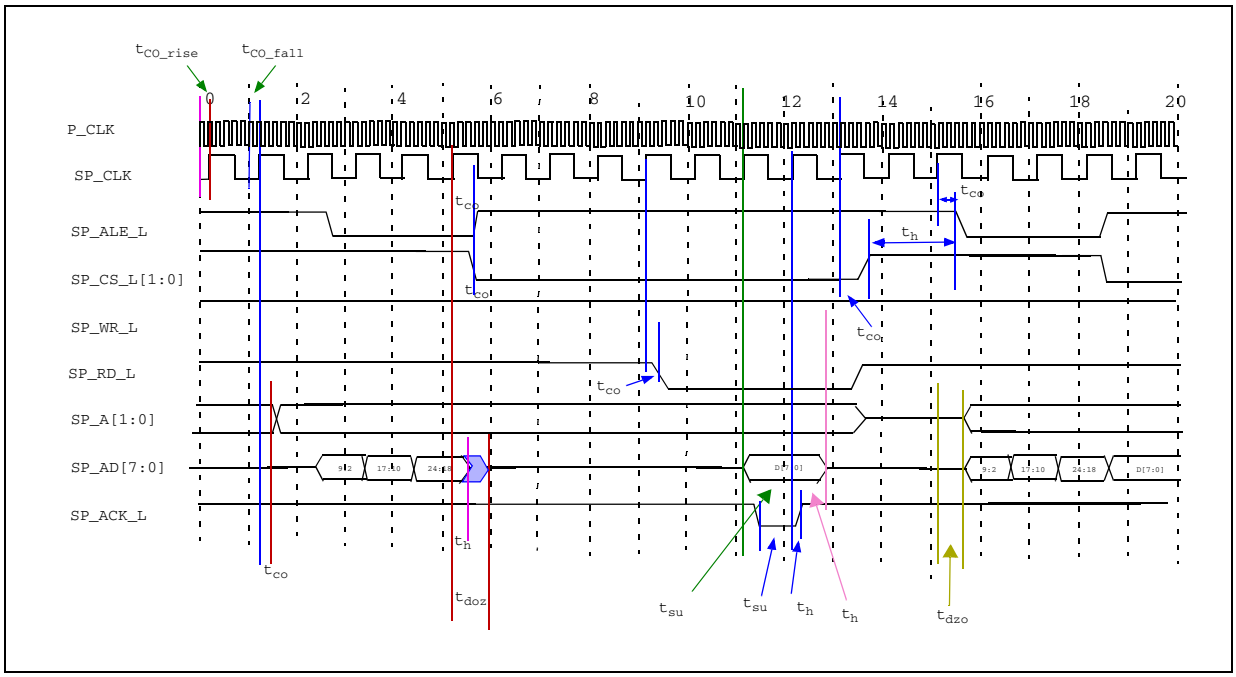


Table 60. SlowPort Read Timing

External Signals	tco rise (default) (ns)		tco fall (default) (ns)		th (ns)		tsu (ns)		tpw		toz/zo	
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min		
SP_ALE	8.5	5.3	9.0	5.4	—	—	—	—	—	—	—	—
SP_CS[0]	8.4	5.3	9.0	5.4	1	2						
SP_CS[1]	8.4	5.3	9.0	5.4	—	—	—	—	—	—	—	—
SP_WR					—	—	—	—	3	4		
SP_RD	9.1	5.4	9.2	7.2	—	—	—	—	—	—	—	—
SP_ACK	—	—	—	—	0	0	6.8	4.5	—	—	—	—
SP_AD[1:0]	8.4	5.3	9.0	5.4	—	—	—	—	—	—	—	—
SP_AD[7:0] output to external device	9.0	5.5	9.2	5.6	9.2	5.5	—	—	—	—	7.8	6.0
SP_AD[7:0] input from external device	—	—	—	—	0	0	7.2	4.6	—	—	—	—

1. The hold cycle can be programmed by SP_RTC1 and SP_RTC2 registers.
2. The hold cycle can be programmed by SP_RTC1 and SP_RTC2 registers.
3. The pulse width depends on the pulse-width parameter set in the SP_RTC1 and SP_RTC2 registers and the clock divisor as well. The minimum is 20 ns for one clock cycle at 50 MHz.

4. The pulse width depends on the pulse-width parameter set in the SP_RTC1 and SP_RTC2 registers and the clock divisor as well. The minimum is 20 ns for one clock cycle at 50 MHz.

4.2.8 JTAG

4.2.8.1 JTAG DC Electrical Characteristics

Table 61. JTAG DC Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit	Notes
VIH	Input high (Logic 1) voltage	—	2.0	VCC3.3 + 0.3	V	1
VIL	Input low (Logic 0) voltage	—	-0.3	0.8	V	—
ILI	Input leakage current	Output(s) disabled, 0V ≤ Vin ≤ VDD	-10.0	+10.0	µA	—
VOH	Output high voltage	IOH = -2.0 mA	2.4	—	V	1, 2
VOL	Output low voltage	IOL = 2.0 mA		0.4	V	1, 2
VCC3.3	Supply voltage	—	3.0	3.6	V	1

1. All voltages referenced to Vss (GND).
2. AC load current is higher than the shown DC values.

4.2.8.2 JTAG AC Characteristics

Figure 42. Boundary Scan General Timing

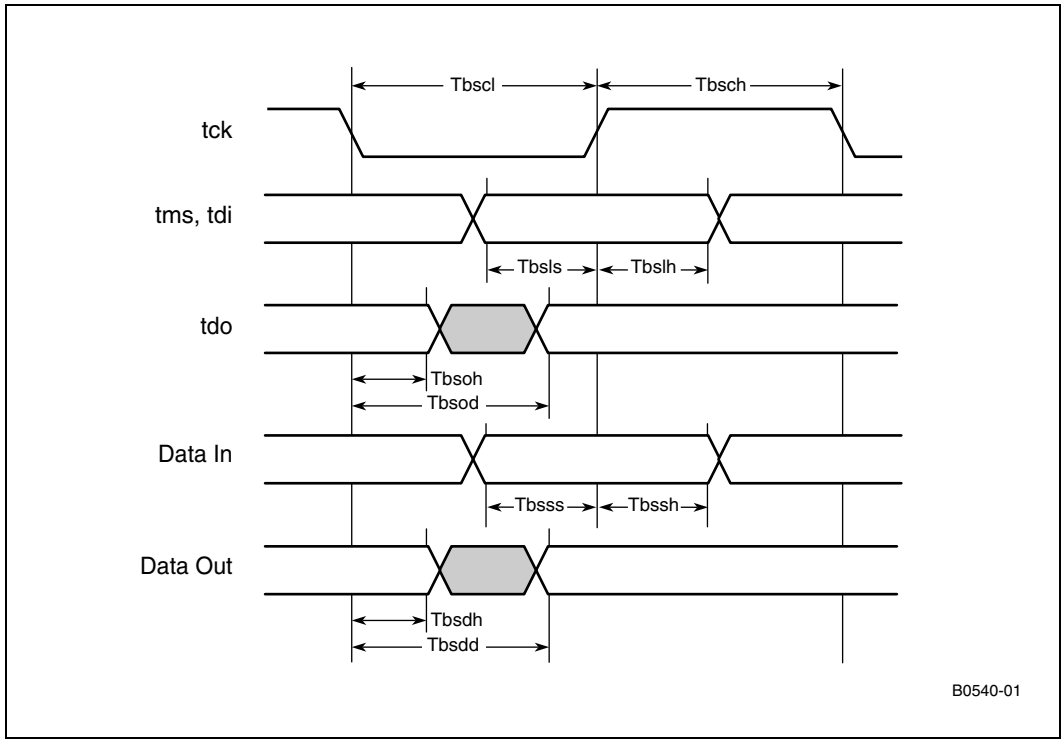


Figure 43. Boundary Scan Tristate Timing

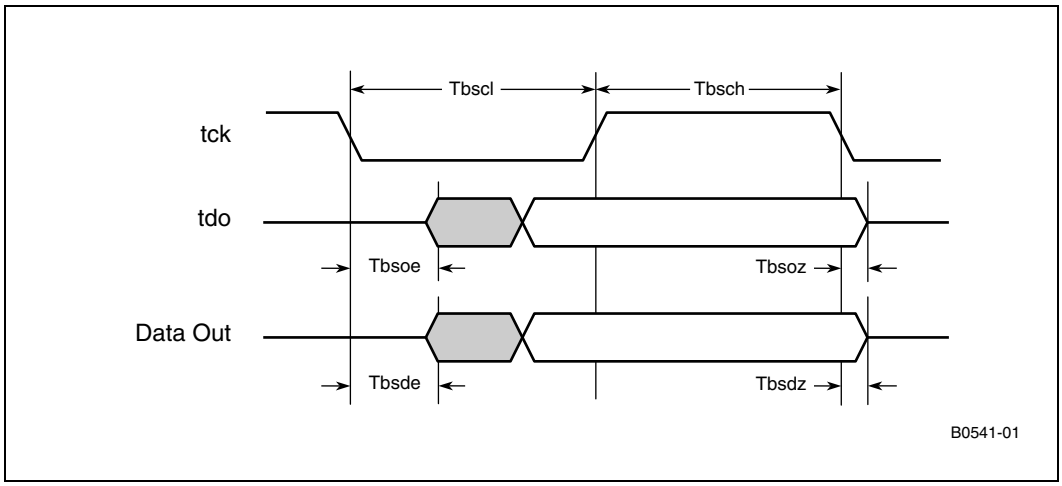


Figure 44. Boundary Scan Reset Timing

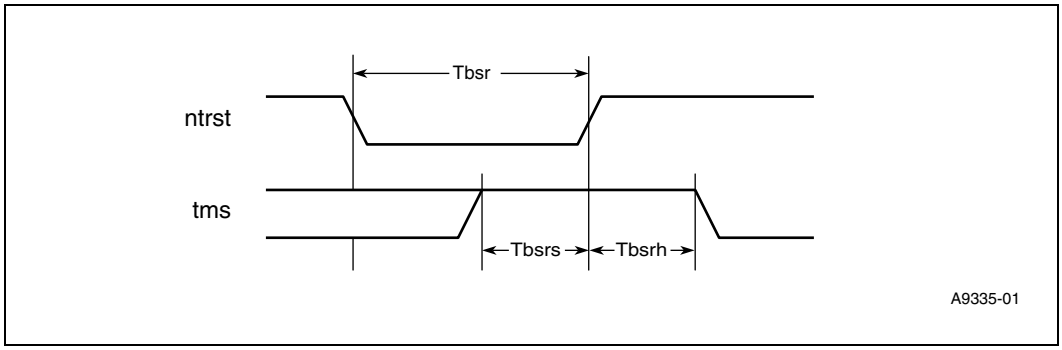


Table 62. JTAG AC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
Tbscl	TCK low period	50	—	—	ns	—
Tbsch	TCK high period	50	—	—	ns	—
Tbsis	TDI, TMS setup to tck	10	—	—	ns	—
Tbsih	TDI, TMS hold from tck	10	—	—	ns	—
Tbsoh	TDO hold time	5	—	—	ns	1
Tbsod	TCf to TDO valid	—	—	40	ns	1
Tbsss	I/O signal setup to tck	5	—	—	ns	2
Tbssh	I/O signal hold from tck	20	—	—	ns	2
Tbsdh	Data output hold time	5	—	—	ns	3
Tbsdd	TCr to data output valid	—	—	40	ns	—
Tbsoe	TDO enable time	5	—	—	ns	1, 4
Tbsoz	TDO disable time	—	—	40	ns	1, 5
Tbsde	Data output enable time	5	—	—	ns	3, 6

Table 62. JTAG AC Specifications (Continued)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
Tbsdz	Data output disable time	—	—	40	ns	3, 7
Tbsr	Reset period	30	—	—	ns	
Tbsrs	TMS setup to ntrst	10	—	—	ns	8
Tbsrh	TMS hold from ntrst	10	—	—	ns	8

1. Assumes a 25 pF load on TDO. Output timing derates at 0.072 ns/pF of extra load applied.
2. For correct data latching, the I/O signals (from the core and the pads) must be set up and held with respect to the rising edge of TCK in the CAPTURE-DR state of the SAMPLE/PRELOAD and EXTEST instructions.
3. Assumes that the data outputs are loaded with the AC test loads.
4. TDO enable time applies when the TAP controller enters the Shift-DR or Shift-IR states.
5. TDO disable time applies when the TAP controller leaves the Shift-DR or Shift-IR states
6. Data output enable time applies when the boundary scan logic is used to enable the output drivers.
7. Data output disable time applies when the boundary scan logic is used to disable the output drivers.
8. TCK may be stopped indefinitely in either the low or high phase.

5.0 Mechanical Specifications

5.1 Package Dimensions

The IXP2400 is contained in a 1356 package, as shown in Figure 45. Symbols in Figure 45 are described in Table 63.

Figure 45. IXP2400 Network Processor General Mechanical Drawing

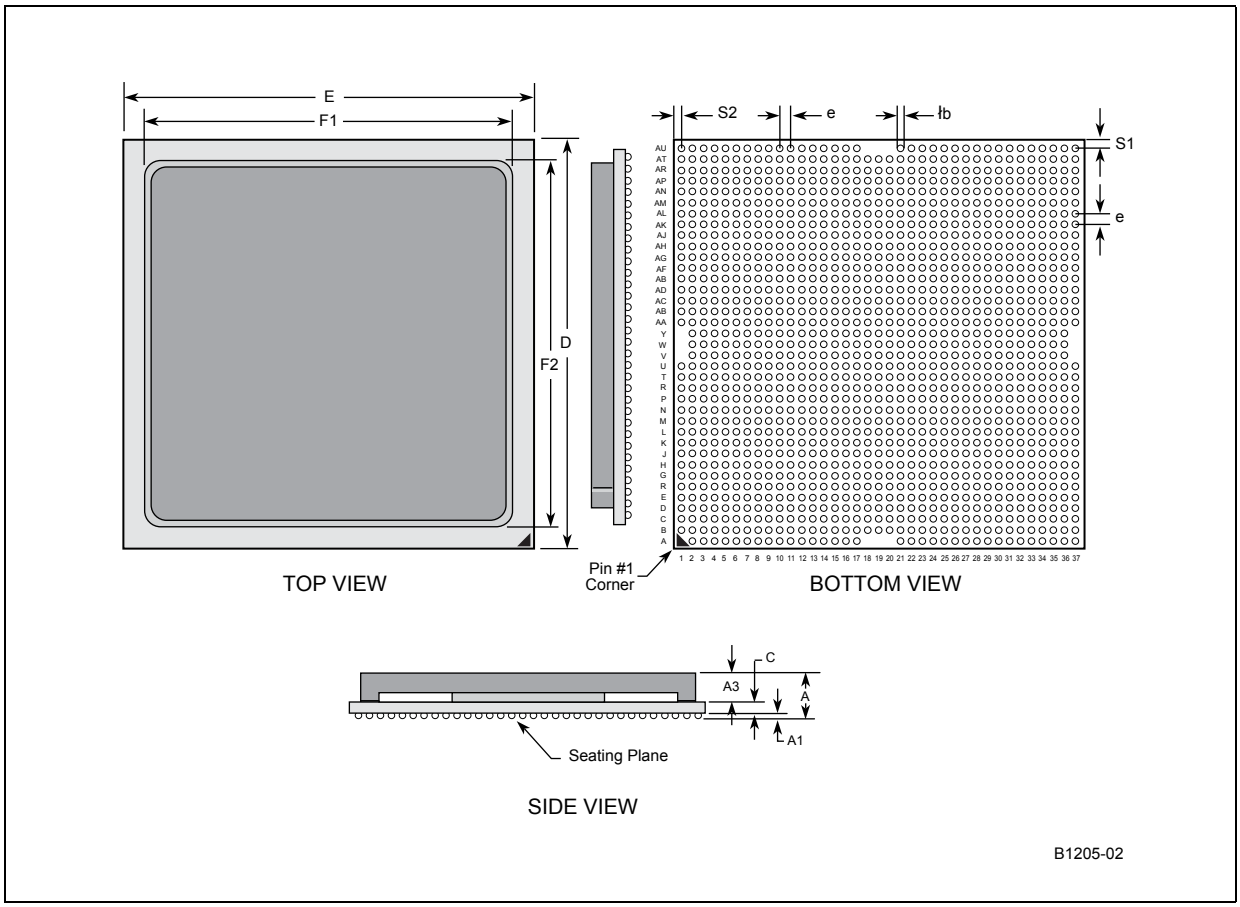


Table 63. IXP2400 Network Processor Package Dimensions

1356 BGA		
Symbol	**Minimum**	**Maximum**
A	3.816	4.46
A1	0.40	0.60
A3	2.266	2.49
b	0.61 Ref.	
C	1.15	1.37

Table 63. IXP2400 Network Processor Package Dimensions (Continued)

1356 BGA		
Symbol	**Minimum**	**Maximum**
D	37.45	37.55
E	37.45	37.55
F1	33.4	33.6
F2	33.4	33.6
e	1.00	
S1	0.750	
S2	0.750	
NOTE: Measurements in millimeters.		

Table 64. IXP2400 Network Processor Die Size

X	Y	Z
17.20	18.67	0.815
NOTE: Measurements in millimeters.		

This page is intentionally left blank.