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	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17										

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
27 October 1986

AMSC N/A

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M. A. Frank

SIZE
A

CODE IDENT. NO.
14933

REV

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL HMOS 80-BIT NUMERIC PROCESSOR EXTENSION MONOLITHIC SILICON

DWG NO. 5962-85133

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5962-E943-01

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85133	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	80287-10	80-bit HMOS numeric processor extension	10 MHz
02	80287-8	80-bit HMOS numeric processor extension	8 MHz
03	80287-6	80-bit HMOS numeric processor extension	6 MHz

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0 V dc to +7 V dc
Maximum power dissipation (P_D)	3.15 W
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage (V_{CC})	4.75 V dc to 5.25 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions T_C = -55°C to +125°C V_{CC} = 5.0 V ±5%	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input low voltage	V_{IL}		1, 2, 3	All	-.5	.8	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC} +.5	V
Clock input low voltage:	V_{ILC}		1, 2, 3	All			V
CKM = 1					2.0	V_{CC}+1	
CKM = 0					3.8	V_{CC}+1	
Output low voltage	V_{OL}	I_{OL} = 0.3 mA	1, 2, 3	All		.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA	1, 2, 3	All	2.4		V
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{CC}	1, 2, 3	All		±10	µA
Output leakage current	I_{LO}	.45 V ≤ V_{OUT} ≤ V_{CC}	1, 2, 3	All		±10	µA
Power supply current	I_{CC}	T_C = -55°C	3	All		600	mA
Input capacitance	C_{IN}	FC = 1 MHz See 4.3.1c	4	All		10	pF
Input/output capacitance (D0-D15)	C_O	FC = 1 MHz See 4.3.1c	4	All		20	pF
CLK capacitance	C_{CLK}	FC = 1 MHz See 4.3.1c	4	All		12	pF
CLK period	t_{CLCL}	1/	9, 10, 11				ns
CKM = 1				01	100	500	
				02	125	500	
				03	166	500	
CKM = 0				01	40	166	
				02	50	166	
				03	62.5	166	
CLK low time	t_{CLCH}	1/	9, 10, 11				ns
CKM = 1		at 0.8 V		01	53	343	
				02	68	343	
				03	100	343	
CKM = 0		at 0.6 V		01	11	146	
				02, 03	15	146	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions T_C = -55°C to +125°C V_{CC} = 5.0 V ±5%	Group A subgroups	Device type	Limits Min	Limits Max	Unit
CLK high time	t_{CHCL}	1/	9, 10, 11				ns
CKM = 1		at 2.0 V		01	28	230	
				02	43	230	
				03	50	230	
CKM = 0		at 3.6 V		01	18	151	
				02, 03	20	151	
CLK rise time	t_{CH1CH2} 2/	1.0 V to 3.6 V if CKM = 1 1/	9, 10, 11	All		10	ns
CLK fall time	t_{CL2CL1} 2/	3.6 V to 1.0 V if CKM = 1 1/	9, 10, 11	All		10	ns
Data setup to $\overline{NPWR}$ inactive	t_{DVWH}	1/	9, 10, 11	All	75		ns
Data hold from $\overline{NPWR}$ inactive	t_{WHDX}	1/	9, 10, 11	01, 02	18		ns
				03	30		
$\overline{NPWR}$, $\overline{NPRD}$ active time	t_{WLWH} t_{RLRH}	at 0.8 V 1/	9, 10, 11	01, 02	90		ns
				03	95		
Command valid to $\overline{NPWR}$ or $\overline{NPRD}$ active	t_{AVRL} t_{AVWL}	1/	9, 10, 11	All	0		ns
Minimum delay from $\overline{PEREQ}$ active to $\overline{NPRD}$ active	t_{MHRL}	1/	9, 10, 11	01	100		ns
				02, 03	130		
$\overline{PEACK}$ active time	t_{KLKH}	at 0.8 V 1/	9, 10, 11	01	60		ns
				02, 03	85		
$\overline{PEACK}$ inactive time	t_{KHKL}	at 2.0 V 1/	9, 10, 11	01	200		ns
				02, 03	250		
$\overline{PEACK}$ inactive to $\overline{NPWR}$, $\overline{NPRD}$ inactive	t_{KHCH}	1/	9, 10, 11	01, 02	40		ns
				03	50		
$\overline{NPWR}$, $\overline{NPRD}$ inactive to $\overline{PEACK}$ active	t_{CHKL}	1/	9, 10, 11	All	-30		ns
Command hold from $\overline{NPWR}$, $\overline{NPRD}$ inactive	t_{WHAX} t_{RHAX}	1/	9, 10, 11	01	22		ns
				02, 03	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions T_C = -55°C to +125°C, V_{CC} = 5.0 V ±5%	Group A subgroups	Device type	Limits Min	Limits Max	Unit
PEACK active setup to NPWR, NPRD active	t_{KLCL}	1/	9, 10, 11	01, 02 03	40 50		ns
NPWR, NPRD to CLK setup time	t_{IVCL}	1/ 3/	9, 10, 11	01 02, 03	53 70		ns
NPWR, NPRD from CLK hold time	t_{CLIH}	1/ 3/	9, 10, 11	01 02, 03	37 45		ns
RESET to CLK setup time	t_{RSCL}	1/ 3/	9, 10, 11	All	20		ns
RESET from CLK hold time	t_{CLRS}	1/ 3/	9, 10, 11	All	20		ns
NPRD inactive to data float	t_{RHQZ}	1/ 4/	9, 10, 11	01 02 03		25 35 37.5	ns
NPRD active to data valid	t_{RLQV} 5/	D0-D15 loading: C_L = 100 pF 1/	9, 10, 11	All		60	ns
ERROR active to BUSY inactive	t_{ILBH}	BUSY loading = C_L = 100 pF 1/	9, 10, 11	All	100		ns
NPWR active to BUSY active	t_{WLBV} 5/	BUSY loading = C_L = 100 pF 1/	9, 10, 11	All		100	ns
PEACK active to PEREQ inactive	t_{KLML}	On last data transfer of numeric instruction 1/	9, 10, 11	All		127	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions T_C = -55°C to +125°C V_{CC} = 5.0 V ±5%	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Command inactive time	t_{CMDI}	at 2.0 V 1/	9, 10, 11				ns
Write-to-write				01	75		
				02, 03	95		
Read-to-read				01	75		
				02, 03	95		
Write-to-read				01	75		
				02, 03	95		
Read-to-write				01	75		
				02, 03	95		
Data hold from NPRD inactive	t_{RHQH}	D0-D15 loading = C_L = 100 pF 1/	9, 10, 11	All	3		ns

1/ See figures 3 and 4.
2/ Guaranteed if not tested.
3/ This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
4/ Float condition occurs when output current is less than I_{LO} on D0-D15.
5/ Due to test equipment limitations, actual tested values may differ from those specified, but specified values are guaranteed.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(Hot), 10
Additional electrical subgroups for group C periodic inspections	---

*PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_O, and C_{CLK} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

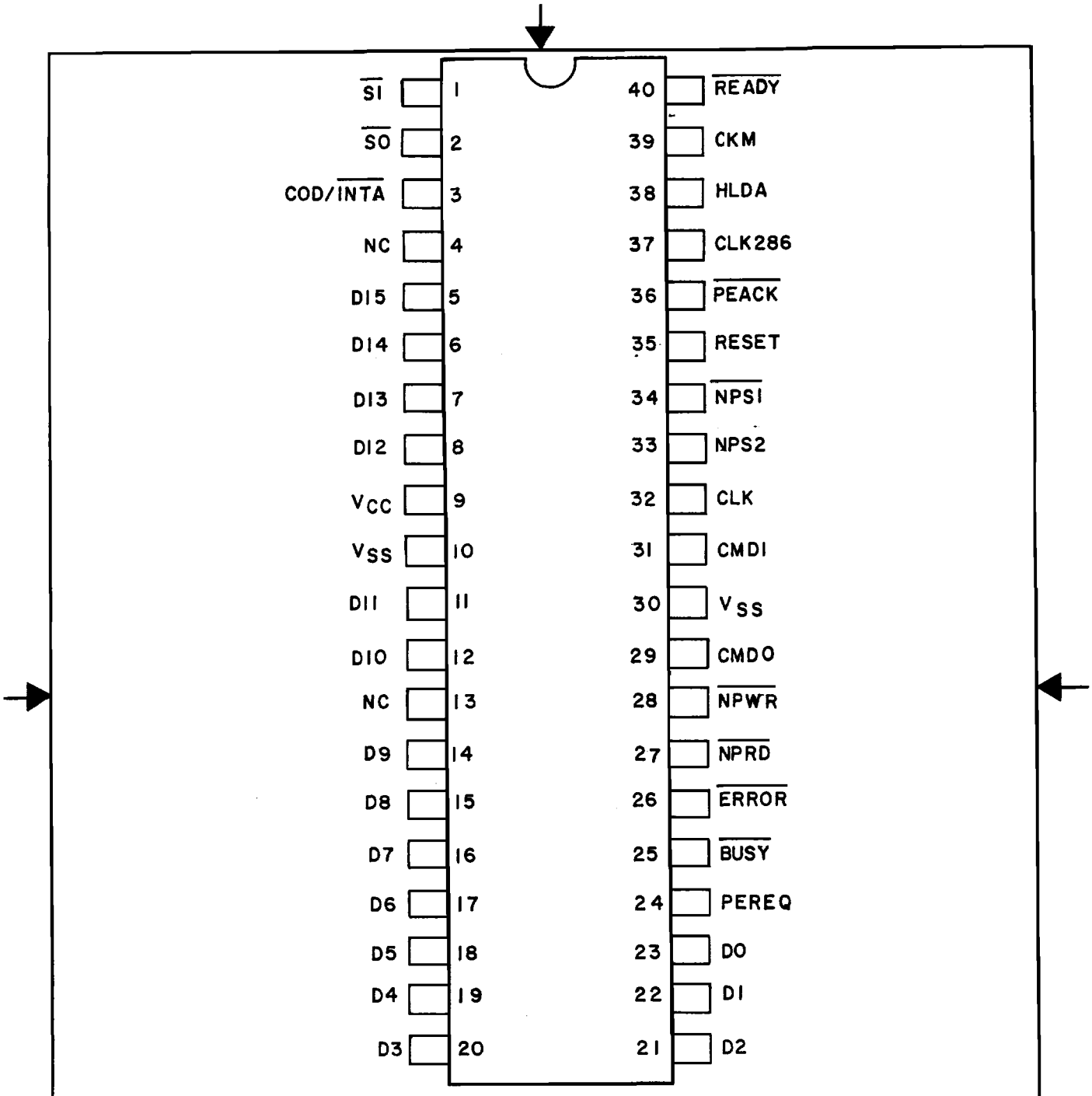
(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.



NOTE:
N.C. pin must not be connected.

FIGURE 1. Terminal connections.

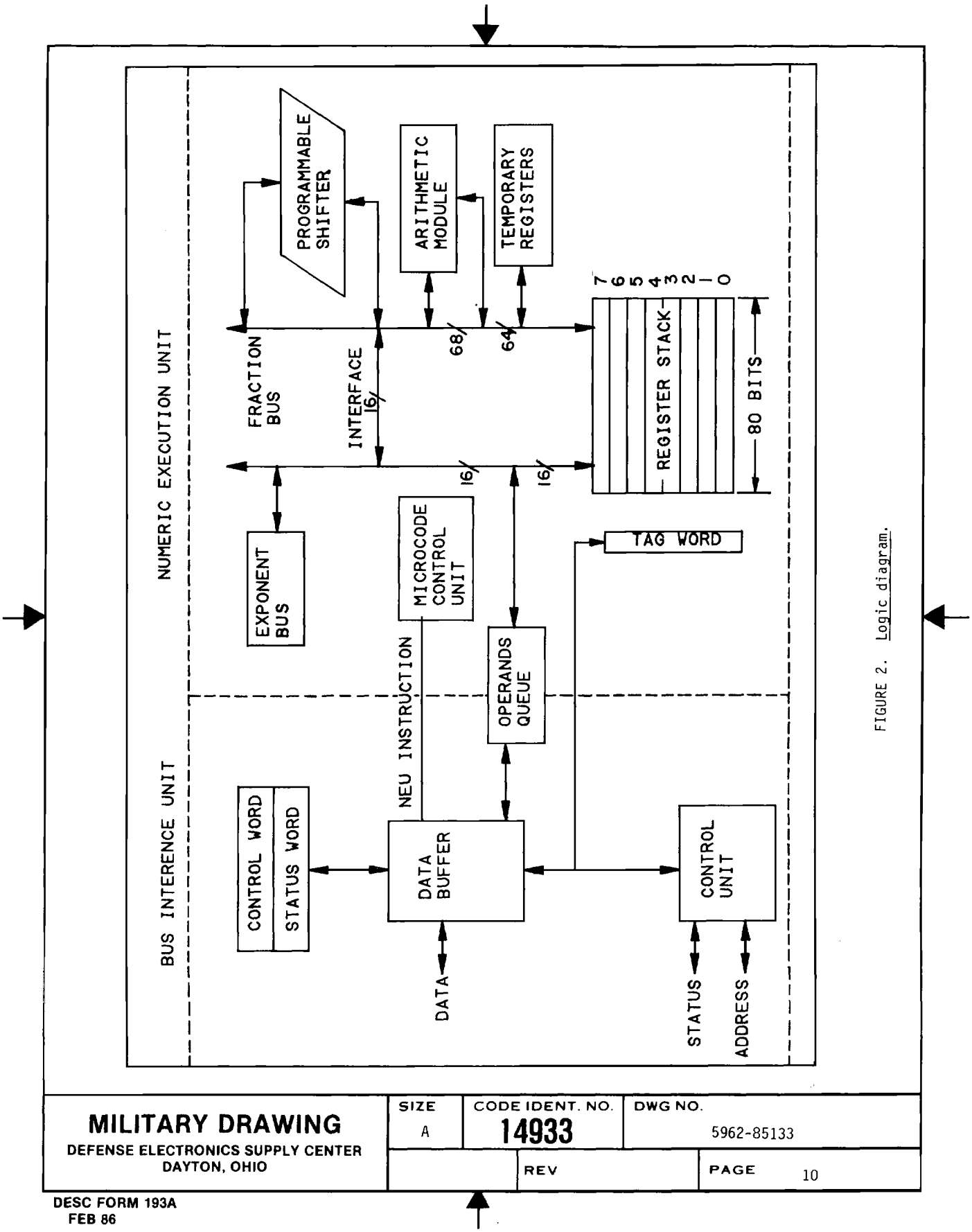


FIGURE 2. Logic diagram.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-85133
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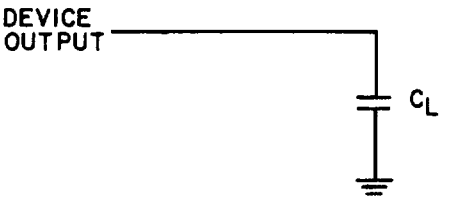
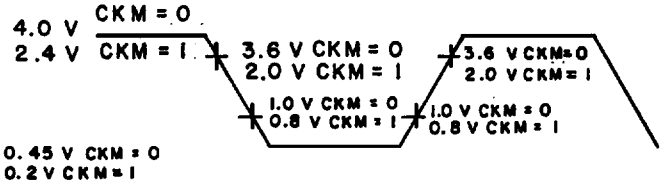
FEB 86

AC test loading on output

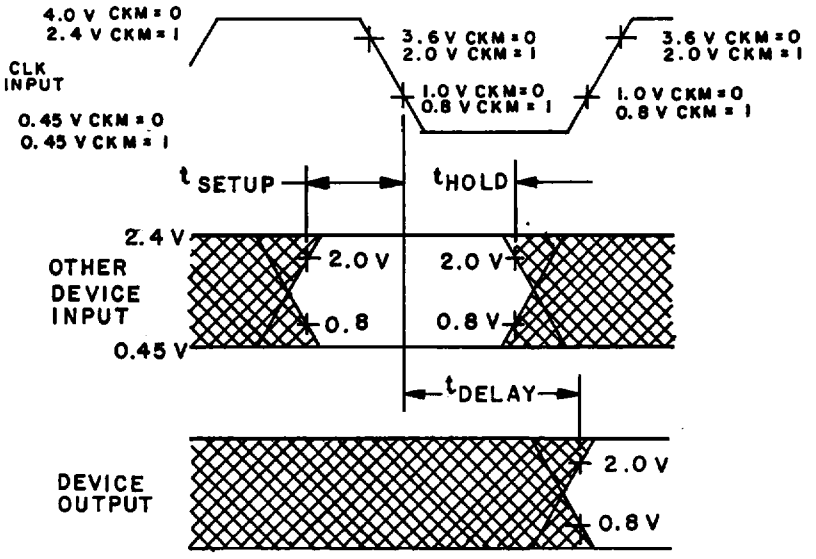


AC test loading on outputs

FIGURE 3. Output load.



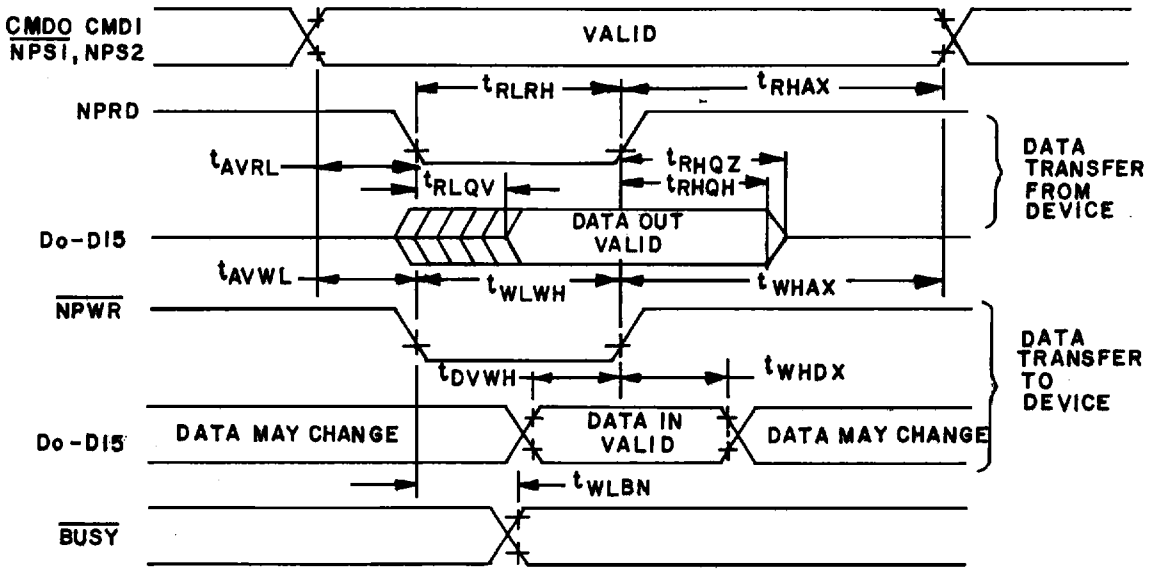
AC drive and measurement points -CLK input



AC setup, hold and delay time measurement - general

FIGURE 4. Waveforms.

DATA TRANSFER TIMING (INITIATED BY MICROPROCESSOR)



DATA CHANNEL TIMING (INITIATED BY PROCESSOR EXTENSION)

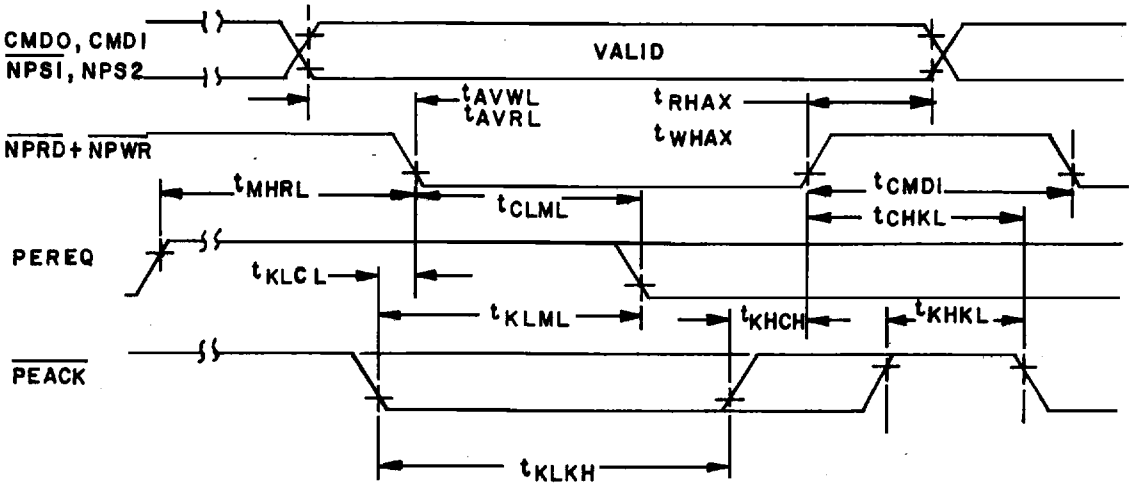
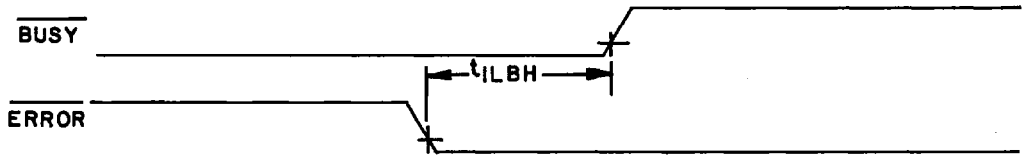
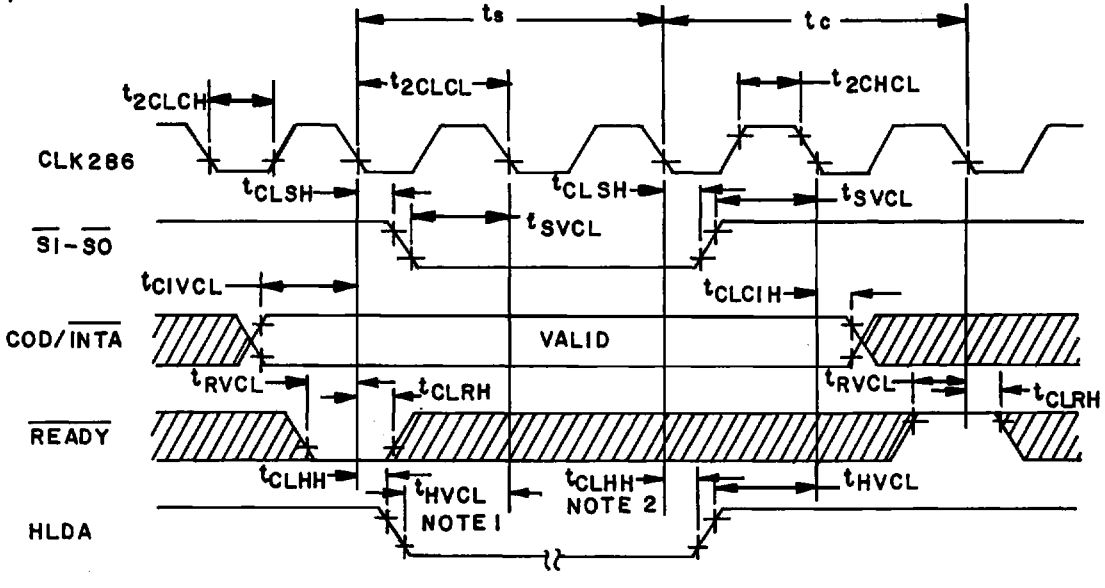


FIGURE 4. Waveforms - Continued

ERROR OUTPUT TIMING



μP STATUS TIMING

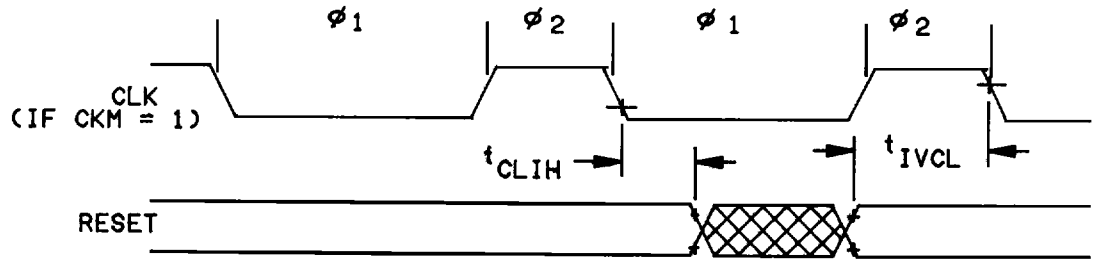


NOTES:
1. This input transition occurs before t_S.
2. This input transition occurs after t_C.

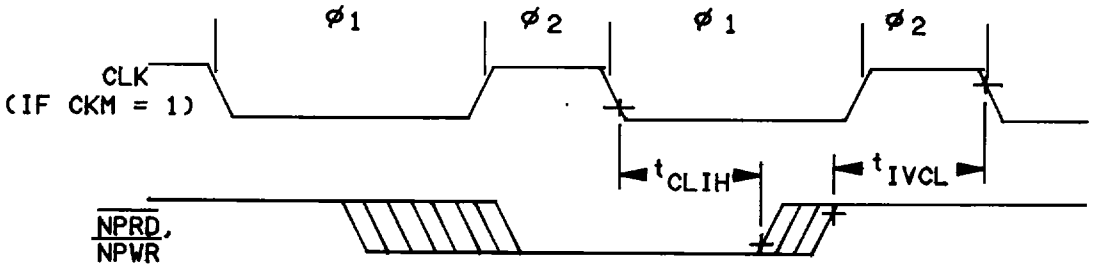
FIGURE 4. Waveforms - Continued.

(Reset, NPWR,NPRD are inputs asynchronous to CLK. Timing requirements on this page are given for testing purposes only to assure recognition at a specific CLK edge).

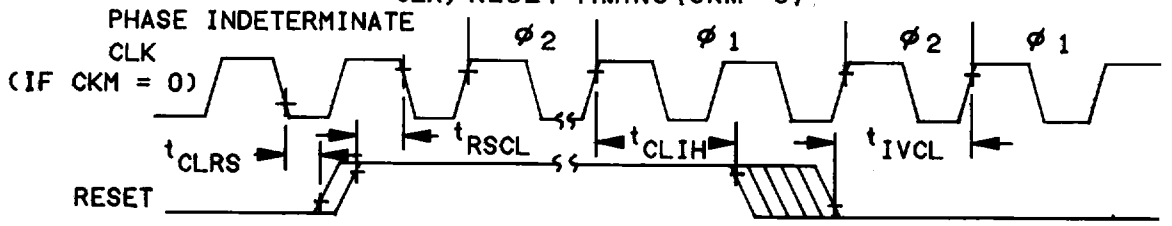
CLK, RESET TIMING (CKM = 1)



CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ TIMING (CKM = 1)



CLK, RESET TIMING (CKM = 0)



NOTE: Reset must meet timing shown to guarantee known phase of internal $\div 3$ circuit.

CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ TIMING (CKM = 0)

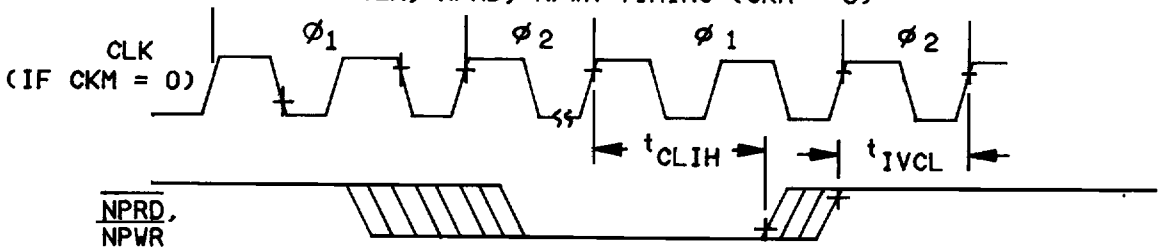


FIGURE 4. Waveforms - Continued.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions. Pin descriptions and functions are as follows:

Symbols	Type	Name and function
CLK	I	Clock input: This clock provides the basic timing for internal device operations. Special MOS level inputs are required.
CKM	I	Clock mode signal: Indicates whether CLK is to be divided by 3 or used directly. A high input will cause CLK to be used directly. This input may be connected to V_{CC} or V_{SS} as appropriate. This input must be either high or low 20 CLK cycles before RESET goes low.
RESET	I	System reset: Causes the device to immediately terminate its present activity and enter a dormant state. RESET is required to be high for more than 4 device CLK cycles. For proper initialization the high-low transition must occur no sooner than 50 µs after V_{CC} and CLK meet their dc and ac specifications.
D15-D0	I/O	Data: 16-bit bidirectional data bus. Inputs to these pins may be applied asynchronous to the device clock.
$\overline{\text{BUSY}}$	O	Busy status: Asserted by the device to indicate that it is currently executing a command.
$\overline{\text{ERROR}}$	O	Error status: Reflects the ES bit of the status word. This signal indicates that an unmasked error condition exists.
PEREQ	O	Processor extension data channel operand transfer request: A high on this output indicates that the device is ready to transfer data. PEREQ will be disabled upon assertion of $\overline{\text{PEACK}}$ or upon actual data transfer, whichever occurs first, if no more transfers are required.
$\overline{\text{PEACK}}$	I	Processor extension data channel operand transfer acknowledge: Acknowledges that the request signal (PEREQ) has been recognized. Will cause the request (PEREQ) to be withdrawn in case there are no more transfers required. $\overline{\text{PEACK}}$ may be asynchronous to the device clock.

Symbols	Type	Name and function
$\overline{NPRD}$	I	Numeric processor read: Enables transfer of data from the device. This input may be asynchronous to the device clock.
$\overline{NPWR}$	I	Numeric processor write: Enables transfer of data to the device. This input may be asynchronous to the device clock.
$\overline{NPS1}$, NPS2	I	Numeric processor selects: Indicates the CPU is performing an ESCAPE instruction. Concurrent assertion of these signals (i.e., $\overline{NPS1}$ is low and NPS2 is high) enables the device to perform floating point instructions. No data transfers involving the device will occur unless the device is selected via these lines. These inputs may be asynchronous to the device clock.
CMD1, CMD0	I	Command lines: These along with select inputs, allow the CPU to direct the operation of the device. These inputs may be asynchronous to the device clock.
CLK286	I	CPU clock: This input provides a sampling edge for the device inputs $\overline{SI}$, $\overline{SO}$, COD/$\overline{INTA}$, $\overline{READY}$, and HLDA. It must be connected to the central processor CLK input.
$\overline{SI}$, $\overline{SO}$ COD/$\overline{INTA}$	I	Status: These inputs must be connected to the corresponding device pins.
HLDA	I	Hold acknowledge: This input informs the device when the central processor controls the local bus. It must be connected to the central processor HLDA output.
$\overline{READY}$	I	Ready: The end of a bus cycle is signaled by this input. It must be connected to the central processor $\overline{READY}$ input.
V_{SS}	I	System ground, both pins must be connected to ground.
V_{CC}	I	+5 V supply.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8513301QX	34649	MD80287-10/B	
5962-8513302QX	34649	MD80287-8/B	
5962-8513303QX	34649	MD80287-6/B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224