Intel® IXP2800 and IXP2850 Network Processors

Datasheet

Product Features

The Intel® IXP2800 and IXP2850 Network Processors enable fast deployment of complete content processing by providing unlimited programming flexibility, code re-use, and high-performance processing. These network processors support a wide variety of WAN and LAN applications that require support for a broad range of speeds — currently ranging from OC-3 to OC-192. High-performance and scalability are achieved through an innovative Microengine architecture that includes a multi-threaded distribution cache architecture that enables pipeline features in software.

In addition to the standard feature set available with the IXP2800, the IXP2850 integrates functionality for secure network traffic at 10 Gbits/s. This enables the up-front design of secure network equipment and results in lower overall system cost for power consumption, board real estate, and silicon investment.

- Sixteen Integrated Microengines (Version 2)
  - Operating frequency of up to 1.4 GHz
  - Configurable to four or eight threads per Microengine
  - 640 Dwords of local memory per Microengine
  - Sixteen-entry CAM per Microengine with single-cycle lookup
  - Next Neighbor bus accessing adjacent Microengines
  - CRC unit per Microengine
  - 8K instructions control store per Microengine
  - Support for Generalized Thread Signaling
- Integrated Intel XScale® Core
  - Operating frequency of up to 700 MHz
  - High Performance, low-power 32-bit embedded RISC processor
  - 32 Kbyte instruction cache
  - 32 Kbyte data cache
- Two Integrated Cryptographic Units (IXP2850 only)
  - Operating frequency of up to 700 MHz
  - Support for DES, 3DES, AES, and SHA-1 algorithms
  - Support for AES 128, 192, and 256 bit keys
- Three industry standard RDRAM Interfaces
  - Peak bandwidth of 2.1 Gbytes/s
  - 800-MHz and 1066-MHz RDRAM
  - Error Correction Code (ECC)
  - Addressable from Intel XScale® core, Microengines, and PCI
- Four industry standard 32-bit QDR SRAM Interfaces
  - Peak bandwidth of 1.9 Gbytes/s per channel
  - Up to 233-MHz SRAM
  - Hardware support for Linked List and Ring operations
  - Atomic bit operations
  - Atomic arithmetic support
  - Addressable from Intel XScale® core, Microengines, and PCI
- Integrated Media Switch Fabric Interface
  - Two unidirectional 16-bit Low-Voltage Differential Signaling (LVDS) data interfaces
  - Up to 500 MHz per channel
  - Separately configurable for either SPI-4 or CSIX protocols
- Industry standard PCI Bus
  - *PCI Local Bus Specification, Version 2.2** interface for 64-bit 66-MHz I/O
- Additional integrated features
  - Hardware Hash Unit (48, 64, and 128 bit)
  - 16 KByte Scratchpad Memory
  - Serial UART port for debugging
  - Eight general-purpose I/O pins
  - Four 32-bit timers
- 1356 Ball FCBGA package
  - Dimensions of 37.5 mm x 37.5 mm
  - 1 mm solder ball pitch

Order Number: 278537-017

Revision History

Date	Revision	Description
October 2001	001	Release for the Customer Information Book V0.3.
December 2001	002	Release for the Customer Information Book V0.4.
February 2002	003	Advanced Information version.
May 2002	004	Release for the IXA SDK 3.0.
August 2002	005	Updated with miscellaneous changes.
October 2002	006	Added IXP2850 Network Processor.
December 2002	007	Added IXP2850 power values and other miscellaneous changes.
February 2003	008	Removed Advance Information labeling.
April 2003	009	Miscellaneous changes.
November 2003	010	Changed: Figures 5 and 27; Tables 5, 6, 7, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 41, 42, 43, 45, 47, 51, 56, 60, and 63; Sections 3.3, 4.4.8.2, 4.4.9, and 5.1.
January 2004	011	Added: Tables 61, 62; Figures 19, 23, and 24. Changed: Tables 17, 22, 25, 26, 27, 28, 52, and 53; Figure 18; Section 4.2.
April 2004	012	Changed: Sections 2.6, 3.3, 4.2.2, 4.4.1, 4.4.6, and 5.1; Figure 17; Tables 8, 22, 23, 24, 26, 28, 30, 32, 33, 39, 40, 42, 43, 51, and 55.
July 2004	013	Added information for 650 MHz version of IXP2800 and IXP2850 and removed A-stepping information.
December 2004	014	Miscellaneous updates.
June 2005	015	Miscellaneous updates.
July 2005	016	Updated Tables 53 and 54 and Figures 17 and 18.
September 2005	017	Updated Figures 20 and 21

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1.0 Product Description

The Intel® IXP2800 and IXP2850 network processors are second-generation high-performance network processors based on the first generation Intel® IXP1200 network processor design. They are fully programmable network processors that implement a high-performance parallel processing architecture on a single chip designed for processing complex algorithms, deep packet inspection, traffic management, and forwarding at wire-speed. Its store-and-forward architecture combines a high-performance Intel XScale® core with sixteen 32-bit independent multithreaded Microengines that cumulatively provide more than 25 giga-operations per second. The Microengines provide the processing power to perform dataplane tasks that traditionally required expensive high-speed ASICs.

Intel's second-generation network processors are the first implementation of Intel's Hyper Task Chaining technology. This unique network processing approach allows a single stream packet/cell processing problem to be decomposed into multiple, sequential tasks that can be linked together easily. The hardware design uses fast and flexible sharing of data and event signals among threads and Microengines to manage data-dependent operations using multiple parallel processing stages, with low latency. Through this combination of flexible software pipelining and fast inter-process communication, Hyper Task Chaining delivers rich processing capability at OC-192/10 Gbps line rates.

1.1 Hyper Task Chaining

Hyper Task Chaining implements several significant innovations to ensure low latency communication among processes. These mechanisms include "Next Neighbor" registers that enable individual Microengines to rapidly pass data and state information to adjacent Microengines. Reflector Mode pathways ensure that data and global event signals can be shared with multiple Microengines, using 32-bit unidirectional buses that connect the network processor's internal processing and memory resources. A third enhancement, Ring Buffer registers, provides a highly efficient mechanism for flexibly linking tasks among multiple software pipelines.

Ring buffers allow developers to establish "producer-consumer" relationships among Microengines, efficiently propagating results along the pipeline in FIFO order. To minimize latency associated with external memory references, register structures are complemented by 16 entries of Content Addressable Memory (CAM) associated with each Microengine. Configured as a distributed cache, the CAM enables multiple threads and Microengines to manipulate the same data simultaneously, while maintaining data coherency.

Figure 1 is a block diagram of the IXP2800 network processor, and Figure 2 is a block diagram of the IXP2850 network processor.

Figure 3 shows two IXP2800 network processors in a typical 10 Gb/s full duplex line card with a switch fabric interface.

Figure 1. IXP2800 Network Processor Block Diagram

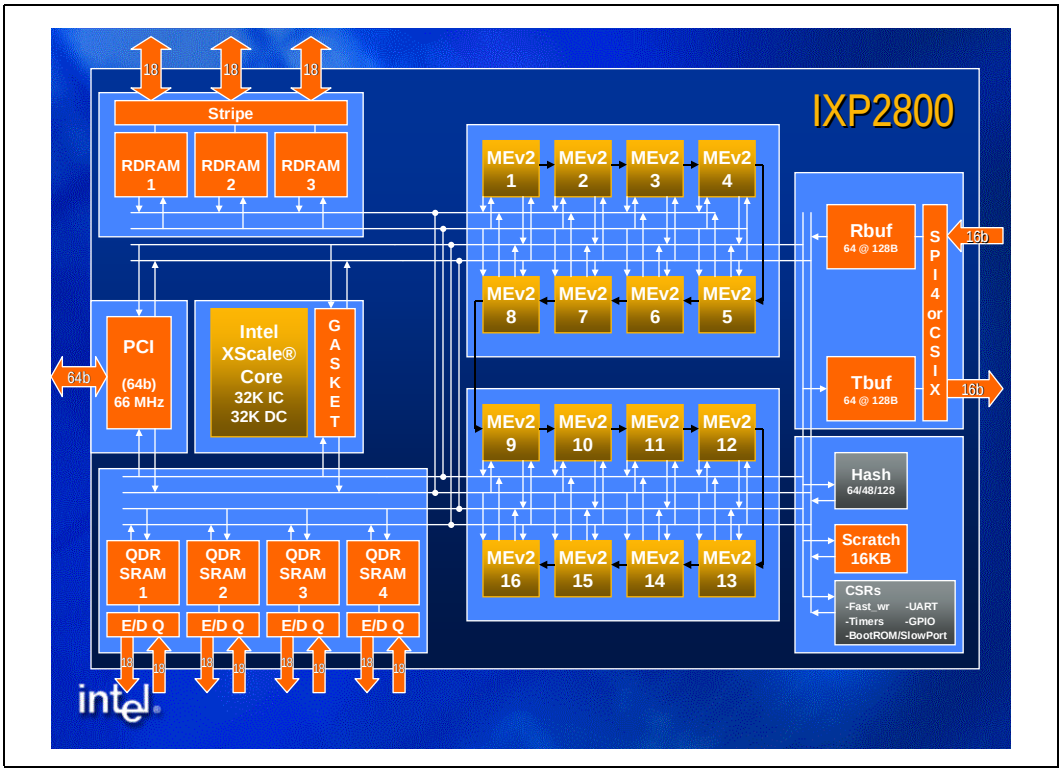


Figure 2. IXP2850 Network Processor Block Diagram

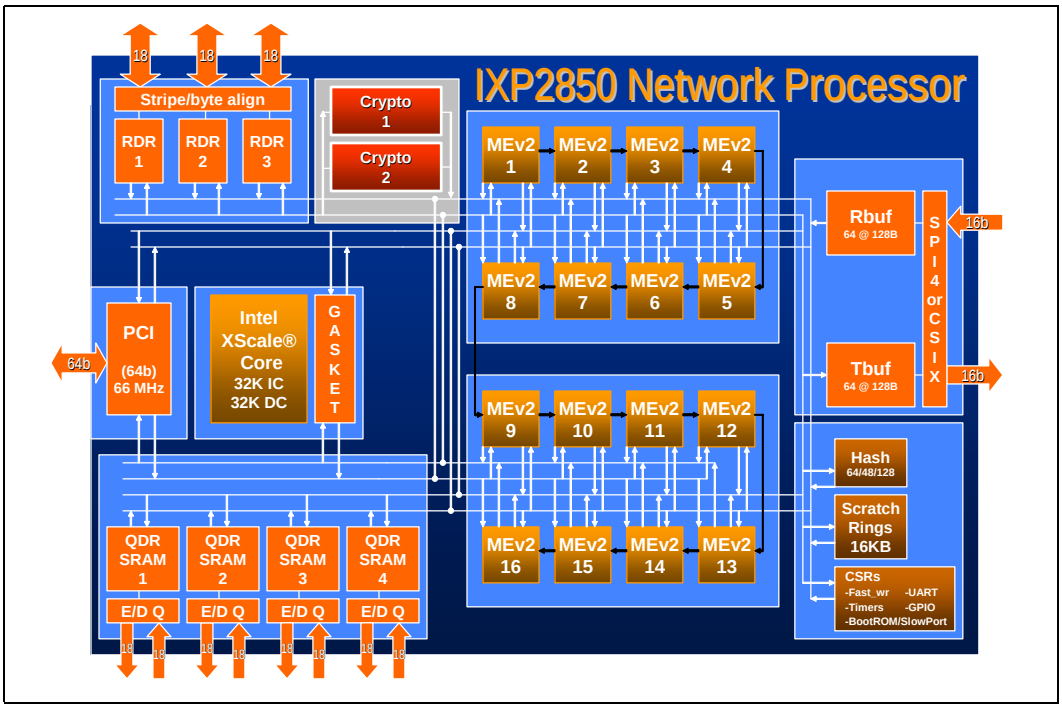
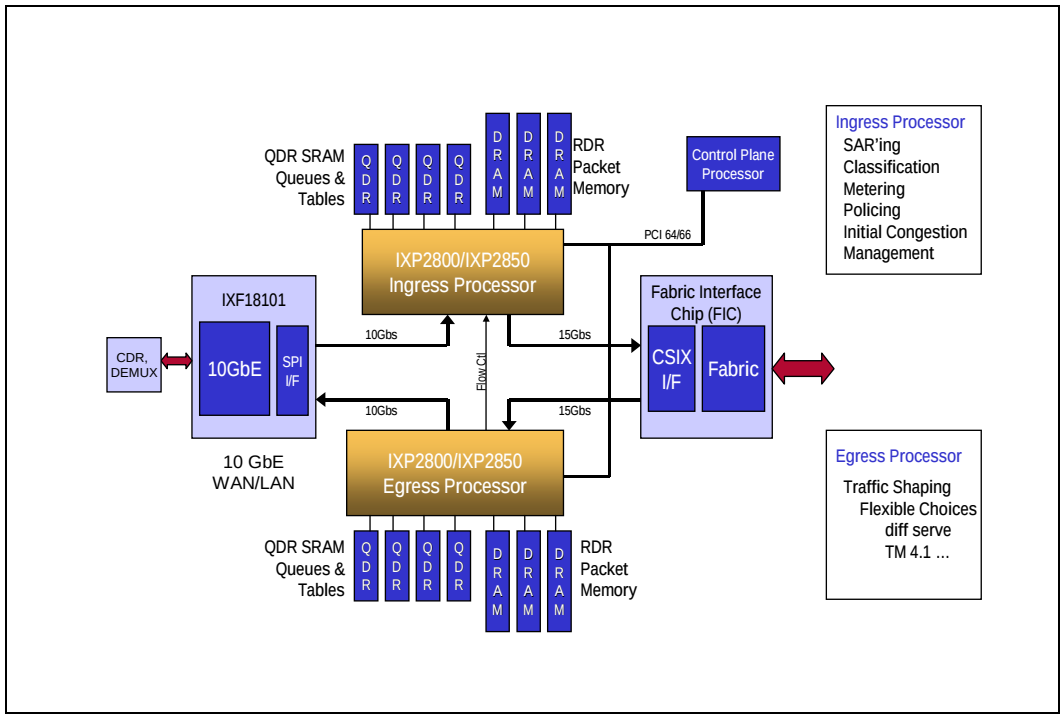


Figure 3. IXP2800/IXP2850 Network Processor Based Ethernet Line Card



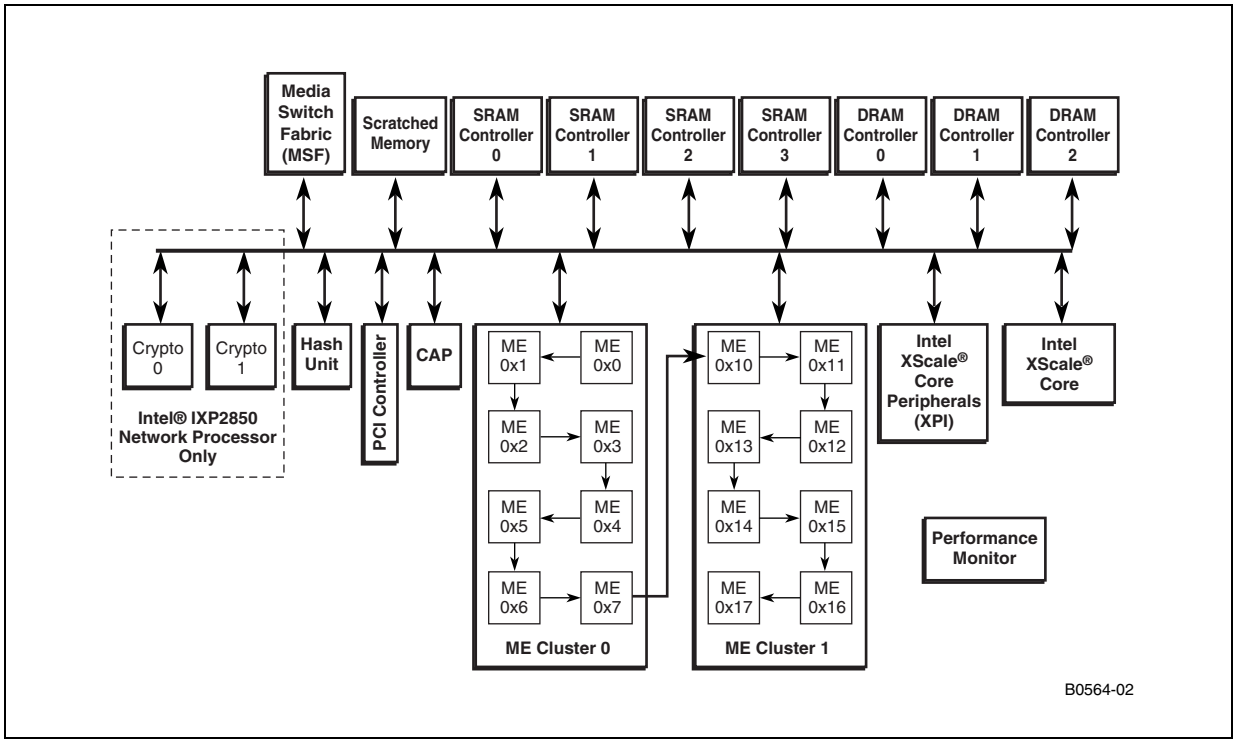
2.0 Functional Units

2.1 Functional Overview

This section provides a brief overview of the IXP2800 and IXP2850 network processor internal hardware.

Figure 4 shows the major internal blocks.

Figure 4. IXP2800/IXP2850 Network Processor Functional Block Diagram



2.2 The Intel XScale® Core

The Intel XScale® core is a 32-bit general-purpose RISC processor. It incorporates an extensive list of architectural features that enable it to achieve high performance. It is compatible to the ARM* Version 5 (V5) Architecture. It implements the integer instruction set of ARM V5, but does not provide hardware support for the floating-point instructions.

The Intel XScale® core provides the Thumb instruction set (ARM V5T) and the ARM V5E DSP extensions.

Backward compatibility with the first generation of StrongARM* products is maintained for user-mode applications. Operating systems may require modifications to match the specific hardware features of the Intel XScale® core and to take advantage of the performance enhancements added to it.

2.3 Microengines

The Microengines do most of the programmable per-packet processing in the network processor. There are 16 Microengines, connected as shown in Figure 4. The Microengines can access all of the shared resources (SRAM, DRAM, MSF, etc.) and the private connections between adjacent Microengines.

The Microengines provide support for software-controlled multi-threaded operation. Given the disparity in processor cycle times compared to external memory times, a single thread of execution often blocks, waiting for external memory operations to complete. Multiple threads enable interleave operations — there is usually at least one thread ready to run while others are waiting.

2.4 Cryptography Unit

The IXP2850 network processor has two cryptography units – Crypto 0 and Crypto 1 (see Figure 4) that perform bulk data encryption and authentication. The cryptography units interface only to the Microengines and Media Switch Fabric, and contain input RAM available for receiving input data from the Microengine and RBUF (receive buffer) elements. Both cryptography units support the Data Encryption Standard (DES), Triple DES (3DES), and Advanced Encryption Standard (AES) algorithms, and Secure Hash Algorithm (SHA-1) hashing.

Each cryptography unit has two 3DES cores, one AES core, and two SHA-1 cores:

- Each 3DES core can access three encryption/decryption Key states and three Initialization Vectors (IV).
- The AES core can access six Key states and six IVs.
- The 3DES and AES cores can be used with or without Cipher Block Chaining.
- The AES cores support a block size of 128 bits, and Key lengths of 128, 192, and 256 bits.
- The SHA-1 cores have hardware support to implement the Keyed-Hash Message Authentication Code (HMAC) algorithm, with minimal Microengine intervention.
- The cryptography units operate at half the Microengine frequency.

2.5 RDRAM

The IXP2800/IXP2850 has controllers for three Rambus* DRAM (RDRAM) channels. Each of the controllers independently accesses its own RDRAMs, and can operate concurrently with the other controllers (i.e., they are not operating as a single, wider memory). DRAM provides high density, high bandwidth storage and is typically used for data buffers.

RDRAM sizes of 64, 128, 256, and 512 Mbytes, and 1 Gbyte are supported. However, each of the channels must have the same number, size, and speed of RDRAMs populated. Each channel can be populated with one to four per bank, for short-channel and one RIMM for long-channel.

Up to two Gbytes of DRAM is supported. If less than two Gbytes of memory is available, the upper part of the address space is not used. It is also possible (for system cost and area savings) to have Channels 0 and 1 populated with Channel 2 empty, or Channel 0 populated with Channels 1 and 2 empty.

Reads and writes to RDRAM are generated by Microengines, Intel XScale® core, and PCI (external Bus Masters and DMA Channels). The controllers also do refresh and calibration cycles to the RDRAMs, transparently to software.

Note: RDRAM Powerdown and Nap modes are not supported.

Hardware interleaving of addresses (also called striping) provides balanced access to all populated channels; the interleave size is 128 bytes. Interleaving helps to maintain utilization of available bandwidth by spreading consecutive accesses to multiple channels. The interleaving is done in the hardware so that the three channels appear to software as a single contiguous memory space.

ECC (Error Correcting Code) is supported, but can be disabled. Enabling ECC requires that x18 RDRAMs be used; if ECC is disabled, x16 RDRAMs can be used. ECC can detect and correct all single-bit errors, and detect all double-bit errors. When ECC is enabled, partial writes (writes of less than eight bytes) must be done as read-modify-writes.

2.6 SRAM

The network processor has four independent SRAM controllers, each of which supports pipelined QDR synchronous static RAM (SRAM) and/or a coprocessor that adheres to QDR signaling. Any or all controllers can be left unpopulated if the application does not need to use them. SRAM is accessible by the Microengines, the Intel XScale® core, and the PCI Unit (external bus masters and DMA).

The memory is logically four bytes (32-bits) wide; physically, the data pins are two bytes wide and are double-clocked. Byte parity is supported, and each of the four bytes has a parity bit, which is written when the byte is written and checked when the data is read. There are byte enables that select the bytes to be written, for writes of less than 32-bits.

Each of the four QDR ports are QDR- and QDRII-compatible; each port implements the "_K" and "_C" output clocks and "_CIN" as an input and their inversions. (*Note*: the "_C" and "_CIN" clocks are optional). Extensive work has been done to provide impedance controls within the IXP2800/IXP2850 for IXP2800/IXP2850-initiated signals driving to QDR parts. Providing a clean signaling environment is critical to achieving 200- to 233-MHz QDRII data transfers.

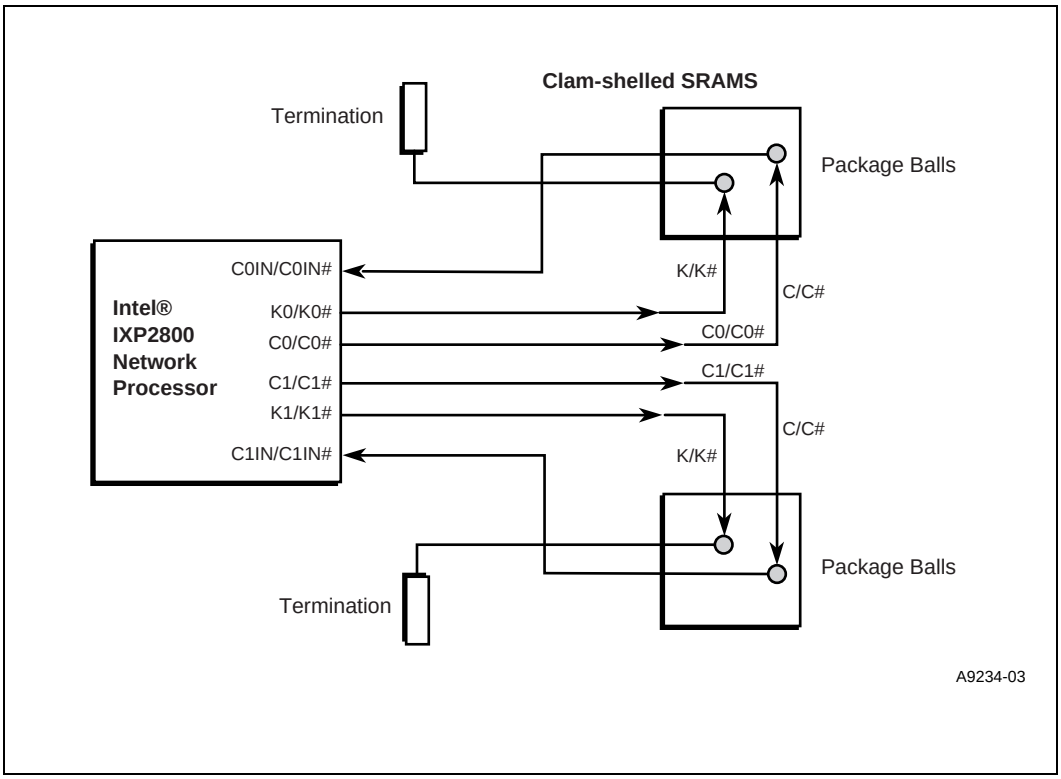
The configuration assumptions for the network processor I/O driver/receiver development includes four QDR loads and the network processor. The network processor supports bursts of two SRAMs (bursts of four SRAMs are not supported).

The SRAM controller can also be configured to interface to an external coprocessor that adheres to the QDR electricals and protocol. Each SRAM controller can also interface to an external coprocessor through its standard QDR interface. This interface enables both SRAM devices and coprocessors to operate on the same bus. The coprocessor behaves as a memory-mapped device on the SRAM bus.

2.6.1 QDR Clocking Scheme

The controller drives out two pairs of K clock (K and K#), and two pairs of C clock (C and C#). Both C/C# clocks externally return to the controller for reading data. Figure 5 shows the clock diagram of the clocking scheme for a QDR interface driving four SRAM chips.

Figure 5. Clocking Scheme for a QDR Interface Driving Four SRAMs



2.6.2 SRAM Controller Configurations

Each channel has enough address pins (24) to support up to 64 Mbyte of SRAM. The SRAM controllers can directly generate multiple port enables (up to four pairs) to allow for depth expansion. Two pairs of pins are dedicated for port enables. Smaller RAMs use fewer address signals than the number provided to accommodate the largest RAMs, so some address pins (23:20) are configurable as either address or port-enable, based on the CSR setting as shown in Table 1.

Note: All of the SRAMs on a given channel must be the same size.

Table 1. SRAM Controller Configurations

SRAM Configuration	SRAM Size	Addresses Needed to Index SRAM	Addresses Used as Port Enables	Total Number of Port Select Pairs Available
512K x 18	1 Mbyte	17:0	23:22, 21:20	4
1M x 18	2 Mbyte	18:0	23:22, 21:20	4
2M x 18	4 Mbyte	19:0	23:22, 21:20	4
4M x 18	8 Mbyte	20:0	23:22	3
8M x 18	16 Mbyte	21:0	23:22	3
16M x 18	32 Mbyte	22:0	None	2
32M x 18	64 Mbyte	23:0	None	1

Each channel can be expanded by depth, according to the number of port enables available. If external decoding is used, then the number of SRAMs used is not limited by the number of port enables generated by the SRAM controller.

Note: External decoding may require external pipeline registers to account for the decode time, depending on the desired frequency.

Table 2 lists the QDR Address/RPE/WPE Mapping.

Table 2. QDR Address/RPE/WPE Mapping

SRAM Configuration/Size	SRAM_CONTROL [SRAM_SIZE][9:7]	SRAM_CONTROL [PORT_CTL][5:4]	RPE[2]/WPE[2]	RPE[3]/WPE[3]
512K x 18 - 1MB	000	11	QDR_ADDR[23:22]	QDR_ADDR[21:20]
1Mb x 18 - 2MB	001	11	QDR_ADDR[23:22]	QDR_ADDR[21:20]
2Mb x 18 - 4MB	010	11	QDR_ADDR[23:22]	QDR_ADDR[21:20]
4Mb x 18 - 8MB	011	10	QDR_ADDR[23:22]	N/A
8Mb x 18 - 16MB	100	10	QDR_ADDR[23:22]	N/A
16Mb x 18 - 32MB	101	00	N/A	N/A
32Mb x 18 - 64MB	110	00	N/A	N/A

Maximum SRAM system sizes are shown in Table 3. Shaded entries require external decoding, because they use more port enables than the SRAM controller can supply directly.

Table 3. Total Memory per Channel

SRAM Size	Number of SRAMs on Channel							
	1	2	3	4	5	6	7	8
512K x 18	1 MB	2 MB	3 MB	4 MB	5 MB	6 MB	7 MB	8 MB
1M x 18	2 MB	4 MB	6 MB	8 MB	10 MB	12 MB	14 MB	16 MB
2M x 18	4 MB	8 MB	12 MB	16 MB	20 MB	24 MB	28 MB	32 MB
4M x 18	8 MB	16 MB	24 MB	32 MB	64 MB	NA	NA	NA
8M x 18	16 MB	32 MB	48 MB	64 MB	NA	NA	NA	NA
16M x 18	32 MB	64 MB	NA	NA	NA	NA	NA	NA
32M x 18	64 MB	NA	NA	NA	NA	NA	NA	NA

2.7 Media and Switch Fabric Interface

The Media and Switch Fabric (MSF) Interface connects the network processor to a physical layer device (PHY) and/or a Switch Fabric Interface. The MSF consists of the following external interfaces:

- Receive and transmit interfaces, each of which can be individually configured for either the SPI-4 Phase 2 (System Packet Interface) to a PHY or the CSIX–L1 protocol to a switch fabric.
- A Flow Control Interface, which provides a point-to-point connection used primarily to pass CSIX-L1 flow control C-Frames either between two network processors or between a network processor and a switch fabric.

The MSF supports 16-bit DDR LVDS signaling for the SPI-4 data path channel, and can be configured to support either LVTTL or LVDS signaling for the SPI-4 FIFO status channel. The MSF supports 16-bit LVDS signaling for CSIX-L1 protocol and 4-bit LVDS signaling for the Flow Control interface.

2.7.1 SPI-4.2

SPI-4.2 is an interface for packet and cell transfer between a physical layer (PHY) device and a link layer device (network processor), for aggregate bandwidths of OC-192 ATM and Packet over SONET/SDH (POS), as well as 10 Gb/s Ethernet applications.

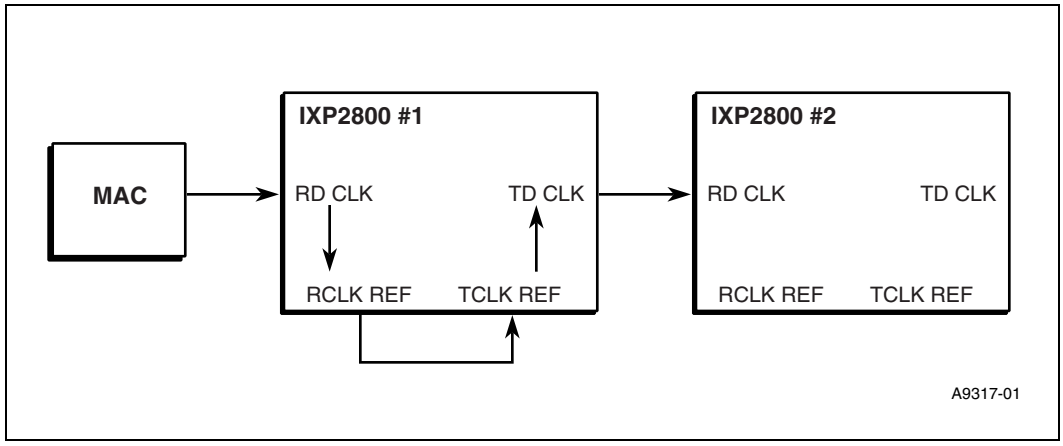
The SPI-4.2 protocol transfers data in bursts of variable length. Associated with each burst is information such as port number (for a multi-port device such as a 10 x 1 GbE), SOP, and EOP. This information is collected by the MSF and passed to the Microengines.

There are two options that do *not* require an extra oscillator to provide a clock for the data that moves between two network processors on the same line card:

- In the first option, the MAC device creates an RD_CLK to the first network processor, as shown in Figure 6. RCLK_REF loops back into TCLK_REF for network processor 1, and TCLK_REF is used as the source of the TD_CLK to network processor 2.
- In the second option, the TD_CLK from network processor 1 to network processor 2 can be created using a divide of network processor 1's internal fast clock. The multiplex that selects between the two possible sources of TD_CLK is controlled by a bit in the MSF_Tx_Control CSR.

The Optical Internetworking Forum (OIF) controls the SPI-4.2 Implementation Agreement document (available at http://www.oiforum.com).

Figure 6. SPI-4 Clock Configuration for Dual Network Processors



2.7.2 CSIX

CSIX-L1 (Common Switch Interface, Level 1) defines an interface between a Traffic Manager (TM) and a Switch Fabric (SF) for ATM, IP, MPLS, Ethernet, and similar data communication applications.

The Network Processor Forum (NPF) controls the CSIX-L1 specification (available at http://www.npforum.org and www.csix.org).

The unit of information transferred between Traffic Managers and Switch Fabrics is called a CFrame. There are three categories of CFrames:

- Data
- Control (one type of which is flow control)
- Idle

The MSF automatically discards any Idle CFrames that it receives from the SF, and transmits Idle CFrames to the SF when required. The MSF stores Data and Control CFrames in buffers during transmit and receive operations. The buffers may be partitioned according to CFrame category — guaranteeing that neither control nor data CFrames will block each other.

There are two types of CSIX-L1 flow control:

- Link Level
- Virtual Output Queue (VOQ)

Every CFrame Base Header contains a Ready Field, which contains two Link Level flow control bits: one for Flow Control traffic and one for Data traffic. Due to the CSIX-L1 requirement for bounded response to Link Level flow control, the MSF manages all Link Level flow control.

Virtual Output Queue Flow Control is carried in Flow Control CFrames. As with Data CFrames, the MSF places Flow Control CFrames in internal buffers before passing them to the Microengines for processing.

2.7.3 Flow Control Bus

The MSF Flow Control Bus passes CSIX-L1 flow control CFrames between two network processors or between a Switch Fabric and a single network processor. The bus is implemented as two independent unidirectional buses. It uses LVDS signaling with the same clocking rate as the MSF receive and transmit channels, and has a 4-bit data bus — yielding an available bandwidth equal to 25 percent of the receive and transmit channels.

The Flow Control Bus can be configured in one of two modes:

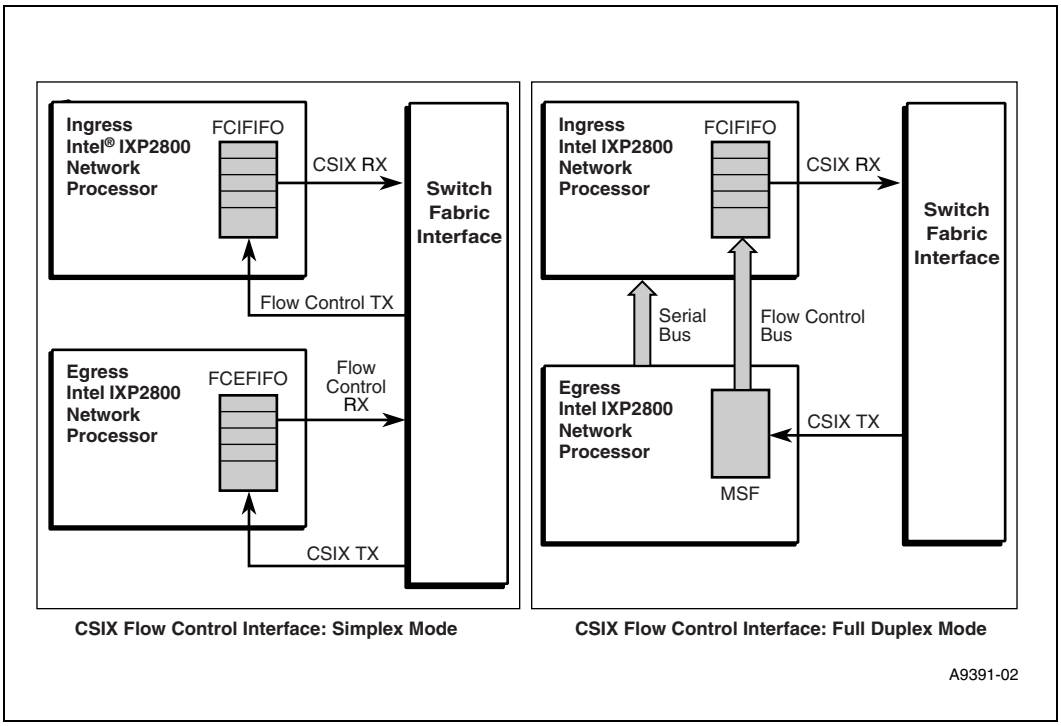
- Dual Chip, Full Duplex Mode for applications where the Fabric Interface uses the transmit and receive channels to pass flow control CFrames
- Simplex Mode for applications where the Fabric Interface is designed to use the Flow Control Bus to pass flow control CFrames

When the IXP2800/IXP2850 is configured in Dual Chip, Full Duplex Mode, the Egress IXP2800/IXP2850 automatically forwards CFrames received from the Switch Fabric across the Flow Control Bus to the Ingress IXP2800/IXP2850. Additionally, the Egress IXP2800/IXP2850 sends incoming and outgoing Link Level flow control information across the Flow Control Serial Bus to the Ingress IXP2800/IXP2850.

When the IXP2800/IXP2850 is configured in Simplex Mode, the Flow Control Bus signals are connected directly to the Switch Fabric. The Egress IXP2800/IXP2850 sends flow control CFrames directly to the Switch Fabric, and the Switch Fabric sends flow control CFrames directly to the Ingress IXP2800/IXP2850.

Figure 7 shows the IXP2800 connected in both modes.

Figure 7. CSIX Flow Control Interfaces: Simplex and Full Duplex Modes



2.8 PCI Controller

The PCI Controller provides a 64-bit, 66 MHz-capable *PCI Local Bus Specification, Version 2.2** interface. It is also compatible to 32-bit and/or 33 MHz PCI devices. The PCI controller provides the following functions:

- Target Access (external Bus Master access to SRAM, DRAM, and CSRs)
- Master Access (Intel XScale® core or Microengine access to PCI Target devices)
- Two DMA Channels
- Mailbox and Doorbell Registers for Intel XScale® core to host communication
- PCI Arbiter

The network processor can be configured to act as a PCI central function (for use in a stand-alone system), where it provides the PCI reset signal, or as an add-in device, where it uses the PCI reset signal as the chip reset input.

2.9 GPIO

The network processor contains eight General Purpose I/O (GPIO) pins. These can be programmed as either input or output, and can be used for slow speed I/O, such as LEDs or input switches. They can also be used as interrupts to the Intel XScale® core, or to clock the programmable timers.

2.10 Serial Port

The network processor contains a standard RS-232 compatible Universal Asynchronous Receiver/Transmitter (UART), which can be used for communication with a debugger or maintenance console. Modem controls are not supported; if they are needed, GPIO pins can be used for that purpose.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the processor. The processor can read the complete status of the UART at any time during operation. Available status information includes the type and condition of the transfer operations being performed by the UART and any error conditions (parity, overrun, framing, or break interrupt).

The serial ports can operate in either FIFO or non-FIFO mode. In FIFO mode, a 64-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 64-byte receive FIFO buffers data from the serial link, until the data is read by the processor.

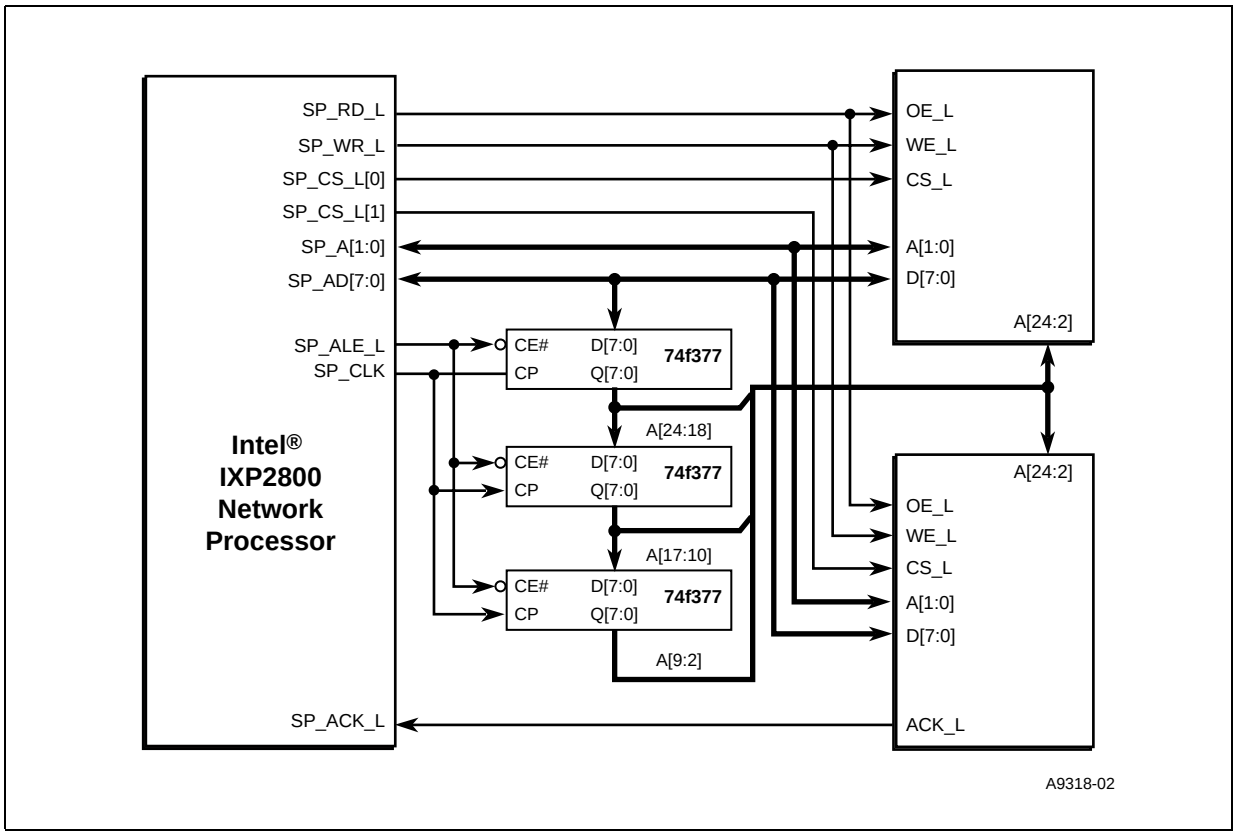
The UART includes a programmable baud rate generator, which is capable of dividing the internal clock input by divisors of 1 to 2^{16} - 1 and produces a 16x clock that drives the internal transmitter logic and the receive logic. The UART can be operated in polled or in interrupt-driven mode, as selected by software.

2.11 Slowport

The Slowport is an external interface to the network processor, and is used for 8-bit flash ROM access and 8, 16, or 32-bit microprocessor device access. It allows the Intel XScale® core to do read/write data transfers to these slave devices. The Slowport supports 4-, 8-, and 16-Mbyte flash sizes.

The address bus and data bus are multiplexed to reduce the pincount. In addition, 24 bits of address are shifted out on three clock cycles. Therefore, an external set of buffers is needed to latch the address; two chip selects are provided — see Figure 8 (note that the ACK signal is optional).

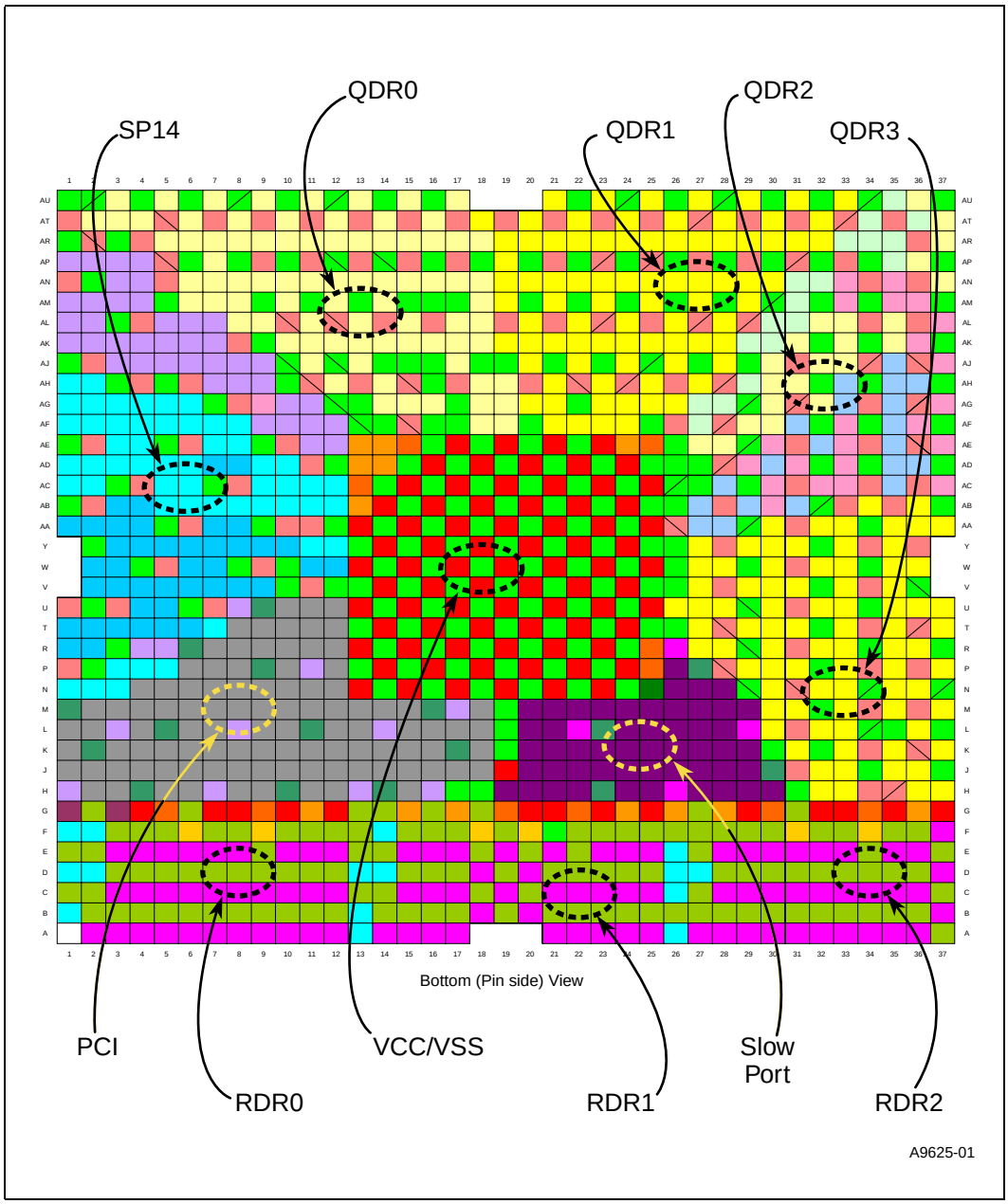
Figure 8. Generic Slowport Connection



3.0 Signal Description

3.1 Pinout Diagram

Figure 9. Pinout Diagram



3.2 Pin Description, Grouped by Function

This section provides an overview of the network processor I/O signals. Detailed definitions and descriptions of signal usage can be found in sections specific to each interface.

The network processor signals are categorized into one of several groups, as shown in Table 4.

Table 4. IO Signal Prefix Categories

IO Signal Group Prefix	Description
CLK	Clocks, reset, and test control signals related to the PLL clock
SP	Slowport
TEST	Test port
JTAG	Joint Test Action Group
GPIO	General purpose IO
SR	Serial port
SPI4	SPI-4
FC	Flow control
QDRn	Four QDR ports
RDRn	Three Rambus* ports
PCI	PCI

3.2.1 RDRAM

There are three channels of RDRAM. The I/O design supports long-channel and short-channel board implementations. Long-channel is RIMM based, and short-channel is board-mounted. The RDR channels support PC600, PC800, and 1066-MHz RDR parts. The RDR channels allow programmatic selection of ECC. Long- and short-channel design guides are available from Rambus*. The long-channel design supports one RIMM load.

There are three Rambus* DRAM (RDRAM) channels, and each channel has the signals shown in Table 5. The DRAMs use RSL signaling levels, with the exception of SIO, CMD, SCK, PClkM, and SynClkN, which are CMOS.

Table 5. RDRAM Signals (Sheet 1 of 3)

Signal Name	I/O	Description	Number
RDR0_SIO RDR1_SIO RDR2_SIO	I/O	Serial Data	3
RDR0_CMD RDR1_CMD RDR2_CMD	O	Command	3
RDR0_SCK RDR1_SCK RDR2_SCK	O	Serial Clock	3

Table 5. RDRAM Signals (Sheet 2 of 3)

Signal Name	I/O	Description	Number
RDR0_DQA(0) RDR0_DQA(1) RDR0_DQA(2) RDR0_DQA(3) RDR0_DQA(4) RDR0_DQA(5) RDR0_DQA(6) RDR0_DQA(7) RDR0_DQA(8) RDR1_DQA(0) RDR1_DQA(1) RDR1_DQA(2) RDR1_DQA(3) RDR1_DQA(4) RDR1_DQA(5) RDR1_DQA(6) RDR1_DQA(7) RDR1_DQA(8) RDR2_DQA(0) RDR2_DQA(1) RDR2_DQA(2) RDR2_DQA(3) RDR2_DQA(4) RDR2_DQA(5) RDR2_DQA(6) RDR2_DQA(7) RDR2_DQA(8)	I/O	Low Byte	27
RDR0_DQB(0) RDR0_DQB(1) RDR0_DQB(2) RDR0_DQB(3) RDR0_DQB(4) RDR0_DQB(5) RDR0_DQB(6) RDR0_DQB(7) RDR0_DQB(8) RDR1_DQB(0) RDR1_DQB(1) RDR1_DQB(2) RDR1_DQB(3) RDR1_DQB(4) RDR1_DQB(5) RDR1_DQB(6) RDR1_DQB(7) RDR1_DQB(8) RDR2_DQB(0) RDR2_DQB(1) RDR2_DQB(2) RDR2_DQB(3) RDR2_DQB(4) RDR2_DQB(5) RDR2_DQB(6) RDR2_DQB(7) RDR2_DQB(8)	I/O	High Byte	27
PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	I	Logic Threshold Voltage for RSL	6

Table 5. RDRAM Signals (Sheet 3 of 3)

Signal Name	I/O	Description	Number
RDR0_CFM RDR1_CFM RDR2_CFM	O	Clock from Master (High)	3
RDR0_CFMN RDR1_CFMN RDR2_CFMN	O	Clock from Master (Low)	3
RDR0_CTM RDR1_CTM RDR2_CTM	I	Clock to Master (High)	3
RDR0_CTMN RDR1_CTMN RDR2_CTMN	I	Clock to Master (Low)	3
RDR0_RQ(5) RDR0_RQ(6) RDR0_RQ(7) RDR1_RQ(5) RDR1_RQ(6) RDR1_RQ(7) RDR2_RQ(5) RDR2_RQ(6) RDR2_RQ(7)	O	Row[2:0]	9
RDR0_RQ(0) RDR0_RQ(1) RDR0_RQ(2) RDR0_RQ(3) RDR0_RQ(4) RDR1_RQ(0) RDR1_RQ(1) RDR1_RQ(2) RDR1_RQ(3) RDR1_RQ(4) RDR2_RQ(0) RDR2_RQ(1) RDR2_RQ(2) RDR2_RQ(3) RDR2_RQ(4)	O	Column[4:0]	15
RDR0_PCLKM RDR1_PCLKM RDR2_PCLKM	O	Phase Detector Output to DRCG = Internal RDRAM CLK/4	3
RDR0_SCLKN RDR1_SCLKN RDR2_SCLKN	O	Phase Detector Output to DRCG = CTM/16	3
Total			111

3.2.2 SRAM

There are four SRAM interfaces to Quad Data Rate (QDR) SRAMs, and each interface has the signals found in Table 6. The SRAMs use HSTL signaling levels.

Table 6. SRAM Signals (Sheet 1 of 7)

Signal Name	I/O	Description	Number
QDR0_K_H(0) QDR0_K_H(1) QDR1_K_H(0) QDR1_K_H(1) QDR2_K_H(0) QDR2_K_H(1) QDR3_K_H(0) QDR3_K_H(1)	O	Positive and negative output clocks. Address, Port Enable, Data Out are referenced to these clocks.	8
QDR0_K_L(0) QDR0_K_L(1) QDR1_K_L(0) QDR1_K_L(1) QDR2_K_L(0) QDR2_K_L(1) QDR3_K_L(0) QDR3_K_L(1)	O		8
QDR0_C_H(0) QDR0_C_H(1) QDR1_C_H(0) QDR1_C_H(1) QDR2_C_H(0) QDR2_C_H(1) QDR3_C_H(0) QDR3_C_H(1)	O	Positive input clocks. Data In is referenced to these clocks.	8
QDR0_C_L(0) QDR0_C_L(1) QDR1_C_L(0) QDR1_C_L(1) QDR2_C_L(0) QDR2_C_L(1) QDR3_C_L(0) QDR3_C_L(1)	O	Negative input clocks. Data In is referenced to these clocks.	8
QDR0_CIN_H(0) QDR0_CIN_H(1) QDR1_CIN_H(0) QDR1_CIN_H(1) QDR2_CIN_H(0) QDR2_CIN_H(1) QDR3_CIN_H(0) QDR3_CIN_H(1)	I	Positive clock inputs. These differential clocks are used as a reference for Data In. They are the feedback of Sn_C and Sn_C_L.	8
QDR0_CIN_L(0) QDR0_CIN_L(1) QDR1_CIN_L(0) QDR1_CIN_L(1) QDR2_CIN_L(0) QDR2_CIN_L(1) QDR3_CIN_L(0) QDR3_CIN_L(1)	I	***Note*:** QDRn_CIN_L(1) and QDRn_CIN_H(1) input pad outputs are not connected/used internally. The QDRn_CIN_L(1) and QDRn_CIN_H(1) input pins/pads are provided in the device and can be used for termination.	8

Table 6. SRAM Signals (Sheet 2 of 7)

Signal Name	I/O	Description	Number
QDR0_Q_H(0) QDR0_Q_H(1) QDR0_Q_H(2) QDR0_Q_H(3) QDR0_Q_H(4) QDR0_Q_H(5) QDR0_Q_H(6) QDR0_Q_H(7) QDR0_Q_H(9) QDR0_Q_H(10) QDR0_Q_H(11) QDR0_Q_H(12) QDR0_Q_H(13) QDR0_Q_H(14) QDR0_Q_H(15) QDR0_Q_H(16)	I	Data input bus.	16
QDR0_Q_H(8) QDR0_Q_H(17)	I	Byte parity for data in QDR0_Q_H(17) and QDR0_Q_H(8) correspond to QDR0_Q_H[16:9] and QDR0_Q_H[7:0] respectively.	2
QDR0_D_H(0) QDR0_D_H(1) QDR0_D_H(2) QDR0_D_H(3) QDR0_D_H(4) QDR0_D_H(5) QDR0_D_H(6) QDR0_D_H(7) QDR0_D_H(9) QDR0_D_H(10) QDR0_D_H(11) QDR0_D_H(12) QDR0_D_H(13) QDR0_D_H(14) QDR0_D_H(15) QDR0_D_H(16)	O	Data output bus.	16
QDR0_D_H(8) QDR0_D_H(17)	O	Byte parity for data in QDR0_D_H(17)] and QDR0_D_H(8) correspond to QDR0_D_H[16:9] and QDR0_D_H[7:0] respectively.	2
QDR1_Q_H(0) QDR1_Q_H(1) QDR1_Q_H(2) QDR1_Q_H(3) QDR1_Q_H(4) QDR1_Q_H(5) QDR1_Q_H(6) QDR1_Q_H(7) QDR1_Q_H(9) QDR1_Q_H(10) QDR1_Q_H(11) QDR1_Q_H(12) QDR1_Q_H(13) QDR1_Q_H(14) QDR1_Q_H(15) QDR1_Q_H(16)	I	Data input bus.	16
QDR1_Q_H(8) QDR1_Q_H(17)	I	Byte parity for data in QDR1_Q_H(17) and QDR1_Q_H(8) correspond to QDR1_Q_H[16:9] and QDR1_Q_H[7:0] respectively.	2

Table 6. SRAM Signals (Sheet 3 of 7)

Signal Name	I/O	Description	Number
QDR1_D_H(0) QDR1_D_H(1) QDR1_D_H(2) QDR1_D_H(3) QDR1_D_H(4) QDR1_D_H(5) QDR1_D_H(6) QDR1_D_H(7) QDR1_D_H(9) QDR1_D_H(10) QDR1_D_H(11) QDR1_D_H(12) QDR1_D_H(13) QDR1_D_H(14) QDR1_D_H(15) QDR1_D_H(16)	O	Data output bus.	16
QDR1_D_H(8) QDR1_D_H(17)	O	Byte parity for data in QDR1_D_H(17)] and QDR1_D_H(8) correspond to QDR1_D_H[16:9] and QDR1_D_H[7:0] respectively.	2
QDR2_Q_H(0) QDR2_Q_H(1) QDR2_Q_H(2) QDR2_Q_H(3) QDR2_Q_H(4) QDR2_Q_H(5) QDR2_Q_H(6) QDR2_Q_H(7) QDR2_Q_H(9) QDR2_Q_H(10) QDR2_Q_H(11) QDR2_Q_H(12) QDR2_Q_H(13) QDR2_Q_H(14) QDR2_Q_H(15) QDR2_Q_H(16)	I	Data input bus.	16
QDR2_Q_H(8) QDR2_Q_H(17)	I	Byte parity for data in QDR2_Q_H(17) and QDR2_Q_H(8) correspond to QDR2_Q_H[16:9] and QDR2_Q_H[7:0] respectively.	2
QDR2_D_H(0) QDR2_D_H(1) QDR2_D_H(2) QDR2_D_H(3) QDR2_D_H(4) QDR2_D_H(5) QDR2_D_H(6) QDR2_D_H(7) QDR2_D_H(9) QDR2_D_H(10) QDR2_D_H(11) QDR2_D_H(12) QDR2_D_H(13) QDR2_D_H(14) QDR2_D_H(15) QDR2_D_H(16)	O	Data output bus.	16
QDR2_D_H(8) QDR2_D_H(17)	O	Byte parity for data in QDR2_D_H(17)] and QDR2_D_H(8) correspond to QDR2_D_H[16:9] and QDR2_D_H[7:0] respectively.	2

Table 6. SRAM Signals (Sheet 4 of 7)

Signal Name	I/O	Description	Number
QDR3_Q_H(0) QDR3_Q_H(1) QDR3_Q_H(2) QDR3_Q_H(3) QDR3_Q_H(4) QDR3_Q_H(5) QDR3_Q_H(6) QDR3_Q_H(7) QDR3_Q_H(9) QDR3_Q_H(10) QDR3_Q_H(11) QDR3_Q_H(12) QDR3_Q_H(13) QDR3_Q_H(14) QDR3_Q_H(15) QDR3_Q_H(16)	I	Data input bus.	16
QDR3_Q_H(8) QDR3_Q_H(17)	I	Byte parity for data in QDR3_Q_H(17) and QDR3_Q_H(8) correspond to QDR3_Q_H[16:9] and QDR3_Q_H[7:0] respectively.	2
QDR3_D_H(0) QDR3_D_H(1) QDR3_D_H(2) QDR3_D_H(3) QDR3_D_H(4) QDR3_D_H(5) QDR3_D_H(6) QDR3_D_H(7) QDR3_D_H(9) QDR3_D_H(10) QDR3_D_H(11) QDR3_D_H(12) QDR3_D_H(13) QDR3_D_H(14) QDR3_D_H(15) QDR3_D_H(16)	O	Data output bus.	16
QDR3_D_H(8) QDR3_D_H(17)	O	Byte parity for data in QDR3_D_H(17)] and QDR3_D_H(8) correspond to QDR3_D_H[16:9] and QDR3_D_H[7:0] respectively.	2
QDR0_BWS_L(0) QDR0_BWS_L(1) QDR1_BWS_L(0) QDR1_BWS_L(1) QDR2_BWS_L(0) QDR2_BWS_L(1) QDR3_BWS_L(0) QDR3_BWS_L(1)	O	Byte Write Enables. Asserted to enable writing each byte during writes.	8
QDR0_RPS_L(0) QDR0_RPS_L(1) QDR1_RPS_L(0) QDR1_RPS_L(1) QDR2_RPS_L(0) QDR2_RPS_L(1) QDR3_RPS_L(0) QDR3_RPS_L(1)	O	Read Port Enable. Asserted to start a read.	8

Table 6. SRAM Signals (Sheet 5 of 7)

Signal Name	I/O	Description	Number
QDR0_WPS_L(0) QDR0_WPS_L(1) QDR1_WPS_L(0) QDR1_WPS_L(1) QDR2_WPS_L(0) QDR2_WPS_L(1) QDR3_WPS_L(0) QDR3_WPS_L(1)	O	Write Port Enable. Asserted to start a write.	8
QDR0_A(0) QDR0_A(1) QDR0_A(2) QDR0_A(3) QDR0_A(4) QDR0_A(5) QDR0_A(6) QDR0_A(7) QDR0_A(8) QDR0_A(9) QDR0_A(10) QDR0_A(11) QDR0_A(12) QDR0_A(13) QDR0_A(14) QDR0_A(15) QDR0_A(16) QDR0_A(17) QDR0_A(18) QDR0_A(19) QDR0_A(20) QDR0_A(21) QDR0_A(22) QDR0_A(23)	O	Address to SRAMs. Some addresses signals can be programmed to act as additional Port Enables (via CSR control). Refer to Table 2 QDR Address/RPE/WPE Mapping.	24
QDR1_A(0) QDR1_A(1) QDR1_A(2) QDR1_A(3) QDR1_A(4) QDR1_A(5) QDR1_A(6) QDR1_A(7) QDR1_A(8) QDR1_A(9) QDR1_A(10) QDR1_A(11) QDR1_A(12) QDR1_A(13) QDR1_A(14) QDR1_A(15) QDR1_A(16) QDR1_A(17) QDR1_A(18) QDR1_A(19) QDR1_A(20) QDR1_A(21) QDR1_A(22) QDR1_A(23)	O	Address to SRAMs. Some addresses signals can be programmed to act as additional Port Enables (via CSR control). Refer to Table 2 QDR Address/RPE/WPE Mapping.	24

Table 6. SRAM Signals (Sheet 6 of 7)

Signal Name	I/O	Description	Number
QDR2_A(0) QDR2_A(1) QDR2_A(2) QDR2_A(3) QDR2_A(4) QDR2_A(5) QDR2_A(6) QDR2_A(7) QDR2_A(8) QDR2_A(9) QDR2_A(10) QDR2_A(11) QDR2_A(12) QDR2_A(13) QDR2_A(14) QDR2_A(15) QDR2_A(16) QDR2_A(17) QDR2_A(18) QDR2_A(19) QDR2_A(20) QDR2_A(21) QDR2_A(22) QDR2_A(23)	O	Address to SRAMs. Some addresses signals can be programmed to act as additional Port Enables (via CSR control). Refer to Table 2 QDR Address/RPE/WPE Mapping.	24
QDR3_A(0) QDR3_A(1) QDR3_A(2) QDR3_A(3) QDR3_A(4) QDR3_A(5) QDR3_A(6) QDR3_A(7) QDR3_A(8) QDR3_A(9) QDR3_A(10) QDR3_A(11) QDR3_A(12) QDR3_A(13) QDR3_A(14) QDR3_A(15) QDR3_A(16) QDR3_A(17) QDR3_A(18) QDR3_A(19) QDR3_A(20) QDR3_A(21) QDR3_A(22) QDR3_A(23)	O	Address to SRAMs. Some addresses signals can be programmed to act as additional Port Enables (via CSR control). Refer to Table 2 QDR Address/RPE/WPE Mapping.	24

Table 6. SRAM Signals (Sheet 7 of 7)

Signal Name	I/O	Description	Number
VREF_QDR0, VREF_QDR1, VREF_QDR2, VREF_QDR3	I	HSTL Reference Voltage.	8
QDR0_ZQ(0) QDR0_ZQ(1) QDR1_ZQ(0) QDR1_ZQ(1) QDR2_ZQ(0) QDR2_ZQ(1) QDR3_ZQ(0) QDR3_ZQ(1)	I	Impedance Match. The QDRn_ZQ(0) pin for each channel should be connected to GND through a 50-ohm resistor. The QDRn_ZQ(1) pins for each channel should be connected to VDDQ (1.5 V) through a 50-ohm resistor. Internal circuits match the impedance of the output drivers to the value of this resistor. *Note*: the nominal value is 50 ohms, and the resistor range is 25 to 65 ohms. The resistor tolerance is +/- 1%.	8
Total			321

3.2.3 Media and Switch Fabric Interface (MSF)

The Media and Switch Fabric Interface is used to interface the network processor to SPI-4 PHY chips, CSIX Switch Fabrics, and to other network processors. MSF uses IEEE LVDS signaling levels for clock, data, control, and parity. The status channel and its clock use LVTTL signaling., or alternatively, can be configured to use LVDS I/O.

Table 7. MSF Data Signals (Sheet 1 of 4)

Signal Name	I/O	Type	SPI-4 Use	CSIX Use	Description	Number
SPI4_RCLK_H, SPI4_RCLK_L	I	LVDS	RDCLK	TxClk	Receive Clock. Used to register RDAT, RCTL, RPAR and RPROT.	2
SPI4_RCLK_REF_H, SPI4_RCLK_REF_L	O	LVDS	RCLK_REF		Receive Clock Reference. Buffered version of RCLK.	2

Table 7. MSF Data Signals (Sheet 2 of 4)

Signal Name	I/O	Type	SPI-4 Use	CSIX Use	Description	Number
SPI4_RDAT_H(0) SPI4_RDAT_H(1) SPI4_RDAT_H(2) SPI4_RDAT_H(3) SPI4_RDAT_H(4) SPI4_RDAT_H(5) SPI4_RDAT_H(6) SPI4_RDAT_H(7) SPI4_RDAT_H(8) SPI4_RDAT_H(9) SPI4_RDAT_H(10) SPI4_RDAT_H(11) SPI4_RDAT_H(12) SPI4_RDAT_H(13) SPI4_RDAT_H(14) SPI4_RDAT_H(15) SPI4_RDAT_L(0) SPI4_RDAT_L(1) SPI4_RDAT_L(2) SPI4_RDAT_L(3) SPI4_RDAT_L(4) SPI4_RDAT_L(5) SPI4_RDAT_L(6) SPI4_RDAT_L(7) SPI4_RDAT_L(8) SPI4_RDAT_L(9) SPI4_RDAT_L(10) SPI4_RDAT_L(11) SPI4_RDAT_L(12) SPI4_RDAT_L(13) SPI4_RDAT_L(14) SPI4_RDAT_L(15)	I	LVDS	RDAT[15:0]	TxData[15:0]	Receive Data. From PHY/Switch Fabric.	32
SPI4_RPAR_H SPI4_RPAR_L	I	LVDS	Not Used	TxPar	Receive Parity. If not used (i.e, SPI-4 mode) then this differential pair should be set to a logical 1 (SPI4_RPAR_H = 1 and SPI4_RPAR_L = 0). This is required for the dynamic training to function properly.[1]	2
SPI4_RCTL_H SPI4_RCTL_L	I	LVDS	RCTL	TxSOF	Receive Framing indicator.	2
SPI4_RPROT_H SPI4_RPROT_L	I	LVDS	RPROT	TPROT	Receive Protocol Type. It indicates the protocol type, SPI-4 or CSIX-L1, of the receive data, and can be tied statically low or high: 0 = SPI-4, 1 = CSIX-L1. RPROT must be driven to 1 during the entire CFRAME or 0 for the entire SPI-4 burst. If not used (i.e, SPI-4 mode) then this differential pair should be set to a logical 0 (SPI4_RPROT_H = 0 and SPI4_RPROT_L = 1). This is required for the dynamic training to function properly.[1.]	2
SPI4_RSCLK	O	LVTTL	RSCLK	--	Receive Status Clock. Reference for RSTAT.	2
SPI4_RSTAT(0) SPI4_RSTAT(1)	O	LVTTL	RSTAT[1:0]	--	Receive FIFO Status.	2

Table 7. MSF Data Signals (Sheet 3 of 4)

Signal Name	I/O	Type	SPI-4 Use	CSIX Use	Description	Number
SPI4_TCLK_REF_H, SPI4_TCLK_REF_L	I	LVDS	TCLK_REF		Transmit Clock Reference. Buffered and used to generate TCLK.	2
SPI4_TCLK_H, SPI4_TCLK_L	O	LVDS	TDCLK	RxClk	Transmit Clock. Used to register TDAT, TCTL, TPAR, and TPROT.	2
SPI4_TDAT_H(0) SPI4_TDAT_H(1) SPI4_TDAT_H(2) SPI4_TDAT_H(3) SPI4_TDAT_H(4) SPI4_TDAT_H(5) SPI4_TDAT_H(6) SPI4_TDAT_H(7) SPI4_TDAT_H(8) SPI4_TDAT_H(9) SPI4_TDAT_H(10) SPI4_TDAT_H(11) SPI4_TDAT_H(12) SPI4_TDAT_H(13) SPI4_TDAT_H(14) SPI4_TDAT_H(15) SPI4_TDAT_L(0) SPI4_TDAT_L(1) SPI4_TDAT_L(2) SPI4_TDAT_L(3) SPI4_TDAT_L(4) SPI4_TDAT_L(5) SPI4_TDAT_L(6) SPI4_TDAT_L(7) SPI4_TDAT_L(8) SPI4_TDAT_L(9) SPI4_TDAT_L(10) SPI4_TDAT_L(11) SPI4_TDAT_L(12) SPI4_TDAT_L(13) SPI4_TDAT_L(14) SPI4_TDAT_L(15)	O	LVDS	TDAT[15:0]	RxData[15:0]	Transmit Data to PHY/Switch Fabric.	32
SPI4_TCTL_H, SPI4_TCTL_L	O	LVDS	TCTL	RxSOF	Transmit Framing indicator.	2
SPI4_TPAR_H, SPI4_TPAR_L	O	LVDS	Not Used	RxPar	Transmit Parity.	2
SPI4_TPROT_H, SPI4_TPROT_L	O	LVDS	TPROT	RPROT	Transmit Protocol Type. It indicates the protocol type, SPI-4 or CSIX-L1, of the transmit data, and can be ignored if not needed: 0 = SPI-4, 1 = CSIX-L1. TPROT is driven to 1 during the entire CFRAME or 0 for the entire SPI-4 burst.	2
SPI4_TSCLK	I	LVTTL	TSCLK	--	Transmit Status Clock. Used to register TSTAT.	1
SPI4_TSTAT(0), SPI4_TSTAT(1)	I	LVTTL	TSTAT[1:0]	--	Transmit FIFO Status.	2
SPI4_PREEMP	I	LVTTL			Impedance Match. In normal operation, should be tied to logical 0.	1

Table 7. MSF Data Signals (Sheet 4 of 4)

Signal Name	I/O	Type	SPI-4 Use	CSIX Use	Description	Number
SPI4_ZQ2 SPI4_ZQ1	I/O				Impedance Match. The ZQ1 and ZQ2 pins should be connected together through a 100-ohm resistor. Internal circuitry matches the impedance of the internal termination resistors on all LVDS input pairs to value of this resistor.	2
Total						95

1. Floating and unused LVDS inputs should be terminated, as specified in Section 3.3.

The next group in Table 8 is used to communicate flow control information between two network processors.

Table 8. MSF Flow Control Signals (Sheet 1 of 2)

Signal Name	I/O	Type	SPI-4 Use[1] (Note 1)	CSIX Use	Description	Number
FC_TXCCLK_H, FC_TXCCLK_L	O	LVDS	RSCLK	TXCCLK	Flow Control Egress Clock. Reference for TXCSRB, TXCDAT, TXCSOF, TXCPAR, and RXCFC. FIFO status clock for SPI-4.	2
FC_TXCSRB_H, FC_TXCSRB_L	O	LVDS	--	TXCSRB	Flow Control Egress Serialized Ready Bits.	2
FC_TXCDAT_H(0) FC_TXCDAT_H(1) FC_TXCDAT_H(2) FC_TXCDAT_H(3) FC_TXCDAT_L(0) FC_TXCDAT_L(1) FC_TXCDAT_L(2) FC_TXCDAT_L(3)	O	LVDS	RSTAT[1:0]	TXCDAT[3:0]	Flow Control Egress Data – CSIX. Receive FIFO Status – SPI-4. *Note*: When used in LVDS RSTAT mode, only FC_TXCDAT_H/_L[1:0] are used. FC_TXCDAT_H/_L[3:2] are unused.	8
FC_TXCSOF_H, FC_TXCSOF_L	O	LVDS	--	TXCSOF	Flow Control Egress Start of Frame.	2
FC_TXCPAR_H, FC_TXCPAR_L	O	LVDS	--	TXCPAR	Flow Control Egress Parity.	2
FC_TXCFC_H, FC_TXCFC_L	I	LVDS	--	TXCFC	Flow Control Egress FIFO Full. This signal is received relative to TXCCLK, but is treated as asynchronous; also used during Flow Control pin training.[2]	2
FC_RXCCLK_H, FC_RXCCLK_L	I	LVDS	TSCLK	RXCCLK	Transmit Status Ingress Clock. Used to register RXCSRB, RXCDAT, RXCSOF, and RXCPAR. FIFO status clock for SPI-4.[2]	2
FC_RXCSRB_H, FC_RXCSRB_L	I	LVDS	--	RXCSRB	Flow Control Ingress Serialized Ready Bits.[2]	2

Table 8. MSF Flow Control Signals (Sheet 2 of 2)

Signal Name	I/O	Type	SPI-4 Use[1] (Note 1)	CSIX Use	Description	Number
FC_RXCDAT_H(0) FC_RXCDAT_H(1) FC_RXCDAT_H(2) FC_RXCDAT_H(3) FC_RXCDAT_L(0) FC_RXCDAT_L(1) FC_RXCDAT_L(2) FC_RXCDAT_L(3)	I	LVDS	TSTAT[1:0]	RXCDAT[3:0]	Flow Control Ingress Data – CSIX. Transmit Status – SPI-4. *Note*: When used in LVDS TSTAT mode, only FC_RXCDAT_H/_L[1:0] are used. FC_RXCDAT_H/_L[3:2] are unused.[2]	8
FC_RXCSOF_H, FC_RXCSOF_L	I	LVDS		RXCSOF	Flow Control Ingress Start of Frame.[2]	2
FC_RXCPAR_H, FC_RXCPAR_L	I	LVDS		RXCPAR	Flow Control Ingress Parity. If not used, then this differential pair should be set to a logical 0 (FC_RXCPAR_H = 0 and FC_RXCPAR_L = 1). This is required for the dynamic training to function properly.[2]	2
FC_RXCFC_H, FC_RXCFC_L	O	LVDS		RXCFC	Flow Control Ingress FIFO Full.	2
FC_ZQ(1) FC_ZQ(2)	I/O				Impedance Match. The ZQ1 and ZQ2 pins should be connected together through a 100-ohm resistor.	2
VREFLO VREFLO	I				Reference Voltage.	2
VREFHI VREFHI	I				Reference Voltage.	2
FC_PREEMP	I	LVTTL			Impedance Match. In normal operation, should be tied to logical 0.	1
Total						43

1. SPI-4 can use LVDS Status channel in place of LVTTL pins defined in Table 5. LVDS pins are enabled by MSF_RX_Control[RSTAT_Select] and MSF_TX_Control[TSTAT_Select].
2. Floating and unused LVDS inputs should be terminated, as specified in Section 3.3.

3.2.4 PCI

The PCI Bus can be used to interface to industry standard I/O devices, or to a Host processor; see Table 9 for a list of signals. PCI signaling levels are defined in *PCI Local Bus Specification, Version 2.2**.

Table 9. PCI Signals (Sheet 1 of 3)

Signal Name	I/O	Description	Number
PCI_AD(0) PCI_AD(1) PCI_AD(2) PCI_AD(3) PCI_AD(4) PCI_AD(5) PCI_AD(6) PCI_AD(7) PCI_AD(8) PCI_AD(9) PCI_AD(10) PCI_AD(11) PCI_AD(12) PCI_AD(13) PCI_AD(14) PCI_AD(15) PCI_AD(16) PCI_AD(17) PCI_AD(18) PCI_AD(19) PCI_AD(20) PCI_AD(21) PCI_AD(22) PCI_AD(23) PCI_AD(24) PCI_AD(25) PCI_AD(26) PCI_AD(27) PCI_AD(28) PCI_AD(29) PCI_AD(30) PCI_AD(31) PCI_AD(32) PCI_AD(33) PCI_AD(34) PCI_AD(35) PCI_AD(36) PCI_AD(37) PCI_AD(38) PCI_AD(39) PCI_AD(40) PCI_AD(41) PCI_AD(42) PCI_AD(43) PCI_AD(44) PCI_AD(45) PCI_AD(46) PCI_AD(47) PCI_AD(48) PCI_AD(49) PCI_AD(50) PCI_AD(51) PCI_AD(52) PCI_AD(53) PCI_AD(54)	I/O	Address/data bus	64

Table 9. PCI Signals (Sheet 2 of 3)

Signal Name	I/O	Description	Number
PCI_AD(55) PCI_AD(56) PCI_AD(57) PCI_AD(58) PCI_AD(59) PCI_AD(60) PCI_AD(61) PCI_AD(62) PCI_AD(63)			
PCI_CBE_L(0) - PCI_CBE_L(7)	I/O	Cycle Status/Byte Enable	8
PCI_PAR	I/O	Parity Data	1
PCI_PAR64	I/O	Parity Data	1
PCI_FRAME_L	I/O	Frame	1
PCI_IRDY_L	I/O	Initiator Ready	1
PCI_TRDY_L	I/O	Target Ready	1
PCI_STOP_L	I/O	Stop	1
PCI_DEVSEL_L	I/O	Device Select	1
PCI_IDSEL	I	Initialization Device Select	1
PCI_REQ64_L	I/O	64-Bit Request	1
PCI_ACK64_L	I/O	64-Bit Acknowledge	1
PCI_PERR_L	I/O	Parity Error	1
PCI_SERR_L	I/O D	System Error	1
PCI_REQ_L(0)	I/O	Bus Request. Input from external bus master when internal PCI arbiter is used. Output to external arbiter when internal arbiter is not used.	1
PCI_REQ_L(1)	I	Bus Request. Input from external bus master when internal PCI arbiter is used.	1
PCI_GNT_L(0)	I/O	Bus Grant. Output to external bus master when IXP2800/IXP2850 arbiter is used. Input to IXP2800/IXP2850 from external PCI arbiter when internal arbiter is not used.	1
PCI_GNT_L(1)	O	Bus Grant. Output to external bus master when internal PCI arbiter is used.	1
PCI_INTA_L	I/O D	PCI Interrupt. Input when IXP2800/IXP2850 is host; output when IXP2800/IXP2850 is not host.	1
PCI_INTB_L	I	Interrupt	1
PCI_RST_L	I/O	Bus Reset	1
PCI_CLK	I	Bus clock	1
PCI_M66EN	I	66-MHz Enable	1

Table 9. PCI Signals (Sheet 3 of 3)

Signal Name	I/O	Description	Number
PCI_ZQ1, PCI_ZQ2	I/O	Impedance Match. The PCI_ZQ1 pin should be tied to VSS through a 31.6-ohm resistor. Internal circuits match the impedance of the output drivers to the value of this resistor when the outputs are driving a high logic level. *Note*: The nominal value for ZQ1 is 31.6 ohms, and the resistor range is 30.1 to 34 ohms. The resistor tolerance should be +/- 1%. The PCI_ZQ2 pin should be connected to VCC3.3 through a 28-ohm resistor. Internal circuits match the impedance of the output drivers to the value of this resistor when the outputs are driving a low logic level. *Note*: The nominal value for ZQ2 is 28 ohms, and the resistor range is 27.4 to 31.6 ohms. The resistor tolerance should be +/- 1%.	2
Total			95

3.2.5 Slowport Signals

The Slowport is used to interface to asynchronous devices. Typically this will be a Flash ROM (Boot ROM) and maintenance port of MAC devices. Slowport signals use LVTTL signaling levels (see Table 10).

Table 10. Slowport Signals

Signal Name	I/O	Description	Number
SP_CLK	O	Clock.	1
SP_WR_L	O	Write strobe.	1
SP_RD_L	O	Read strobe.	1
SP_AD(0) SP_AD(1) SP_AD(2) SP_AD(3) SP_AD(4) SP_AD(5) SP_AD(6) SP_AD(7)	I/O	Multiplexed Address and Data.	8
SP_ACK_L	I	Acknowledge signal.	1
SP_CS_L(0), SP_CS_L(1)	O	Device selects.	2
SP_ALE_L	O	Address latch enable.	1
SP_CP/SP_A0	O	Latch enable for 16 or 32-bit data bus devices. Address [0] for 8-bit devices.	1
SP_OE_L	O	Output enable.	1
SP_DIR/SP_A1	O	Data transaction direction. Low for read, high for write. Address [1] for 8-bit devices.	1
Total			18

3.2.6 GPIO Signals

GPIO are general-purpose I/O signals. They can be used for slow speed, software-controlled I/O such as LEDs and input switches. They are also three-stated during reset to bring configuration information into the network processor; the information is latched at the deassertion of CLK_NRESET. The GPIO signals use LVTTL signaling levels – see Table 11.

Table 11. GPIO Signals

Signal Name	I/O	Description	Number
GPIO(0) GPIO(1) GPIO(2) GPIO(3) GPIO(4) GPIO(5) GPIO(6) GPIO(7)	I/O	General Purpose I/O.	8
Total			8

3.2.7 Serial Port Signals

The serial port is an RS-232 compatible UART used for debug and diagnostics. See Table 12 for the serial port signals.

Table 12. Serial Port Signals

Signal Name	I/O	Description	Number
SR_RX	I	Receive data into the UART.	1
SR_TX	O	Transmit data from the UART.	1
Total			2

3.2.8 Clock and Reset Signals

All Clock and Reset signals, except for CLK_REF_CLK_H and CLK_REF_CLK_L, use LVTTL signaling levels. Table 13 lists the clock and reset signals.

Table 13. Clock Signals (Sheet 1 of 2)

Signal Name	I/O	Description	Number
CLK_REF_CLK_H CLK_REF_CLK_L	I	PLL Clock Reference (LVDS). The CLK_REF_CLK input pair does not have active on-die termination. This input pair must be terminated on the PCB with a 100-ohm resistor between the CLK_REF_CLK_H and CLK_REF_CLK_L pins.	2
CLK_PHASE_REF	O	Reference clock phase delay output. In test mode, this output pin determines the REF_CLK_LVDS input buffer delay. In normal operation, this pin outputs the programmed DRAM_N clock frequency from the on-board PLL divided by 2, which is then used as the reference clock for the Direct Rambus Clock Generator (DRCG).	1
CLK_STOP	I	PLL Stop Test Mode. Tie to logical 0 in normal operation.	1

Table 13. Clock Signals (Sheet 2 of 2)

Signal Name	I/O	Description	Number
CLK_PLL_BYP	I	PLL Bypass Test Mode. When asserted, the IXP2800/IXP2850 uses the external clock inputs (CLK_REF_CLK in place of PLL clocks. This pin should be tied to logical 0 during normal operation.	1
CLK_NRESET	I	Master Reset Input. Active low. All configuration strap options are latched on the deassertion of this signal. This signal must be toggled even in PCI BOOT mode to latch the configuration straps options.	1
CLK_NRESET_OUT	O	Reset Output. Active low. This output is controlled by configuration pin SP_AD[7] listed in Table 16 Configuration Pins.	1
Total			7

3.2.9 Power Supply Pins

Table 14. Power Supply Pins (Sheet 1 of 2)

Signal Names	Total	Pin Descriptions
VCC_CLK	1	2.5 V supply. May be tied to the same board level supply as VCC25V.
VCC_FUSE	4	1.35/1.3/1.2 V supply for the fuse logic. May be tied to the same board level supply as VCC. The fuse circuit supply has been isolated from VCC because this supply must be elevated during the fuse programming sequence, which only occurs during final manufacturing test (not user accessible).
VREFHI_CLK	1	These pins should be tied to VSS (logical 0).
VREFLO_CLK	1	These pins should be tied to VSS (logical 0).
VCC_PLL	1	1.35/1.3/1.2 V supply for the on-chip PLL. If the board level supply is exceptionally clean, this supply could be tied to the same board level supply as VCC. Given that most applications witness substantial noise on VCC, the VCC_PLL should be generated by filtering VCC with an LC network (see Figure 10).
VCC	78	Core power supply.
VSS	371	Core ground.
VCC25V	28	SPI-4 supply (also for PCI).
VCCA_FC	1	DLL power. Should be generated by filtering VCC with an LC network (see Figure 10).
VCCA_SPI4	1	DLL power. Should be generated by filtering VCC with an LC network (see Figure 10).
VREFHI	2	SPI-4/flow reference voltage.
VREFLO	2	SPI-4/flow reference voltage.
VCC33	4	GPIO, JTAG, SP power.
VCC33_PCI	12	PCI power supply.
VDDQ	101	QDR power supply.
PAS0_VCCA	1	DLL power. Should be generated by filtering VCC with an LC network (see Figure 10).

Table 14. Power Supply Pins (Sheet 2 of 2)

Signal Names	Total	Pin Descriptions
PAS1_VCCA	1	DLL power. Should be generated by filtering VCC with an LC network (see Figure 10).
PAS2_VCCA	1	DLL power. Should be generated by filtering VCC with an LC network (see Figure 10).
PAS3_VCCA	1	DLL power. Should be generated by filtering VCC with an LC network (see Figure 10).
VREF_QDR0	2	QDR reference voltage.
VREF_QDR1	2	QDR reference voltage.
VREF_QDR2	2	QDR reference voltage.
VREF_QDR3	2	QDR reference voltage.
VCCR	14	RDRAM core processor.
VCCRA	6	RDRAM clean power. Should be generated by filtering VCC with an LC network (see Figure 10).
VCCRIO	9	RDRAM I/O power.
PAR0_PADVREFA	1	RDRAM reference voltage.
PAR0_PADVREFB	1	RDRAM reference voltage.
PAR1_PADVREFA	1	RDRAM reference voltage.
PAR1_PADVREFB	1	RDRAM reference voltage.
PAR2_PADVREFA	1	RDRAM reference voltage.
PAR2_PADVREFB	1	RDRAM reference voltage.
Total Power Supply Pins	655	

3.2.10 Test and JTAG Signals

JTAG is the IEEE 1149.1 test access port. The JTAG input signals have a weak pullup resistor internal to the chip, so that any input that is not terminated, is interpreted as a high. Other test signals are network processor specific, for manufacturing use only. See Table 15.

Table 15. Test and JTAG Signals (Sheet 1 of 2)

Signal Name	I/O	Description	Number
JTAG_TCK	I	Test interface reference clock that times all the transfers on the JTAG test interface.	1
JTAG_TMS	I	Test interface mode select. **Tms** causes state transitions in the test access port (TAP) controller.	1
JTAG_TDI	I	Test interface data input. **Tdi** is the serial input through which JTAG instructions and test data enter the JTAG interface.	1
JTAG_TDO	OZ	Test interface data output. **Tdo** is the serial output through which test instructions and data from the test logic leave the network processor.	1

Table 15. Test and JTAG Signals (Sheet 2 of 2)

Signal Name	I/O	Description	Number
JTAG_TRST	I	Test interface reset. When asserted low, the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. This pin must be driven or held low to achieve normal device operation.	1
TEST_SCAN_CLK_A TEST_SCAN_CLK_B	I	Scan Chain Clocks. These pins are used to input the scan clocks used during scan testing and must be tied to a logical 1 in a system environment.	2
TEST_SCAN_EN	I	Scan Chain Enable. This input pin places the chip in scan test mode when asserted, and is only used during scan testing. This pin should be tied to a logical 0 in a system environment.	1
TEST_SCAN_MODE	I	Strobe Test Mode Pins. This input pin is used to latch values into the Test Mode Register and is used in conjunction with INTERRUPT_MODE, SP_AD[7:0] and GPIO[3:0] during scan testing. This pin should be tied to a logical 0 in a system environment. *Note*: For the A stepping of the device, the name of this pin was TEST_CLK. The name was changed in the B stepping; however, the functionality of the pin is identical.	1
TEST_DIODE_A	I	Thermal Diode Anode. This pin should be tied to a logical 0 if the pin is not being used.	1
INTERRUPT_MODE	I	1—Selects signals from the GPIO and Slowport pins to be routed to the Test Box instead of the GPIO and Slowport ports, and sets the JTAG_TMS, TEST_SCAN_MODE, JTAG_TDI, and TEST_SCAN_EN pins to operate in their test mode. 0—These pins have their normal function. This pin should be tied to a logical 0 in a system environment. *Note*: For the A stepping of the device, the name of this pin was TEST_MODE_LOAD. The name was changed in the B stepping; however, the functionality of the pin is identical.	1
TEST_DIODE_C	I	Thermal Diode Cathode. This pin should be tied to a logical 0 if the pin is not being used.	1
CLK_RST_DIS	I	This is a test mode control input to the IXP2800/IXP2850 and is only used during scan testing. This signal must be tied to a logical 0 in a system environment.	
Total			12

3.2.11 Configuration Pins

These pins are tied statically high or low through a resistor to provide configuration information into the network processor at reset. For all but CFG_RST_DIR, these pins are used for other purposes after reset. For those pins, the configuration information is sampled at the deassertion (rising) edge of CLK_NRESET. The values sampled can be read in the Strap_Options register.

Table 16. Configuration Pins

Pin	Configuration Function	Description
CLK_CFG_RST_DIR	CFG_RST_DIR	Determines direction of PCI_RST# signal: • 1—Network processor is the host supporting central functions. PCI_RST# is an output. NRESET is used as reset input. • 0—External PCI host supporting central functions. PCI_RST# is an input.
GPIO[0]	CFG_PROM_BOOT	Indicates if Boot ROM is present: • 0—No Boot ROM; host must download Boot image into DRAM • 1—Boot ROM is present
GPIO[1]	CFG_PCI_BOOT_HOST	Indicates if the Host or Intel XScale® core will configure PCI devices: • 0—External Host • 1—IXP2800
GPIO[2]	CFG_PCI_ARB	PCI Arbiter Used: • 0—IXP2800/IXP2850 is not the arbiter • 1—IXP2800/IXP2850 is the arbiter
GPIO[4:3]	CFG_PCI_DWIN[1:0]	Select DRAM BAR Window Size: • 11—1024 Mbyte • 10—512 Mbyte • 01—256 Mbyte • 00—128 Mbyte
GPIO[6:5]	CFG_PCI_SWIN[1:0]	Select SRAM BAR Window Size: • 11—256 Mbyte • 10—128 Mbyte • 01—64 Mbyte • 00—32 Mbyte
SP_AD[5:0]	CFG_PLL_MULT[5:0]	Select PLL Multiplier: • 0x10—16 • 0x12—18 • ... • 0x30—48 *Note*: Only even multipliers between 0x16 - 0x48 are supported.
SP_AD[6]	CFG_MSF_FREQ_SEL	Select source of MSF Tx Clock: • 0—TCLK_Ref input pin • 1—Internally generated clock
SP_AD[7]	RESET_OUT_STRAP	• 1—nRESET_OUT is removed after PLL locks. • 0—nRESET_OUT is removed by software using bit IXP_RESET0[17].

3.2.12 Pin State During Reset

Table 17 defines the state of both the output (O) and bidirectional (TS) pins during reset.

Table 17. Pin State During Reset (Sheet 1 of 4)

Function	Pin name	Initial Values	Comment
SRAM	QDRn_A_H[23:0]	Output, low	
SRAM	QDRn_RPS_L[1:0]	Output, high	
SRAM	QDRn_WPS_L[1:0]	Output, high	
SRAM	QDRn_BWS_L[1:0]	Output, high	
SRAM	QDRn_K_L[1:0] QDRn_K_H[1:0]	Clock out	
SRAM	QDRn_C_L[1:0] QDRn_C_H[1:0]	Clock out	
SRAM	QDRn_D_H[17:0]	Output, low	
SRAM	QDRn_Cin_L[1:0] QDRn_Cin_H[1:0]	Clock in	QDRn_CIN_L(1) and QDRn_CIN_H(1) input pad outputs are not connected internally.
SRAM	QDRn_Q_H[17:0]	Input	
SRAM	QDRn_VREF[2:0]	0.75 V	
SRAM	QDRn_ZQ[0]	Pull down to GND through a 50-ohm resistor.	
SRAM	QDRn_ZQ[1]	Pull up to 1.5 V through a 50-ohm resistor.	
SRAM	VDDQ	1.5 V	
RDRAM	RDRn_DQA	RSL 0 1.8 V	Pin is to be 1.8 V by the external terminator when RSL 0.
RDRAM	RDRn_DQB	RSL 0	Pin is to be 1.8 V by the external terminator when RSL 0.
RDRAM	RDRn_RQ	RSL 0	Pin is to be 1.8 V by the external terminator when RSL 0.
RDRAM	RDRn_CTM, RDRn_CTMN	Clock	
RDRAM	RDRn_CFM, RDRn_CFMN	Clock	CFM and CFMN are directly connected to CTM and CTMN, respectively, inside the chip.
RDRAM	RDRn_SIO	Output, low	
RDRAM	RDRn_SCK	Output, high	
RDRAM	RDRn_CMD	Output, low	
RDRAM	RDRn_SYNCLKM	Clock	
RDRAM	RDRn_PCLKN	Clock	
RDRAM	VSS	GND	

Table 17. Pin State During Reset (Sheet 2 of 4)

Function	Pin name	Initial Values	Comment
PCI	PCI_AD[31:0]	Low = Central High = Non-Central	***Central Function:*** • During PCI reset (PCI_RST_L =0), the network processor needs to drive PCI_AD[31:0] and PCI_BE[3:0], PCI_PAR to low.The rest of the I/O devices will be in three states. • After PCI_RST_L is deasserted, the network processor will drive these I/O devices (PCI_AD[31:0], PCI_BE[3:0], and PCI_PAR) to three states unless the network processor owns the grant. ***Non-Central Function:*** • During PCI reset (PCI_RST_L =0), the network processor needs to drive all of the I/O devices to three states. Once the network processor owns the bus (grant), the network processor needs to drive these I/O devices PCI_AD[31:0], PCI_BE[3:0], and PCI_PAR to known values.
PCI	PCI_AD[63:32]	High-Z	Need external pullup.
PCI	PCI_CBE_L[3:0]	Low = Central High = Non-Central	***Central Function:*** • During PCI reset (PCI_RST_L =0), the network processor needs to drive PCI AD[31:0] and PCI_BE[3:0], PCI_PAR to low.The rest of the I/O devices will be in three states. • After PCI_RST_L is deasserted, the network processor will drive these I/O devices (PCI_AD[31:0], PCI_BE[3:0], and PCI_PAR) to three states unless the network processor owns the grant. ***Non-Central Function:*** • During PCI reset (PCI_RST_L =0), the network processor needs to drive all the I/O devices to three states. Once the network processor owns the bus (grant), the network processor needs to drive these I/O devices PCI_AD[31:0], PCI_BE[3:0], and PCI_PAR to known values.
PCI	PCI_CBE_L7:4	High-Z	Need external pullup.

Table 17. Pin State During Reset (Sheet 3 of 4)

Function	Pin name	Initial Values	Comment
PCI	PCI_PAR	Low = Central High = Non-Central	***Central Function***: • During PCI reset (PCI_RST_L =0), the network processor needs to drive PCI AD[31:0] and PCI_BE[3:0], PCI_PAR. In addition, The rest of the I/O devices will be in three states. • After PCI_RST_L is deasserted, the network processor will drive these I/O devices (PCI_AD[31:0], PCI_BE[3:0], PCI_PAR) to three states unless the network processor owns the grant. ***Non-Central Function:*** • During PCI reset (PCI_RST_L =0), the network processor needs to drive all the I/O devices to three states. Once the network processor owns the bus (grant), the network processor needs to drive these I/O devices PCI_AD[31:0], PCI_BE[3:0], and PCI_PAR to known values.
PCI	PCI_PAR64	High-Z	Need external pullup.
PCI	PCI_FRAME_L	High-Z	
PCI	PCI_IRDY_L	High-Z	
PCI	PCI_TRFY_L	High-Z	
PCI	PCI_STOP_L	High-Z	
PCI	PCI_DEVSEL_L	High-Z	
PCI	PCI_IDSEL	High-Z	
PCI	PCI_REQ64_L	Low = Central High-Z = Non_Central	***Central Function***: During PCI reset (PCI_RST_L =0), the network processor needs to drive PCI_Req64L low.
PCI	PCI_ACK64_L	High-Z	
PCI	PCI_PERR_L	High-Z	
PCI	PCI_SERR	High-Z	
PCI	PCI_REQ_L(0)	High-Z	
PCI	PCI_REQ_L(1)	High-Z	
PCI	PCI_GNT_L(0)	High-Z	
PCI	PCI_GNT_L(1)	High-Z	
PCI	PCI_INTA_L	High-Z	
PCI	PCI_INTB_L	High-Z	
PCI	PCI_RST_L	Input	
PCI	PCI_CLK	Input	
PCI	PCI_M66EN	Input	
PCI	PCI_ZQ1, PCI_ZQ2	Input	
GPIO	GPIO[7:0]	High Z	

Table 17. Pin State During Reset (Sheet 4 of 4)

Function	Pin name	Initial Values	Comment
Serial Port	SR_RX	Input	
Serial Port	SR_TX	Low	
Slowport	SP_CP, SP_DIR	Low	
Slowport	SP_AD[7:0]	High Z	
Slowport	SP_CLK	High	
Slowport	SP_WR_L	High	
Slowport	SP_RD_L	High	
Slowport	SP_ACK_L	High	
Slowport	SP_CS_Ln	High	
Slowport	SP_ALE_L	High	
Slowport	SP_OE_L	High	
Clock Signals	CLK_PHASE_REF	Outputs the clock signal driven from core.	
Clock Signals	CLK_NRESET_OUT	During reset, the value is 0; once reset goes away, the value changes to 1 after some delay.	
Clock Signals	CLK_REF_CLK_H, CLK_REF_CLK_L	Input	
Clock Signals	CLK_STOP	Input	
Clock Signals	CLK_PLL_BYP	Input	
Clock Signals	CLK_NRESET	Input	
MSF Data Signals	SPI4_RSTAT[1:0]	Output, high	
MSF Data Signals	SPI4_RCTL_REF, SPI4_TCLK	High Z	
MSF Data Signals	All other pins	Output, low	
MSF Flow Control SIgnals	FC_TXCCLK	Outputs the clock signal presented by the core logic.	
MSF Flow Control Signals	All other pins	Output, low	
Test and JTAG Signals	All pins	High Z	

3.2.13 Ball Assignment

This section describes the network processor ball assignment and lists the pins according to location (numeric) and in alphabetic order.

3.2.13.1 Pins Listed in Numeric Order

Table 18 lists the network processor pins in order of location (numeric), showing the location code and name of each pin.

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 1 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
A1	N/C	B1	RDR0_CMD
A2	RDR0_DQB[8]	B2	VSS
A3	RDR0_DQB[5]	B3	VSS
A4	RDR0_DQB[2]	B4	VSS
A5	RDR0_RQ[0]	B5	VSS
A6	RDR0_RQ[3]	B6	VSS
A7	RDR0_RQ[6]	B7	VSS
A8	RDR0_CTMN	B8	VSS
A9	RDR0_CTM	B9	VSS
A10	RDR0_DQA[2]	B10	VSS
A11	RDR0_DQA[5]	B11	VSS
A12	RDR0_DQA[6]	B12	VSS
A13	RDR1_CMD	B13	RDR1_SCLKN
A14	RDR1_DQB[8]	B14	VSS
A15	RDR1_DQB[7]	B15	VSS
A16	RDR1_DQB[4]	B16	VSS
A17	RDR1_RQ[0]	B17	VSS
A18	N/C	B18	RDR1_RQ[1]
A19	N/C	B19	VSS
A20	N/C	B20	RDR1_RQ[5]
A21	RDR1_CTMN	B21	VSS
A22	RDR1_CTM	B22	VSS
A23	RDR1_DQA[0]	B23	VSS
A24	RDR1_DQA[2]	B24	VSS
A25	RDR1_DQA[6]	B25	VSS
A26	RDR2_SIO	B26	VSS
A27	RDR2_DQB[8]	B27	VSS
A28	RDR2_DQB[7]	B28	VSS
A29	RDR2_DQB[4]	B29	VSS
A30	RDR2_RQ[0]	B30	VSS
A31	RDR2_RQ[1]	B31	VSS
A32	RDR2_RQ[4]	B32	VSS
A33	RDR2_CTMN	B33	VSS
A34	RDR2_CTM	B34	VSS
A35	RDR2_DQA[0]	B35	VSS
A36	RDR2_DQA[3]	B36	VSS
A37	VSS	B37	RDR2_DQA[8]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 2 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
C1	VSS	D1	RDR0_SIO
C2	VSS	D2	RDR0_PCLKM
C3	RDR0_DQB[6]	D3	VSS
C4	RDR0_DQB[3]	D4	VSS
C5	RDR0_DQB[1]	D5	VSS
C6	RDR0_RQ[2]	D6	VSS
C7	RDR0_RQ[5]	D7	VSS
C8	RDR0_CFMN	D8	VSS
C9	RDR0_CFM	D9	VSS
C10	RDR0_DQA[1]	D10	VSS
C11	RDR0_DQA[4]	D11	VSS
C12	RDR0_DQA[7]	D12	VSS
C13	VSS	D13	RDR1_SCK
C14	VSS	D14	RDR1_PCLKM
C15	RDR1_DQB[5]	D15	VSS
C16	RDR1_DQB[2]	D16	VSS
C17	RDR1_DQB[1]	D17	VSS
C18	VSS	D18	RDR1_RQ[2]
C19	RDR1_RQ[3]	D19	VSS
C20	VSS	D20	RDR1_RQ[7]
C21	RDR1_CFMN	D21	VSS
C22	RDR1_CFM	D22	VSS
C23	RDR1_DQA[1]	D23	VSS
C24	RDR1_DQA[4]	D24	VSS
C25	RDR1_DQA[8]	D25	VSS
C26	RDR2_SCK	D26	RDR2_SCLKN
C27	VSS	D27	RDR2_PCLKM
C28	RDR2_DQB[6]	D28	VSS
C29	RDR2_DQB[3]	D29	VSS
C30	RDR2_DQB[1]	D30	VSS
C31	RDR2_RQ[2]	D31	VSS
C32	RDR2_RQ[5]	D32	VSS
C33	RDR2_CFMN	D33	VSS
C34	RDR2_CFM	D34	VSS
C35	RDR2_DQA[1]	D35	VSS
C36	RDR2_DQA[4]	D36	VSS
C37	VSS	D37	RDR2_DQA[6]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 3 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
E1	VSS	F1	RDR0_SCK
E2	VSS	F2	RDR0_SCLKN
E3	RDR0_DQB[7]	F3	VSS
E4	RDR0_DQB[4]	F4	VSS
E5	RDR0_DQB[0]	F5	VSS
E6	RDR0_RQ[1]	F6	PAR0_PADVREFB
E7	RDR0_RQ[4]	F7	VSS
E8	RDR0_RQ[7]	F8	VSS
E9	VSS	F9	PAR0_PADVREFA
E10	RDR0_DQA[0]	F10	VSS
E11	RDR0_DQA[3]	F11	VSS
E12	RDR0_DQA[8]	F12	VSS
E13	VSS	F13	VSS
E14	VSS	F14	RDR1_SIO
E15	RDR1_DQB[6]	F15	VSS
E16	RDR1_DQB[3]	F16	VSS
E17	RDR1_DQB[0]	F17	VSS
E18	VSS	F18	PAR1_PADVREFB
E19	RDR1_RQ[4]	F19	VSS
E20	VSS	F20	PAR1_PADVREFA
E21	RDR1_RQ[6]	F21	VSS
E22	VSS	F22	VSS
E23	RDR1_DQA[3]	F23	VSS
E24	RDR1_DQA[5]	F24	VSS
E25	RDR1_DQA[7]	F25	VSS
E26	RDR2_CMD	F26	VSS
E27	VSS	F27	VSS
E28	RDR2_DQB[5]	F28	VSS
E29	RDR2_DQB[0]	F29	VSS
E30	RDR2_DQB[2]	F30	VSS
E31	RDR2_RQ[3]	F31	PAR2_PADVREFB
E32	RDR2_RQ[6]	F32	VSS
E33	RDR2_RQ[7]	F33	VSS
E34	VSS	F34	PAR2_PADVREFA
E35	RDR2_DQA[2]	F35	VSS
E36	RDR2_DQA[5]	F36	VSS
E37	VSS	F37	RDR2_DQA[7]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 4 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
G1	VCCRIO	H1	VCC33_PCI
G2	VSS	H2	PCI_AD[15]
G3	VCCRIO	H3	PCI_AD[9]
G4	VCCR	H4	VSS
G5	VCCRA	H5	PCI_AD[42]
G6	VSS	H6	PCI_AD[38]
G7	VCCR	H7	VCC33_PCI
G8	VCCR	H8	PCI_AD[35]
G9	VCCRA	H9	PCI_AD[33]
G10	VCCR	H10	VSS
G11	VCCRIO	H11	PCI_AD[53]
G12	VCCR	H12	PCI_AD[59]
G13	VSS	H13	VCC33_PCI
G14	VSS	H14	VSS
G15	VCCRIO	H15	PCI_AD[47]
G16	VSS	H16	VCC33_PCI
G17	VCCRIO	H17	VSS
G18	VSS	H18	VSS
G19	VCCRA	H19	SP_AD[0]
G20	VCCR	H20	TEST_SCAN_EN
G21	VCCR	H21	GPIO[7]
G22	VCCRA	H22	SR_RX
G23	VCCR	H23	VSS
G24	VCCRIO	H24	SP_RD_L
G25	VCCR	H25	SP_AD[1]
G26	VCCRIO	H26	VCC33
G27	VSS	H27	GPIO[1]
G28	VCCRIO	H28	SP_AD[5]
G29	VCCR	H29	VREFHI_CLK
G30	VCCRA	H30	VREFLO_CLK
G31	VSS	H31	VSS
G32	VCCR	H32	QDR3_Q_H[9]
G33	VCCR	H33	QDR3_Q_H[10]
G34	VCCRA	H34	VDDQ
G35	VCCR	H35	VDDQ
G36	VCCRIO	H36	VREF_QDR3
G37	VCCR	H37	VREF_QDR3

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 5 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
J1	PCI_AD[29]	K1	PCI_GNT_L[0]
J2	PCI_PAR	K2	VSS
J3	PCI_AD[10]	K3	PCI_AD[20]
J4	PCI_AD[8]	K4	PCI_AD[13]
J5	PCI_AD[61]	K5	PCI_AD[5]
J6	PCI_AD[56]	K6	PCI_AD[1]
J7	PCI_AD[55]	K7	PCI_CBE_L[7]
J8	PCI_AD[48]	K8	PCI_PAR64
J9	PCI_AD[44]	K9	PCI_AD[54]
J10	PCI_AD[40]	K10	PCI_AD[45]
J11	PCI_AD[34]	K11	PCI_AD[32]
J12	PCI_AD[2]	K12	PCI_AD[25]
J13	VCC25V	K13	PCI_AD[11]
J14	PCI_ACK64_L	K14	PCI_AD[51]
J15	PCI_CBE_L[4]	K15	PCI_AD[57]
J16	PCI_AD[39]	K16	PCI_AD[49]
J17	VCC25V	K17	VSS
J18	PCI_AD[41]	K18	PCI_AD[36]
J19	VCC_CLK	K19	VSS
J20	SP_CS_L[1]	K20	SP_AD[4]
J21	GPIO[3]	K21	JTAG_TRST
J22	JTAG_TMS	K22	CLK_STOP
J23	JTAG_TDI	K23	CLK_CFG_RST_DIR
J24	SP_AD[7]	K24	GPIO[5]
J25	SP_ACK_L	K25	GPIO[0]
J26	GPIO[2]	K26	SR_TX
J27	GPIO[4]	K27	SP_AD[2]
J28	SP_AD[6]	K28	SP_DIR
J29	TEST_DIODE_A	K29	TEST_DIODE_C
J30	VSS	K30	VSS
J31	VDDQ	K31	QDR3_Q_H[7]
J32	QDR3_Q_H[6]	K32	VSS
J33	QDR3_Q_H[11]	K33	QDR3_Q_H[12]
J34	VSS	K34	VDDQ
J35	QDR3_Q_H[5]	K35	QDR3_Q_H[4]
J36	QDR3_Q_H[13]	K36	VDDQ
J37	VSS	K37	QDR3_D_H[9]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 6 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
L1	PCI_GNT_L[1]	M1	VSS
L2	PCI_AD[28]	M2	PCI_INTA_L
L3	VCC33_PCI	M3	PCI_IDSEL
L4	PCI_AD[17]	M4	PCI_AD[22]
L5	VSS	M5	PCI_AD[31]
L6	PCI_AD[21]	M6	PCI_AD[30]
L7	PCI_TRDY_L	M7	PCI_AD[16]
L8	VCC33_PCI	M8	PCI_AD[7]
L9	PCI_AD[0]	M9	PCI_AD[3]
L10	PCI_AD[60]	M10	PCI_AD[62]
L11	VSS	M11	PCI_AD[46]
L12	PCI_M66EN	M12	PCI_AD[37]
L13	PCI_CBE_L[0]	M13	VCC25V
L14	VCC33_PCI	M14	PCI_AD[14]
L15	PCI_STOP_L	M15	PCI_CBE_L[6]
L16	PCI_AD[63]	M16	VSS
L17	PCI_AD[43]	M17	VCC33_PCI
L18	PCI_AD[50]	M18	VCC25V
L19	VSS	M19	VSS
L20	CLK_NRESET	M20	JTAG_TCK
L21	CLK_NRESET_OUT	M21	TEST_SCAN_MODE
L22	VCC33	M22	INTERRUPT_MODE
L23	VSS	M23	SP_CP
L24	GPIO[6]	M24	SP_CS_L[0]
L25	SP_ALE_L	M25	JTAG_TDO
L26	SP_WR_L	M26	SP_CLK
L27	SP_AD[3]	M27	SP_OE_L
L28	TEST_SCAN_CLK_A	M28	TEST_SCAN_CLK_B
L29	VCC33	M29	CLK_PHASE_REF
L30	QDR3_Q_H[8]	M30	QDR3_Q_H[3]
L31	VDDQ	M31	QDR3_Q_H[15]
L32	QDR3_Q_H[14]	M32	VSS
L33	QDR3_CIN_H[1]	M33	QDR3_CIN_H[0]
L34	VSS	M34	VDDQ
L35	VSS	M35	QDR3_CIN_L[1]
L36	QDR3_D_H[10]	M36	VDDQ
L37	VSS	M37	QDR3_D_H[11]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 7 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
N1	SPI4_RSTAT[0]	P1	VCC25V
N2	SPI4_RSCLK	P2	VSS
N3	SPI4_RSTAT[1]	P3	SPI4_TSTAT[1]
N4	PCI_CBE_L[3]	P4	SPI4_TSCLK
N5	PCI_DEVSEL_L	P5	SPI4_TSTAT[0]
N6	PCI_REQ_L[1]	P6	PCI_AD[26]
N7	PCI_AD[19]	P7	PCI_IRDY_L
N8	PCI_ZQ1	P8	PCI_SERR_L
N9	PCI_AD[4]	P9	VSS
N10	PCI_CBE_L[5]	P10	PCI_AD[6]
N11	PCI_AD[58]	P11	VCC33_PCI
N12	PCI_AD[52]	P12	PCI_REQ64_L
N13	VCC	P13	VSS
N14	VSS	P14	VCC
N15	VCC	P15	VSS
N16	VSS	P16	VCC
N17	VCC	P17	VSS
N18	VSS	P18	VCC
N19	VCC	P19	VSS
N20	VSS	P20	VCC
N21	VCC	P21	VSS
N22	VSS	P22	VCC
N23	VCC	P23	VSS
N24	VSS	P24	VCC
N25	VSS	P25	VCC_PLL
N26	CLK_RST_DIS	P26	CLK_PLL_BYP
N27	CLK_REF_CLK_L	P27	VSS
N28	CLK_REF_CLK_H	P28	VDDQ
N29	VSS	P29	QDR3_Q_H[17]
N30	QDR3_Q_H[16]	P30	QDR3_D_H[6]
N31	VDDQ	P31	QDR3_D_H[3]
N32	QDR3_D_H[8]	P32	VSS
N33	QDR3_D_H[7]	P33	QDR3_D_H[5]
N34	VSS	P34	VDDQ
N35	QDR3_CIN_L[0]	P35	QDR3_D_H[12]
N36	QDR3_A_H[23]	P36	VDDQ
N37	VSS	P37	QDR3_A_H[20]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 8 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
R1	SPI4_TDAT[3]	T1	SPI4_TDAT[11]
R2	SPI4_TDAT_L[3]	T2	SPI4_TDAT_L[11]
R3	VSS	T3	SPI4_TCLK
R4	VCC33_PCI	T4	SPI4_TCLK_L
R5	VCC33_PCI	T5	SPI4_TDAT[2]
R6	VSS	T6	SPI4_TDAT_L[2]
R7	PCI_INTB_L	T7	SPI4_PREEMP
R8	PCI_FRAME_L	T8	PCI_RST_L
R9	PCI_AD[23]	T9	PCI_CLK
R10	PCI_CBE_L[1]	T10	PCI_AD[18]
R11	PCI_AD[12]	T11	PCI_PERR_L
R12	PCI_ZQ2	T12	PCI_CBE_L[2]
R13	VCC	T13	VSS
R14	VSS	T14	VCC
R15	VCC	T15	VSS
R16	VSS	T16	VCC
R17	VCC	T17	VSS
R18	VSS	T18	VCC
R19	VCC	T19	VSS
R20	VSS	T20	VCC
R21	VCC	T21	VSS
R22	VSS	T22	VCC
R23	VCC	T23	VSS
R24	VSS	T24	VCC
R25	PAS3_VCCA	T25	VSS
R26	VCC33	T26	VSS
R27	QDR3_Q_H[1]	T27	QDR3_Q_H[0]
R28	QDR3_Q_H[2]	T28	VDDQ
R29	VSS	T29	QDR3_D_H[1]
R30	QDR3_D_H[15]	T30	QDR3_D_H[16]
R31	VDDQ	T31	QDR3_A_H[14]
R32	QDR3_D_H[14]	T32	VSS
R33	QDR3_D_H[4]	T33	QDR3_C_L[1]
R34	VSS	T34	VDDQ
R35	QDR3_D_H[13]	T35	QDR3_C_L[0]
R36	QDR3_A_H[22]	T36	VDDQ
R37	VSS	T37	QDR3_A_H[21]

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 9 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
U1	VCC25V	V1	N/C
U2	VSS	V2	SPI4_TDAT[6]
U3	VCC25V	V3	SPI4_TDAT_L[6]
U4	SPI4_TDAT[1]	V4	SPI4_TDAT[10]
U5	SPI4_TDAT_L[1]	V5	SPI4_TDAT_L[10]
U6	VSS	V6	SPI4_TDAT[5]
U7	VCC25V	V7	SPI4_TDAT_L[5]
U8	VCC33_PCI	V8	SPI4_TDAT[7]
U9	VSS	V9	SPI4_TDAT_L[7]
U10	PCI_REQ_L[0]	V10	VSS
U11	PCI_AD[27]	V11	VCC25V
U12	PCI_AD[24]	V12	VSS
U13	VCC	V13	VSS
U14	VSS	V14	VCC
U15	VCC	V15	VSS
U16	VSS	V16	VCC
U17	VCC	V17	VSS
U18	VSS	V18	VCC
U19	VCC	V19	VSS
U20	VSS	V20	VCC
U21	VCC	V21	VSS
U22	VSS	V22	VCC
U23	VCC	V23	VSS
U24	VSS	V24	VCC
U25	VCC	V25	VSS
U26	QDR3_D_H[2]	V26	VSS
U27	QDR3_D_H[0]	V27	QDR3_A_H[19]
U28	QDR3_D_H[17]	V28	VDDQ
U29	VSS	V29	QDR3_A_H[3]
U30	QDR3_ZQ[0]	V30	QDR3_A_H[11]
U31	VDDQ	V31	QDR3_A_H[9]
U32	QDR3_ZQ[1]	V32	VSS
U33	QDR3_C_H[1]	V33	QDR3_BWS_L[1]
U34	VSS	V34	VDDQ
U35	QDR3_C_H[0]	V35	QDR3_A_H[10]
U36	QDR3_A_H[0]	V36	VSS
U37	QDR3_K_H[1]	V37	N/C

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 10 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
W1	N/C	Y1	N/C
W2	SPI4_TDAT[15]	Y2	VSS
W3	SPI4_TDAT_L[15]	Y3	SPI4_TDAT[8]
W4	VSS	Y4	SPI4_TDAT_L[8]
W5	VCC25V	Y5	SPI4_TDAT[13]
W6	SPI4_TDAT[14]	Y6	SPI4_TDAT_L[13]
W7	SPI4_TDAT_L[14]	Y7	SPI4_TDAT[4]
W8	VSS	Y8	SPI4_TDAT_L[4]
W9	VCC25V	Y9	SPI4_TDAT[12]
W10	VSS	Y10	SPI4_TDAT_L[12]
W11	SPI4_TDAT[9]	Y11	SPI4_RCLK_REF
W12	SPI4_TDAT_L[9]	Y12	SPI4_RCLK_REF_L
W13	VCC	Y13	VSS
W14	VSS	Y14	VCC
W15	VCC	Y15	VSS
W16	VSS	Y16	VCC
W17	VCC	Y17	VSS
W18	VSS	Y18	VCC
W19	VCC	Y19	VSS
W20	VSS	Y20	VCC
W21	VCC	Y21	VSS
W22	VSS	Y22	VCC
W23	VCC	Y23	VSS
W24	VSS	Y24	VCC
W25	VCC	Y25	VSS
W26	VSS	Y26	VSS
W27	QDR3_A_H[13]	Y27	QDR3_A_H[18]
W28	QDR3_A_H[8]	Y28	VDDQ
W29	VSS	Y29	QDR3_A_H[12]
W30	QDR3_RPS_L[1]	Y30	QDR3_A_H[16]
W31	VDDQ	Y31	QDR3_RPS_L[0]
W32	QDR3_BWS_L[0]	Y32	VSS
W33	QDR3_WPS_L[0]	Y33	QDR3_WPS_L[1]
W34	VSS	Y34	VDDQ
W35	QDR3_A_H[6]	Y35	QDR3_A_H[17]
W36	QDR3_K_H[0]	Y36	VDDQ
W37	N/C	Y37	N/C

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 11 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AA1	SPI4_TPROT	AB1	VSS
AA2	SPI4_TPROT_L	AB2	VCC25V
AA3	SPI4_TCTL	AB3	SPI4_TPAR
AA4	SPI4_TCTL_L	AB4	SPI4_TPAR_L
AA5	VSS	AB5	SPI4_RDAT_L[11]
AA6	VCC25V	AB6	SPI4_RDAT[11]
AA7	SPI4_TDAT[0]	AB7	SPI4_RDAT_L[13]
AA8	SPI4_TDAT_L[0]	AB8	SPI4_RDAT[13]
AA9	VSS	AB9	SPI4_RPAR_L
AA10	VCC25V	AB10	SPI4_RPAR
AA11	VCC25V	AB11	SPI4_RPROT_L
AA12	VSS	AB12	SPI4_RPROT
AA13	VCC	AB13	VCCA_SPI4
AA14	VSS	AB14	VCC
AA15	VCC	AB15	VSS
AA16	VSS	AB16	VCC
AA17	VCC	AB17	VSS
AA18	VSS	AB18	VCC
AA19	VCC	AB19	VSS
AA20	VSS	AB20	VCC
AA21	VCC	AB21	VSS
AA22	VSS	AB22	VCC
AA23	VCC	AB23	VSS
AA24	VSS	AB24	VCC
AA25	VCC	AB25	VSS
AA26	VDDQ	AB26	VSS
AA27	QDR2_A_H[19]	AB27	QDR2_A_H[18]
AA28	QDR2_A_H[12]	AB28	VDDQ
AA29	VSS	AB29	QDR2_A_H[11]
AA30	QDR3_A_H[7]	AB30	QDR2_A_H[9]
AA31	VDDQ	AB31	QDR2_A_H[14]
AA32	QDR3_A_H[5]	AB32	VSS
AA33	QDR3_A_H[4]	AB33	VDDQ
AA34	VSS	AB34	QDR3_A_H[2]
AA35	QDR3_A_H[15]	AB35	VDDQ
AA36	QDR3_K_L[1]	AB36	QDR3_A_H[1]
AA37	QDR3_K_L[0]	AB37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 12 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AC1	SPI4_RDAT_L[15]	AD1	SPI4_RDAT_L[7]
AC2	SPI4_RDAT[15]	AD2	SPI4_RDAT[7]
AC3	VSS	AD3	SPI4_RDAT_L[14]
AC4	VCC25V	AD4	SPI4_RDAT[14]
AC5	SPI4_RCLK_L	AD5	SPI4_RCTL_L
AC6	SPI4_RCLK	AD6	SPI4_RCTL
AC7	VSS	AD7	SPI4_TCLK_REF_L
AC8	VCC25V	AD8	SPI4_TCLK_REF
AC9	SPI4_ZQ1	AD9	SPI4_RDAT_L[12]
AC10	SPI4_ZQ2	AD10	SPI4_RDAT[12]
AC11	VREFHI	AD11	VCC25V
AC12	VREFLO	AD12	VSS
AC13	VCCA_FC	AD13	VCC_FUSE
AC14	VSS	AD14	VCC_FUSE
AC15	VCC	AD15	VSS
AC16	VSS	AD16	VCC
AC17	VCC	AD17	VSS
AC18	VSS	AD18	VCC
AC19	VCC	AD19	VSS
AC20	VSS	AD20	VCC
AC21	VCC	AD21	VSS
AC22	VSS	AD22	VCC
AC23	VCC	AD23	VSS
AC24	VSS	AD24	VCC
AC25	VCC	AD25	VSS
AC26	VSS	AD26	VSS
AC27	VSS	AD27	VSS
AC28	QDR2_A_H[3]	AD28	VDDQ
AC29	VSS	AD29	QDR2_RPS_L[1]
AC30	QDR2_A_H[21]	AD30	QDR2_RPS_L[0]
AC31	VDDQ	AD31	QDR2_BWS_L[0]
AC32	QDR2_A_H[22]	AD32	VSS
AC33	QDR2_A_H[20]	AD33	QDR2_WPS_L[1]
AC34	VDDQ	AD34	VSS
AC35	QDR2_A_H[10]	AD35	QDR2_A_H[8]
AC36	VDDQ	AD36	QDR2_A_H[13]
AC37	QDR2_K_L[0]	AD37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 13 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AE1	VSS	AF1	SPI4_RDAT_L[5]
AE2	VCC25V	AF2	SPI4_RDAT[5]
AE3	SPI4_RDAT_L[2]	AF3	SPI4_RDAT_L[10]
AE4	SPI4_RDAT[2]	AF4	SPI4_RDAT[10]
AE5	VSS	AF5	SPI4_RDAT_L[3]
AE6	VCC25V	AF6	SPI4_RDAT[3]
AE7	SPI4_RDAT_L[6]	AF7	SPI4_RDAT_L[8]
AE8	SPI4_RDAT[6]	AF8	SPI4_RDAT[8]
AE9	VSS	AF9	FC_TXCDAT[1]
AE10	VCC25V	AF10	FC_TXCDAT_L[1]
AE11	FC_TXCDAT_L[0]	AF11	FC_TXCSRB_L
AE12	FC_TXCDAT[0]	AF12	FC_TXCSRB
AE13	VCC_FUSE	AF13	VSS
AE14	VCC_FUSE	AF14	VSS
AE15	PAS0_VCCA	AF15	VDDQ
AE16	VSS	AF16	VSS
AE17	VCC	AF17	VSS
AE18	VSS	AF18	QDR0_A_H[12]
AE19	VCC	AF19	QDR0_K_H[0]
AE20	VSS	AF20	VSS
AE21	VCC	AF21	QDR1_A_H[1]
AE22	VSS	AF22	QDR1_A_H[5]
AE23	VCC	AF23	QDR1_A_H[23]
AE24	PAS1_VCCA	AF24	QDR1_Q_H[0]
AE25	PAS2_VCCA	AF25	VSS
AE26	VSS	AF26	VDDQ
AE27	QDR2_D_H[6]	AF27	QDR2_Q_H[8]
AE28	QDR2_D_H[8]	AF28	VDDQ
AE29	VSS	AF29	QDR2_D_H[10]
AE30	QDR2_A_H[23]	AF30	QDR2_ZQ[1]
AE31	VDDQ	AF31	QDR2_A_H[0]
AE32	QDR2_A_H[7]	AF32	VSS
AE33	QDR2_WPS_L[0]	AF33	QDR2_BWS_L[1]
AE34	VDDQ	AF34	VSS
AE35	QDR2_A_H[16]	AF35	QDR2_A_H[15]
AE36	VDDQ	AF36	QDR2_K_H[0]
AE37	QDR2_K_L[1]	AF37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 14 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AG1	SPI4_RDAT_L[4]	AH1	SPI4_RDAT_L[0]
AG2	SPI4_RDAT[4]	AH2	SPI4_RDAT[0]
AG3	SPI4_RDAT_L[1]	AH3	VSS
AG4	SPI4_RDAT[1]	AH4	VCC25V
AG5	SPI4_RDAT_L[9]	AH5	VSS
AG6	SPI4_RDAT[9]	AH6	VCC25V
AG7	VSS	AH7	FC_TXCCLK
AG8	VCC25V	AH8	FC_TXCCLK_L
AG9	FC_PREEMP	AH9	FC_TXCDAT[3]
AG10	FC_TXCDAT[2]	AH10	VSS
AG11	FC_TXCDAT_L[2]	AH11	VDDQ
AG12	VSS	AH12	QDR0_Q_H[7]
AG13	VSS	AH13	VDDQ
AG14	QDR0_Q_H[8]	AH14	QDR0_Q_H[9]
AG15	QDR0_D_H[8]	AH15	VDDQ
AG16	QDR0_D_H[6]	AH16	VSS
AG17	VSS	AH17	VDDQ
AG18	QDR0_A_H[11]	AH18	QDR0_A_H[9]
AG19	QDR0_A_H[3]	AH19	QDR0_K_L[0]
AG20	QDR1_A_H[4]	AH20	VDDQ
AG21	QDR1_BWS_L[0]	AH21	QDR1_A_H[17]
AG22	VSS	AH22	VDDQ
AG23	QDR1_D_H[2]	AH23	QDR1_D_H[0]
AG24	QDR1_Q_H[2]	AH24	VDDQ
AG25	QDR1_Q_H[1]	AH25	QDR1_Q_H[17]
AG26	QDR1_Q_H[16]	AH26	VDDQ
AG27	QDR2_Q_H[7]	AH27	QDR1_Q_H[15]
AG28	QDR2_Q_H[9]	AH28	VDDQ
AG29	VSS	AH29	QDR2_Q_H[6]
AG30	QDR2_D_H[9]	AH30	QDR2_D_H[7]
AG31	VDDQ	AH31	QDR2_D_H[11]
AG32	QDR2_ZQ[0]	AH32	VSS
AG33	QDR2_A_H[1]	AH33	QDR2_A_H[2]
AG34	VDDQ	AH34	VSS
AG35	QDR2_A_H[6]	AH35	QDR2_C_H[0]
AG36	VDDQ	AH36	QDR2_A_H[17]
AG37	QDR2_K_H[1]	AH37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 15 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AJ1	VSS	AK1	FC_RXCFC
AJ2	VCC25V	AK2	FC_RXCFC_L
AJ3	FC_TXCFC	AK3	FC_RXCPAR
AJ4	FC_TXCFC_L	AK4	FC_RXCPAR_L
AJ5	FC_TXCSOF	AK5	FC_RXCDAT[3]
AJ6	FC_TXCSOF_L	AK6	FC_RXCDAT_L[3]
AJ7	FC_TXCPAR	AK7	FC_ZQ2
AJ8	FC_TXCPAR_L	AK8	VDDQ
AJ9	FC_TXCDAT_L[3]	AK9	VSS
AJ10	VSS	AK10	QDR0_Q_H[10]
AJ11	QDR0_Q_H[6]	AK11	QDR0_D_H[2]
AJ12	VSS	AK12	QDR0_D_H[12]
AJ13	QDR0_D_H[10]	AK13	QDR0_ZQ[0]
AJ14	VSS	AK14	QDR0_D_H[9]
AJ15	VSS	AK15	QDR0_RPS_L[0]
AJ16	VSS	AK16	QDR0_A_H[23]
AJ17	QDR0_A_H[14]	AK17	QDR0_A_H[22]
AJ18	VSS	AK18	QDR0_A_H[19]
AJ19	VSS	AK19	QDR1_A_H[22]
AJ20	QDR1_A_H[3]	AK20	QDR1_A_H[12]
AJ21	VSS	AK21	QDR1_A_H[21]
AJ22	QDR1_D_H[17]	AK22	QDR1_RPS_L[0]
AJ23	VSS	AK23	QDR1_D_H[1]
AJ24	QDR1_D_H[6]	AK24	QDR1_D_H[16]
AJ25	VSS	AK25	QDR1_D_H[10]
AJ26	QDR1_Q_H[3]	AK26	QDR1_D_H[8]
AJ27	VSS	AK27	QDR1_Q_H[14]
AJ28	QDR1_Q_H[8]	AK28	QDR1_Q_H[7]
AJ29	VSS	AK29	QDR2_Q_H[10]
AJ30	QDR2_D_H[5]	AK30	QDR2_Q_H[11]
AJ31	VDDQ	AK31	QDR2_D_H[2]
AJ32	QDR2_D_H[13]	AK32	VSS
AJ33	QDR2_D_H[12]	AK33	QDR2_D_H[3]
AJ34	VDDQ	AK34	VSS
AJ35	QDR2_C_L[0]	AK35	QDR2_D_H[4]
AJ36	VDDQ	AK36	QDR2_A_H[4]
AJ37	QDR2_C_H[1]	AK37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 16 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AL1	FC_RXCSOF	AM1	FC_RXCCLK
AL2	FC_RXCSOF_L	AM2	FC_RXCCLK_L
AL3	VSS	AM3	FC_RXCDAT[2]
AL4	VCC25V	AM4	FC_RXCDAT_L[2]
AL5	VREFHI	AM5	VSS
AL6	VREFLO	AM6	QDR0_Q_H[0]
AL7	FC_ZQ1	AM7	QDR0_Q_H[5]
AL8	QDR0_Q_H[11]	AM8	QDR0_Q_H[13]
AL9	QDR0_Q_H[12]	AM9	VSS
AL10	VDDQ	AM10	QDR0_D_H[17]
AL11	QDR0_D_H[0]	AM11	VSS
AL12	VDDQ	AM12	QDR0_ZQ[1]
AL13	QDR0_D_H[11]	AM13	VSS
AL14	VDDQ	AM14	QDR0_D_H[7]
AL15	QDR0_RPS_L[1]	AM15	VSS
AL16	VDDQ	AM16	VSS
AL17	QDR0_A_H[20]	AM17	VSS
AL18	QDR0_A_H[0]	AM18	QDR0_A_H[7]
AL19	VDDQ	AM19	QDR1_A_H[20]
AL20	QDR1_A_H[11]	AM20	VSS
AL21	VDDQ	AM21	QDR1_A_H[9]
AL22	QDR1_RPS_L[1]	AM22	VSS
AL23	VDDQ	AM23	QDR1_ZQ[0]
AL24	QDR1_ZQ[1]	AM24	VSS
AL25	VDDQ	AM25	QDR1_D_H[3]
AL26	QDR1_D_H[9]	AM26	VSS
AL27	VDDQ	AM27	QDR1_D_H[7]
AL28	QDR1_Q_H[4]	AM28	VSS
AL29	VDDQ	AM29	QDR1_Q_H[13]
AL30	QDR2_Q_H[12]	AM30	VSS
AL31	QDR2_Q_H[5]	AM31	QDR2_Q_H[13]
AL32	QDR2_D_H[16]	AM32	VSS
AL33	QDR2_D_H[0]	AM33	QDR2_CIN_H[0]
AL34	VDDQ	AM34	VSS
AL35	QDR2_D_H[14]	AM35	QDR2_CIN_L[0]
AL36	VDDQ	AM36	QDR2_A_H[5]
AL37	QDR2_C_L[1]	AM37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 17 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AN1	VCC25V	AP1	FC_RXCSRB
AN2	VSS	AP2	FC_RXCSRB_L
AN3	FC_RXCDAT[1]	AP3	FC_RXCDAT[0]
AN4	FC_RXCDAT[1]_L	AP4	FC_RXCDAT[0]_L
AN5	VCC25V	AP5	VDDQ
AN6	QDR0_Q_H[1]	AP6	VSS
AN7	QDR0_Q_H[4]	AP7	QDR0_Q_H[17]
AN8	QDR0_CIN_H[1]	AP8	VSS
AN9	QDR0_CIN_H[0]	AP9	VDDQ
AN10	QDR0_D_H[15]	AP10	VSS
AN11	QDR0_D_H[14]	AP11	VDDQ
AN12	QDR0_D_H[5]	AP12	VSS
AN13	QDR0_A_H[18]	AP13	VDDQ
AN14	QDR0_A_H[17]	AP14	VSS
AN15	QDR0_WPS_L[0]	AP15	VDDQ
AN16	QDR0_BWS_L[1]	AP16	VSS
AN17	QDR0_A_H[8]	AP17	VDDQ
AN18	QDR0_WPS_L[1]	AP18	VSS
AN19	QDR1_A_H[19]	AP19	QDR1_K_H[0]
AN20	QDR1_WPS_L[1]	AP20	VSS
AN21	QDR1_WPS_L[0]	AP21	VDDQ
AN22	QDR1_BWS_L[1]	AP22	VSS
AN23	QDR1_A_H[0]	AP23	VDDQ
AN24	QDR1_A_H[14]	AP24	VSS
AN25	QDR1_D_H[15]	AP25	VDDQ
AN26	QDR1_D_H[5]	AP26	VSS
AN27	QDR1_D_H[11]	AP27	VDDQ
AN28	QDR1_CIN_H[0]	AP28	VSS
AN29	QDR1_CIN_H[1]	AP29	VDDQ
AN30	QDR1_Q_H[9]	AP30	VSS
AN31	QDR2_Q_H[15]	AP31	VDDQ
AN32	QDR2_Q_H[4]	AP32	VSS
AN33	QDR2_CIN_H[1]	AP33	VDDQ
AN34	VDDQ	AP34	VSS
AN35	QDR2_CIN_L[1]	AP35	QDR2_Q_H[14]
AN36	VDDQ	AP36	QDR2_D_H[1]
AN37	QDR2_D_H[15]	AP37	VSS

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 18 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AR1	VSS	AT1	VDDQ
AR2	VDDQ	AT2	VREF_QDR0
AR3	VSS	AT3	QDR0_Q_H[2]
AR4	VDDQ	AT4	QDR0_Q_H[16]
AR5	QDR0_Q_H[3]	AT5	VDDQ
AR6	QDR0_Q_H[15]	AT6	QDR0_D_H[16]
AR7	QDR0_Q_H[14]	AT7	VDDQ
AR8	QDR0_CIN_L[1]	AT8	QDR0_A_H[1]
AR9	QDR0_CIN_L[0]	AT9	VDDQ
AR10	QDR0_D_H[4]	AT10	QDR0_A_H[2]
AR11	QDR0_D_H[13]	AT11	VDDQ
AR12	QDR0_C_L[0]	AT12	QDR0_A_H[5]
AR13	QDR0_C_H[0]	AT13	VDDQ
AR14	QDR0_BWS_L[0]	AT14	QDR0_K_L[1]
AR15	QDR0_A_H[21]	AT15	VDDQ
AR16	QDR0_A_H[6]	AT16	QDR0_A_H[16]
AR17	QDR0_K_H[1]	AT17	VDDQ
AR18	QDR0_A_H[10]	AT18	QDR1_A_H[2]
AR19	QDR1_K_L[0]	AT19	VDDQ
AR20	QDR1_A_H[6]	AT20	QDR1_A_H[18]
AR21	QDR1_A_H[15]	AT21	VDDQ
AR22	QDR1_A_H[13]	AT22	QDR1_K_L[1]
AR23	QDR1_K_H[1]	AT23	VDDQ
AR24	QDR1_A_H[10]	AT24	QDR1_C_H[0]
AR25	QDR1_A_H[7]	AT25	VDDQ
AR26	QDR1_D_H[14]	AT26	QDR1_C_L[0]
AR27	QDR1_D_H[4]	AT27	VDDQ
AR28	QDR1_CIN_L[0]	AT28	QDR1_D_H[13]
AR29	QDR1_CIN_L[1]	AT29	VDDQ
AR30	QDR1_Q_H[11]	AT30	QDR1_Q_H[5]
AR31	QDR1_Q_H[6]	AT31	VDDQ
AR32	QDR1_Q_H[10]	AT32	VREF_QDR1
AR33	QDR2_Q_H[0]	AT33	VDDQ
AR34	QDR2_Q_H[1]	AT34	QDR2_Q_H[17]
AR35	QDR2_Q_H[3]	AT35	VDDQ
AR36	VDDQ	AT36	QDR2_Q_H[16]
AR37	QDR2_D_H[17]	AT37	VREF_QDR2

Table 18. IXP2800/IXP2850 Network Processor FCBGA Location Pin List (Sheet 19 of 19)

FCBGA Location	Pin Name	FCBGA Location	Pin Name
AU1	VSS	AU19	N/C
AU2	VSS	AU20	N/C
AU3	VREF_QDR0	AU21	QDR1_A_H[16]
AU4	VSS	AU22	VSS
AU5	QDR0_D_H[1]	AU23	QDR1_A_H[8]
AU6	VSS	AU24	VSS
AU7	QDR0_D_H[3]	AU25	QDR1_C_H[1]
AU8	VSS	AU26	VSS
AU9	QDR0_C_L[1]	AU27	QDR1_C_L[1]
AU10	VSS	AU28	VSS
AU11	QDR0_C_H[1]	AU29	QDR1_D_H[12]
AU12	VSS	AU30	VSS
AU13	QDR0_A_H[4]	AU31	QDR1_Q_H[12]
AU14	VSS	AU32	VSS
AU15	QDR0_A_H[15]	AU33	VREF_QDR1
AU16	VSS	AU34	VSS
AU17	QDR0_A_H[13]	AU35	QDR2_Q_H[2]
AU18	N/C	AU36	VREF_QDR2
AU37	VSS		

3.2.13.2 Pins Listed in Alphabetic Order

Table 19 lists the network processor pins in alphabetic order, showing the name and location code of each pin.

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 1 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
CLK_CFG_RST_DIR	K23	FC_TXCDAT_L[0]	AE11
CLK_NRESET	L20	FC_TXCDAT_L[1]	AF10
CLK_NRESET_OUT	L21	FC_TXCDAT_L[2]	AG11
CLK_PHASE_REF	M29	FC_TXCDAT_L[3]	AJ9
CLK_PLL_BYP	P26	FC_TXCFC	AJ3
CLK_REF_CLK_H	N28	FC_TXCFC_L	AJ4
CLK_REF_CLK_L	N27	FC_TXCPAR	AJ7
CLK_RST_DIS	N26	FC_TXCPAR_L	AJ8
CLK_STOP	K22	FC_TXCSOF	AJ5
FC_PREEMP	AG9	FC_TXCSOF_L	AJ6
FC_RXCCLK	AM1	FC_TXCSRB	AF12
FC_RXCCLK_L	AM2	FC_TXCSRB_L	AF11
FC_RXCDAT[0]	AP3	FC_ZQ1	AL7
FC_RXCDAT[0]_L	AP4	FC_ZQ2	AK7
FC_RXCDAT[1]	AN3	GPIO[0]	K25
FC_RXCDAT[1]_L	AN4	GPIO[1]	H27
FC_RXCDAT[2]	AM3	GPIO[2]	J26
FC_RXCDAT[2]_L	AM4	GPIO[3]	J21
FC_RXCDAT[3]	AK5	GPIO[4]	J27
FC_RXCDAT_L[3]	AK6	GPIO[5]	K24
FC_RXCFC	AK1	GPIO[6]	L24
FC_RXCFC_L	AK2	GPIO[7]	H21
FC_RXCPAR	AK3	JTAG_TCK	M20
FC_RXCPAR_L	AK4	JTAG_TDI	J23
FC_RXCSOF	AL1	JTAG_TDO	M25
FC_RXCSOF_L	AL2	JTAG_TMS	J22
FC_RXCSRB	AP1	JTAG_TRST	K21
FC_RXCSRB_L	AP2	N/C	A1
FC_TXCCLK	AH7	N/C	A18
FC_TXCCLK_L	AH8	N/C	A19
FC_TXCDAT[0]	AE12	N/C	A20
FC_TXCDAT[1]	AF9	N/C	AU18
FC_TXCDAT[2]	AG10	N/C	AU19
FC_TXCDAT[3]	AH9	N/C	AU20

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 2 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
N/C	V1	PCI_AD[18]	T10
N/C	V37	PCI_AD[19]	N7
N/C	W1	PCI_AD[20]	K3
N/C	W37	PCI_AD[21]	L6
N/C	Y1	PCI_AD[22]	M4
N/C	Y37	PCI_AD[23]	R9
PAR0_PADVREFA	F9	PCI_AD[24]	U12
PAR0_PADVREFB	F6	PCI_AD[25]	K12
PAR1_PADVREFA	F20	PCI_AD[26]	P6
PAR1_PADVREFB	F18	PCI_AD[27]	U11
PAR2_PADVREFA	F34	PCI_AD[28]	L2
PAR2_PADVREFB	F31	PCI_AD[29]	J1
PAS0_VCCA	AE15	PCI_AD[30]	M6
PAS1_VCCA	AE24	PCI_AD[31]	M5
PAS2_VCCA	AE25	PCI_AD[32]	K11
PAS3_VCCA	R25	PCI_AD[33]	H9
PCI_ACK64_L	J14	PCI_AD[34]	J11
PCI_AD[0]	L9	PCI_AD[35]	H8
PCI_AD[1]	K6	PCI_AD[36]	K18
PCI_AD[2]	J12	PCI_AD[37]	M12
PCI_AD[3]	M9	PCI_AD[38]	H6
PCI_AD[4]	N9	PCI_AD[39]	J16
PCI_AD[5]	K5	PCI_AD[40]	J10
PCI_AD[6]	P10	PCI_AD[41]	J18
PCI_AD[7]	M8	PCI_AD[42]	H5
PCI_AD[8]	J4	PCI_AD[43]	L17
PCI_AD[9]	H3	PCI_AD[44]	J9
PCI_AD[10]	J3	PCI_AD[45]	K10
PCI_AD[11]	K13	PCI_AD[46]	M11
PCI_AD[12]	R11	PCI_AD[47]	H15
PCI_AD[13]	K4	PCI_AD[48]	J8
PCI_AD[14]	M14	PCI_AD[49]	K16
PCI_AD[15]	H2	PCI_AD[50]	L18
PCI_AD[16]	M7	PCI_AD[51]	K14
PCI_AD[17]	L4	PCI_AD[52]	N12

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 3 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
PCI_AD[53]	H11	PCI_RST_L	T8
PCI_AD[54]	K9	PCI_SERR_L	P8
PCI_AD[55]	J7	PCI_STOP_L	L15
PCI_AD[56]	J6	PCI_TRDY_L	L7
PCI_AD[57]	K15	PCI_ZQ1	N8
PCI_AD[58]	N11	PCI_ZQ2	R12
PCI_AD[59]	H12	QDR0_A_H[0]	AL18
PCI_AD[60]	L10	QDR0_A_H[1]	AT8
PCI_AD[61]	J5	QDR0_A_H[2]	AT10
PCI_AD[62]	M10	QDR0_A_H[3]	AG19
PCI_AD[63]	L16	QDR0_A_H[4]	AU13
PCI_CBE_L[0]	L13	QDR0_A_H[5]	AT12
PCI_CBE_L[1]	R10	QDR0_A_H[6]	AR16
PCI_CBE_L[2]	T12	QDR0_A_H[7]	AM18
PCI_CBE_L[3]	N4	QDR0_A_H[8]	AN17
PCI_CBE_L[4]	J15	QDR0_A_H[9]	AH18
PCI_CBE_L[5]	N10	QDR0_A_H[10]	AR18
PCI_CBE_L[6]	M15	QDR0_A_H[11]	AG18
PCI_CBE_L[7]	K7	QDR0_A_H[12]	AF18
PCI_CLK	T9	QDR0_A_H[13]	AU17
PCI_DEVSEL_L	N5	QDR0_A_H[14]	AJ17
PCI_FRAME_L	R8	QDR0_A_H[15]	AU15
PCI_GNT_L[0]	K1	QDR0_A_H[16]	AT16
PCI_GNT_L[1]	L1	QDR0_A_H[17]	AN14
PCI_IDSEL	M3	QDR0_A_H[18]	AN13
PCI_INTA_L	M2	QDR0_A_H[19]	AK18
PCI_INTB_L	R7	QDR0_A_H[20]	AL17
PCI_IRDY_L	P7	QDR0_A_H[21]	AR15
PCI_M66EN	L12	QDR0_A_H[22]	AK17
PCI_PAR	J2	QDR0_A_H[23]	AK16
PCI_PAR64	K8	QDR0_BWS_L[0]	AR14
PCI_PERR_L	T11	QDR0_BWS_L[1]	AN16
PCI_REQ_L[0]	U10	QDR0_C_H[0]	AR13
PCI_REQ_L[1]	N6	QDR0_C_H[1]	AU11
PCI_REQ64_L	P12	QDR0_C_L[0]	AR12

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 4 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
QDR0_C_L[1]	AU9	QDR0_Q_H[8]	AG14
QDR0_CIN_H[0]	AN9	QDR0_Q_H[9]	AH14
QDR0_CIN_H[1]	AN8	QDR0_Q_H[10]	AK10
QDR0_CIN_L[0]	AR9	QDR0_Q_H[11]	AL8
QDR0_CIN_L[1]	AR8	QDR0_Q_H[12]	AL9
QDR0_D_H[0]	AL11	QDR0_Q_H[13]	AM8
QDR0_D_H[1]	AU5	QDR0_Q_H[14]	AR7
QDR0_D_H[2]	AK11	QDR0_Q_H[15]	AR6
QDR0_D_H[3]	AU7	QDR0_Q_H[16]	AT4
QDR0_D_H[4]	AR10	QDR0_Q_H[17]	AP7
QDR0_D_H[5]	AN12	QDR0_RPS_L[0]	AK15
QDR0_D_H[6]	AG16	QDR0_RPS_L[1]	AL15
QDR0_D_H[7]	AM14	QDR0_WPS_L[0]	AN15
QDR0_D_H[8]	AG15	QDR0_WPS_L[1]	AN18
QDR0_D_H[9]	AK14	QDR0_ZQ[0]	AK13
QDR0_D_H[10]	AJ13	QDR0_ZQ[1]	AM12
QDR0_D_H[11]	AL13	QDR1_A_H[0]	AN23
QDR0_D_H[12]	AK12	QDR1_A_H[1]	AF21
QDR0_D_H[13]	AR11	QDR1_A_H[2]	AT18
QDR0_D_H[14]	AN11	QDR1_A_H[3]	AJ20
QDR0_D_H[15]	AN10	QDR1_A_H[4]	AG20
QDR0_D_H[16]	AT6	QDR1_A_H[5]	AF22
QDR0_D_H[17]	AM10	QDR1_A_H[6]	AR20
QDR0_K_H[0]	AF19	QDR1_A_H[7]	AR25
QDR0_K_H[1]	AR17	QDR1_A_H[8]	AU23
QDR0_K_L[0]	AH19	QDR1_A_H[9]	AM21
QDR0_K_L[1]	AT14	QDR1_A_H[10]	AR24
QDR0_Q_H[0]	AM6	QDR1_A_H[11]	AL20
QDR0_Q_H[1]	AN6	QDR1_A_H[12]	AK20
QDR0_Q_H[2]	AT3	QDR1_A_H[13]	AR22
QDR0_Q_H[3]	AR5	QDR1_A_H[14]	AN24
QDR0_Q_H[4]	AN7	QDR1_A_H[15]	AR21
QDR0_Q_H[5]	AM7	QDR1_A_H[16]	AU21
QDR0_Q_H[6]	AJ11	QDR1_A_H[17]	AH21
QDR0_Q_H[7]	AH12	QDR1_A_H[18]	AT20

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 5 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
QDR1_A_H[19]	AN19	QDR1_K_L[0]	AR19
QDR1_A_H[20]	AM19	QDR1_K_L[1]	AT22
QDR1_A_H[21]	AK21	QDR1_Q_H[0]	AF24
QDR1_A_H[22]	AK19	QDR1_Q_H[1]	AG25
QDR1_A_H[23]	AF23	QDR1_Q_H[2]	AG24
QDR1_BWS_L[0]	AG21	QDR1_Q_H[3]	AJ26
QDR1_BWS_L[1]	AN22	QDR1_Q_H[4]	AL28
QDR1_C_H[0]	AT24	QDR1_Q_H[5]	AT30
QDR1_C_H[1]	AU25	QDR1_Q_H[6]	AR31
QDR1_C_L[0]	AT26	QDR1_Q_H[7]	AK28
QDR1_C_L[1]	AU27	QDR1_Q_H[8]	AJ28
QDR1_CIN_H[0]	AN28	QDR1_Q_H[9]	AN30
QDR1_CIN_H[1]	AN29	QDR1_Q_H[10]	AR32
QDR1_CIN_L[0]	AR28	QDR1_Q_H[11]	AR30
QDR1_CIN_L[1]	AR29	QDR1_Q_H[12]	AU31
QDR1_D_H[0]	AH23	QDR1_Q_H[13]	AM29
QDR1_D_H[1]	AK23	QDR1_Q_H[14]	AK27
QDR1_D_H[2]	AG23	QDR1_Q_H[15]	AH27
QDR1_D_H[3]	AM25	QDR1_Q_H[16]	AG26
QDR1_D_H[4]	AR27	QDR1_Q_H[17]	AH25
QDR1_D_H[5]	AN26	QDR1_RPS_L[0]	AK22
QDR1_D_H[6]	AJ24	QDR1_RPS_L[1]	AL22
QDR1_D_H[7]	AM27	QDR1_WPS_L[0]	AN21
QDR1_D_H[8]	AK26	QDR1_WPS_L[1]	AN20
QDR1_D_H[9]	AL26	QDR1_ZQ[0]	AM23
QDR1_D_H[10]	AK25	QDR1_ZQ[1]	AL24
QDR1_D_H[11]	AN27	QDR2_A_H[0]	AF31
QDR1_D_H[12]	AU29	QDR2_A_H[1]	AG33
QDR1_D_H[13]	AT28	QDR2_A_H[2]	AH33
QDR1_D_H[14]	AR26	QDR2_A_H[3]	AC28
QDR1_D_H[15]	AN25	QDR2_A_H[4]	AK36
QDR1_D_H[16]	AK24	QDR2_A_H[5]	AM36
QDR1_D_H[17]	AJ22	QDR2_A_H[6]	AG35
QDR1_K_H[0]	AP19	QDR2_A_H[7]	AE32
QDR1_K_H[1]	AR23	QDR2_A_H[8]	AD35

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 6 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
QDR2_A_H[9]	AB30	QDR2_D_H[10]	AF29
QDR2_A_H[10]	AC35	QDR2_D_H[11]	AH31
QDR2_A_H[11]	AB29	QDR2_D_H[12]	AJ33
QDR2_A_H[12]	AA28	QDR2_D_H[13]	AJ32
QDR2_A_H[13]	AD36	QDR2_D_H[14]	AL35
QDR2_A_H[14]	AB31	QDR2_D_H[15]	AN37
QDR2_A_H[15]	AF35	QDR2_D_H[16]	AL32
QDR2_A_H[16]	AE35	QDR2_D_H[17]	AR37
QDR2_A_H[17]	AH36	QDR2_K_H[0]	AF36
QDR2_A_H[18]	AB27	QDR2_K_H[1]	AG37
QDR2_A_H[19]	AA27	QDR2_K_L[0]	AC37
QDR2_A_H[20]	AC33	QDR2_K_L[1]	AE37
QDR2_A_H[21]	AC30	QDR2_Q_H[0]	AR33
QDR2_A_H[22]	AC32	QDR2_Q_H[1]	AR34
QDR2_A_H[23]	AE30	QDR2_Q_H[2]	AU35
QDR2_BWS_L[0]	AD31	QDR2_Q_H[3]	AR35
QDR2_BWS_L[1]	AF33	QDR2_Q_H[4]	AN32
QDR2_C_H[0]	AH35	QDR2_Q_H[5]	AL31
QDR2_C_H[1]	AJ37	QDR2_Q_H[6]	AH29
QDR2_C_L[0]	AJ35	QDR2_Q_H[7]	AG27
QDR2_C_L[1]	AL37	QDR2_Q_H[8]	AF27
QDR2_CIN_H[0]	AM33	QDR2_Q_H[9]	AG28
QDR2_CIN_H[1]	AN33	QDR2_Q_H[10]	AK29
QDR2_CIN_L[0]	AM35	QDR2_Q_H[11]	AK30
QDR2_CIN_L[1]	AN35	QDR2_Q_H[12]	AL30
QDR2_D_H[0]	AL33	QDR2_Q_H[13]	AM31
QDR2_D_H[1]	AP36	QDR2_Q_H[14]	AP35
QDR2_D_H[2]	AK31	QDR2_Q_H[15]	AN31
QDR2_D_H[3]	AK33	QDR2_Q_H[16]	AT36
QDR2_D_H[4]	AK35	QDR2_Q_H[17]	AT34
QDR2_D_H[5]	AJ30	QDR2_RPS_L[0]	AD30
QDR2_D_H[6]	AE27	QDR2_RPS_L[1]	AD29
QDR2_D_H[7]	AH30	QDR2_WPS_L[0]	AE33
QDR2_D_H[8]	AE28	QDR2_WPS_L[1]	AD33
QDR2_D_H[9]	AG30	QDR2_ZQ[0]	AG32

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 7 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
QDR2_ZQ[1]	AF30	QDR3_D_H[0]	U27
QDR3_A_H[0]	U36	QDR3_D_H[1]	T29
QDR3_A_H[1]	AB36	QDR3_D_H[2]	U26
QDR3_A_H[2]	AB34	QDR3_D_H[3]	P31
QDR3_A_H[3]	V29	QDR3_D_H[4]	R33
QDR3_A_H[4]	AA33	QDR3_D_H[5]	P33
QDR3_A_H[5]	AA32	QDR3_D_H[6]	P30
QDR3_A_H[6]	W35	QDR3_D_H[7]	N33
QDR3_A_H[7]	AA30	QDR3_D_H[8]	N32
QDR3_A_H[8]	W28	QDR3_D_H[9]	K37
QDR3_A_H[9]	V31	QDR3_D_H[10]	L36
QDR3_A_H[10]	V35	QDR3_D_H[11]	M37
QDR3_A_H[11]	V30	QDR3_D_H[12]	P35
QDR3_A_H[12]	Y29	QDR3_D_H[13]	R35
QDR3_A_H[13]	W27	QDR3_D_H[14]	R32
QDR3_A_H[14]	T31	QDR3_D_H[15]	R30
QDR3_A_H[15]	AA35	QDR3_D_H[16]	T30
QDR3_A_H[16]	Y30	QDR3_D_H[17]	U28
QDR3_A_H[17]	Y35	QDR3_K_H[0]	W36
QDR3_A_H[18]	Y27	QDR3_K_H[1]	U37
QDR3_A_H[19]	V27	QDR3_K_L[0]	AA37
QDR3_A_H[20]	P37	QDR3_K_L[1]	AA36
QDR3_A_H[21]	T37	QDR3_Q_H[0]	T27
QDR3_A_H[22]	R36	QDR3_Q_H[1]	R27
QDR3_A_H[23]	N36	QDR3_Q_H[2]	R28
QDR3_BWS_L[0]	W32	QDR3_Q_H[3]	M30
QDR3_BWS_L[1]	V33	QDR3_Q_H[4]	K35
QDR3_C_H[0]	U35	QDR3_Q_H[5]	J35
QDR3_C_H[1]	U33	QDR3_Q_H[6]	J32
QDR3_C_L[0]	T35	QDR3_Q_H[7]	K31
QDR3_C_L[1]	T33	QDR3_Q_H[8]	L30
QDR3_CIN_H[0]	M33	QDR3_Q_H[9]	H32
QDR3_CIN_H[1]	L33	QDR3_Q_H[10]	H33
QDR3_CIN_L[0]	N35	QDR3_Q_H[11]	J33
QDR3_CIN_L[1]	M35	QDR3_Q_H[12]	K33

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 8 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
QDR3_Q_H[13]	J36	RDR0_RQ[0]	A5
QDR3_Q_H[14]	L32	RDR0_RQ[1]	E6
QDR3_Q_H[15]	M31	RDR0_RQ[2]	C6
QDR3_Q_H[16]	N30	RDR0_RQ[3]	A6
QDR3_Q_H[17]	P29	RDR0_RQ[4]	E7
QDR3_RPS_L[0]	Y31	RDR0_RQ[5]	C7
QDR3_RPS_L[1]	W30	RDR0_RQ[6]	A7
QDR3_WPS_L[0]	W33	RDR0_RQ[7]	E8
QDR3_WPS_L[1]	Y33	RDR0_SCK	F1
QDR3_ZQ[0]	U30	RDR0_SCLKN	F2
QDR3_ZQ[1]	U32	RDR0_SIO	D1
RDR0_CFM	C9	RDR1_CFM	C22
RDR0_CFMN	C8	RDR1_CFMN	C21
RDR0_CMD	B1	RDR1_CMD	A13
RDR0_CTM	A9	RDR1_CTM	A22
RDR0_CTMN	A8	RDR1_CTMN	A21
RDR0_DQA[0]	E10	RDR1_DQA[0]	A23
RDR0_DQA[1]	C10	RDR1_DQA[1]	C23
RDR0_DQA[2]	A10	RDR1_DQA[2]	A24
RDR0_DQA[3]	E11	RDR1_DQA[3]	E23
RDR0_DQA[4]	C11	RDR1_DQA[4]	C24
RDR0_DQA[5]	A11	RDR1_DQA[5]	E24
RDR0_DQA[6]	A12	RDR1_DQA[6]	A25
RDR0_DQA[7]	C12	RDR1_DQA[7]	E25
RDR0_DQA[8]	E12	RDR1_DQA[8]	C25
RDR0_DQB[0]	E5	RDR1_DQB[0]	E17
RDR0_DQB[1]	C5	RDR1_DQB[1]	C17
RDR0_DQB[2]	A4	RDR1_DQB[2]	C16
RDR0_DQB[3]	C4	RDR1_DQB[3]	E16
RDR0_DQB[4]	E4	RDR1_DQB[4]	A16
RDR0_DQB[5]	A3	RDR1_DQB[5]	C15
RDR0_DQB[6]	C3	RDR1_DQB[6]	E15
RDR0_DQB[7]	E3	RDR1_DQB[7]	A15
RDR0_DQB[8]	A2	RDR1_DQB[8]	A14
RDR0_PCLKM	D2	RDR1_PCLKM	D14

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 9 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
RDR1_RQ[0]	A17	RDR2_RQ[0]	A30
RDR1_RQ[1]	B18	RDR2_RQ[1]	A31
RDR1_RQ[2]	D18	RDR2_RQ[2]	C31
RDR1_RQ[3]	C19	RDR2_RQ[3]	E31
RDR1_RQ[4]	E19	RDR2_RQ[4]	A32
RDR1_RQ[5]	B20	RDR2_RQ[5]	C32
RDR1_RQ[6]	E21	RDR2_RQ[6]	E32
RDR1_RQ[7]	D20	RDR2_RQ[7]	E33
RDR1_SCK	D13	RDR2_SCK	C26
RDR1_SCLKN	B13	RDR2_SCLKN	D26
RDR1_SIO	F14	RDR2_SIO	A26
RDR2_CFM	C34	SP_ACK_L	J25
RDR2_CFMN	C33	SP_AD[0]	H19
RDR2_CMD	E26	SP_AD[1]	H25
RDR2_CTM	A34	SP_AD[2]	K27
RDR2_CTMN	A33	SP_AD[3]	L27
RDR2_DQA[0]	A35	SP_AD[4]	K20
RDR2_DQA[1]	C35	SP_AD[5]	H28
RDR2_DQA[2]	E35	SP_AD[6]	J28
RDR2_DQA[3]	A36	SP_AD[7]	J24
RDR2_DQA[4]	C36	SP_ALE_L	L25
RDR2_DQA[5]	E36	SP_CLK	M26
RDR2_DQA[6]	D37	SP_CP	M23
RDR2_DQA[7]	F37	SP_CS_L[0]	M24
RDR2_DQA[8]	B37	SP_CS_L[1]	J20
RDR2_DQB[0]	E29	SP_DIR	K28
RDR2_DQB[1]	C30	SP_OE_L	M27
RDR2_DQB[2]	E30	SP_RD_L	H24
RDR2_DQB[3]	C29	SP_WR_L	L26
RDR2_DQB[4]	A29	SPI4_PREEMP	T7
RDR2_DQB[5]	E28	SPI4_RCLK	AC6
RDR2_DQB[6]	C28	SPI4_RCLK_L	AC5
RDR2_DQB[7]	A28	SPI4_RCLK_REF	Y11
RDR2_DQB[8]	A27	SPI4_RCLK_REF_L	Y12
RDR2_PCLKM	D27	SPI4_RCTL	AD6

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 10 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
SPI4_RCTL_L	AD5	SPI4_RPROT	AB12
SPI4_RDAT[0]	AH2	SPI4_RPROT_L	AB11
SPI4_RDAT[1]	AG4	SPI4_RSCLK	N2
SPI4_RDAT[2]	AE4	SPI4_RSTAT[0]	N1
SPI4_RDAT[3]	AF6	SPI4_RSTAT[1]	N3
SPI4_RDAT[4]	AG2	SPI4_TCLK	T3
SPI4_RDAT[5]	AF2	SPI4_TCLK_L	T4
SPI4_RDAT[6]	AE8	SPI4_TCLK_REF	AD8
SPI4_RDAT[7]	AD2	SPI4_TCLK_REF_L	AD7
SPI4_RDAT[8]	AF8	SPI4_TCTL	AA3
SPI4_RDAT[9]	AG6	SPI4_TCTL_L	AA4
SPI4_RDAT[10]	AF4	SPI4_TDAT[0]	AA7
SPI4_RDAT[11]	AB6	SPI4_TDAT[1]	U4
SPI4_RDAT[12]	AD10	SPI4_TDAT[2]	T5
SPI4_RDAT[13]	AB8	SPI4_TDAT[3]	R1
SPI4_RDAT[14]	AD4	SPI4_TDAT[4]	Y7
SPI4_RDAT[15]	AC2	SPI4_TDAT[5]	V6
SPI4_RDAT_L[0]	AH1	SPI4_TDAT[6]	V2
SPI4_RDAT_L[1]	AG3	SPI4_TDAT[7]	V8
SPI4_RDAT_L[2]	AE3	SPI4_TDAT[8]	Y3
SPI4_RDAT_L[3]	AF5	SPI4_TDAT[9]	W11
SPI4_RDAT_L[4]	AG1	SPI4_TDAT[10]	V4
SPI4_RDAT_L[5]	AF1	SPI4_TDAT[11]	T1
SPI4_RDAT_L[6]	AE7	SPI4_TDAT[12]	Y9
SPI4_RDAT_L[7]	AD1	SPI4_TDAT[13]	Y5
SPI4_RDAT_L[8]	AF7	SPI4_TDAT[14]	W6
SPI4_RDAT_L[9]	AG5	SPI4_TDAT[15]	W2
SPI4_RDAT_L[10]	AF3	SPI4_TDAT_L[0]	AA8
SPI4_RDAT_L[11]	AB5	SPI4_TDAT_L[1]	U5
SPI4_RDAT_L[12]	AD9	SPI4_TDAT_L[2]	T6
SPI4_RDAT_L[13]	AB7	SPI4_TDAT_L[3]	R2
SPI4_RDAT_L[14]	AD3	SPI4_TDAT_L[4]	Y8
SPI4_RDAT_L[15]	AC1	SPI4_TDAT_L[5]	V7
SPI4_RPAR	AB10	SPI4_TDAT_L[6]	V3
SPI4_RPAR_L	AB9	SPI4_TDAT_L[7]	V9

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 11 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
SPI4_TDAT_L[8]	Y4	VCC	AB18
SPI4_TDAT_L[9]	W12	VCC	AB20
SPI4_TDAT_L[10]	V5	VCC	AC21
SPI4_TDAT_L[11]	T2	VCC	AC23
SPI4_TDAT_L[12]	Y10	VCC	AC25
SPI4_TDAT_L[13]	Y6	VCC	AD16
SPI4_TDAT_L[14]	W7	VCC	AD18
SPI4_TDAT_L[15]	W3	VCC	AD20
SPI4_TPAR	AB3	VCC	AD22
SPI4_TPAR_L	AB4	VCC	AD24
SPI4_TPROT	AA1	VCC	AE17
SPI4_TPROT_L	AA2	VCC	AE19
SPI4_TSCLK	P4	VCC	AE21
SPI4_TSTAT[0]	P5	VCC	AE23
SPI4_TSTAT[1]	P3	VCC	N13
SPI4_ZQ1	AC9	VCC	N15
SPI4_ZQ2	AC10	VCC	N17
SR_RX	H22	VCC	N19
SR_TX	K26	VCC	N21
TEST_SCAN_MODE	M21	VCC	N23
TEST_DIODE_A	J29	VCC	P14
TEST_DIODE_C	K29	VCC	P16
INTERRUPT_MODE	M22	VCC	P18
TEST_SCAN_CLK_A	L28	VCC	P20
TEST_SCAN_CLK_B	M28	VCC	P22
TEST_SCAN_EN	H20	VCC	P24
VCC	AA13	VCC	R13
VCC	AA15	VCC	R15
VCC	AA17	VCC	R17
VCC	AA19	VCC	R19
VCC	AA21	VCC	R21
VCC	AA23	VCC	R23
VCC	AA25	VCC	T14
VCC	AB14	VCC	T16
VCC	AB16	VCC	T18

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 12 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VCC	AB22	VCC_FUSE	AD13
VCC	AB24	VCC_FUSE	AD14
VCC	AC15	VCC_FUSE	AE13
VCC	AC17	VCC_FUSE	AE14
VCC	AC19	VCC_PLL	P25
VCC	U17	VCC25V	AE2
VCC	U19	VCC25V	AE6
VCC	U21	VCC25V	AG8
VCC	U23	VCC25V	AH4
VCC	U25	VCC25V	AH6
VCC	V14	VCC25V	AJ2
VCC	V16	VCC25V	AL4
VCC	V18	VCC25V	AN1
VCC	V20	VCC25V	AN5
VCC	V22	VCC25V	J13
VCC	V24	VCC25V	J17
VCC	W13	VCC25V	M13
VCC	W15	VCC25V	M18
VCC	W17	VCC25V	P1
VCC	W19	VCC25V	U1
VCC	W21	VCC25V	U3
VCC	W23	VCC25V	U7
VCC	W25	VCC25V	V11
VCC	Y14	VCC25V	W5
VCC	Y16	VCC25V	W9
VCC	Y18	VCC25V	AA10
VCC	Y20	VCC25V	AA11
VCC	Y22	VCC25V	AA6
VCC	Y24	VCC25V	AB2
VCC	T20	VCC25V	AC4
VCC	T22	VCC25V	AC8
VCC	T24	VCC25V	AD11
VCC	U13	VCC25V	AE10
VCC	U15	VCC33	H26
VCC_CLK	J19	VCC33	L22

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 13 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VCC33	L29	VCCRA	G9
VCC33	R26	VCCRIO	G1
VCC33_PCI	H1	VCCRIO	G11
VCC33_PCI	H13	VCCRIO	G15
VCC33_PCI	H16	VCCRIO	G17
VCC33_PCI	H7	VCCRIO	G24
VCC33_PCI	L14	VCCRIO	G26
VCC33_PCI	L3	VCCRIO	G28
VCC33_PCI	L8	VCCRIO	G3
VCC33_PCI	M17	VCCRIO	G36
VCC33_PCI	P11	VDDQ	AE31
VCC33_PCI	R4	VDDQ	AE34
VCC33_PCI	R5	VDDQ	AE36
VCC33_PCI	U8	VDDQ	AF15
VCCA_FC	AC13	VDDQ	AF26
VCCA_SPI4	AB13	VDDQ	AF28
VCCR	G10	VDDQ	AG31
VCCR	G12	VDDQ	AG34
VCCR	G20	VDDQ	AG36
VCCR	G21	VDDQ	AH11
VCCR	G23	VDDQ	AH13
VCCR	G25	VDDQ	AH15
VCCR	G29	VDDQ	AH17
VCCR	G32	VDDQ	AH20
VCCR	G33	VDDQ	AH22
VCCR	G35	VDDQ	AH24
VCCR	G37	VDDQ	AH26
VCCR	G4	VDDQ	AH28
VCCR	G7	VDDQ	AJ31
VCCR	G8	VDDQ	AJ34
VCCRA	G19	VDDQ	AJ36
VCCRA	G22	VDDQ	AK8
VCCRA	G30	VDDQ	AL10
VCCRA	G34	VDDQ	AL12
VCCRA	G5	VDDQ	AL14

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 14 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VDDQ	AL16	VDDQ	AL21
VDDQ	AL19	VDDQ	AL23
VDDQ	AA26	VDDQ	AL25
VDDQ	AA31	VDDQ	AL27
VDDQ	AB28	VDDQ	AL29
VDDQ	AB33	VDDQ	AL34
VDDQ	AB35	VDDQ	AL36
VDDQ	AC31	VDDQ	AN34
VDDQ	AC34	VDDQ	AN36
VDDQ	AC36	VDDQ	AP11
VDDQ	AD28	VDDQ	AP13
VDDQ	AP15	VDDQ	AT29
VDDQ	AP17	VDDQ	AT31
VDDQ	AP21	VDDQ	AT33
VDDQ	AP23	VDDQ	AT35
VDDQ	AP25	VDDQ	AT5
VDDQ	AP27	VDDQ	AT7
VDDQ	AP29	VDDQ	AT9
VDDQ	AP31	VDDQ	H34
VDDQ	AP33	VDDQ	M36
VDDQ	AP5	VDDQ	N31
VDDQ	AP9	VDDQ	P28
VDDQ	AR2	VDDQ	P34
VDDQ	AR36	VDDQ	P36
VDDQ	AR4	VDDQ	R31
VDDQ	AT1	VDDQ	T28
VDDQ	AT11	VDDQ	T34
VDDQ	AT13	VDDQ	T36
VDDQ	AT15	VDDQ	U31
VDDQ	AT17	VDDQ	V28
VDDQ	AT19	VDDQ	V34
VDDQ	AT21	VDDQ	W31
VDDQ	AT23	VDDQ	Y28
VDDQ	AT25	VDDQ	Y34
VDDQ	AT27	VDDQ	Y36

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 15 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VDDQ	H35	VSS	B30
VDDQ	J31	VSS	B31
VDDQ	K34	VSS	B32
VDDQ	K36	VSS	B33
VDDQ	L31	VSS	B34
VDDQ	M34	VSS	B35
VREFHI	AC11	VSS	B2
VREFHI	AL5	VSS	B5
VREFHI_CLK	H29	VSS	B6
VREFLO	AC12	VSS	B7
VREFLO	AL6	VSS	B8
VREFLO_CLK	H30	VSS	B9
VREF_QDR0	AT2	VSS	B10
VREF_QDR0	AU3	VSS	B11
VREF_QDR1	AT32	VSS	AB17
VREF_QDR1	AU33	VSS	AB19
VREF_QDR2	AT37	VSS	AB21
VREF_QDR2	AU36	VSS	AB23
VREF_QDR3	H36	VSS	AB25
VREF_QDR3	H37	VSS	AB26
VSS	B12	VSS	AB32
VSS	B14	VSS	AB37
VSS	B15	VSS	AC14
VSS	B16	VSS	AC16
VSS	B17	VSS	AC18
VSS	B19	VSS	AC20
VSS	B21	VSS	AC22
VSS	B22	VSS	AC24
VSS	B23	VSS	AC26
VSS	B24	VSS	AC27
VSS	B25	VSS	AC29
VSS	B26	VSS	AC3
VSS	B27	VSS	AC7
VSS	B28	VSS	AD12
VSS	B29	VSS	AD15

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 16 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VSS	B36	VSS	AD17
VSS	B3	VSS	AD19
VSS	B4	VSS	AD21
VSS	A37	VSS	AD23
VSS	AA12	VSS	AD25
VSS	AA14	VSS	AD26
VSS	AA16	VSS	AD27
VSS	AA18	VSS	AD32
VSS	AA20	VSS	AD34
VSS	AA22	VSS	AD37
VSS	AA24	VSS	AE1
VSS	AA29	VSS	AE16
VSS	AA34	VSS	AE18
VSS	AA5	VSS	AE20
VSS	AA9	VSS	AE22
VSS	AB1	VSS	AE26
VSS	AB15	VSS	AE29
VSS	AE5	VSS	AK34
VSS	AE9	VSS	AK37
VSS	AF13	VSS	AK9
VSS	AF14	VSS	AL3
VSS	AF16	VSS	AM11
VSS	AF17	VSS	AM13
VSS	AF20	VSS	AM15
VSS	AF25	VSS	AM16
VSS	AF32	VSS	AM17
VSS	AF34	VSS	AM20
VSS	AF37	VSS	AM22
VSS	AG12	VSS	AM24
VSS	AG13	VSS	AM26
VSS	AG17	VSS	AM28
VSS	AG22	VSS	AM30
VSS	AG29	VSS	AM32
VSS	AG7	VSS	AM34
VSS	AH10	VSS	AM37

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 17 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VSS	AH16	VSS	AM5
VSS	AH3	VSS	AM9
VSS	AH32	VSS	AN2
VSS	AH34	VSS	AP10
VSS	AH37	VSS	AP12
VSS	AH5	VSS	AP14
VSS	AJ1	VSS	AP16
VSS	AJ10	VSS	AP18
VSS	AJ12	VSS	AP20
VSS	AJ14	VSS	AP22
VSS	AJ15	VSS	AP24
VSS	AJ16	VSS	AP26
VSS	AJ18	VSS	AP28
VSS	AJ19	VSS	AP30
VSS	AJ21	VSS	AP32
VSS	AJ23	VSS	AP34
VSS	AJ25	VSS	AP37
VSS	AJ27	VSS	AP6
VSS	AJ29	VSS	AP8
VSS	AK32	VSS	AR1
VSS	AR3	VSS	D28
VSS	AU1	VSS	D29
VSS	AU10	VSS	D3
VSS	AU12	VSS	D30
VSS	AU14	VSS	D31
VSS	AU16	VSS	D32
VSS	AU2	VSS	D33
VSS	AU22	VSS	D34
VSS	AU24	VSS	D35
VSS	AU26	VSS	D36
VSS	AU28	VSS	D4
VSS	AU30	VSS	D5
VSS	AU32	VSS	D6
VSS	AU34	VSS	D7
VSS	AU37	VSS	D8

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 18 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VSS	AU4	VSS	D9
VSS	AU6	VSS	E1
VSS	AU8	VSS	E13
VSS	C1	VSS	E14
VSS	C13	VSS	E18
VSS	C14	VSS	E2
VSS	C18	VSS	E20
VSS	C2	VSS	E22
VSS	C20	VSS	E27
VSS	C27	VSS	E34
VSS	C37	VSS	E37
VSS	D10	VSS	E9
VSS	D11	VSS	F10
VSS	D12	VSS	F11
VSS	D15	VSS	F12
VSS	D16	VSS	F13
VSS	D17	VSS	F15
VSS	D19	VSS	F16
VSS	D21	VSS	F17
VSS	D22	VSS	F19
VSS	D23	VSS	F21
VSS	D24	VSS	F22
VSS	D25	VSS	F23
VSS	F24	VSS	K32
VSS	F25	VSS	L11
VSS	F26	VSS	L19
VSS	F27	VSS	L23
VSS	F28	VSS	L34
VSS	F29	VSS	L35
VSS	F3	VSS	L37
VSS	F30	VSS	L5
VSS	F32	VSS	M1
VSS	F33	VSS	M16
VSS	F35	VSS	M19
VSS	F36	VSS	M32

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 19 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VSS	F4	VSS	N14
VSS	F5	VSS	N16
VSS	F7	VSS	N18
VSS	F8	VSS	N20
VSS	G13	VSS	N22
VSS	G14	VSS	N24
VSS	G16	VSS	N29
VSS	G18	VSS	N34
VSS	G2	VSS	N37
VSS	G27	VSS	P13
VSS	G31	VSS	P15
VSS	G6	VSS	P17
VSS	H10	VSS	P19
VSS	H14	VSS	P2
VSS	H17	VSS	P21
VSS	H18	VSS	P23
VSS	H23	VSS	P27
VSS	H31	VSS	P32
VSS	H4	VSS	P9
VSS	J30	VSS	R14
VSS	J34	VSS	R16
VSS	J37	VSS	R18
VSS	K17	VSS	R20
VSS	K19	VSS	R22
VSS	K2	VSS	R24
VSS	K30	VSS	R29
VSS	R3	VSS	V21
VSS	R34	VSS	V23
VSS	R37	VSS	V25
VSS	R6	VSS	V26
VSS	T13	VSS	V32
VSS	T15	VSS	V36
VSS	T17	VSS	W10
VSS	T19	VSS	W14
VSS	T21	VSS	W16

Table 19. IXP2800/IXP2850 Network Processor Alphabetical Pin List (Sheet 20 of 20)

Pin Name	FCBGA Location	Pin Name	FCBGA Location
VSS	T23	VSS	W18
VSS	T25	VSS	W20
VSS	T26	VSS	W22
VSS	T32	VSS	W24
VSS	U14	VSS	W26
VSS	U16	VSS	W29
VSS	U18	VSS	W34
VSS	U2	VSS	W4
VSS	U20	VSS	W8
VSS	U22	VSS	Y13
VSS	U24	VSS	Y15
VSS	U29	VSS	Y17
VSS	U34	VSS	Y19
VSS	U6	VSS	Y2
VSS	U9	VSS	Y21
VSS	V10	VSS	Y23
VSS	V12	VSS	Y25
VSS	V13	VSS	Y26
VSS	V15	VSS	Y32
VSS	V17	VSS	N25
VSS	V19		

3.3 Pullup/Pulldown and Unused Pin Guidelines

All unused inputs should be tied to their inactive state. Typical pullup/pulldown resistor values are in the range of 1 – 5K ohms.

The following unused or floating LVDS input pins should be terminated to VCC25, using a 400-ohm pullup resistor and to VSS, using a 330-ohm pulldown resistor.

- SPI4_RPROT_H
- SPI4_RPROT_L
- SPI4_RCTL_H
- SPI4_RCTL_L
- SPI4_RPAR_H
- SPI4_RPAR_L
- FC_RXCPAR_H
- FC_RXCPAR_L
- FC_RXCSOF_H
- FC_RXCSOF_L
- FC_RXCDAT_H(0)
- FC_RXCDAT_H(1)
- FC_RXCDAT_H(2)
- FC_RXCDAT_H(3)
- FC_RXCDAT_L(0)
- FC_RXCDAT_L(1)
- FC_RXCDAT_L(2)
- FC_RXCDAT_L(3)
- FC_TXCFC_H
- FC_TXCFC_L
- FC_RXCCLK_H
- FC_RXCCLK_L
- FC_RXCSRB_H
- FC_RXCSRB_L

Alternatively, these pins can be tied directly to the 1.4 V (pullup) or 1.0 V (pulldown) supplies without the need for termination resistors. In this scenario, the 1.0 V / 1.4 V supplies must be capable of suppling the extra 7 mA of power per differential pin pair required for the termination.

All of the following test signals should be tied to logical 0 when not used:

- CLK_STOP
- CLK_PLL_BYP

- TEST_SCAN_EN
- TEST_SCAN_MODE
- TEST_DIODE_A
- TEST_DIODE_C
- SPI4_PREEMP
- FC_PREEMP

All of the following test signals should be tied to logical 1 when not used:

- TEST_SCAN_CLK_A
- TEST_SCAN_CLK_B

4.0 Electrical Specifications

This chapter specifies the following electrical behavior of the network processor:

- Absolute maximum ratings
- DC values and AC timing specifications for the following:
  - PCI I/O Unit
  - QDR
  - RDRAM
  - Flow Control Bus
  - SPI-4 and CSIX
  - Slowport I/O Buffer.
  - GPIO
  - JTAG
  - Serial Port

4.1 Absolute Maximum Ratings

Operating beyond the functional operating temperature range (Table 21) is not recommended and extended exposure beyond the functional operating temperature range may affect reliability. Table 23 lists the functional operating voltage range.

Warning: Under all operating conditions, the 3.3 V – 1.35/1.3/1.2 V and 3.3 V – 2.5 V supply voltage difference (Vdelta) must *not* be exceeded; otherwise, permanent damage to the device may result. Also, the Core/PLL supply voltage must never be less than 1.1 V (refer to Table 20).

Table 20. Absolute Maximum Ratings Table

Parameter	Minimum	Maximum	Comment
Junction Temp Tj (Commercial)	—	120° C	
Junction Temp Tj (Extended)	—	120° C	
Storage Temperature Range	-55° C	125° C	
Supply Voltage Difference Vdelta	—	2.7 V	• 3.3 V to 2.5 V rail difference. • 3.3 V to 1.35/1.3/1.2 V rail difference.
Vcore (1.35/1.3 V) Minimum Operating Voltage	1.1 V	—	
Vcore (1.2 V) Minimum Operating Voltage	1.1 V	—	

Table 21. Functional Operating Temperature Range

Parameter	Minimum	Maximum	Comment
Commercial temperature operating range	0° C	70° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.
Extended temperature operating range	-40° C	85° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.
Maximum Junction Temperature (Extended)	—	120° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.
Maximum Junction Temperature (Commercial)	—	120° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.

Table 22. Typical and Maximum Power[1]

Device[2]	Typical	Maximum	Frequency
IXP2800 - B*n*[3]	25.5 W	31.5 W	1.4 GHz
IXP2800 - B*n*	18.5 W	23 W	1.0 GHz
IXP2800 - B*n*	12.5 W	16 W	650 MHz
IXP2850 - B*n*	27.5 W	34 W	1.4 GHz
IXP2850 - B*n*	20.5 W	25 W	1.0 GHz
IXP2850 - B*n*	14 W	17.5 W	650 MHz

1. The maximum power parameters represent the worst case power consumption as measured running the Intel Packet Over SONET (POS) reference design processing minimum size packets (49 bytes) running at full OC-192 line rate.
2. Total power.
3. B*n* refers to B0 and B1.

Table 23. Functional Operating Voltage Range – 1.4/1.0 GHz

Interface	Supply Name	Description	Voltage (V)	Tolerance (+/-%)	Notes 1,2,3,4,5
Core	VCC VSS	Core power supply Core ground	1.3 V GND	5% N/A	3
Clock/PLL	VCC_PLL VSS VCC_CLK	PLL power PLL ground Ref. Clock power (also for GPIO)	1.3 V GND 2.50 V	5% N/A 5%	1,3
SPI-4/CSIX/FLOW	VCC25V VCCA_FC VCCA_SPI4 VREFHI VREFLO	SPI-4 supply (also for PCI) DLL power DLL power SPI-4/flow reference voltage SPI-4/flow reference voltage	2.50 V 1.3 V 1.3 V 1.40 V 1.00 V	5% 5% 5% 5% 5%	1 1 4 4
GPIO	VCC33	GPIO, JTAG, SP power	3.30 V	5%	
PCI	VCC33_PCI	PCI power supply	3.30 V	5%	5
QDR	VDDQ PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	QRD power supply DLL power DLL power DLL power DLL power QDR reference voltage QDR reference voltage QDR reference voltage QDR reference voltage	1.50 V 1.3 V 1.3 V 1.3 V 1.3 V 0.75 V 0.75 V 0.75 V 0.75 V	1.4 V to 1.6 V 5% 5% 5% 5% 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V	 1 1 1 1 2 2 2 2
RDR	VCCR VCCRA VCCRIO PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	RDRAM core processor RDRAM clean power RDRAM I/O power RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage	1.3 V 1.3 V 1.80 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V	5% 5% 1.7 V to 1.9 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V	1
FUSE	VCC_FUSE	Fuse power supply	1.3 V	5%	

1. These supplies can be derived from core Vcc, but should be filtered appropriately.
2. QDR references should be derived from Vddq so that they track fluctuations in Vddq.
3. During power-up, after NRESET is de-asserted, the device will experience an increase in current consumption after the PLL locks and the system clocks begin to operate at full speed. During this time a droop on the core power supply may occur due to this increase in current consumption. It is acceptable that the core power supply droop a maximum of 100 mV to a minimum of 1.2 V during this time. It is expected that the device be Idle during this time and that no instructions be executing until the power is within the 5% regulation specification. The behavior is undefined if instructions are executed while the power is not within the 5% regulation specification.
4. SPI-4 reference should be derived from VCC25V so that they track fluctuations in VCC25V.
5. The tolerance on the PCI supply is tighter than specified in the *PCI Local Bus Specification, Version 2.2**.

Table 24. Functional Operating Voltage Range – 650 MHz

Interface	Supply Name	Description	Voltage (V)	Tolerance (+/-%)	Notes 1,2,3,4
Core	VCC VSS	Core power supply Core ground	1.2 V GND	5% N/A	
Clock/PLL	VCC_PLL VSS VCC_CLK	PLL power PLL ground Ref. Clock power (also for GPIO)	1.2 V GND 2.50 V	5% N/A 5%	1
SPI-4/CSIX/FLOW	VCC25V VCCA_FC VCCA_SPI4 VREFHI VREFLO	SPI-4 supply (also for PCI) DLL power DLL power SPI-4/flow reference voltage SPI-4/flow reference voltage	2.50 V 1.2 V 1.2 V 1.40 V 1.00 V	5% 5% 5% 5% 5%	1 1 3 3
GPIO	VCC33	GPIO, JTAG, SP power	3.30 V	5%	
PCI	VCC33_PCI	PCI power supply	3.30 V	5%	4
QDR	VDDQ PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	QRD power supply DLL power DLL power DLL power DLL power QDR reference voltage QDR reference voltage QDR reference voltage QDR reference voltage	1.50 V 1.2 V 1.2 V 1.2 V 1.2 V 0.75 V 0.75 V 0.75 V 0.75 V	1.4 V to 1.6 V 5% 5% 5% 5% 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V	1 1 1 1 2 2 2 2
RDR	VCCR VCCRA VCCRIO PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	RDRAM core processor RDRAM clean power RDRAM I/O power RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage	1.2 V 1.2 V 1.80 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V	5% 5% 1.7 V to 1.9 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V	1
FUSE	VCC_FUSE	Fuse power supply	1.2 V	5%	

1. These supplies can be derived from core Vcc, but should be filtered appropriately.
2. QDR references should be derived from Vddq so that they track fluctuations in Vddq.
3. SPI-4 reference should be derived from VCC25V so that they track fluctuations in VCC25V.
4. The tolerance on the PCI supply is tighter than specified in the *PCI Local Bus Specification, Version 2.2**.

Table 25. Example Power by Supply – 1.4 GHz

Type	Group	Names	IXP2800 Max Power[1]	IXP2850 Max Power[1]
Power Supplies	1.3 V logic	VCC VCCR VCCRA VCC_FUSE	25.5 W	28.0 W
	1.3 V PLL/DLL	VCC_PLL VCCA_FC VCCA_SPI4 PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA	1.0 W	1.0 W
	1.50 V	VDDQ	2.0 W	2.0 W
	1.80 V	VCCRIO	0.5 W	0.5 W
	2.5 V	VCC_CLK VCC25V	1.8 W	1.8 W
	3.3 V	VCC33 VCC33_PCI	0.7 W	0.7 W
Voltage References	0.75	VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	< 0.01 W	< 0.01 W
	1.0 V	VREFLO	< 0.01 W	< 0.01 W
	1.4 V	VREFHI PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	< 0.01 W	< 0.01 W

1. Power specified is in the total for all the supplies/references in each group.

Table 26. Example Power by Supply – 1.0 GHz

Type	Group	Names	IXP2800 Max Power[1]	IXP2850 Max Power[1]
Power Supplies	1.3 V logic	VCC VCCR VCCRA VCC_FUSE	17.0 W	19.0 W
	1.3 V PLL/DLL	VCC_PLL VCCA_FC VCCA_SPI4 PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA	1.0 W	1.0 W
	1.50 V	VDDQ	2.0 W	2.0 W
	1.80 V	VCCRIO	0.5 W	0.5 W
	2.5 V	VCC_CLK VCC25V	1.8 W	1.8 W
	3.3 V	VCC33 VCC33_PCI	0.7 W	0.7 W
Voltage References	0.75 V	VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	< 0.01 W	< 0.01 W
	1.0 V	VREFLO	< 0.01 W	< 0.01 W
	1.4 V	VREFHI PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	< 0.01 W	< 0.01 W

1. Power specified is in the total for all the supplies/references in each group.

Table 27. Example Power by Supply – 650 MHz

Type	Group	Names	IXP2800 Max Power[1]	IXP2850 Max Power[1]
Power Supplies	1.2 V logic	VCC VCCR VCCRA VCC_FUSE	10.4 W	11.8 W
	1.2 V PLL/DLL	VCC_PLL VCCA_FC VCCA_SPI4 PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA	1.0 W	1.0 W
	1.50 V	VDDQ	1.9 W	1.9 W
	1.80 V	VCCRIO	0.4 W	0.4 W
	2.5 V	VCC_CLK VCC25V	1.7 W	1.7 W
	3.3 V	VCC33 VCC33_PCI	0.7 W	0.7 W
Voltage References	0.75 V	VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	< 0.01 W	< 0.01 W
	1.0 V	VREFLO	< 0.01 W	< 0.01 W
	1.4 V	VREFHI PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	< 0.01 W	< 0.01 W

1. Power specified is in the total for all the supplies/references in each group.

4.2 Supply Voltage Power-up Sequence

Caution: The IXP2800/IXP2850 has a prescribed supply voltage bring-up sequence that must be followed or permanent damage to the device may result.

4.2.1 Sequence for 1.4 / 1.0 GHz Devices

The sequence for the 1.4 / 1.0 GHz B-stepping devices is as follows:

1. The 2.5 V supply must come up before the 1.3 V supply.
2. The 1.3 V supply must come up after the 2.5 V supply and must not start to ramp until the 2.5 V supply has reached greater than 1 V.
3. The 3.3 V supply must come up only after the 2.5 V and 1.3 V supplies are up and stable.
    a. It is acceptable to ramp the 1.3 V and 3.3 V supplies together as long as the two supplies rise linearly together and do not deviate by more than 10% of the nominal ramp rate until both supplies reach their respective final voltage levels.

It is expected that all supplies will be up and stable within the maximum power-up time requirement of 700 ms. Additionally, the maximum time from when the 2.5 V supply is up and stable to when the 1.3 V supply begins to ramp should not exceed 200 ms.

Note: The 1.8 V and 1.5 V supplies can come up in any order before or after the 2.5 V, 1.3 V, and 3.3 V supplies.

Note: No 3.3 V devices should drive any of the IXP2800/IXP2850 pins until its 3.3 V supply is up and stable.

4.2.2 Sequence for 650 MHz Devices

The sequence for the 650 MHz B-stepping devices is as follows:

1. The 2.5 V supply must come up before the 1.2 V supply.
2. The 1.2 V supply must come up after the 2.5 V supply and must not start to ramp until the 2.5 V supply has reached greater than 1 V.
3. The 3.3 V supply should begin to ramp after the 2.5 V and 1.2 V supplies are up and stable.
    a. It is acceptable to ramp the 1.2 V and 3.3 V supplies together as long as the two supplies rise linearly together and do not deviate by more than 10% of the nominal ramp rate until both supplies reach their respective final voltage levels.

It is expected that all supplies will be up and stable within the maximum power-up time requirement of 700 ms. Additionally, the maximum time from when the 2.5 V supply is up and stable to when the 1.2 V supply begins to ramp should not exceed 200 ms.

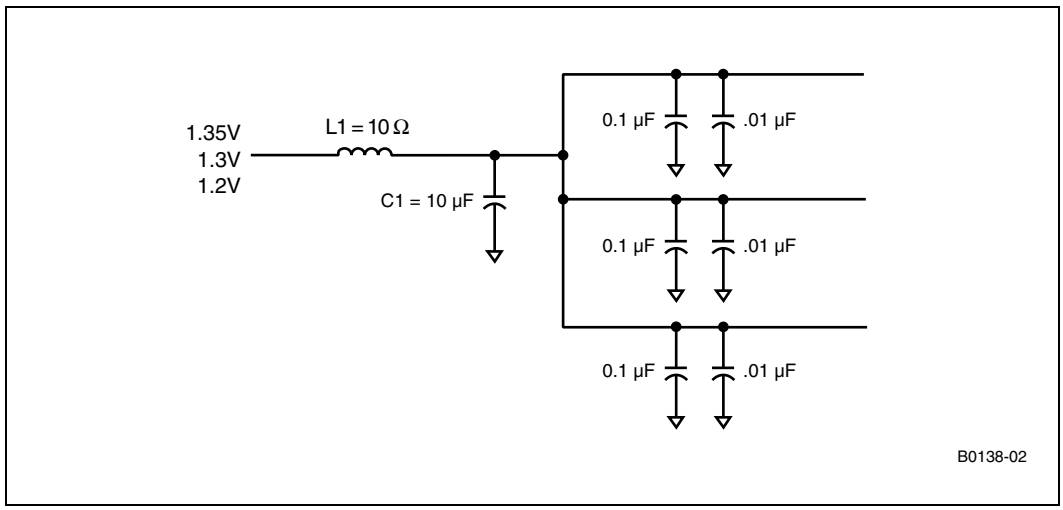
Note: The 1.8 V and 1.5 V supplies can come up in any order before or after the 2.5 V, 1.2 V, and 3.3 V supplies.

Note: No 3.3 V devices should drive any of the IXP2800/IXP2850 pins until its 3.3 V supply is up and stable.

4.3 LC Filter Network

Figure 10 shows an example of an LC filter design that can be used to derive the power for the analog and DLL power supplies for the IXP2800/IXP2850. For L1, a 10-ohm ferrite bead with a DCR of less than 0.1 ohms should be used. For C1, a 10 microfarad capacitor should be used and each analog VCC pin should be de-coupled with a 0.1 microfarad and a 0.01 microfarad capacitor.

Figure 10. LC Filter Network



4.4 AC/DC Specifications

4.4.1 Clock Timing Specifications

The IXP2800/IXP2850 has a centralized clock generator that takes an external reference frequency and multiplies it to a higher base frequency clock, using a PLL. The resulting clock frequency is then divided down by a set of programmable divisors to provide clocks to the SRAM, DRAM, and optionally, the Media and Switch Fabric (MSF) controllers. All of the DRAM controllers are clocked at the same rate, and therefore derive their clocks from a single divisor. Each SRAM controller has a divisor, enabling it to be clocked individually. The Intel XScale® core and Microengines derive their clocks from fixed-divide ratios.

The MSF derives its clock from either the internal PLL or an external source, such as a MAC device. The selection is based on a the SP_AD[6] strap pin. When the pin is high, the MSF uses an internally-generated clock using the programmable divisor. When the pin is low, the MSF uses an externally-received clock. Refer to Section 3.2.11, “Configuration Pins” on page 41 for additional details. The PCI controller also uses external clocks.

An external oscillator (CLK_REF_CLK_H/L) generates the initial IXP2800/IXP2850 clock frequency. The CLK_REF_CLK range is between 75 to 125 MHz. The multiplier, used to generate the PLL output frequency, is selected from strap bits SP_AD[5:0], and is in the range from 16 to 48.

Note: Only even multipliers are supported; refer to Section 3.2.11, “Configuration Pins” on page 41 for more information. The individual internal clocks are generated by dividing the highest frequency clock by various programmable integers (in the range from 3 to 15) followed by another division by 2.

Note: The APB clock frequency cannot be configured to operate slower than the Slowport clock (SP_CLK) frequency; otherwise, the Slowport I/O may be repeated indefinitely. The APB clock frequency is controlled via the CAP CLOCK_CONTROL register and the SP_CLK frequency is controlled via the CAP SP_CCR register.

Note: The DRAM_CLK_RATIO divisor value programmed in the CAP CLOCK_CONTROL register must always be greater than or equal to 6, to avoid data corruption.

Note: No external device (MSF) can be configured to run faster than the internal Command Push-Pull (CPP) bus frequency. The CPP frequency is always ½ of the microengine frequency, which at 1.4 GHz is 700 MHz, at 1.0 GHz is 500 MHz, and at 650 MHz is 325 MHz.

Figure 11. REF_CLK Timing

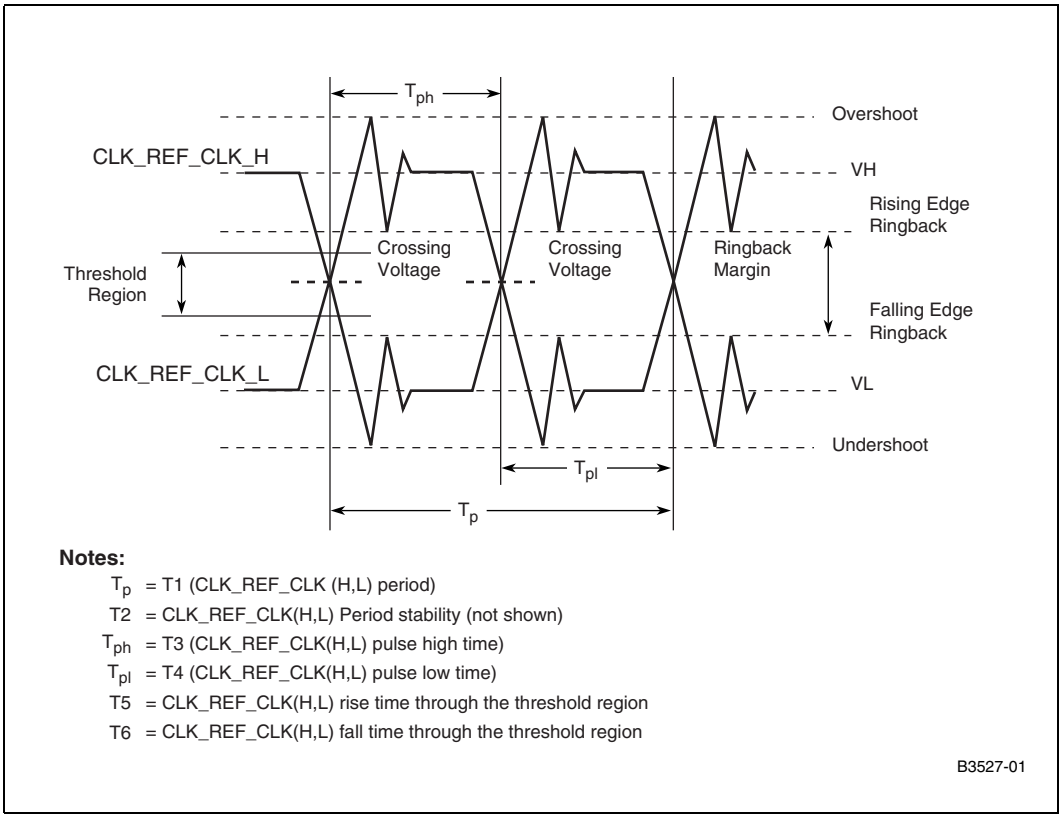


Table 28. REF_CLK DC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes 1, 2, 3 4, 5, 6, 7, 8
Vabsolute	Absolute Voltage Range	– 0.3	—	VCC25 + 0.3	V	1
Vi	Input Common Mode Voltage Range	825	—	1575	mV	
VCROSS	Crossing Voltage	875	1200	1525	mV	2, 3, 4
VOV	Overshoot	N/A	N/A	VCC25 + 0.3	V	5 , 4
VUS	Undershoot	– 0.3	N/A	N/A	V	6, 4
VRBM	Ringback Margin	0.200	N/A	N/A	V	7, 4
VTH	Threshold Margin	VCROSS – 0.100	—	VCROSS + 0.100	V	8, 4

1. Not a functional spec. Reliability limit.
2. Crossing Voltage is defined as the absolute voltage where the rising edge of CLK_REF_CLK_H is equal to the falling edge of CLK_REF_CLK_L. Guaranteed by design simulations.
3. As defined in IEEE 1596.3.
4. Guaranteed by design.
5. Overshoot is defined as the absolute value of the maximum voltage allowed.
6. Undershoot is defined as the absolute minimum voltage allowed.
7. Ringback margin is defined as the absolute voltage difference between the maximum rising edge ringback and the maximum falling edge ringback.
8. Threshold region is defined as a region entered at the crossing voltage in which the differential receiver switches. It includes input threshold hysteresis.

Table 29. REF_CLK AC Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes 1,2,3,4,5,6
Reference Clock Input Frequency	75	100	125 [2]	MHz	
T1: CLK_REF_CLK_(L/H) Period	13.3	—	8	ns	3
CLK_REF_CLK Input Duty Cycle	40	50	60	%	2
T5: CLK_REF_CLK_(L/H) Rise Time	—	—	1	ns	2, 4
T6: CLK_REF_CLK_(L/H) Fall Time	—	—	1	ns	2, 4
PERIOD JITTER Peak-to-Peak			50 [2]	ps	
JITTER Cycle-toCycle			16	ps	5, 6

1. These specifications apply to CLK_REF_CLK.
2. Guaranteed by design.
3. The period specified here is the average period. A given period may vary from this specification, as governed by the period stability specification.
4. Rise/Fall time is measured between the 20% and 80% points of the clock swing.
5. Maximum combination of determinstic and random jitter components.
6. This parameter is not tested. It is guaranteed by design. Low cycle-to-cycle input jitter (<16ps) can be guaranteed by design if all the following conditions are met: good board layout, good supply decoupling, <1" between resistor terminator and IXP28XX, and a high-quality oscillator (such as an EPSON ultra-low jitter SAW oscillator). The use of translators is allowed, but not recommended because additional jitter will be introduced. If any of these conditions are not met, the cycle-to-cycle jitter must be measured in the system to confirm that max jitter spec is met.

Table 30 shows the frequencies that are available for DRAM, SRAM, and MSF, based on various values of the PLL output clock.

Table 30. Clock Rates Examples

Input Oscillator Frequency (MHz)			100						
PLL Output Frequency (MHz) [PLL Multiplier][1]			2000 [20]	2200 [22]	2400 [24]	2600 [26]	2800 [28]	4000 [40]	4800 [48]
Microengine Frequency[2]			1000	1100	1200	1300	1400	2000	2400
Intel XScale® core & Command/Push/Pull Bus Frequency [3]			500	550	600	650	700	1000	1200
Divide Ratio for other Units (except APB)[4]	Divisor[5]	2[6]	500	550	600	650	700	1000	1200
		3	333	367	400	433	467	666	800
		4	250	275	300	325	350	500	600
		5	200	220	240	260	280	400	480
		6	167	183	200	217	233	334	400
		7	143	157	171	186	200	286	342
		8	125	138	150	163	175	250	300
		9	111	122	133	144	156	222	266
		10	100	110	120	130	140	200	240
		11	91	100	109	118	127	182	218
		12	83	92	100	108	117	166	200
		13	77	85	92	100	107	154	184
		14	71	79	86	93	100	142	172
		15	67	73	80	87	93	134	160

1. This multiplier is selected via SP_AD[5:0] strap pins.
2. This frequency is the PLL output frequency divided by 2.
3. This frequency is the PLL output frequency divided by 4.
4. The ABP divisor specified in the CLOCK_CONTROL CAP CSR is scaled by an additional x4.
5. This divisor is selected via the CLOCK_CONTROL CAP CSR. Base Frequency is the PLL output frequency divided by 2.
6. This divide ratio is only used by test logic. In the normal functional mode, this ratio is reserved for Push/Pull clocks only.

4.4.2 Maximum Supported Operating Frequencies

Table 31 lists the maximum operating frequencies for the associated network processor internal/external functional units. The maximum external interface operating frequencies are only available using the 1.4 GHz parts.

Table 31. Maximum Supported Operating Frequencies

Device	Microengine Frequency	QDR Frequency	RDR[1] Frequency	MSF[2,3] Frequency	PCI Frequency
RPIXP2800BB	1.4 GHz	233 MHz[4]	533 MHz[4]	500 MHz	66 MHz
RPIXP2800BA	1.0 GHz	200 MHz	400 MHz	400 MHz	66 MHz
RPIXP2800BC	650 MHz	163 MHz	432 MHz	400 MHz	66 MHz
RPIXP2850BB	1.4 GHz	233 MHz	533 MHz	500 MHz	66 MHz
RPIXP2850BA	1.0 GHz	200 MHz	400 MHz	400 MHz	66 MHz
RPIXP2850BC	650 MHz	163 MHz	432 MHz	400 MHz	66 MHz

1. The minimum supported frequency for the RDR interface is 400 MHz.
2. Derived from an external source.
3. The minimum supported frequency for the MSF interface is 200 MHz.
4. These frequencies cannot be achieved simultaneously with a 1.4 GHz Microengine operating frequency.

4.4.3 Maximum Clock Frequencies

The clock frequency for each interface is derived from an integer divide in the range of 3 to 15 of the Microengine operating frequency. As such, a device running at 1.4 GHz cannot simultaneously achieve the maximum operating frequency for all of the external interfaces. Table 32 lists examples of the maximum frequencies achievable, based on the Microengine clock frequency.

Table 32. Example Maximum Clock Frequencies[1]

Device	REF_CLK	PLL Multiplier	PLL Output	Microengine	QDR	RDR[2]	MSF[3]
RPIXP2800BC RPIXP2850BC	81.25	16	1300	650	163	432/108	325
				Divisors	4	6	2
RPIXP2800BB, RPIXP2850BB	100	28	2800	1400	233	508/127	466
				Divisors	6	11	3
RPIXP2800BB, RPIXP2850BB	100	24	2400	1200	200	533/133	400
				Divisors	6	9	3
RPIXP2800BB, RPIXP2850BB	100	25	2500	1250	208	500/125	416
				Divisors	6	10	3
RPIXP2800BA, RPIXP2850BA	100	20	2000	1000	200	400/100	333
				Divisors	5	10	3

1. All values are in MHz.
2. Actual internal frequency is the RDR frequency divided by 4.
3. If internally derived from the PLL, the maximum frequency for an external source is listed in Table 31.

4.4.4 Clock DC Parameters

The following clock-related signals use LVTTL signaling levels as shown in Table 33.

- CLK_PHASE_REF
- CLK_STOP
- CLK_PLL_BYP
- CLK_NRESET
- CLK_NRESET_OUT

Table 33. Clock Buffer DC Specifications (Sheet 1 of 2)

Parameter	Conditions	Symbol	Minimum	Maximum	Unit	Notes[1, 2]
Input High (Logic 1) Voltage	Vcc = 3.0 to 3.6 V	VIH	2.0	VDD + 0.3	V	1
Input Low (Logic 0) Voltage	Vcc = 3.0 to 3.6 V	VIL	-0.3	0.8	V	1
Input Leakage Current	0 V ≤ Vin ≤ VDD	ILI	-10.0	10.0	uA	
Output Leakage Current	Outputs disabled, 0 V ≤ Vin ≤ VDD	ILo	-10.0	10.0	uA	

Table 33. Clock Buffer DC Specifications (Sheet 2 of 2)

Parameter	Conditions	Symbol	Minimum	Maximum	Unit	Notes[1, 2]
Output High Voltage	IOH = -4.0 mA	VOH	2.4	N/A	V	1, 2
Output Low Voltage	IOL = 4.0 mA	VOL	N/A	0.4	V	1, 2
Supply Voltage		VDD	3.1	3.5	V	1

1. All voltages referenced to Vss (GND).
2. The load used for VOH and VOL testing is shown in Figure 22. AC load current is higher than the shown DC values.

4.4.5 PCI I/O Unit

This section specifies the following electrical behavior for the PCI I/O unit.

- DC specifications
- AC timing specifications

4.4.5.1 PCI DC Specifications

Table 34. PCI DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input High Voltage		0.5 x Vcc33	Vcc33 + 0.5 V
V_{il}	Input Low Voltage		—	0.3 x Vcc33
V_{oh}	Output High Voltage	Ioh = -500 uA	0.9 x Vcc33	—
V_{ol}	Output Low Voltage	Iol = 1500 uA	—	0.1 x Vcc33
I_i	Input Leakage Current[1]	0 ≤ Vin ≤ Vcc33	-10 uA	10 uA
C_{in}	Pin Capacitance		5 pF	10 pF

1. Input leakage currents include high-impedance output leakage for all bidirectional buffers with three-state outputs.

Note: In Table 34, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (-) current. Input leakage currents include high-Z output leakage for all bidirectional buffers with three-state outputs. The electrical specifications are preliminary and subject to change.

4.4.5.2 PCI Overshoot/Undershoot Specifications

The PCI I/Os are designed to be tolerant of overshoot and undershoot associated with normal I/O switching. However, excessive overshoot or undershoot of I/O signals can cause the device to latch up. Table 35 specifies limits on I/O overshoot and undershoot that should *never* be exceeded. Table 36 lists the maximum PCI Interface loading.

Table 35. Overshoot/Undershoot Specifications

Pin Type	Undershoot	Overshoot	Maximum Duration
Input	– 0.7 V [1]	VCC33 +0.7 [1]	4 ns
Output	– 0.7 V [1]	VCC33 +0.7[1]	4 ns

1. Design requirement. Guaranteed by design.

Table 36. Maximum Loading

Bus Interface	Maximum Number of Loads	Trace Length (inches)
PCI	Four loads at 66-MHz bus frequency Eight loads at 33-MHz bus frequency	5 to 7

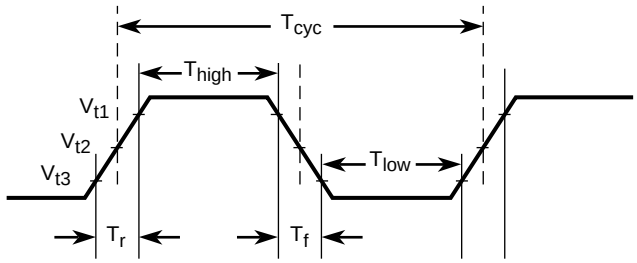
4.4.5.3 PCI AC Specifications

The AC specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal.

The PCI pins support the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Version 2.2**, which describes the PCI I/O protocol and pin AC specifications.

4.4.5.4 PCI Clock Signal AC Parameter Measurements

Figure 12. PCI Clock Signal AC Parameter Measurements



Notes:
V_{t1} = 0.5 ± V_{CC} 33
V_{t2} = 0.4 ± V_{CC} 33
V_{t2} = 0.3 ± V_x 33

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Table 37. 66 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	PCI_CLK cycle time	15	—	ns
T_{high}	PCI_CLK high time[1]	6	—	ns
Tl_{ow}	PCI_CLK low time[1]	6	—	ns
	PCI_CLK slew rate[1, 2]	1.5	4	V/ns

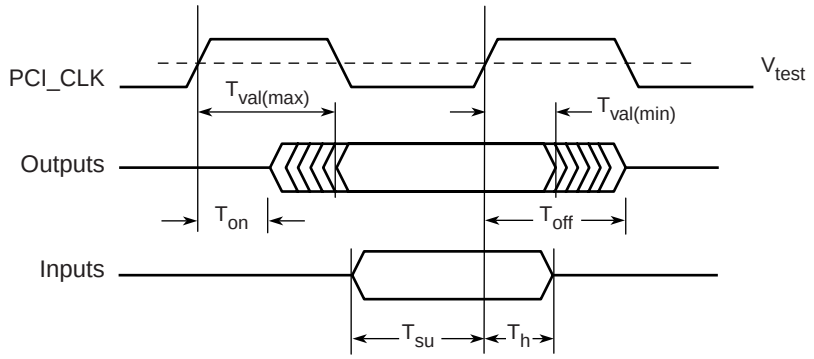
1. Not tested. Guaranteed by design.
2. 0.2 Vcc33 to 0.6 Vcc33.

Table 38. 33 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	PCI_CLK cycle time	30	—	ns
T_{high}	PCI_CLK high time[1]	11	—	ns
T_{low}	PCI_CLK low time[1]	11	—	ns
	PCI_CLK slew rate[1,2]	1	4	V/ns

1. Not tested. Guaranteed by design.
2. 0.2 Vcc33 to 0.6 Vcc33.

Figure 13. PCI Bus Signals



Note: V_{test} = 0.4 V_{CC}33 for 3.3 volt PCI signals

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4.4.5.5 PCI Bus Signals Timing

Table 39. 33 MHz PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay, bused signals[1]	2	11	ns
T_{val} (point-to-point)	CLK to signal valid delay, point-to-point signals[2]	2	12	ns
T_{on}	Float to active delay[3]	2	—	
T_{off}	Active to float delay [3]	—	28	ns
T_{su}	Input setup time to CLK, bused signals[4]	7	—	ns
T_{su} (point-to-point)	Input setup time to CLK, point-to-point signals[5]	10	—	ns
T_h	Input signal hold time from CLK	0	—	ns

1. Bused signals are AD, CBE_L, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, DEVSEL_L, and STOP_L.
2. Point-to-point signals are REQ_L and GNT_L.
3. Not tested. Guaranteed by design.
4. Bused signals are AD, CBE_L, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, DEVSEL_L, and STOP_L.
5. Point-to-point signals are REQ_L and GNT_L.

Table 40. 66 MHz PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay, bused signals[1]	1	6	ns
T_{val} (point-to-point)	CLK to signal valid delay, point-to-point signals[2]	1	6	ns
T_{on}	Float to active delay[3]	2	—	
T_{off}	Active to float delay[3]	—	6	ns
T_{su}	Input setup time to CLK, bused signals[4]	3	—	ns
T_{su} (point-to-point)	Input setup time to CLK, point-to-point signals[5]	5	—	ns
T_h	Input signal hold time from CLK	0	—	ns

1. Bused signals are AD, CBE_L, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, DEVSEL_L, and STOP_L.
2. Point-to-point signals are REQ_L and GNT_L.
3. Not tested. Guaranteed by design.
4. Bused signals are AD, CBE_L, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, DEVSEL_L, and STOP_L.
5. Point-to-point signals are REQ_L and GNT_L.

4.4.6 SRAM

This section contains AC and DC parameters for the QDR.

Table 41. QDR DC Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit	Notes 1,2,3,4
V_{IH}	Input High Voltage (Logic 1)		VREF + 0.1	VDDQ + 0.3	V	1, 2
V_{IL}	Input Low Voltage (Logic 0)		-0.3	VREF - 0.1	V	1, 2
V_{IN}	Clock Input Signal Voltage		-0.3	VDDQ + 0.3	V	1, 2, 3
I_{LI}	Input Leakage Current	0 V ≤ VIN ≤ VDDQ	-25	25	uA	
I_{LO}	Output Leakage Current	Output(s) disabled, 0 V ≤ VIN ≤ VDDQ (Q)	-25	25	uA	
V_{OH}	Output High Voltage	|IOH| ≤ 0.1mA	VDDQ - 0.2	VDDQ	V	1, 4
V_{OL}	Output Low Voltage	IOL ≤ 0.1mA	VSS	0.2	V	1, 4
V_{DD}	Supply Voltage		1.25	1.45	V	1
V_{DDQ}	Isolated Output Buffer Supply		1.4	1.6	V	1
V_{REF}	Reference Voltage		0.7	0.8	V	1

1. All voltages are referenced to VSS (GND).
2. Overshoot: VIH (AC) ≤ VDD + 0.7 V for t ≤ t3.0 ns.
3. Not tested. Design requirement validated by simulations.
4. HSTL outputs meet JEDEC HSTL Class I standard.

Table 42. QDR Signal Timing

	QDRII							
Frequency	**233 MHz**		**200 MHz**		**167 MHz**		**133 MHz**	
	MIN	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
Input Timing								
Setup Time[1, 2] (ns)	-0.70		-0.77		-0.97		-1.27	
Hold Time (ns)[1]	1.45		1.73		2.03		2.43	
Output Timing								
Output Valid (ns)[1]		-0.65		-0.9		-1.10		-1.37
Output Hold (ns) [1]	0.65		0.9		1.10		1.37	
K_0/1 to Output Skew at C4 Bump[1, 3] (ns)	-0.19	0.19	-0.20	0.20	-0.22	0.22	-0.23	0.23
K_0/1 to Output Skew at Package Ball [1, 4] (ns)	-0.28	0.28	-0.29	0.29	-0.31	0.31	-0.32	0.32

1. Not tested. Guaranteed by simulations
2. The specified setup time is negative, which means that the data can arrive at the pins up to the specified time after the rising edge of the clock as shown in Figure 14.
3. The C4 Bump is the connection point of the silicon die to the package. This parameter specifies the skew between K0 and K1 clock and Write Data, Address, and Write/Read Port Select output signals, but does not include the mismatch introduced by the package substrate routing.
4. This parameter specifies the skew between K0 and K1 clock and Write Data, Address, and Write/Read Port Select output signals, including the mismatch introduced in the package substrate routing.

Figure 14 shows the timing goals for the IXP2800/IXP2850 QDRII interface. All timing references are the rising edges of C and C# or K and K#, for receiver and transmitter, respectively.

Note: The system designer must ensure that the design implementation meets the SRAM K-clock-to-C-clock timing relationship, as specified in the SRAM datasheet. This may require additional trace routing on the baseboard to the C_0/1 clock, to ensure that it always lags the K clock.

Table 43 lists the QDR clock skew and Figure 14 shows timing goals for the QDRII interface.

Table 43. QDR Clock Skew (Sheet 1 of 2)

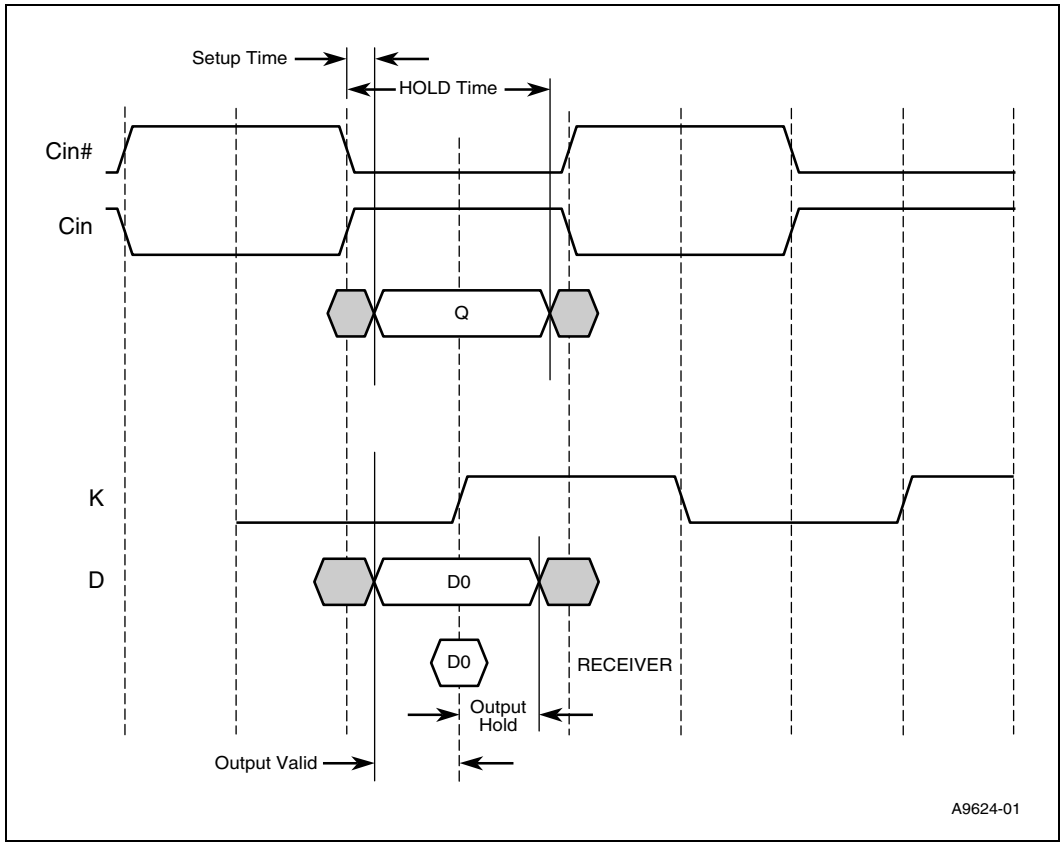
Description[1, 2]	**166 MHz**		**200 MHz**		**233 MHz**	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
K Rise to K# Rise [3]	2.78 ns	3.22 ns	2.30 ns	2.70 ns	1.81 ns	2.19 ns
K# Rise to K Rise [3]	2.78 ns	3.22 ns	2.30 ns	2.70 ns	1.81 ns	2.19 ns
C Rise to C# Rise [3]	2.78 ns	3.22 ns	2.30 ns	2.70 ns	1.81 ns	2.19 ns
C# Rise to C Rise [3]	2.78 ns	3.22 ns	2.30 ns	2.70 ns	1.81 ns	2.19 ns
K_m Rise to K_n Rise [3]	-0.18 ns	0.18 ns	-0.15 ns	0.15 ns	-0.14 ns	0.14 ns
K_m# Rise to K_n# Rise [3]	-0.18 ns	0.18 ns	-0.15 ns	0.15 ns	-0.14 ns	0.14 ns
C_m Rise to C_n Rise [3]	-0.18 ns	0.18 ns	-0.15 ns	0.15 ns	-0.14 ns	0.14 ns

Table 43. QDR Clock Skew (Sheet 2 of 2)

Description[1], [2]	166 MHz		200 MHz		233 MHz	
	Min	Max	Min	Max	Min	Max
C_m# Rise to C_n# Rise [3]	-0.18 ns	0.18 ns	-0.15 ns	0.15 ns	-0.14 ns	0.14 ns
K_m Rise to C_m Rise [3]	-0.22 ns	0.22 ns	-0.20 ns	0.20 ns	-0.19 ns	0.19 ns
K_m# Rise to C_m# Rise [3]	-0.22 ns	0.22 ns	-0.20 ns	0.20 ns	-0.19 ns	0.19 ns

1. $m \in \{0, 1\}, n \in \{0, 1\}, m \neq n$
2. Specified at device package ball, which includes package substrate routing skew.
3. Not tested. Guaranteed by design simulations

Figure 14. QDR Signal Timing



4.4.7 RDRAM

Table 45 lists the supported loading configurations, Table 44 lists the RDRAM DC parameters, and Table 46 lists the RDRAM AC parameters.

Table 44. RDRAM DC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
VCCR, VCCRA	Supply voltage	1.28	1.42	V
VTERM	Termination voltage	1.7	1.9	V
VREF	Reference voltage	1.2	1.6	V
VCIS,CTM[1, 2]	Clock input voltage swing on CTM pin	0.25	0.70	V
VCIS, CFM[1, 2]	Clock voltage swing on CFM pin	0.25	0.70	V
VX [2]	Clock differential crossing-point voltage	1.30	1.80	V
VCM [2]	Clock input common-mode voltage	1.40	1.70	V
VDIL[3]	Data input low voltage	VREF -0.5	VREF -0.175	V
VDIH [2]	Data input high voltage	VREF +0.175	VREF +0.5	V
VDIS [2]	Data input voltage swing	0.4	1.0	V
ADI [2]	Data input asymmetry about V REF	-15%	15%	VDIS
IOL,TEST	Output current test condition @ VOL = 0.9 V	—	30	mA
CMD, SCK [3]	VOL	–0.3	0.5*Vccrio – 0.25	V
CMD, SCK[3]	VOH	0.5*Vccrio + 0.25	0.5*Vccrio + 0.3	V
PCLKM, SYNCLKN, SIO [4]	VOL	– 0.3	0.3*Vccrio	V
PCLKM, SYNCLKN, SIO [4]	VOH	0.7*Vccrio	Vccrio + 0.3	V
SIO	VIL	– 0.3	0.3*Vccrio	V
SIO	VIH	0.7*Vccrio	Vccrio + 0.3	V

1. VCIS applies to both Clock and $\overline{\text{Clock}}$.
2. Guaranteed by design.
3. 28-ohm external termination with 0.9 V (Thevenin equivalent).
4. No termination.

Table 45. RDRAM Loading

Bus Interface	Maximum Number of Loads	Trace Length (inches)
Short Channel: 400 and 533 MHz	4 devices per channel.	20[1]
Long Channel: 400 MHz	2 RIMMs per channel – a maximum of 32 devices in both RIMMs.	20[1]
Long Channel: 533 MHz	1 RIMM and 1 C-RIMM per channel – a maximum of 16 devices.	20[1]

1. For termination, the DRAMs should be located as close as possible to the IXP2800 network processor..

Table 46. RDRAM AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
tCYCLE	CTM, CFM cycle time	1.875	2.50	ns
tCYCLE, SLOW	Slow-mode CTM, CFM cycle time	5.00	—	ns
tCR, tCF[1, 2]	CTM, CFM input rise and fall times	0.20	0.50	ns
tCH, tCL CTM [2]	CFM high and low times	40%	60%	tCYCLE
tTR [2]	CTM-to-CFM differential	—	0.26	ns
tDR, tDF [2]	Data input rise and fall times	0.20	0.50	ns
tS, tH [2, 3]	Data-to-Clock setup and hold times 800 MHz speed grade[3] 1066 MHz speed grade	 0.175 0.140	—	 ns ns
tQR - tQF [2]	Data Output Rise and Fall Time[3]	0.18	0.40	ns
tQ [2]	Clock-to-Data Output Time 800 MHz speed grade[3] 1066 MHz speed grade	 -0.250 -0.180	 0.250 0.180	 ns ns
tCCInterval [2]	IOL calibration interval	—	100	ms
tJ, RC [2]	RDRAM CMOS Clock Jitter SCK	—	1.0	ns
tS, tH, RC [2]	SIO to SCK setup and hold times	1.0	—	ns
tQ, RC [2]	SCK to Data out SCK rise to CMD SCK fall to SIO[3]	—	 -10 -490	ns

1. Measured from 20% – 80% of input voltage swing.
2. Guaranteed by design.
3. For SCK = 1 MHz.

4.4.8 SPI-4 and CSIX

This section describes the parameters for the Media and Switch Fabric (MSF) Interface. These parameters apply whether the bus is configured to carry SPI-4 packets/cells or CSIX C-Frames.

4.4.8.1 DC Parameters

Table 47 lists applicable DC thresholds for LVTTL, Table 48 lists applicable Driver DC thresholds for LVDS, and Table 49 lists applicable Receiver DC thresholds for LVDS.

Table 47. SPI-4 LVTTL DC Thresholds

Symbol	Parameter	Min (V)	Max (V)
V_OH	Output High Voltage	2.4	3.6
V_IH	Input High Voltage	2.0	3.6
V_IL	Input Low Voltage	—	0.8
V_OL	Output Low Voltage	—	0.4

Table 48. SPI-4 LVDS Driver DC Specifications

Symbol	Parameter	Min	Max
Voh	Output Voltage High	—	1375 mV[1]
Vol	Output Voltage Low	1025 mV[1]	—
Vod [2]	Output Differential Voltage	150 mV	250 mV
Vos [2]	Output Offset Voltage	1150 mV	1250 mV[1]
Ro [2]	Output Impedance, Single Ended	40 ohms	140 ohms

1. Output voltage valid when VREFHI = 1.4 V and VREFLO = 1.0 V. The following equations determine the excursions when the voltage references and Rzq are not held at nominal:

Ioh = 2 * ((VREFHI – VREFLO) / Rzq) / 3 (valid when Rload = Rzq)
Iol = -2 * ((VREFHI – VREFLO) / Rzq) / 3 (valid when Rload = Rzq)

2. Guaranteed by design

Table 49. SPI-4 LVDS Receiver DC Specifications

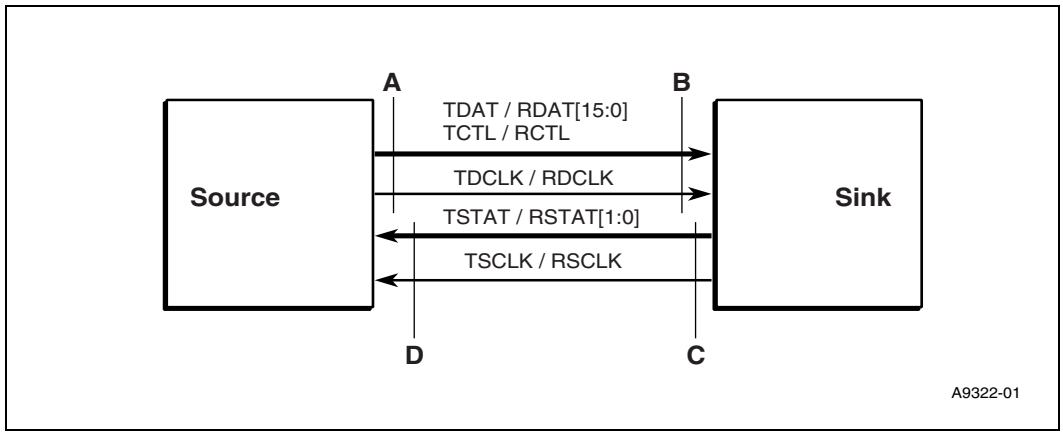
Symbol	Parameter	Min	Max
Vi	Input Voltage Range	825 mV	1575 mV
Vidth	Input Differential Threshold	– 100 mV	+ 100 mV
Vhyst [1]	Input Differential Hysteresis	25 mV	—
Ri [1]	Receiver Differential Input Impedance	80 ohms	120 ohms

1. Guaranteed by design.

4.4.8.2 AC Parameters

System-level reference points for specified parameters are shown in Figure 15. Corresponding reference points with respect to the clock edge are shown in Figure 16, Figure 17, and Figure 18.

Figure 15. System Level Reference Points



Data Path Timing

Two sets of data path timing parameters are specified to support different bit alignment schemes at the receiver. Table 50 provides the corresponding parameters for the case of “static alignment” in which the receiver latches data at a fixed point in time relative to clock (requiring a more precisely specified sampling window).

Table 51 provides the corresponding parameters for the case of “dynamic alignment” in which the receiver has the capability of centering the data and control bits relative to clock. From an AC timing perspective, a compliant interface only needs to meet the parameters at the data path for either static or dynamic alignment, but may also comply to both sets of parameters. A compliant driver must meet both timing specifications to be interoperable with both types of receivers.

Figure 16. Reference Points for Data Path Timing Parameters

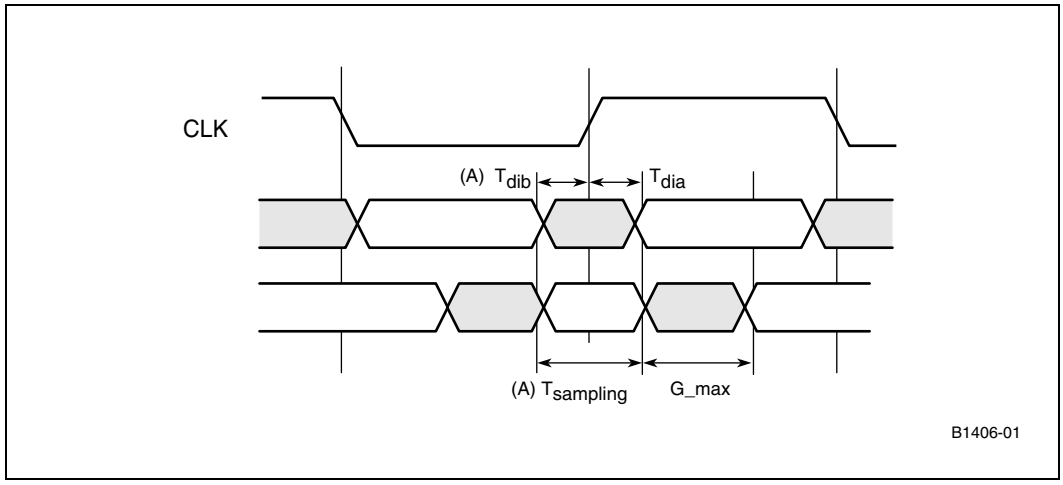


Table 50. Data Path Interface Timing (Static Alignment)

Symbol	Parameter		Min	Max	Units
fD	TDCLK / RDCLK Frequency		200	500	MHz
	TDCLK / RDCLK Duty Cycle [1]		45	55	%
T_dia, T_dib[1]	Data invalid window with respect to clock edge (Reference point A).		—	280	ps
G_max [1]	Worst-case cumulative skew and jitter contribution (Reference point B).		—	790	ps
Tsampling[1]	Data valid window with respect to clock edge. (Reference point B)		—	1/(2ƒD) - G_max	ps
	20% - 80% rise and fall times (UI = ½ fD)	(Reference point A) (Reference point B)	100 ps 100 ps	0.30 UI 0.36 UI	UI UI

Comments:

1. Rise and fall times assume nominal 100-ohm termination and exclude reflections.
2. All timing parameters are measured relative to the differential crossing point of the corresponding clock signal.
3. Jitter parameters are peak-to-peak, measured above fD/1000 and below fD.
4. Receiver sensitivity is assumed to be less than or equal to 100 mV.
5. Assumes a 5 pF output load at reference point A, a 10 pF load at reference point B, and a 50-ohm transmission line in-between.
6. Assumes up to a 20 ps skew between traces of a differential pair.

1. Guaranteed by design.

Table 51. Data Path Interface Timing (Dynamic Alignment)

Symbol	Parameter		Min	Max	Unit
fD	TDCLK / RDCLK Frequency		200	500	MHz
—	TDCLK / RDCLK Jitter (at reference point A) [1]		—	0.10	UI
—	TDAT / RDAT / TCTL / RCTL Jitter (at reference point A) [1]		—	0.24	UI
—	20% - 80% rise and fall times[1] (UI = ½ fD)	(Reference point A) (Reference point B)	100 ps 100 ps	0.30 UI 0.36 UI	UI UI

Comments:

1. Rise and fall times assume nominal 100-ohm termination and exclude reflections.
2. All timing parameters are measured relative to the differential crossing point of the corresponding clock signal.
3. Jitter parameters are peak-to-peak, measured above fD/1000 and below fD.
4. Receiver sensitivity is assumed to be less than or equal to 100 mV.
5. Assumes a 5 pF output load at reference point A, a 10 pF load at reference point B, and a 50-ohm transmission line in-between.
6. Assumes up to a 20 ps skew between traces of a differential pair.

1. Guaranteed by design.

Table 52. Transmitter and Receiver AC Timing Parasitics

Parameter	Min	Max	Units
Transmitter			
Channel-to-Channel Skew [1]	N/A	100	ps
Differential Pair Skew [1]	N/A	50	ps
TCLK Jitter [1]	N/A	100	ps
TCLK_REF Jitter [1]	N/A	50	ps
TCLK Duty Cycle when sourced from internal PLL [1]	45	55	%
TCLK Duty Cycle when sourced from TCLK_REF [1, 2]	45	55	%
TXCCLK Duty Cycle when sourced from internal PLL [1]	45	55	%
TXCCLK Duty Cycle when sourced from TCLK_REF/RCLK [1, 3]	45	55	%
Receiver			
Receiver Data Valid Window [1, 4]	3*(Bit Time/8)[5]	N/A	ps
Receiver Data Valid Window [1, 6]	536	N/A	ps
Receiver Data Valid Window [1, 7]	469	N/A	ps
Receiver Data Valid Window [1, 8]	375	N/A	ps

1. Guaranteed by design.
2. When TCLK_REF is selected as the TCLK source, the TCLK_REF duty cycle must be held to within 47.5% to 52.5% to maintain the 45% to 55% output duty cycle; otherwise, the TCLK duty cycle will be equal to the source TCLK_REF duty cycle +/- 2.5%.
3. When TCLK_REF or RCLK is selected as the TXCCLK source, the TCLK_REF/RCLK duty cycle must be held to within 47.5% to 52.5% to maintain the 45% to 55% output duty cycle; otherwise, the TXCCLK duty cycle will be equal to the source TCLK_REF/RCLK duty cycle +/- 2.5%.
4. This parameter specifies the receiver setup/hold requirement. This is equal to three sample periods, and the sample period is the Bit Time/8. The DLL in the receive path generates 16 unique sample clocks per cycle or 8 sample clocks per bit time. The receive data valid window must be at least 3 sample clocks wide. For example, at 350 MHz this is ((((1/350)/2))/8)*3 or 536 ps.
5. The bit time is the 1/Cycle time of the interface divided by 2 for a double data rate bus. For example, at 350 MHz, the bit time is ((1/350/2) or 1.428 ns.
6. Valid for Interface running at 350 MHz.
7. Valid for Interface running at 400 MHz.
8. Valid for Interface running at 500 MHz.

FIFO Status Channel

The following section describes AC timing parameters for a FIFO status channel implemented using LVTTL I/O. As noted in Table 53, the maximum clock frequency of the LVTTL FIFO Status Channel must not exceed ¼ of the selected data path clock rate. For an optional LVDS FIFO status channel configuration, implementers should refer to the LVDS data path AC timing parameters specified in Table 50, Table 51, and Table 52.

Figure 17. SPI4-2 Receive FIFO Status Bus Timing Diagram

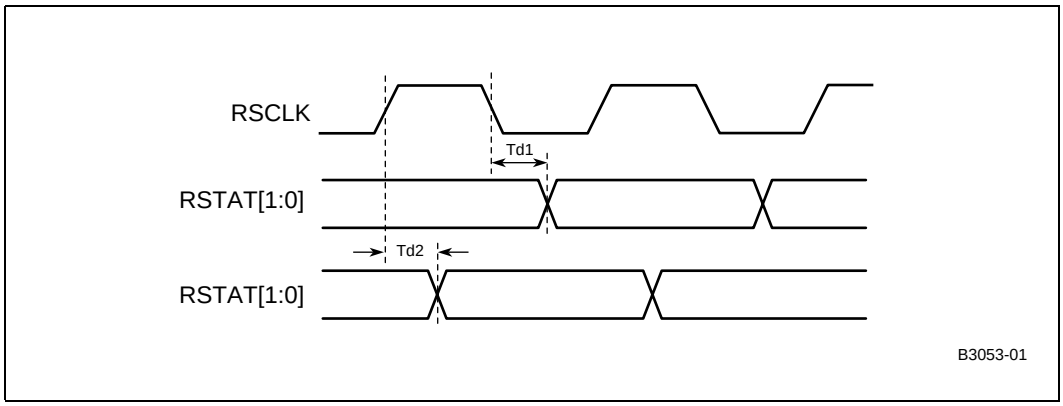


Table 53. SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Max	Units
RSCLK Frequency	fS	—	fD / 4	MHz
RSCLK Falling Edge to RSTAT[1:0] Valid (Active edge flipped to falling) [1]	Td1	0.5	4.0	ns
RSCLK Rising Edge to RSTAT[1:0] Valid (Default operation) [1]	Td2	0.5	4.0	ns

1. Guaranteed by design.

Figure 18. SPI4-2 Transmit FIFO Status Bus Timing Diagram

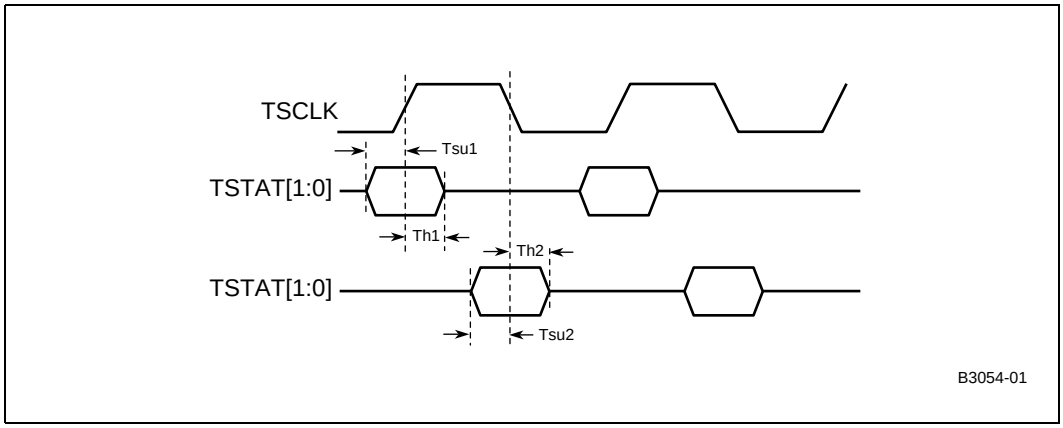


Table 54. SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Max	Units
TSTAT[1:0] Setup to TSCLK Rising Edge (Default Operation) [1]	Tsu1	2.0	—	ns
TSTAT[1:0] Hold from TSCLK Rising Edge (Default Operation) [1]	Th1	0.5	—	ns
TSTAT[1:0] Setup to TSCLK Falling Edge (when active edge flipped to falling) [1]	Tsu2	2.0	—	ns
TSTAT[1:0] Hold from TSCLK Falling Edge (when active edge flipped to falling)[1]	Th2	0.5	—	ns

1. Guaranteed by design.

4.4.9 Flow Control Bus

This section lists the LVDS parameters for the Flow Control Bus. Table 55 lists the Driver DC specifications, Table 56 lists the Receiver DC specifications, and Table 57 lists the Clock specifications. The Flow Control Bus AC timing parameters are the same as those specified for the SPI-4 LVDS data path; implementers should refer to Table 50, Table 51, and Table 52 for AC timing details.

Table 55. Flow Control Bus LVDS Driver DC Specifications

Symbol	Parameter	Min	Max
Voh	Output Voltage High	—	1375 mV
Vol	Output Voltage Low	1025 mV	—
Vod [1]	Output Differential Voltage	150 mV	250 mV
Vos [1]	Output Offset Voltage	1150 mV	1250 mV
Ro [1]	Output Impedance, Single-Ended	40 ohms	140 ohms

1. Guaranteed by design.

Table 56. Flow Control Bus LVDS Receiver DC Specifications

Symbol	Parameter	Min	Max
Vi	Input Voltage Range	825 mV	1575 mV
Vidth	Input Differential Threshold	– 100 mV	+ 100 mV
Vhyst [1]	Input Differential Hysteresis	25 mV	—
Ri [1]	Receiver Differential Input Impedance	80 ohms	120 ohms

1. Guaranteed by design.

Table 57. Flow Control Bus Clock Specifications

Symbol	Parameter	Min	Max
fd	RX/TXCCLK	200 MHz	500 MHz
	RX/TXCCLK Duty Cycle [1]	45%	55%

1. Guaranteed by design.

4.4.10 Slowport I/O Buffer

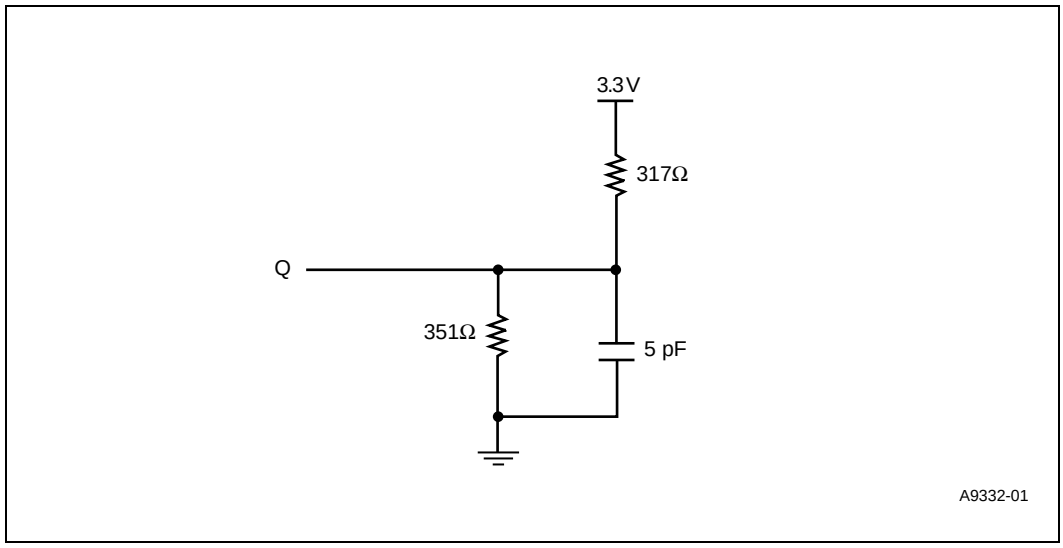
This section lists the AC and DC parameters for the Slowport.

Table 58. Slowport I/O Buffer DC Specifications

Parameter	Conditions	Symbol	Minimum	Maximum	Unit	Notes [1,2]
Input High (Logic 1) Voltage	Vcc = 3.0 to 3.6 V	VIH	2.0	VDD + 0.3	V	1
Input Low (Logic 0) Voltage	Vcc = 3.0 to 3.6 V	VIL	-0.3	0.8	V	1
Input Leakage Current	0 V ≤ Vin ≤ VDD	ILI	-10.0	10.0	uA	
Output Leakage Current	Outputs disabled, 0 V ≤ Vin ≤ VDD	ILo	-10.0	10.0	uA	
Output High Voltage	IOH = -4.0 mA	VOH	2.4	—	V	1, 2
Output Low Voltage	IOL = 4.0 mA	VOL		0.4	V	1, 2
Supply Voltage		VDD	3.1	3.5	V	1

1. All voltages are referenced to Vss (GND).
2. The load used for VOH and VOL testing is shown in Figure 19. AC load current is higher than the DC values shown.

Figure 19. Transient Equivalent Testing Load Circuit for Slowport I/O Buffer



4.4.11 Slowport Timing

4.4.11.1 PROM Device Timing Information

The following figures and tables provide timing information for the Slowport.

Figure 20. Single Write Transfer for Self-Timing Device

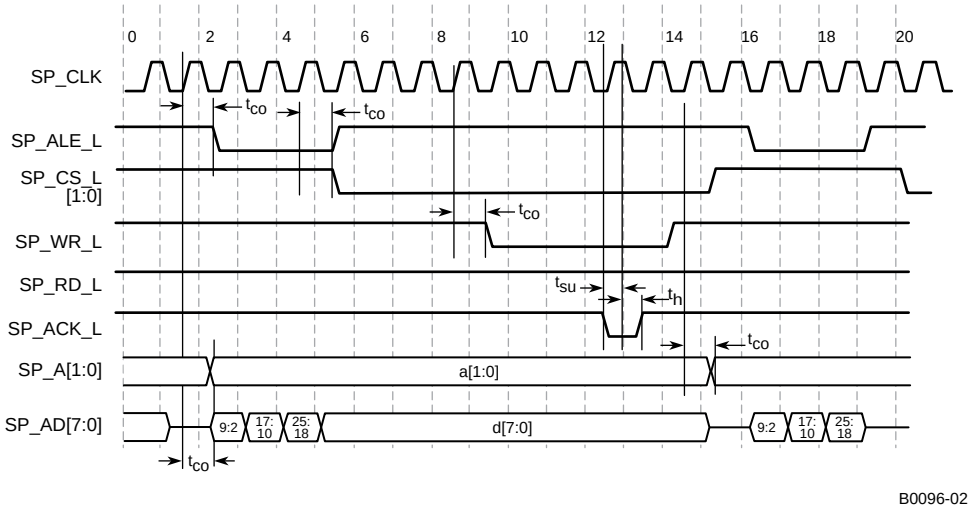


Table 59. Slowport Write AC Parameters [1]

External Signals	tco l max[2]/min (ns)	th[3] (ns) min	tsu[3] (ns) min	tpw (ns)	Loading (pF)
SP_ALE	9.0/1.5				50
SP_CS[0]	9.0/1.5				50
SP_CS[1]	9.0/1.5				50
SP_WR	9.0/1.5				50
SP_ACK		1	12.2		
SP_AD[1:0]	9.0/1.5				50
SP_AD[7:0] output to external device	9.0/1.5				

1. These timing parameters are specified for a 1.4 GHz core frequency and from the rising edge of SP_CLK. Guaranteed by functional test.
2. The default output timing is controlled by the TXE register. Refer to the *Intel® IXP2400 and IXP2800 Programmer's Reference Manual* for further details. By default, this register is set to a value of 0x1. For each increment to this register, a PCLK period delay is added to both the maximum and minimum specified values. For example, for a PCLK frequency of 700 MHz, a period delay is ~ 1.4 ns; using a TXE register value of 0x5, the maximum and minimum delay values would be calculated as follows:
   Max = 9.0 + (5- 1) * 1.4 = 14.6 ns.
   Min = 1.5 + (5 - 1) * 1.4 = 7.1 ns.
   Note: this delay should not exceed the cycle time of SP_CLK.
3. The sampling of the SP_ACK_L signal is controlled by the RXE register. Refer to the *Intel® IXP2400 and IXP2800 Programmer's Reference Manual* for further details. By default, this register is set to a value of 0x1. For each increment to this register, a PCLK period delay is added to the setup and is subtracted from the hold specified values. For example, for a PCLK frequency of 700 MHz, a period delay is ~ 1.4 ns; using an RXE register value of 0x5, the setup and hold delay values would be calculated as follows:
   Setup = 12.2 + (5-1) * 1.4 = 17.8 ns.
   Hold = 1.0 - (5-1) * 1.4 = - 4.6 ns.
   Note: this delay should not exceed the cycle time of SP_CLK.

Figure 21. Read Transaction for Self-Timing Device

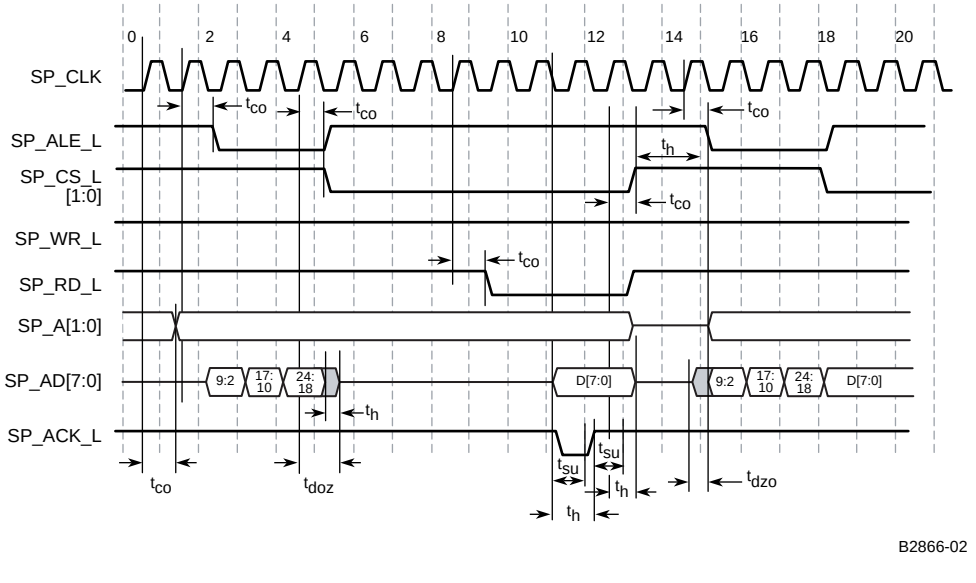


Table 60. Slowport Read AC Parameters[1]

External Signals	tco[2] l max/min (ns)	th[3] (ns) min	tsu (ns) min	tpw (ns)	toz/zo max/min (ns)	loading (pF)
SP_ALE	9.0/1.5					50
SP_CS[0]	9.0/1.5					50
SP_CS[1]	9.0/1.5					50
SP_RD	9.0/1.5					50
SP_ACK		1.0	12.2			
SP_AD[1:0]	9.0/1.5					50
SP_AD[7:0] output to external device	9.0/1.5				12.2/1.0	
SP_AD[7:0] input from external device		1.0	12.2			

1. These timing parameters are specified for a 1.4 GHz core frequency and from the rising edge of SP_CLK. Guaranteed by functional tests.
2. The default output timing is controlled by the TXE register; refer to the *Intel® IXP2400 and IXP2800 Programmer's Reference Manual* for further details. By default, this register is set to a value of 0x1. For each increment to this register, a PCLK period delay is added to both the maximum and minimum specified values. For example, for a PCLK frequency of 700 MHz, a period delay is ~ 1.4 ns; using a TXE register value of 0x5, the maximum and minimum delay values would be calculated as follows:
   Max = 9.0 + (5- 1) * 1.4 = 14.6 ns.
   Min = 1.5 + (5 - 1) * 1.4 = 7.1 ns.
   Note: this delay should not exceed the cycle time of SP_CLK.
3. The sampling of the SP_ACK_L and SP_AD signals is controlled by the RXE register. Refer to the *Intel® IXP2400 and IXP2800 Programmer's Reference Manual* for further details. By default, this register is set to a value of 0x1. For each increment to this register, a PCLK period delay is added to the setup and is subtracted from the hold specified values. For example, for a PCLK frequency of 700 MHz, a period delay is ~ 1.4 ns; using an RXE register value of 0x5, the setup and hold delay values would be calculated as follows:
   Setup = 12.2 + (5-1) * 1.4 = 17.8 ns.
   Hold = 1.0 - (5-1) * 1.4 = - 4.6 ns.
   Note: this delay should not exceed the cycle time of SP_CLK.

4.4.12 GPIO

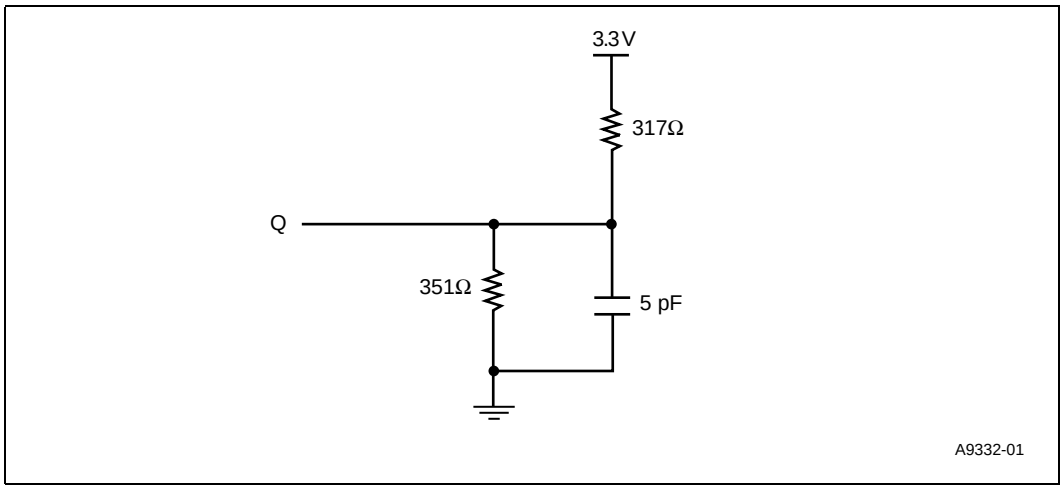
The GPIO can be used with appropriate software in I^2C applications. Refer to Philips Semiconductors* I^2C bus specification for the DC and AC characteristics. Table 61 shows the DC characteristics for a fast mode I^2C bus device. It can also be used for test purposes.

Table 61. GPIO I/O Buffer DC Specifications

Parameter	Conditions	Symbol	Minimum	Maximum	Unit	Notes[1, 2]
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1
Input Leakage Current	0 V ≤ Vin ≤ VDD	ILI	-10.0	10.0	uA	
Output Leakage Current	Outputs disabled, 0 V ≤ Vin ≤ VDD	ILo	-10.0	10.0	uA	
Output High Voltage	IOH = -4.0 mA	VOH	2.4	-	V	1, 2
Output Low Voltage	IOL = 4.0 mA	VOL	-	0.4	V	1, 2
Supply Voltage		VDD	3.1	3.5	V	1

1. All voltages referenced to Vss (GND).
2. The load used for VOH and VOL testing is shown in Figure 22. AC load current is higher than the DC values shown.

Figure 22. Transient Equivalent Testing Load Circuit for GPIO I/O Buffer



4.4.13 JTAG

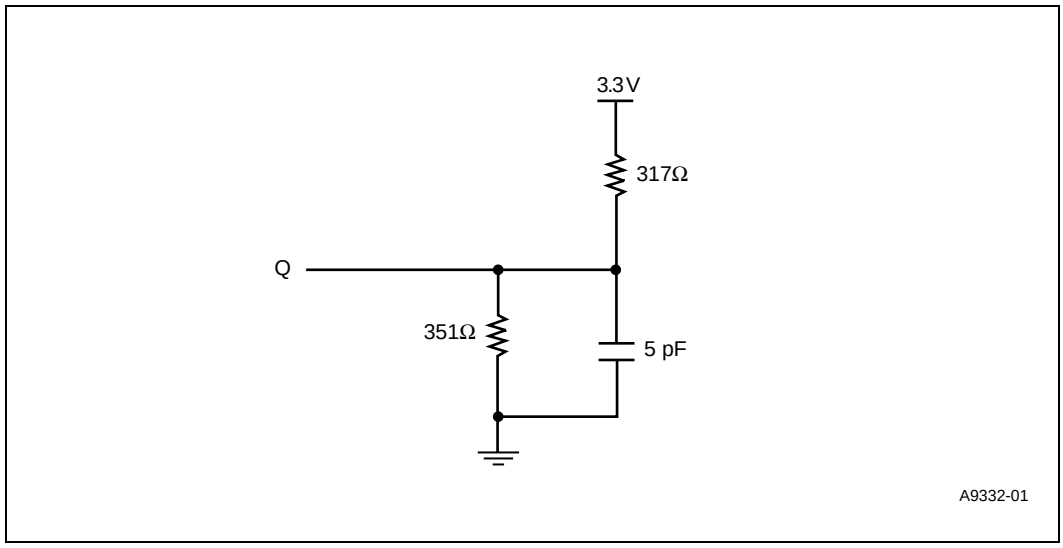
4.4.13.1 JTAG DC Electrical Characteristics

Table 62. JTAG DC Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit	Notes [1, 2]
VIH	Input High (Logic 1) Voltage		2.0	VDD + 0.3	V	1
VIL	Input Low (Logic 0) Voltage		-0.3	0.8	V	
ILI	Input Leakage Current	0 V = Vin = VDD	-10.0	+ 10.0	uA	
ILO	Output Leakage Current	Output(s) disabled, 0 V = Vin = VDD	-10.0	10.0	uA	
VOH	Output High Voltage	IOH = -4.0 mA	2.4		V	1, 2
VOL	Output Low Voltage	IOL = 8.0 mA		0.4	V	1, 2
VDD	Supply Voltage		3.1	3.5	V	1

1. All voltages referenced to Vss (GND).
2. The load used for VOH and VOL testing is shown in Figure 23. AC load current is higher than the DC values shown.

Figure 23. VIH, VOL Load for Testing



4.4.13.2 JTAG AC Characteristics

Figure 24. Boundary Scan General Timing

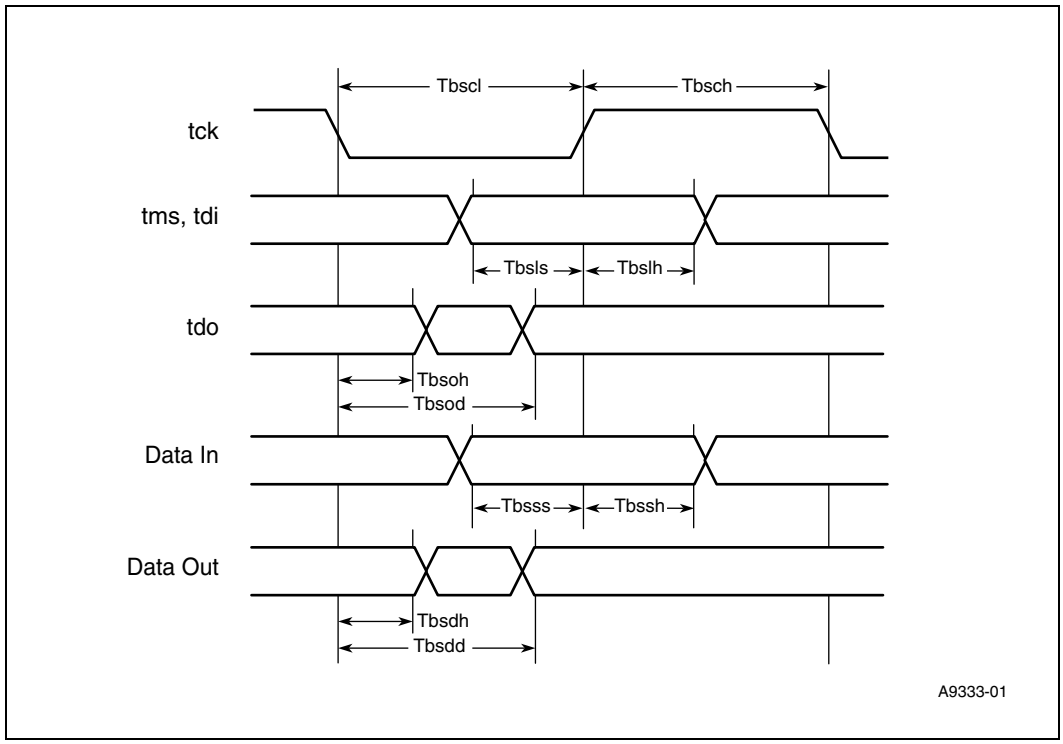


Figure 25. Boundary Scan Three-state Timing

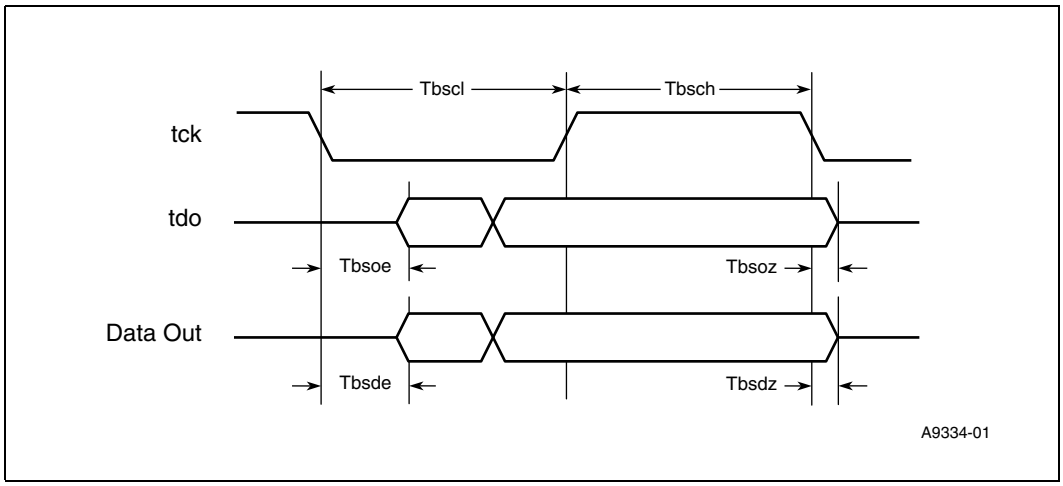


Figure 26. Boundary Scan Reset Timing

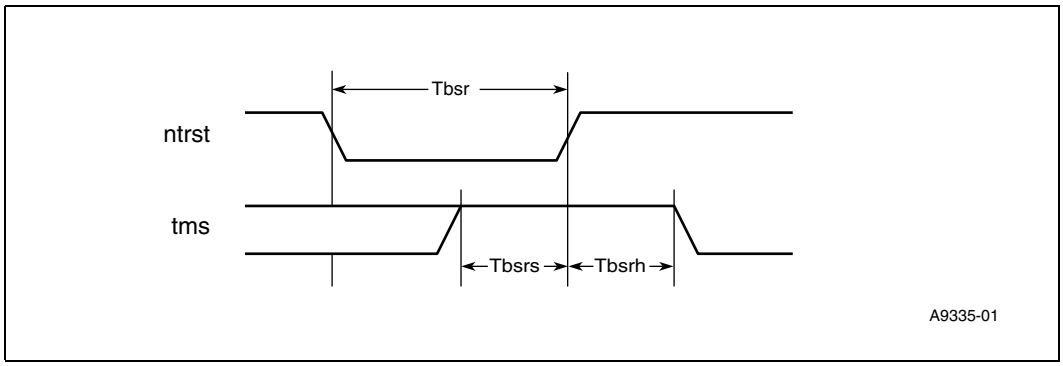


Table 63. JTAG AC Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes 1, 2, 3, 4, 5, 6, 7, 8, 9
Tbscl	TCK low period	50	—	—	ns	1
Tbsch	TCK high period	50	—	—	ns	1
Tbsis	TDI, TMS setup to [TCr]	10	—	—	ns	
Tbsih	TDI, TMS hold from [TCr]	10	—	—	ns	
Tbsoh	TDO hold time	5	—	—	ns	2
Tbsod	TCf to TDO valid	—	—	40	ns	2
Tbsss	I/O signal setup to [TCr]	5	—	—	ns	1,3
Tbssh	I/O signal hold from [TCr]	20	—	—	ns	1, 3
Tbsdh	Data output hold time	5	—	—	ns	1, 4
Tbsdd	TCf to data output valid	—	—	40	ns	1
Tbsoe	TDO enable time	5	—	—	ns	1, 2, 5
Tbsoz	TDO disable time	—	—	40	ns	1, 2, 6
Tbsde	Data output enable time	5	—	—	ns	1, 4, 7
Tbsdz	Data output disable time	—	—	40	ns	1, 4, 8
Tbsr	Reset period	30	—	—	ns	1
Tbsrs	TMS setup to [TRr]	10	—	—	ns	9
Tberh	TMS hold from [TRr]	10	—	—	ns	9

1. aaa Guaranteed by design.
2. Assumes a 25 pF load on TDO. Output timing derates at 0.072 ns/pF of extra load applied.
3. For correct data latching, the I/O signals (from the core and the pads) must be set up and held with respect to the rising edge of TCK in the CAPTURE-DR state of the SAMPLE/PRELOAD and EXTEST instructions.
4. Assumes that the data outputs are loaded with the AC test loads.
5. TDO enable time applies when the TAP controller enters the Shift-DR or Shift-IR states.
6. TDO disable time applies when the TAP controller leaves the Shift-DR or Shift-IR states
7. Data output enable time applies when the boundary scan logic is used to enable the output drivers.
8. Data output disable time applies when the boundary scan logic is used to disable the output drivers.
9. TCK may be stopped indefinitely in either the low or high phase.

4.4.14 Reset Timing

Table 64 shows the reset timing specifications for CLK_NRESET. The basic reset timing sequence is shown in Figure 27.

Table 64. Reset Timing Specification

Symbol	Parameter [1]	Minimum	Maximum	Unit
^{t}RST	CLK_NRESET, must be asserted prior to VDD being stable.	1	—	ms
^{t}SS	Configuration Strap Pins[2] Setup to NRESET	5		Reference Clock Cycles (REF_CLK)[3]
^{t}HS	Configuration Strap Pins[2] Hold from NRESET	5		Reference Clock Cycles (REF_CLK)[3]

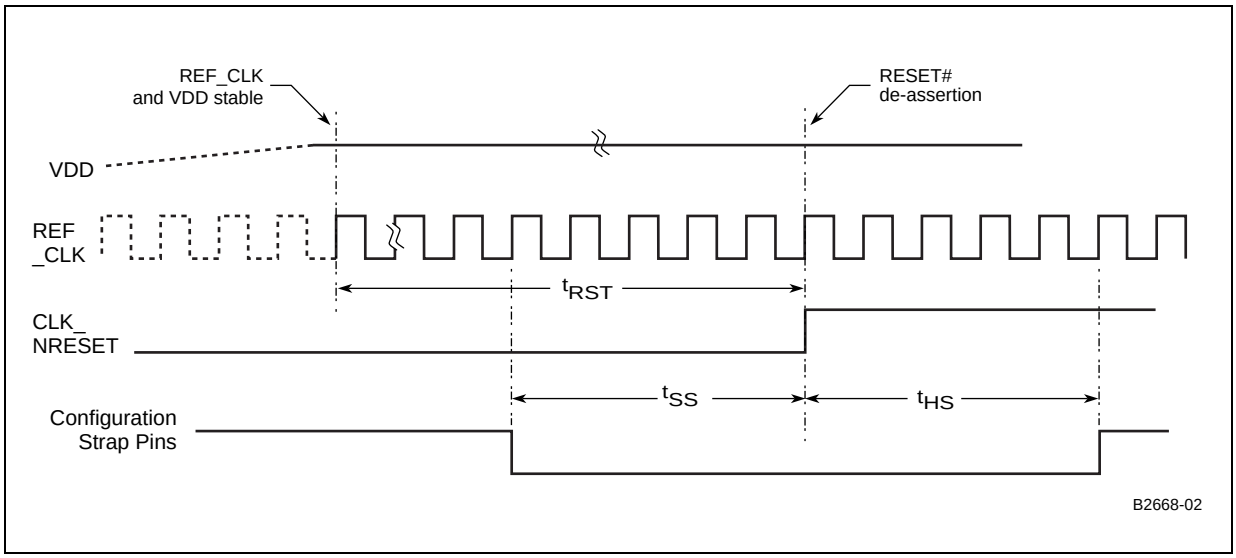
1. Guaranteed by functional testing.

2. This parameter is applicable to all of the configuration pins listed in Section 3.2.11.
3. REF_CLK can be in the range of 75 - 125 MHz, as specified in Table 29 REF_CLK AC Specifications.

When the system is powered up, the bypass clock is sent to all of the units as the chip begins to power up. It will be used to allow a gradual power-up and to begin clocking state elements to remove possible circuit contention. When the PLL gets locked after CLK_NRESET is de-asserted, it will start generating “divide-by-16” clocks for all of the units. A reset from the CLK_NRESET register is also removed at the same time.

The reset sequence shown above is the same in the case when reset happens through the PCI_RST# signal and CFG_RST_DIR is asserted.

Figure 27. Reset Timing



4.4.15 Serial Port

The serial port consists of TXD and RXD, which are asynchronous relative to any device outside of the network processor. The serial port IO buffer DC specifications are the same as the GPIO IO DC buffer specifications.

5.0 Mechanical Specifications

5.1 Package Marking

The IXP2800 network processor package marking is shown in Figure 28, and the IXP2850 network processor package marking is shown in Figure 29.

Product Name	Stepping	QDF Number	Marketing Part Number	Version
RPIXP2800AA	A0	Q424	MM# 848953	1.0 GHz
RPIXP2800AB	A0	Q425	MM# 848954	1.4 GHz
RPIXP2800AA	A1	Q480	MM# 851637	1.0 GHz
RPIXP2800AB	A1	Q481	MM# 851649	1.4 GHz
RPIXP2800AA	A2	Q572	MM# 855314	1.0 GHz
RPIXP2800AB	A2	Q573	MM# 855311	1.4 GHz
RPIXP2800BA	B0	Q668	MM# 857259	1.0 GHz
RPIXP2800BB	B0	Q669	MM# 857266	1.4 GHz
RPIXP2800BA	B1	Q808	MM# 861093	1.0 GHz
RPIXP2800BB	B1	Q809	MM# 861099	1.4 GHz
RPIXP2800BC	B1	Q853	MM# 862906	650 MHz
RPIXP2800BA	B1		MM# 862117[1]	1.0 GHz
RPIXP2800BB	B1		MM# 855650[1]	1.4 GHz
RPIXP2800BC	B1		MM# 862907[1]	650 MHz
RPIXP2850AA	A0	Q454	MM# 850268	1.0 GHz
RPIXP2850AB	A0	Q455	MM# 850269	1.4 GHz
RPIXP2850AA	A1	Q482	MM# 851648	1.0 GHz
RPIXP2850AB	A1	Q483	MM# 851646	1.4 GHz
RPIXP2850AA	A2	Q574	MM# 855312	1.0 GHz
RPIXP2850AB	A2	Q575	MM# 855313	1.4 GHz
RPIXP2850BA	B0	Q670	MM# 858140	1.0 GHz
RPIXP2850BB	B0	Q671	MM# 858141	1.4 GHz
RPIXP2850BA	B1	Q810	MM# 861102	1.0 GHz
RPIXP2850BB	B1	Q811	MM# 861132	1.4 GHz
RPIXP2850BC	B1	Q854	MM# 862908	650 MHz
RPIXP2850BA	B1		MM# 862113[1]	1.0 GHz
RPIXP2850BB	B1		MM# 862114[1]	1.4 GHz
RPIXP2850BC	B1		MM# 862910[1]	650 MHz

1. Production-qualified devices are not marked with a QDF number.

Figure 28. IXP2800 Network Processor Package Marking

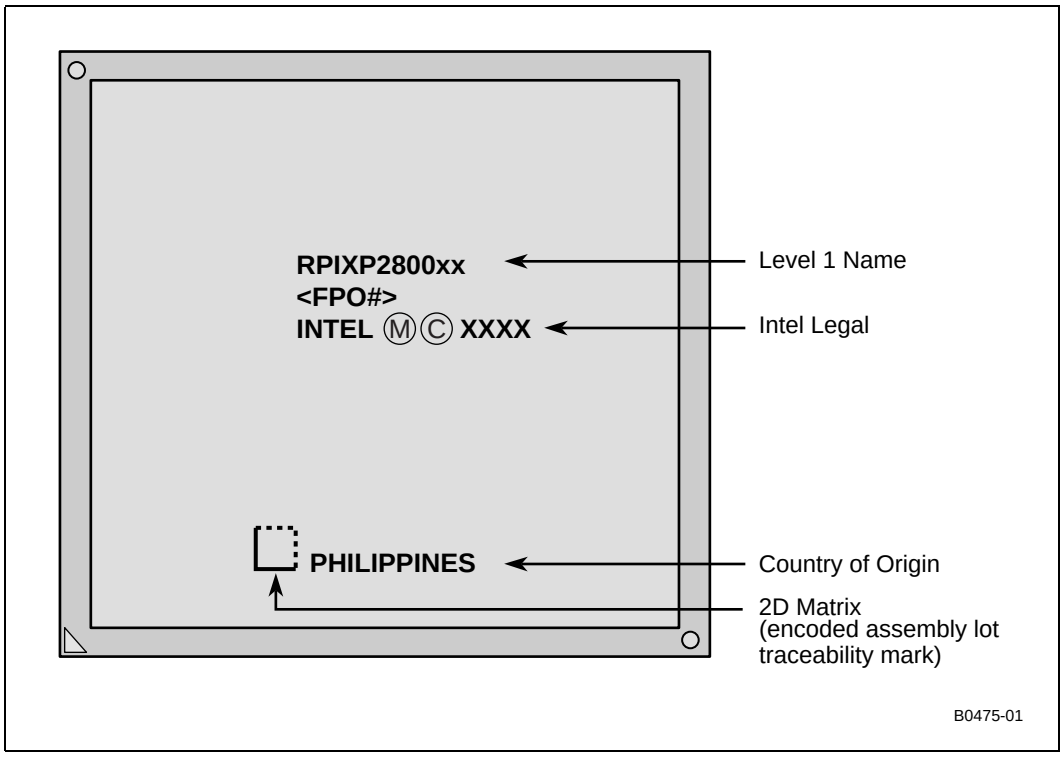
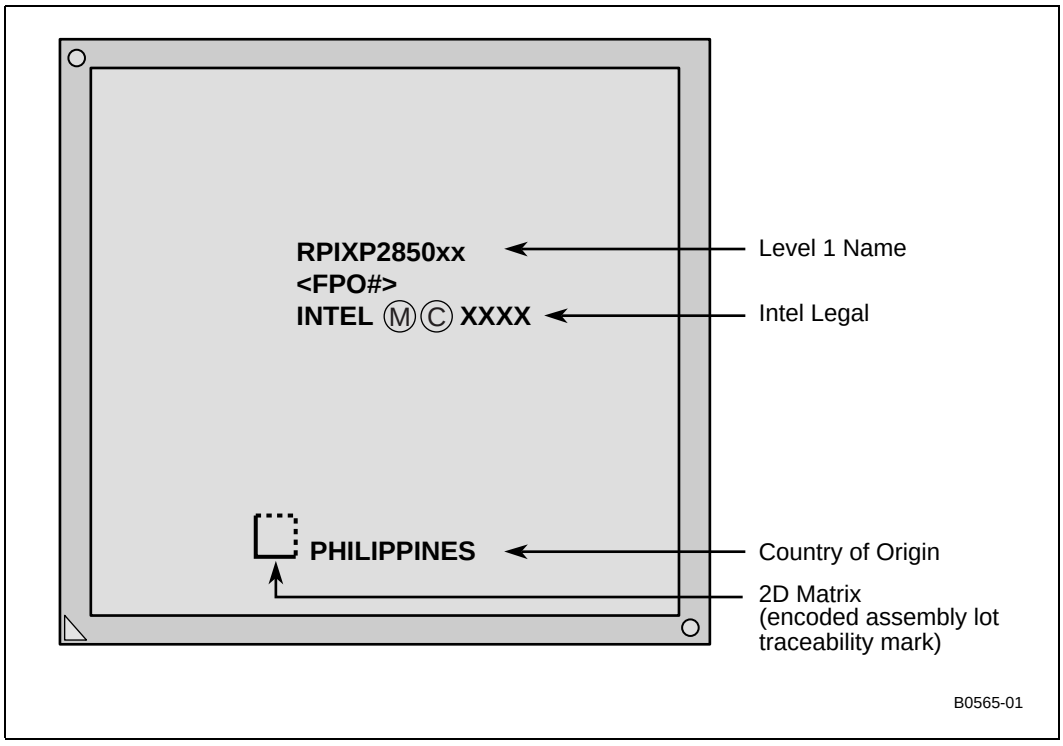


Figure 29. IXP2850 Network Processor Package Marking



5.2 Package Dimensions

The network processor package dimensions are shown in Figure 30, Figure 31, and Figure 32 and detailed in Table 65.

Figure 30. IXP2800/IXP2850 Network Processor Package Ball Grid Array

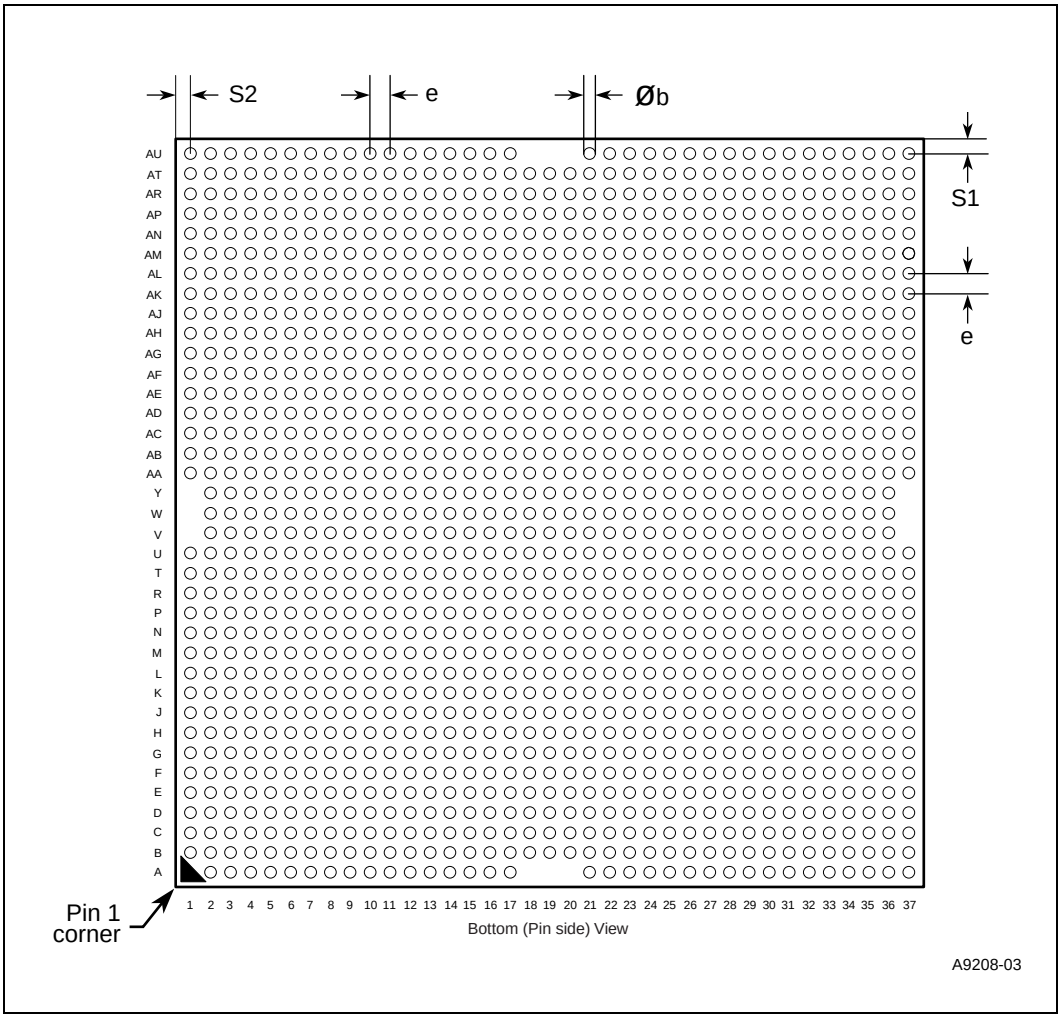


Figure 31. IXP2800/IXP2850 Network Processor Package Top View

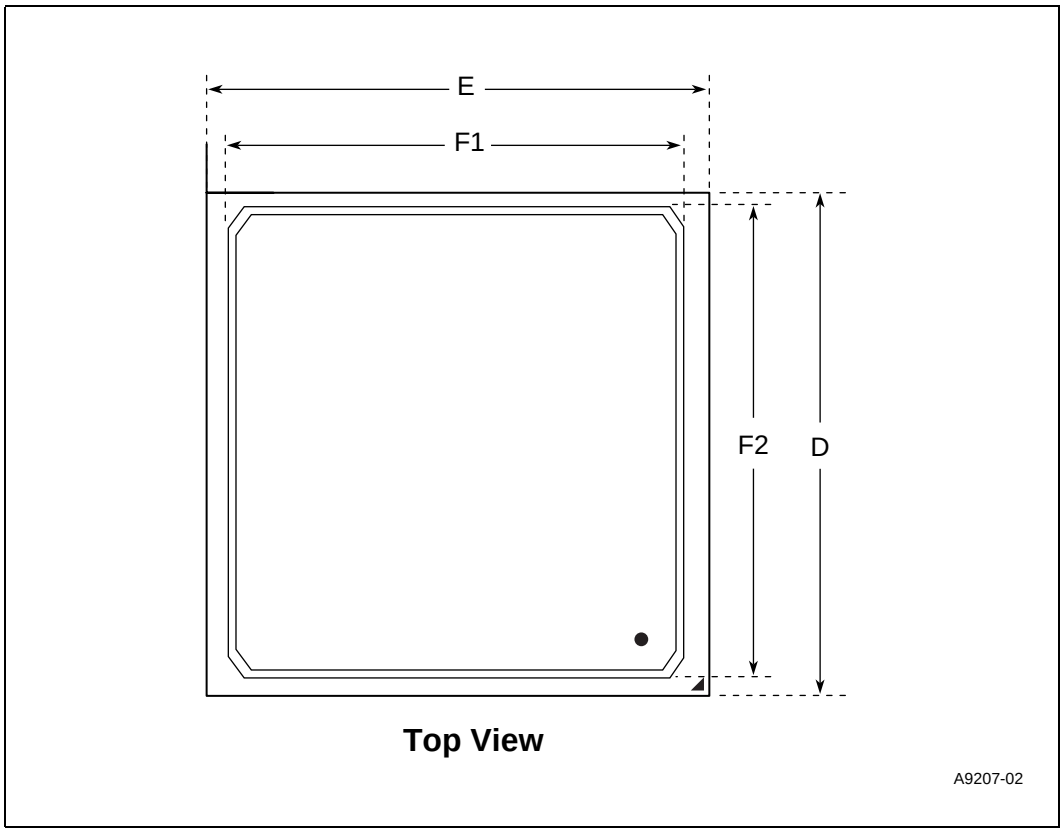


Figure 32. IXP2800/IXP2850 Network Processor Package Side View

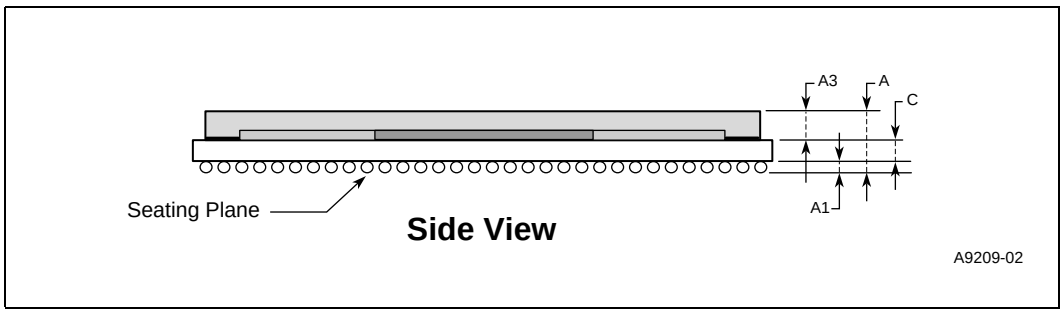


Table 65. IXP2800/IXP2850 Network Processor Package Dimensions

Symbol	Minimum	Maximum
A	3.891	4.565
A1	0.40	0.60
A3	2.266	2.49
b	0.61	
C	1.225	1.475
D	37.45	37.55
E	37.45	37.55
F1	33.4	33.6
F2	33.4	33.6
e	1.00	
S1	0.750	
S2	0.750	
Notes: All dimensions are in millimeters (mm).