82303
LOCAL I/O SUPPORT CHIP

- **High Integration—The 82304, 82303 and 82077 Floppy Disk Controller Replace 50 IC's in IBM Design**
- **Integrated Parallel Port**
- **Integrated Card Setup Port (96H)**
- **Supports System Board Setup**
- **Integrated Peripheral Bus Address Latches**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Package**

The 82303 Local Channel Support Chip, along with its companion chip (the 82304) and the 82077 Floppy Disk Controller, significantly reduce system cost, design effort, and form factor constraints by replacing 50 IC devices in an equivalent IBM system.

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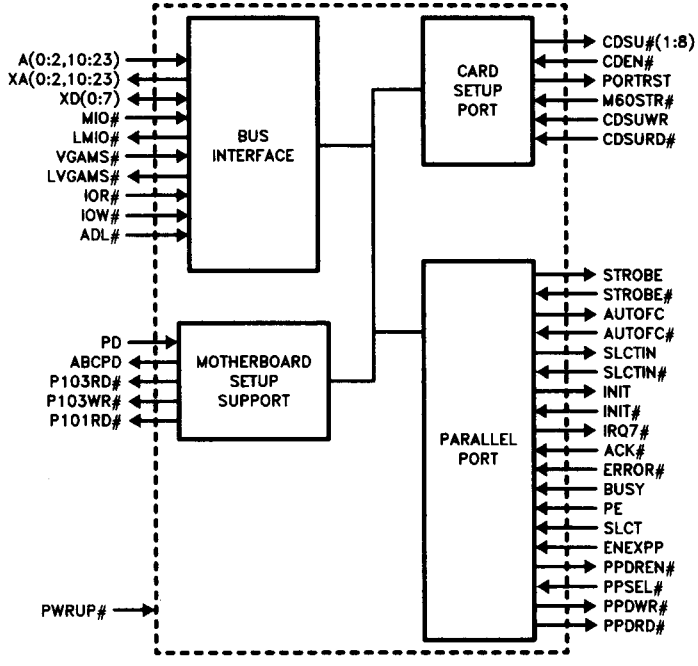
The 82303 integrates most all logic required to implement a parallel port. This port operates either as a standard parallel port or as a Microchannel architecture compatible "extended mode" (bi-directional) port. The 82303 also integrates the Card Setup Port (96H) and several peripheral bus address latches, and provides signals in support of system setup functions.



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Introduction

The 82303 is a high integration device intended for Microchannel compatible system designs. It integrates the Microchannel Card Setup Port, a parallel port, several peripheral bus address latches, and a variety of system board setup functions. The 82303, in conjunction with its sister chip the 82304 and the 82077 Floppy Disk Controller, replaces approximately 50 IC devices in an equivalent IBM system. Included as an appendix to this data sheet is a functional logic diagram of the 82303 that will facilitate understanding of the part. Note that the 82304 and 82303 integrate a variety of system ports. For programming and register level details, please refer to the IBM Technical Reference Manual.

Bus Interface

The Bus Interface unit interfaces the 82303 to the Microchannel and peripheral busses. It inputs the unlatched Microchannel address, latches it for internal use, and makes the latched version available externally for other peripheral bus resources. It also provides additional latches for decodes generated from the Microchannel address.

Parallel Port

The 82303 integrates most all logic required to implement a standard or "extended-mode" parallel port. The only logic not integrated is that which directly drives the physical parallel port connector, specifically one '05 (open collector) inverter package and one '652 data buffer. (This allows the system design to stay clear of directly exposing a VLSI component to an external connector.) The parallel port can serve as LPT1, LPT2, or LPT3, as dictated by the decode received via the input parallel port decode PPSEL#.

Card Setup Port

The 82303 integrates the Card Setup Port (96H), which generates the card setup lines to the individual Microchannel connectors. This port also features a software generated reset capability that resets the Microchannel, serial port, and parallel port independently of the rest of the system.

Motherboard Setup Support

The 82303 generates decoded read/write strobes for system board setup port 103H, and a read strobe for setup port 101H. It also generates a version of the system board POS decode (ABCPD) that is then forwarded to the 82309 Address Bus Controller. Note that other system board setup ports can be easily implemented externally using the same PD (POS Decode) that the 82303 uses.

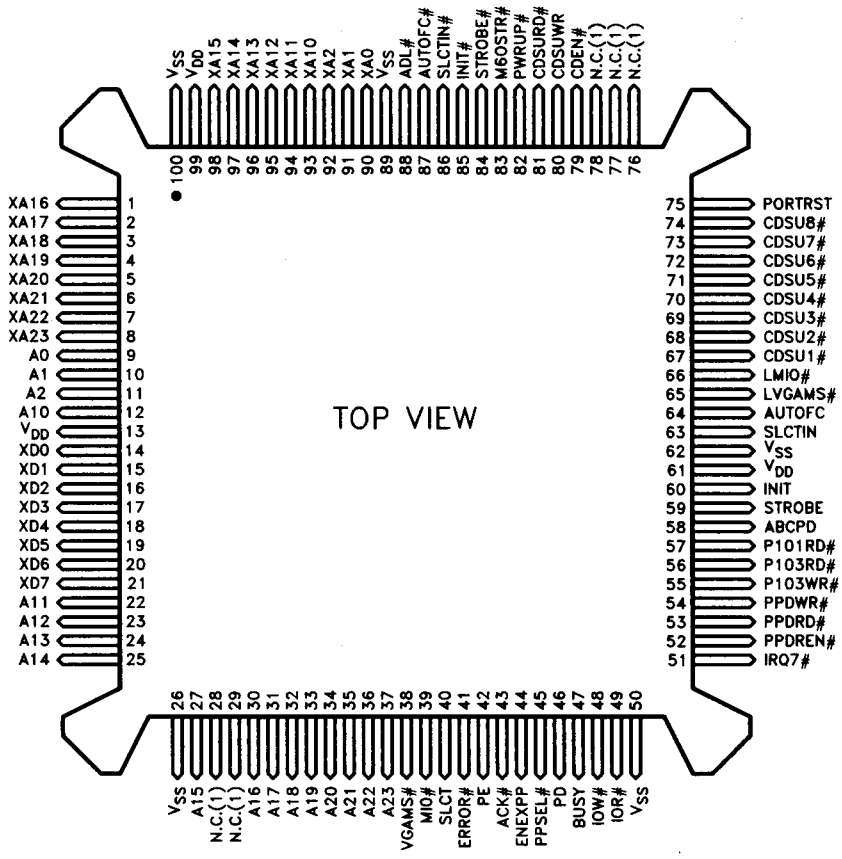
82303 Local Channel Support Chip Pin Definitions

Signal Name	Pin Number	I/O	Description
PWRUP#	82	I	Power-up reset input. Brings 82303 to initial known state.
A[0:2, 10:23]	9–12, 22–25, 27, 30–37	I	Microchannel address inputs. These signals are internally latched. (Note that in systems in which a full 24-bit peripheral address is not required, the upper significant address latches may be used as general purpose decode latches.)
XA[0:2, 10:23]	90–98, 1–8	O	Peripheral Bus Address. These outputs are latched versions of the Microchannel address inputs.
XD[0:7]	14–21	I/O	Bi-directional peripheral data bus.
MIO#	39	I	Microchannel MIO# indicator.
LMIO#	66	O	Latched Microchannel MIO# indicator. The MIO#/LMIO# pin combination may be used as a general purpose latch if LMIO# is not required.
VGAMS#	38	I	VGA memory buffer decode.

82303 Local Channel Support Chip Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
LVGAMS#	65	O	Latched VGA memory buffer decode. The VGAMS#/LVGAMS# pin combination may be used as a general purpose latch if LVGAMS# is not required.
IOR#, IOW#	49, 48	I	82303 read/write strobes.
ADL#	88	I	Microchannel ADL# input.
PD	46	I	POS decode. Decode driven in response to accesses to system board setup Ports 100, 101, 103–107H.
ABCPD	58	O	Address Bus Controller (82309) POS decode. This is simply the PD input gated by an active IOW# signal, and insures that the 82309 does not see a decoding glitch.
P101RD#, P103RD#, P103WR#	57, 56, 55	O	Various system board setup port read/write strobes.
CDSU#[1:8]	67–74	O	Card setup signals to the Microchannel slots.
CDEN#	79	I	Port 100-107H decode used as qualifier for card setup signals.
PORTRST	75	O	Microchannel reset signal. The "OR" of the power-up reset and the reset function built into Port 96H.
M60STR#	83	I	Model 60 strap. When low, the 82303 will drive Port 96H data in either a Port 96 or 97H read. (This is in keeping with the Model 50/60 definition.) When high, the 82303 will remain tri-stated during a Port 97H read.
CDSUWR	80	I	Port 96–97H write strobe.
CDSURD#	81	I	Port 96–97H read strobe.
STROBE, AUTOFC, SLCTIN, INIT	59, 64, 63, 60	O	Parallel port control outputs. These signals are externally buffered with open collector inverters before driving the parallel port connector.
STROBE#, AUTOFC#, SLCTIN#, INIT#	84, 87, 86, 85	I	Parallel port control inputs.
IRQ7#	51	O	Parallel port interrupt request.
ACK#, ERROR#, BUSY, PE, SLCT	43, 41, 47, 42, 40	I	Parallel port status inputs.
ENEXPP	44	I	Enable parallel port extended mode. Allows parallel port to operate bi-directionally.
PPSEL#	45	I	Parallel port chip select.
PPDREN#	52	O	Enables the external '652 parallel port data buffer to be used bi-directionally. This signal is a function of the Control port direction bit (bit 5) and the ENEXPP input.
PPDWR#, PPRD#	54, 53	O	Parallel port data buffer write/read strobes.
V_{DD}	13, 61, 99		Power.
V_{SS}	26, 50, 62, 89, 100		Ground.
N.C.	28, 29, 76, 77, 78		No Connect.

82303 100-Pin PQFP Pinout



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NOTE:
1. N.C. pins must be left not connected.

82303 PARAMETRICS ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to any Pin
with Respect to Ground −0.3V to +(V_{CC} +0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA (Note 1)
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA (Note 2)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA (Note 2)
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	TRI-STATE Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

NOTES:
1. CDSU# [1:8], XA [0:2, 10:23], XD[0:7].
2. All outputs other than those listed in Note 1.

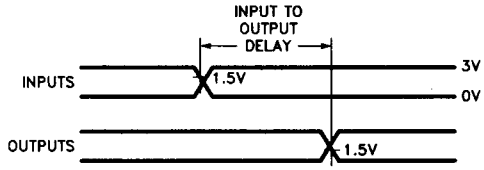
82303 A.C. SPECIFICATIONS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	C_L (pF)	Notes
T_1	PWRUP#, Pulse Width	500			
T_2	IOR#, IOW#, CDSURD#, CDSUWR Pulse Width	170			
T_3	Write Data Setup	25			(Note 1)
T_4	Write Data Hold	10			(Note 2)
T_5	Read Data Valid Delay		60	100	(Note 3)
T_6	Read Data Float Delay		40	100	(Note 5)
T_7	Status Inputs to XD[0:7]		35	100	(Note 6)
T_8	Write Strobe Delays		35	50	(Note 7)
T_9	Read Strobe Delays		40	50	(Note 8)
T_{11}	PPSEL#, PD Setup to IOR#, IOW# ↓	20			
T_{12}	PPSEL#, PD Hold from IOR#, IOW# ↑	5			
T_{13}	XA[0:2, 10:23] DLY from ADL# ↓		35	100	
T_{14}	A[0:2, 10:23], VGAMS#, MIO# Setup to ADL# ↑	30			
T_{17}	CDSU# [1:8] Delay from CDEN#		28	75	
T_{18}	IOR# ↑ to ADL# ↓	30			
T_{19}	LVGAMS#, LMIO# Delay from ADL# ↓		35	50	

NOTES:
1. To IOW# or CDSUWR active, whichever is appropriate.
2. From IOW# or CDSUWR inactive, whichever is appropriate.
3. From IOR# or CDSURD# active, whichever is appropriate.
5. From IOR# or CDSURD# inactive, whichever is appropriate.
6. Parallel port status inputs include SLCT, PE, BUSY, ERROR#, and ACK#.
7. Write strobes include P103WR# and PPDWR#.
8. Read strobes include P103RD#, P101RD#, and PPDRD#.

82303 Drive Levels/Measurement Points for A.C. Specifications

Input/Output Pulse Widths



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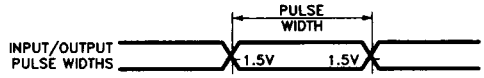

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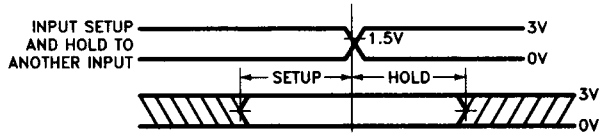
Input Setup and Hold to another Input



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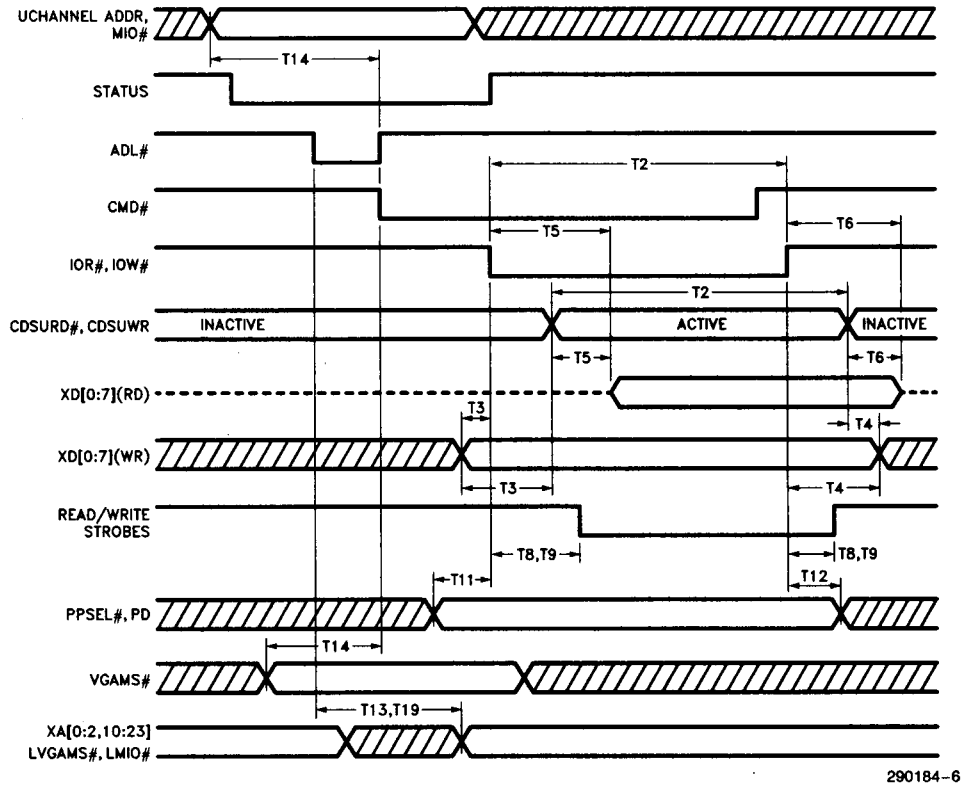
NOTE:
Input Waveforms have $T_R \leq 2.0$ ns from 0.8V to 2.0V.



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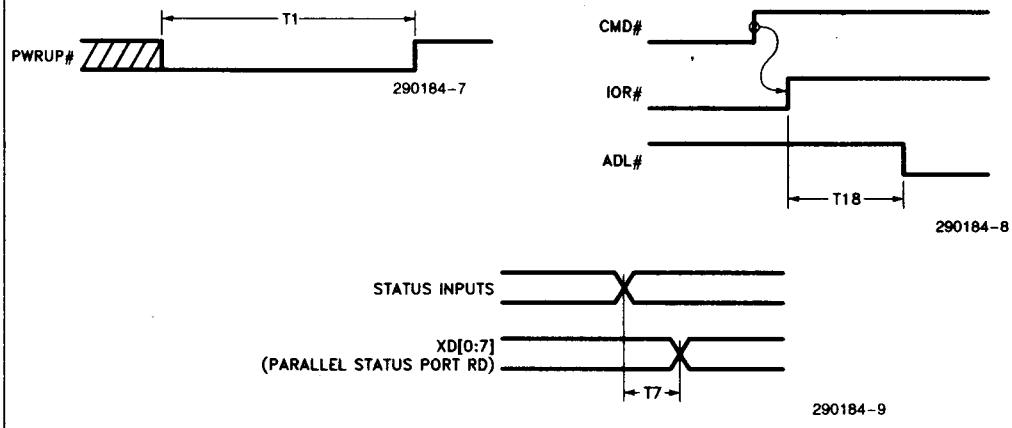
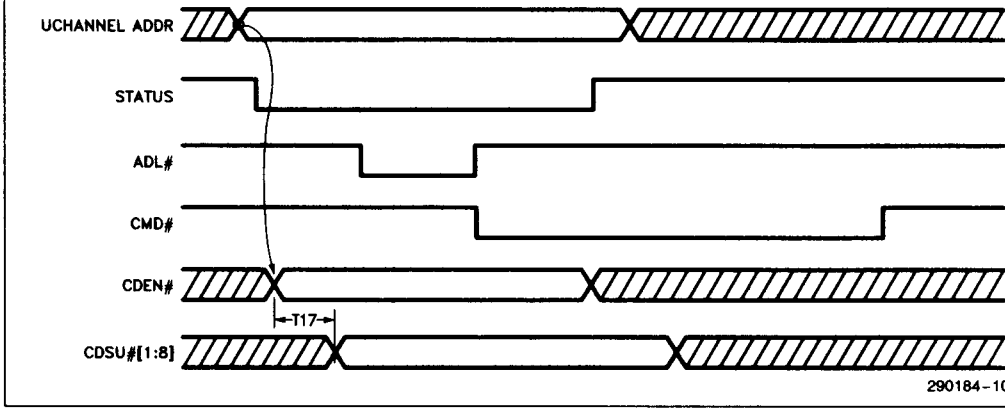
82303 Drive Levels/Measurement Points for A.C. Specifications (Continued)



NOTE:
T7 is the flow through propagation delay, and thus assumes T5A, is not the limiting parameter.



APPENDIX
82303 INTERNAL LOGIC DIAGRAMS

These logic diagrams are provided to aid in understanding the basic functionality of the 82303, and should not be used to estimate signal loading, propagation delays, or any other timing behavior.

The clocked latches in the diagrams are functionally equivalent to 7474 type TTL latches. The transparent latches are equivalent to 74373 type TTL latches except that the gate input is active low rather than active high.

The truth table for the combinatorial PAL is as follows:

RD

PSEL#	IOR#	XA0	XA1	PPDR#	PPCD#	PSR#
0	0	0	0	0	1	1
0	0	0	1	1	0	1
0	0	1	0	1	1	0

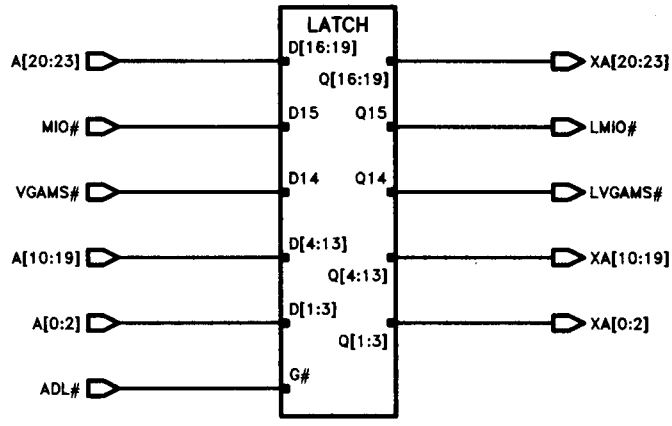
SELPOS	IOR#	XA2	XA1	XA0	POS1R#	POS3R#
1	0	0	0	1	0	1
1	0	0	1	1	1	0

WR

PSEL#	IOW#	XA0	XA1	PPDW#	PSR#
0	0	0	0	0	1
0	0	0	1	1	0

SELPOS	IOW#	XA2	XA1	XA0	POS103W#
1	0	0	1	1	0

Address Latch
Transparent Latch × 19



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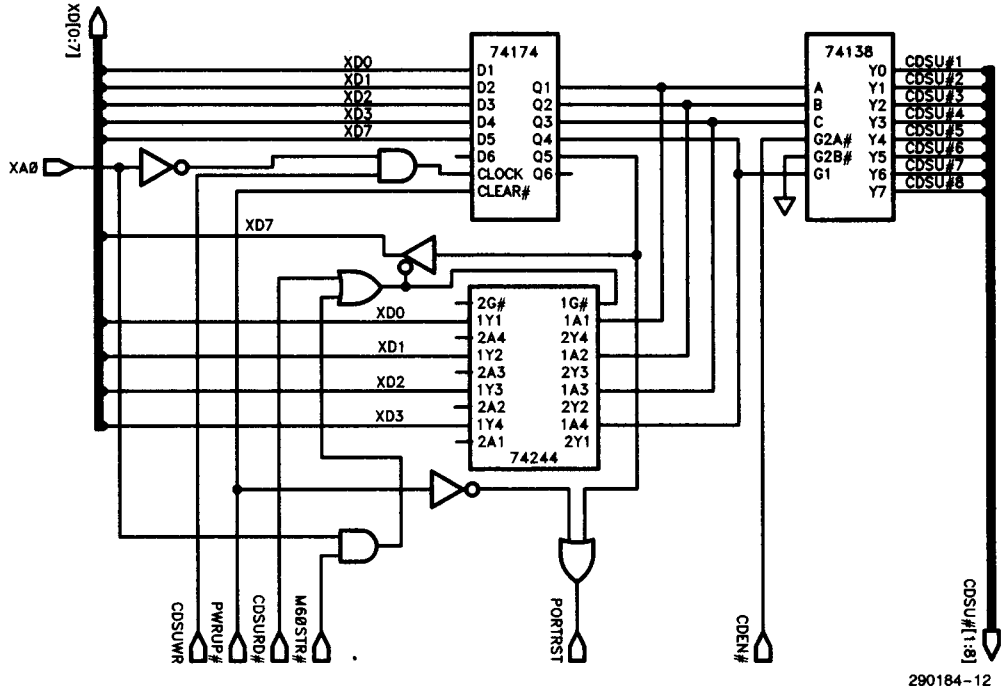
Card Setup Port



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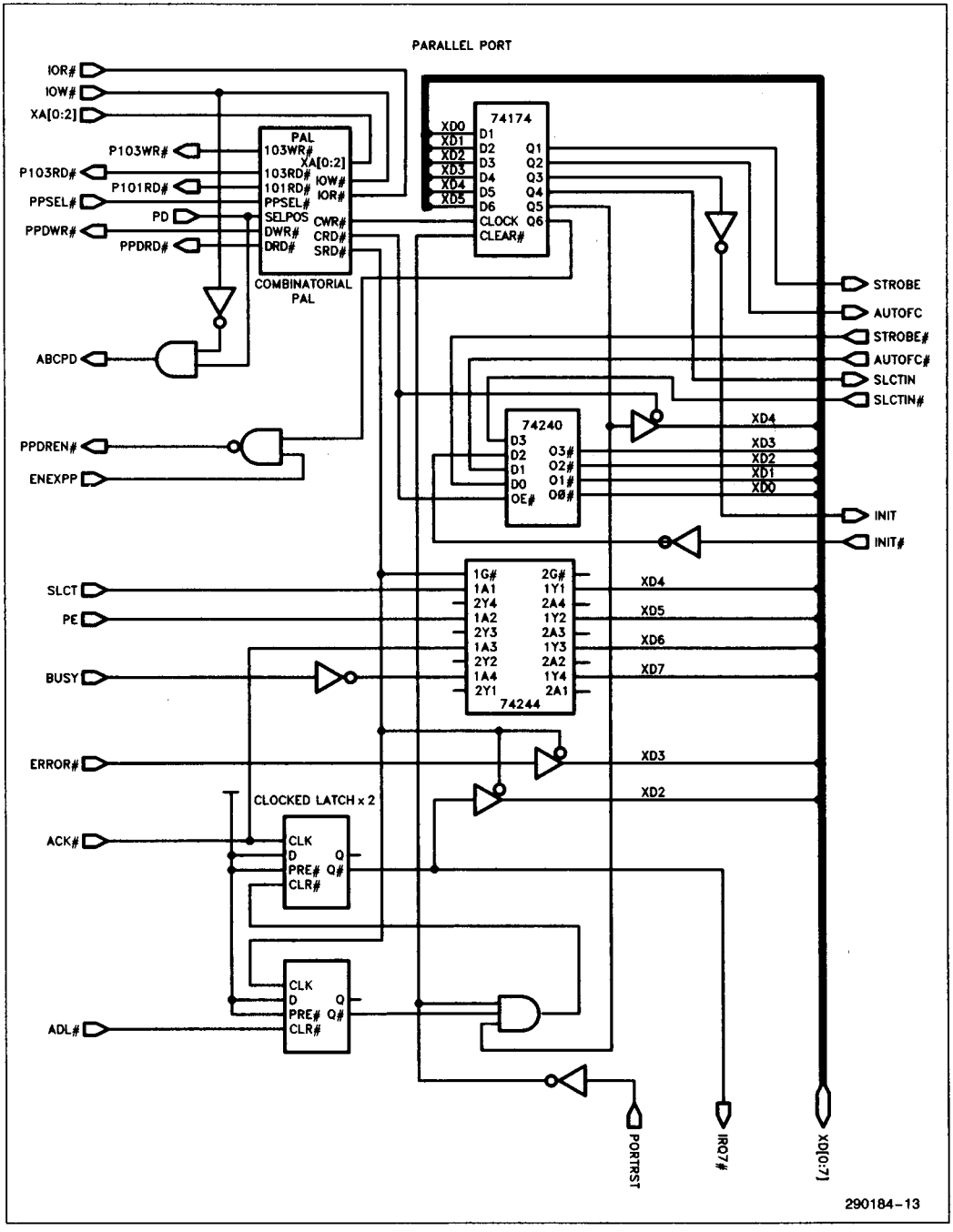
PARALLEL PORT
IOR#
IOW#
XA[0:2]
P103WR#
P103RD#
P101RD#
PPSEL#
PD
PPDWR#
PPDRD#
PAL
103WR#
XA[0:2]
103RD#
IOW#
101RD#
IOR#
PPSEL#
SELPOS
CWR#
DWR#
CRD#
DRD#
SRD#
COMBINATORIAL PAL
ABCPD
PPDREN#
ENEXPP
74174
XD0
XD1
XD2
XD3
XD4
XD5
D1
D2
D3
D4
D5
D6
CLOCK
CLEAR#
Q1
Q2
Q3
Q4
Q5
Q6
74240
D3
D2
D1
D0
OE#
O3#
O2#
O1#
O0#
XD4
XD3
XD2
XD1
XD0
STROBE
AUTOFC
STROBE#
AUTOFC#
SLCTIN
SLCTIN#
INIT
INIT#
SLCT
PE
BUSY
ERROR#
ACK#
ADL#
1G#
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
2G#
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
74244
XD4
XD5
XD6
XD7
XD3
XD2
CLOCKED LATCH x 2
CLK
D
PRE#
CLR#
Q
Q#
PORTRST
IRQ7#
XD[0:7]
290184-13