REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	35	36	37	38															
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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DRAWING APPROVAL DATE
97-02-05

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, 32-BIT MICROPROCESSOR
MONOLITHIC SILICON

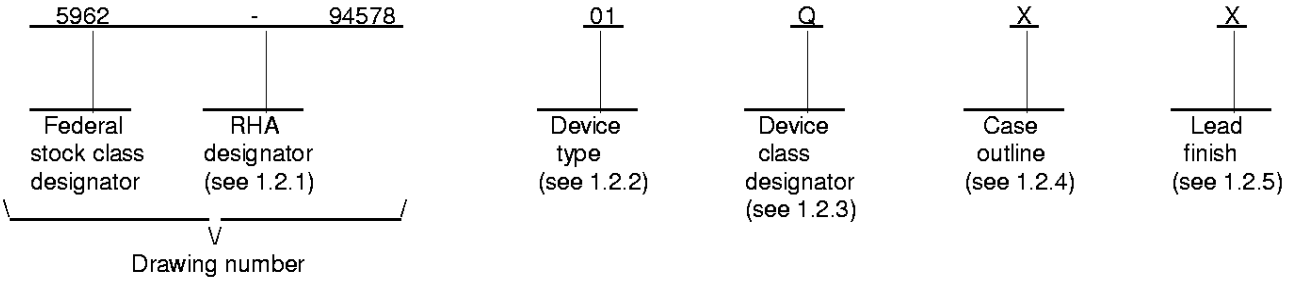
SIZE	CAGE CODE	
A	**67268**	**5962-94578**

SHEET 1 OF 38

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Temperature Range	Speed
01	80502	32-bit Microprocessor	-55°C to +125°C	50/100 MHz
02	80502	32-bit Microprocessor	-40°C to +110°C	50/100 MHz
03	80502	32-bit Microprocessor	-40°C to +85°C	50/100 MHz
04	80502	32-bit Microprocessor	-55°C to +125°C	60/120 MHz
05	80502	32-bit Microprocessor	-40°C to +110°C	60/120 MHz
06	80502	32-bit Microprocessor	-40°C to +85°C	60/120 MHz
07	80502	32-bit Microprocessor	-55°C to +125°C	66/133 MHz
08	80502	32-bit Microprocessor	-40°C to +110°C	66/133 MHz
09	80502	32-bit Microprocessor	-40°C to +85°C	66/133 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figures 1	296	Staggered Pin Grid Array

1/ Any device outside the traditional performance environment; e.g., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/

Storage Temperature Range	-65°C to +150°C
Case Temperature Under Bias	-65°C to +125°C
3 V Supply Voltage with respect to Ground	-0.5 V dc to +4.1 V dc
3 V Only Buffer Input Voltage with respect to Ground	-0.5 V dc to Vcc + 0.5 V dc (not to exceed 4.6 V)
5V Safe Buffer Input Voltage with respect to Ground	-0.5 V dc to 6.5 V dc
Lead Temperature (soldering 10 seconds)	300°C
Thermal Resistance, Junction-to-case (θ_{JC}): Case X	1.7°C/W 3/
Thermal Resistance, Junction-to-ambient (θ_{JA}): Case X	16.2°C/W 3/ 4/

1.4 Recommended operating conditions.

Case Operating Temperature Range	
device type 01, 04 and 07	-55°C to +125°C
device type 02, 05 and 08	-40°C to +110°C
device type 03, 06 and 09	-40°C to +85°C
Supply Voltage, V_{CC3}	3.135 V dc < V_{CC} < 3.465 V dc
Supply Voltage, V_{CC2}	2.935 V dc < V_{CC} < 3.265 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	97.6 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Without heat sink.
4/ Zero airflow.

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Waveform. The waveform shall be as specified on figure 4.

3.2.5 Boundary Scan Instruction Codes. For all devices the boundary scan instruction codes shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL3}	TTL level Applies to all signals except CLK and PICCLK	1,2,3	All	-0.3	0.8	V
Input high voltage	V_{IH3}		1,2,3	All	2.0	V_{CC}+0.3	
Input low voltage (5 V)	V_{IL5}	TTL level;measured at 4mA Applies to CLK and PICCLK only	1,2,3	All	-0.3	0.8	
Input high voltage (5 V)	V_{IH5}		1,2,3	All	2.0	5.55	
Output low voltage	V_{OL3}	Measured at 4 mA. Applies to CLK and PICCLK only	1,2,3	All		0.4	
Output high voltage	V_{OH3}	Measured at 3 mA. Applies to CLK and PICCLK only	1,2,3	All	2.4		
Input leakage current	I_{LI}	$0 < V_{IN} < = V_{CC3}$ (only for inputs without pullups or pulldowns)	1,2,3	All		+/-15	µA
Output leakage current	I_{LO}	$0 < V_{OUT} < = V_{CC3}$ 3-state (only for inputs without pullups or pulldowns)	1,2,3	All		+/-15	
Input leakage current	I_{IH}	$V_{IN} < = 2.4$ V (only for inputs with pulldowns)	1,2,3	All		200	
Output leakage current	I_{IL}	$V_{IN} < = 0.4$ V (only for inputs with pullups)	1,2,3	All		-400	
Supply current	I_{CC3}	100 MHz, 3.465 V 2/	1,2,3	01,02,03		170	mA
		120 MHz, 3.465 V 2/		04,05,06		220	
		133 MHz, 3.465 V 2/		07,08.09		255	
Supply current	I_{CC2}	100 MHz, 3.265 V 2/	1,2,3	01,02,03		1885	mA
		120 MHz, 3.265 V 2/		04,05,06		2300	
		133 MHz, 3.265 V 2/		07,08,09		2575	
Capacitance input	C_{IN}	See 4.4.1c	4	All		15	pF
Capacitance output	C_O		4	All		20	
Capacitance I/O	$C_{I/O}$		4	All		25	
Capacitance CLK input	C_{CLK}		4	All		15	
Capacitance test input	C_{TIN}		4	All		15	
Capacitance test output	C_{TOUT}		4	All		20	
Capacitance test clock	C_{TCK}		4	All		15	
Functional tests		See 4.4.1b	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Frequency		Max. core freq. = 100 MHz at 1/2	9,10,11	01-03	25	50	MHz
CLK period	t_{1a}		9,10,11	01-03	20	40	ns
CLK period stability	t_{1b}	3/ 4/	9,10,11	01-03		±250	ps
CLK high time	t_2	V_{IN} = 2 V 3/	9,10,11	01-03	4.0		ns
CLK low time	t_3	V_{IN} = 0.8 V 3/	9,10,11	01-03	4.0		
CLK fall time	t_4	V_{IN} = 2.0 V - 0.8 V 3/ 5/	9,10,11	01-03	0.15	1.5	
CLK rise time	t_5	V_{IN} = 2.0 V - 0.8 V 3/ 5/	9,10,11	01-03	0.15	1.5	
$\overline{ADS}$, PWT, PCD, $\overline{BEO-7}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{CACHE}$, SCYC, W/$\overline{R}$, valid delay	t_{6a}		9,10,11	01-03	1.0	7.0	
AP valid delay	t_{6b}		9,10,11	01-03	1.0	8.5	
A3-A31, $\overline{LOCK}$ valid delay	t_{6c}		9,10,11	01-03	1.1	7.0	
$\overline{ADS}$, AP, A3-A31, PWT, PCD, $\overline{BEO-7}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{CACHE}$, SCYC, $\overline{LOCK}$ float delay	t_7	3/	9,10,11	01-03		10.0	
$\overline{APCHK}$, $\overline{TERR}$, $\overline{FERR}$, $\overline{PCHK}$ valid delay	t_8	6/	9,10,11	01-03	1.0	8.3	
BREQ, HLDA, $\overline{SMIACT}$ valid delay	t_{9a}	6/	9,10,11	01-03	1.0	8.0	
$\overline{HIT}$ valid delay	t_{10a}		9,10,11	01-03	1.0	8.0	
$\overline{HITM}$ valid delay	t_{10b}		9,10,11	01-03	1.1	6.0	
PM0-1, BPO-3 valid delay	t_{11a}		9,10,11	01-03	1.0	10.0	
PRDY valid delay	t_{11b}		9,10,11	01-03	1.0	8.0	
D0-D63, DPO-7 write data valid delay	t_{12}		9,10,11	01-03	1.3	8.5	
D0-D63, DPO-3 write data float delay	t_{13}	3/	9,10,11	01-03		10.0	
A5-A31 setup time	t_{14}	7/	9,10,11	01-03	6.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 3.135 V $\le V_{CC3} \le$ 3.465 V 2.935 V $\le V_{CC2} \le$ 3.265 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
A5-A31 hold time	t_{15}		9,10,11	01-03	1.0		ns
INV, AP setup time	t_{16a}		9,10,11	01-03	5.0		
EADS setup time	t_{16b}		9,10,11	01-03	6.0		
EADS, INV, AP hold time	t_{17}		9,10,11	01-03	1.0		
KEN setup time	t_{18a}		9,10,11	01-03	5.0		
NA, WB/WT setup time	t_{18b}		9,10,11	01-03	4.5		
KEN, WB/WT, NA hold time	t_{19}		9,10,11	01-03	1.0		
BRDY, setup time	t_{20}		9,10,11	01-03	5.0		
BRDY, hold time	t_{21}		9,10,11	01-03	1.0		
BOFF setup time	t_{22}		9,10,11	01-03	5.5		
AHOLD setup time	t_{22a}		9,10,11	01-03	6.0		
AHOLD, BOFF hold time	t_{23}		9,10,11	01-03	1.0		
BUSCHK, EWBE, HOLD, PEN setup time	t_{24}		9,10,11	01-03	5.0		
BUSCHK, EWBE, PEN hold time	t_{25}		9,10,11	01-03	1.0		
HOLD hold time	t_{25a}		9,10,11	01-03	1.5		
A20M, INTR, STPCLK setup time	t_{26}	8/ 9/	9,10,11	01-03	5.0		
A20M, INTR, STPCLK hold time	t_{27}	10/	9,10,11	01-03	1.0		
INIT, FLUSH, NMI, SMI, IGNNE setup time	t_{28}	8/ 9/ 11/	9,10,11	01-03	5.0		
INIT, FLUSH, NMI, SMI, IGNNE hold time	t_{29}	10/	9,10,11	01-03	1.0		
INIT, FLUSH, NMI, SMI, IGNNE pulse width, async	t_{30}	11/ 12/	9,10,11	01-03	2.0		CLKs
R/S setup time	t_{31}	8/ 9/ 11/	9,10,11	01-03	5.0		ns
R/S hold time	t_{32}	10/	9,10,11	01-03	1.0		
R/S pulse width, async	t_{33}	11/ 12/	9,10,11	01-03	2.0		CLKs
D0-D63, DP0-7 read data setup time	t_{34}		9,10,11	01-03	3.8		ns
D0-D63, DP0-7 read data hold time	t_{35}		9,10,11	01-03	1.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RESET setup time	t_{36}	8/ 9/ 13/	9,10,11	01-03	5.0		ns
RESET hold time	t_{37}	10/ 13/	9,10,11	01-03	1.0		
RESET pulse width, V_{CC} and CLK stable	t_{38}	11/ 13/	9,10,11	01-03	15		CLKs
RESET active after V_{CC} and CLK stable	t_{39}	Power up	9,10,11	01-03	1.0		ms
Reset configuration signals (INIT, FLUSH) setup time	t_{40}	8/ 9/ 11/	9,10,11	01-03	5.0		ns
Reset configuration signals (INIT, FLUSH) hold time	t_{41}	10/	9,10,11	01-03	1.0		
Reset configuration signals (INIT, FLUSH,) setup time, async	t_{42a}	To RESET falling edge 9/	9,10,11	01-03	2.0		CLKs
Reset configuration signals (INIT, FLUSH, BUSCHK, BRDY) hold time, async	t_{42b}	To RESET falling edge 14/	9,10,11	01-03	2.0		
Reset configuration signals (BRDY, BUSCHK) setup time, async	t_{42c}	To RESET falling edge 14/	9,10,11	01-03	3.0		
Reset configuration signals BRDY hold time, RESET driven synchronously	t_{42d}	To RESET falling edge 3/ 14/	9,10,11	01-03	1.0		ns
BF, CPUTYP setup time	t_{43a}	To RESET falling edge 15/	9,10,11	01-03	1.0		ms
BF, CPUTYP hold time	t_{43b}	To RESET falling edge 15/	9,10,11	01-03	2.0		CLKs
TCK frequency	t_{44}		9,10,11	01-03		16.0	MHz
TCK period	t_{45}		9,10,11	01-03	62.5		ns
TCK high time	t_{46}	V_{IN} = 2 V 3/	9,10,11	01-03	25.0		
TCK low time	t_{47}	V_{IN} = 0.8 V 3/	9,10,11	01-03	25.0		
TCK fall time	t_{48}	V_{IN} = 2.0 V -0.8 V 3/ 16/ 17/	9,10,11	01-03		5.0	
TCK rise time	t_{49}	V_{IN} = 2.0 V -0.8 V 3/ 16/ 17/	9,10,11	01-03		5.0	
TRST pulse width	t_{50}	Asynchronous 3/	9,10,11	01-03	40.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TDI, TMS setup time	t_{51}	18/	9,10,11	01-03	5.0		ns
TDI, TMS hold time	t_{52}	18/	9,10,11	01-03	13.0		
TDO valid delay	t_{53}	16/	9,10,11	01-03	3.0	20.0	
TDO float delay	t_{54}	3/ 16/	9,10,11	01-03		25.0	
All nontest outputs valid delay	t_{55}	16/ 19/ 20/	9,10,11	01-03	3.0	20.0	
All nontest outputs float delay	t_{56}	3/ 16/ 19/ 20/	9,10,11	01-03		25.0	
All nontest inputs setup time	t_{57}	18/ 19/ 20/	9,10,11	01-03	5.0		
All nontest inputs hold time	t_{58}	18/ 19/ 20/	9,10,11	01-03	13.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Frequency			9,10,11	04-06	30	60	MHz
CLK period	t_{1a}		9,10,11	04-06	16.67	33.33	ns
CLK period stability	t_{1b}	Adjacent clocks 3/ 4/	9,10,11	04-06		±250	ps
CLK high time	t_2	V_{IN} = 2 V 3/	9,10,11	04-06	4.0		ns
CLK low time	t_3	V_{IN} = 0.8 V 3/	9,10,11	04-06	4.0		
CLK fall time	t_4	V_{IN} = 2.0 V - 0.8 V 3/ 5/	9,10,11	04-06	0.15	1.5	
CLK rise time	t_5	V_{IN} = 2.0 V - 0.8 V 3/ 5/	9,10,11	04-06	0.15	1.5	
$\overline{ADS}$, PWT, PCD, $\overline{BEO}$-7, M/$\overline{IO}$, D/$\overline{C}$, $\overline{CACHE}$, SCYC, W/$\overline{R}$, valid delay	t_{6a}		9,10,11	04-06	1.0	7.0	
AP valid delay	t_{6b}		9,10,11	04-06	1.0	8.5	
$\overline{LOCK}$ valid delay	t_{6c}		9,10,11	04-06	1.1	7.0	
A3-A31 valid delay	t_{6e}		9,10,11	04-06	1.1	6.3	
$\overline{ADS}$, AP, A3-A31, PWT, PCD, $\overline{BEO}$-7, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{CACHE}$, SCYC, $\overline{LOCK}$ float delay	t_7	3/	9,10,11	04-06		10.0	
$\overline{APCHK}$, $\overline{TERR}$, $\overline{FERR}$, valid delay	t_{8a}	6/	9,10,11	04-06	1.0	8.3	
$\overline{PCHK}$ valid delay	t_{8b}	6/	9,10,11	04-06	1.0	7.0	
BREQ, HLDA, valid delay	t_{9a}	6/	9,10,11	04-06	1.0	8.0	
$\overline{SMIACT}$ valid delay	t_{9b}		9,10,11	04-06	1.0	7.6	
$\overline{HIT}$ valid delay	t_{10a}		9,10,11	04-06	1.0	8.0	
$\overline{HITM}$ valid delay	t_{10b}		9,10,11	04-06	1.1	6.0	
PM0-1, BPO-3 valid delay	t_{11a}		9,10,11	04-06	1.0	10.0	
PRDY valid delay	t_{11b}		9,10,11	04-06	1.0	8.0	
D0-D63, DPO-7 write data valid delay	t_{12}		9,10,11	04-06	1.3	7.5	
D0-D63, DPO-3 write data float delay	t_{13}	3/	9,10,11	04-06		10.0	
A5-A31 setup time	t_{14}	7/	9,10,11	04-06	6.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
A5-A31 hold time	t_{15}		9,10,11	04-06	1.0		ns
INV, AP setup time	t_{16a}		9,10,11	04-06	5.0		
EADS setup time	t_{16b}		9,10,11	04-06	5.5		
EADS, INV, AP hold time	t_{17}		9,10,11	04-06	1.0		
KEN setup time	t_{18a}		9,10,11	04-06	5.0		
NA, WB/WT setup time	t_{18b}		9,10,11	04-06	4.5		
KEN, WB/WT NA hold time	t_{19}		9,10,11	04-06	1.0		
BRDY, setup time	t_{20}		9,10,11	04-06	5.0		
BRDY, hold time	t_{21}		9,10,11	04-06	1.0		
BOFF, AHOLD setup time	t_{22}		9,10,11	04-06	5.5		
AHOLD BOFF hold time	t_{23}		9,10,11	04-06	1.0		
BUSCHK, EWBE, HOLD, PEN setup time	t_{24}		9,10,11	04-06	5.0		
BUSCHK, EWBE, PEN hold time	t_{25}		9,10,11	04-06	1.0		
HOLD hold time	t_{25a}		9,10,11	04-06	1.5		
A20M INTR, STPCLK setup time	t_{26}	8/ 9/	9,10,11	04-06	5.0		
A20M INTR, STPCLK hold time	t_{27}	10/	9,10,11	04-06	1.0		
INIT, FLUSH, NMI, SMI, TGNNE setup time	t_{28}	8/ 9/ 11/	9,10,11	04-06	5.0		
INIT, FLUSH, NMI, SMI, TGNNE hold time	t_{29}	10/	9,10,11	04-06	1.0		
INIT, FLUSH, NMI, SMI, TGNNE pulse width, async	t_{30}	11/ 12/	9,10,11	04-06	2.0		CLKs
R/S setup time	t_{31}	8/ 9/ 11/	9,10,11	04-06	5.0		ns
R/S hold time	t_{32}	10/	9,10,11	04-06	1.0		
R/S pulse width, async	t_{33}	11/ 12/	9,10,11	04-06	2.0		CLKs
D0-D63, DP0-7 read data setup time	t_{34}		9,10,11	04-06	3.0		ns
D0-D63, DP0-7 read data hold time	t_{35}		9,10,11	04-06	1.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RESET setup time	t_{36}	8/ 9/ 13/	9,10,11	04-06	5.0		ns
RESET hold time	t_{37}	10/ 13/	9,10,11	04-06	1.0		
RESET pulse width, V_{CC} and CLK stable	t_{38}	11/ 13/	9,10,11	04-06	15		CLKs
RESET active after V_{CC} and CLK stable	t_{39}	Power up	9,10,11	04-06	1.0		ms
Reset configuration signals (INIT, FLUSH) setup time	t_{40}	8/ 9/ 11/	9,10,11	04-06	5.0		ns
Reset configuration signals (INIT, FLUSH) hold time	t_{41}	10/	9,10,11	04-06	1.0		
Reset configuration signals (INIT, FLUSH) setup time, async	t_{42a}	To RESET falling edge 9/	9,10,11	04-06	2.0		CLKs
Reset configuration signals (INIT, FLUSH BUSCHK, BRDY) hold time, async	t_{42b}	To RESET falling edge 14/	9,10,11	04-06	2.0		
Reset configuration signals ($\overline{BUSCHK}$, $\overline{BRDY}$) setup time, async	t_{42c}	To RESET falling edge 14/	9,10,11	04-06	3.0		
Reset configuration signals $\overline{BRDY}$ hold time, RESET driven synchronously	t_{42d}	To RESET falling edge 3/ 14/	9,10,11	04-06	1.0		ns
BF setup time	t_{43a}	To RESET falling edge 15/	9,10,11	04-06	1.0		ms
BF hold time	t_{43b}	To RESET falling edge 15/	9,10,11	04-06	2.0		CLKs
TCK frequency	t_{44}		9,10,11	04-06		16.0	MHz
TCK period	t_{45}		9,10,11	04-06	62.5		ns
TCK high time	t_{46}	V_{IN} = 2 V 3/	9,10,11	04-06	25.0		
TCK low time	t_{47}	V_{IN} = 0.8 V 3/	9,10,11	04-06	25.0		
TCK fall time	t_{48}	V_{IN} = 2.0 V -0.8 V 3/ 16/ 17/	9,10,11	04-06		5.0	
TCK rise time	t_{49}	V_{IN} = 2.0 V -0.8 V 3/ 16/ 17/	9,10,11	04-06		5.0	
$\overline{TRST}$ pulse width	t_{50}	Asynchronous 3/	9,10,11	04-06	40.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TDI, TMS setup time	t_{51}	18/	9,10,11	04-06	5.0		ns
TDI, TMS hold time	t_{52}	18/	9,10,11	04-06	13.0		
TDO valid delay	t_{53}	16/	9,10,11	04-06	3.0	20.0	
TDO float delay	t_{54}	3/ 16/	9,10,11	04-06		25.0	
All nontest outputs valid delay	t_{55}	16/ 19/ 20/	9,10,11	04-06	3.0	20.0	
All nontest outputs float delay	t_{56}	3/ 16/ 19/ 20/	9,10,11	04-06		25.0	
All nontest inputs setup time	t_{57}	18/ 19/ 20/	9,10,11	04-06	5.0		
All nontest inputs hold time	t_{58}	18/ 19/ 20/	9,10,11	04-06	13.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Frequency			9,10,11	07-09	33.33	66.6	MHz
CLK period	t_{1a}		9,10,11	07-09	15.0	30.0	ns
CLK period stability	t_{1b}	Adjacent clocks 3/ 4/	9,10,11	07-09		±250	ps
CLK high time	t_2	V_{IN} = 2 V 3/	9,10,11	07-09	4.0		ns
CLK low time	t_3	V_{IN} = 0.8 V 3/	9,10,11	07-09	4.0		
CLK fall time	t_4	V_{IN} = 2.0 V - 0.8 V 3/ 5/	9,10,11	07-09	0.15	1.5	
CLK rise time	t_5	V_{IN} = 2.0 V - 0.8 V 3/ 5/	9,10,11	07-09	0.15	1.5	
$\overline{ADSC}$, PWT, PCD, $\overline{BEO-7}$, $\overline{CACHE}$, SCYC, W/$\overline{R}$, valid delay	t_{6a}		9,10,11	07-09	1.0	7.0	
AP valid delay	t_{6b}		9,10,11	07-09	1.0	8.5	
$\overline{LOCK}$ valid delay	t_{6c}		9,10,11	07-09	1.1	7.0	
$\overline{ADS}$, valid delay	t_{6d}		9,10,11	07-09	1.0	6.0	
A3-A31 valid delay	t_{6e}		9,10,11	07-09	1.1	6.3	
M/$\overline{IO}$ valid delay	t_{6f}		9,10,11	07-09	1.0	5.9	
$\overline{ADS}$, AP, A3-A31, PWT, PCD, $\overline{BEO-7}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{CACHE}$, SCYC, $\overline{LOCK}$ float delay	t_7	3/	9,10,11	07-09		10.0	
$\overline{APCHK}$, $\overline{TERR}$, $\overline{FERR}$, valid delay	t_{8a}	6/	9,10,11	07-09	1.0	8.3	
$\overline{PCHK}$ valid delay	t_{8b}	6/	9,10,11	07-09	1.0	7.0	
BREQ, valid delay	t_{9a}	6/	9,10,11	07-09	1.0	8.0	
$\overline{SMIACT}$ valid delay	t_{9b}	6/	9,10,11	07-09	1.0	7.3	
HLDA valid delay	t_{9c}		9,10,11	07-09	1.0	6.8	
$\overline{HIT}$ valid delay	t_{10a}		9,10,11	07-09	1.0	6.8	
$\overline{HITM}$ valid delay	t_{10b}		9,10,11	07-09	1.1	6.0	
PM0-1, BPO-3 valid delay	t_{11a}		9,10,11	07-09	1.0	10.0	
PRDY valid delay	t_{11b}		9,10,11	07-09	1.0	8.0	
D0-D63, DPO-7 write data valid delay	t_{12}		9,10,11	07-09	1.3	7.5	
D0-D63, DPO-3 write data float delay	t_{13}	3/	9,10,11	07-09		10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
A5-A31 setup time	t_{14}	7/	9,10,11		6.0		ns
A5-A31 hold time	t_{15}		9,10,11	07-09	1.0		ns
INV, AP setup time	t_{16a}		9,10,11	07-09	5.0		
EADS setup time	t_{16b}		9,10,11	07-09	5.0		
EADS, INV, AP hold time	t_{17}		9,10,11	07-09	1.0		
KEN setup time	t_{18a}		9,10,11	07-09	5.0		
NA, WB/WT setup time	t_{18b}		9,10,11	07-09	4.5		
KEN, WB/WT, NA hold time	t_{19}		9,10,11	07-09	1.0		
BRDY setup time	t_{20}		9,10,11	07-09	5.0		
BRDY hold time	t_{21}		9,10,11	07-09	1.0		
BOFF, AHOLD setup time	t_{22}		9,10,11	07-09	5.5		
AHOLD, BOFF hold time	t_{23}		9,10,11	07-09	1.0		
BUSCHK, EWBE, HOLD, setup time	t_{24a}		9,10,11	07-09	5.0		
PEN setup time	t_{24b}		9,10,11	07-09	4.8		
BUSCHK, EWBE, PEN hold time	t_{25a}		9,10,11	07-09	1.0		
HOLD hold time	t_{25b}		9,10,11	07-09	1.5		
A20M, INTR, STPCLK setup time	t_{26}	8/ 9/	9,10,11	07-09	5.0		
A20M, INTR, STPCLK hold time	t_{27}	10/	9,10,11	07-09	1.0		
INIT, FLUSH, NMI, SMI, IGNNE setup time	t_{28}	8/ 9/ 11/	9,10,11	07-09	5.0		
INIT, FLUSH, NMI, SMI, IGNNE hold time	t_{29}	10/	9,10,11	07-09	1.0		
INIT, FLUSH, NMI, SMI, IGNNE pulse width, async	t_{30}	11/ 12/	9,10,11	07-09	2.0		CLKs
R/S setup time	t_{31}	8/ 9/ 11/	9,10,11	07-09	5.0		ns
R/S hold time	t_{32}	10/	9,10,11	07-09	1.0		
R/S pulse width, async	t_{33}	11/ 12/	9,10,11	07-09	2.0		CLKs
D0-D63, DP0-7 read data setup time	t_{34}		9,10,11	07-09	2.8		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
D0-D63, DP0-7 read data hold time	t_{35}		9,10,11	07-09	1.5		ns
RESET setup time	t_{36}	8/ 9/ 13/	9,10,11	07-09	5.0		
RESET hold time	t_{37}	10/ 13/	9,10,11	07-09	1.0		
RESET pulse width, V_{CC} and CLK stable	t_{38}	11/ 13/	9,10,11	07-09	15.0		CLKs
RESET active after V_{CC} and CLK stable	t_{39}	Power up	9,10,11	07-09	1.0		ms
Reset configuration signals (INIT, FLUSH) setup time	t_{40}	8/ 9/ 11/	9,10,11	07-09	5.0		ns
Reset configuration signals (INIT, FLUSH) hold time	t_{41}	10/	9,10,11	07-09	1.0		
Reset configuration signals (INIT, FLUSH) setup time, async	t_{42a}	To RESET falling edge 9/	9,10,11	07-09	2.0		CLKs
Reset configuration signals (INIT, FLUSH $\overline{\text{BUSCHK}}$, BRDY) hold time, async	t_{42b}	To RESET falling edge 14/	9,10,11	07-09	2.0		
Reset configuration signals ($\overline{\text{BUSCHK}}$, BRDY) setup time, async	t_{42c}	To RESET falling edge 14/	9,10,11	07-09	3.0		
Reset configuration signals BRDY hold time, RESET driven synchronously	t_{42d}	To RESET falling edge 3/ 14/	9,10,11	07-09	1.0		ns
BF, setup time	t_{43a}	To RESET falling edge 15/	9,10,11	07-09	1.0		ms
BF, hold time	t_{43b}	To RESET falling edge 15/	9,10,11	07-09	2.0		CLKs
TCK frequency	t_{44}		9,10,11	07-09		16.0	MHz
TCK period	t_{45}		9,10,11	07-09	62.5		ns
TCK high time	t_{46}	V_{IN} = 2 V 3/	9,10,11	07-09	25.0		
TCK low time	t_{47}	V_{IN} = 0.8 V 3/	9,10,11	07-09	25.0		
TCK fall time	t_{48}	V_{IN} = 2.0 V -0.8 V 3/ 16/ 17/	9,10,11	07-09		5.0	
TCK rise time	t_{49}	V_{IN} = 2.0 V -0.8 V 3/ 16/ 17/	9,10,11	07-09		5.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.135\ V \le V_{CC3} \le 3.465\ V$ $2.935\ V \le V_{CC2} \le 3.265\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{TRST}$ pulse width	t_{50}	Asynchronous 3/	9,10,11	07-09	40.0		ns
TDI, TMS setup time	t_{51}	18/	9,10,11	07-09	5.0		
TDI, TMS hold time	t_{52}	18/	9,10,11	07-09	13.0		
TDO valid delay	t_{53}	16/	9,10,11	07-09	3.0	20.0	
TDO float delay	t_{54}	3/ 16/	9,10,11	07-09		25.0	
All nontest outputs valid delay	t_{55}	16/ 19/ 20/	9,10,11	07-09	3.0	20.0	
All nontest outputs float delay	t_{56}	3/ 16/ 19/ 20/	9,10,11	07-09		25.0	
All nontest inputs setup time	t_{57}	18/ 19/ 20/	9,10,11	07-09	5.0		
All nontest inputs hold time	t_{58}	18/ 19/ 20/	9,10,11	07-09	13.0		

See notes at end of table.

1/ Unless otherwise specified, all testing to be performed using worst-case.conditions. The 50 and 60 Mhz bus operationsno 100% tested, they are guaranteed by design/characterization. Full functionality is verified at both minimum and maximum bus frequency in the production test program.
2/ This value should be used for power supply design. It was determined using a worst case instruciton mix and V_{CC3} = 3.465 V, V_{CC2} = 3.265 V. Power supply y transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurning during transitions from stop clock to full active modes.
3/ Not 100 percent tested. Guaranteed by design/characterization.
4/ These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any poqer spectrum peaking between 500 kHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
5/ 0.8 V/ns ≤ CLK input rise/fall time ≤ 8 V/ns.
6/ $\overline{\text{APCHK}}$, $\overline{\text{FERR}}$, HLDA, $\overline{\text{IERR}}$, $\overline{\text{LOCK}}$, and $\overline{\text{PCHK}}$ are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
7/ In dual processing mode, timing t_{14} is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which $\overline{\text{EADS}}$ is sampled active) in both uniprocessor and dual processor modes.
8/ Setup time is required to guarantee recognition on a specific clock. The device must meet this specification for dual processor operation for the $\overline{\text{FLUSH}}$ and RESET signals.
9/ This input may be driven asynchronously. However, when operating two processing mode, $\overline{\text{FLUSH}}$ and RESET must be asserted synchronously to both processors.
10/ Hold time is requred to guarantee recognition on a specific clock. The device must meet this specification for dual processor operation for the $\overline{\text{FLUSH}}$ and RESET signals.
11/ When driven asynchronously, RESET, NMI, $\overline{\text{FLUSH}}$, R/S, INIT, and $\overline{\text{SMI}}$ must be de-asserted (inactive) for a minimum of 2 clocks before being retumed active.
12/ To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of 2 clocks before being retumed active and must meet the minimum pulse width.
13/ $\overline{\text{TFRCMC}}$ should be tied to V_{CC} (high) to ensure proper operation of the device as a primary processor.
14/ $\overline{\text{BRDYC}}$, $\overline{\text{BUSCHK}}$ are used as reset configuration signals to select buffer size.
15/ BF and CPUTYP should be strapped to V_{CC} or V_{SS}.
16/ Referenced to TCK falling edge.
17/ 1 ns can be added to the maximum TCK rise and fall times for every 10 Mhz of frequency below 33 Mhz.
18/ Referenced to TCK rising edge.
19/ Nontest outputs and inputs are the normal output or input signals (besides TCK, $\overline{\text{TRST}}$, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
20/ During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).

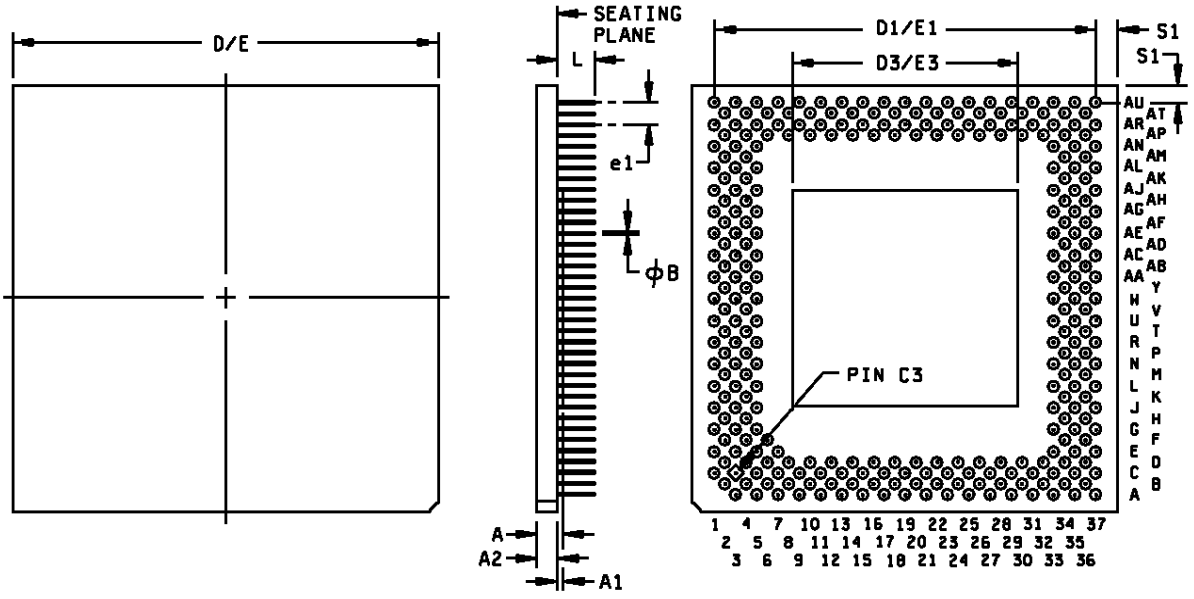


FIGURE 1. Case outline.

Symbol	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	3.27	3.83	0.129	0.151	Ceramic Lid
A1	0.66	0.86	0.026	0.034	Ceramic Lid
A2	2.62	2.97	0.103	0.117	
B	0.43	0.51	0.017	0.020	
D	49.28	49.78	1.940	1.960	
D1	45.59	45.85	1.795	1.805	
D3	24.00	24.25	0.945	0.955	Includes Fillet
e1	2.29	2.79	0.090	0.110	
F		0.127		0.005	Flatness of the top of the package , measured diagonally
L	3.05	3.30	0.120	1.130	
N	296		296		Total Pins
S1	1.52	2.54	0.060	0.100	

Figure 1. Case outline. - Continued

Device type	01-09	Device type	01-09	Device type	01-09	Device type	01-09	Device type	01-09
Case outline	X	Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A3	INC	B26	V_{SS}	D12	D37	G35	D1	N35	TDI
A5	D41	B28	V_{SS}	D14	D35	G37	V_{CC3}	N37	V_{CC3}
A7	V_{CC2}	B30	D20	D16	D33	H2	V_{SS}	P2	V_{SS}
A9	V_{CC2}	B32	D16	D18	DP3	H4	D56	P4	$\overline{TERR}$
A11	V_{CC2}	B34	D13	D20	D30	H34	NC	P34	TMS
A13	V_{CC2}	B36	D11	D22	D28	H36	V_{SS}	P36	V_{SS}
A15	V_{CC2}	C1	INC	D24	D26	J1	V_{CC2}	Q1	V_{CC2}
A17	V_{CC2}	C3	D47	D26	D23	J3	D57	Q3	PM0BP0
A19	V_{CC3}	C5	D45	D28	D19	J5	D58	Q5	$\overline{FERR}$
A21	V_{CC3}	C7	DP4	D30	DP1	J33	NC	Q33	$\overline{TRST}$
A23	V_{CC3}	C9	D38	D32	D12	J35	D2	Q35	NC
A25	V_{CC3}	C11	D36	D34	D6	J37	V_{CC3}	Q37	V_{CC3}
A27	V_{CC3}	C13	D34	D36	DP0	K2	V_{SS}	R2	V_{SS}
A29	V_{CC3}	C15	D32	E1	D54	K4	D59	R4	PM1BP1
A31	D22	C17	D31	E3	D52	K34	D0	R34	NC
A33	D18	C19	D29	E5	D49	K36	V_{SS}	R36	V_{SS}
A35	D15	C21	D27	E7	D46	L1	V_{CC2}	S1	V_{CC2}
A37	NC	C23	D25	E9	D42	L3	D61	S3	BP2
B2	INC	C25	DP2	E33	D7	L5	D60	S5	BP3
B4	D43	C27	D24	E35	D6	L33	V_{CC3}	S33	NC
B6	V_{SS}	C29	D21	E37	V_{CC3}	L35	NC	S35	NC
B8	V_{SS}	C31	D17	F2	DP6	L37	V_{CC3}	S37	V_{CC3}
B10	V_{SS}	C33	D14	F4	D51	M2	V_{SS}	T2	V_{SS}
B12	V_{SS}	C35	D10	F6	DP5	M4	D62	T4	M/$\overline{IO}$
B14	V_{SS}	C37	D9	F34	D5	M34	TCK	T34	V_{CC3}
B16	V_{SS}	D2	D50	F36	D4	M36	V_{SS}	T36	V_{SS}
B18	V_{SS}	D4	D48	G1	V_{CC2}	N1	V_{CC2}	U1	V_{CC2}
B20	V_{SS}	D6	D44	G3	D55	N3	D63	U3	$\overline{CACHE}$
B22	V_{SS}	D8	D40	G5	D53	N5	DP7	U5	INV
B24	V_{SS}	D10	D39	G33	D3	N33	TDO	U33	V_{CC3}

FIGURE 2. Terminal connections.

Device type	01-09	Device type	01-09	Device type	01-09	Device type	01-09	Device type	01-09
Case outline	X	Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
U35	V_{SS}	AA35	$\overline{IGNNE}$	AG35	A24	AL1	INC	AM24	V_{SS}
U37	V_{CC3}	AA37	V_{CC3}	AG37	V_{CC3}	AL3	PWT	AM26	V_{SS}
V2	V_{SS}	AB2	V_{SS}	AH2	V_{SS}	AL5	$\overline{HITM}$	AM28	V_{SS}
V4	AHOLD	AB4	HOLD	AH4	$\overline{LOCK}$	AL7	$\overline{BUSCHK}$	AM30	V_{SS}
V34	$\overline{STPCLK}$	AB34	$\overline{SMI}$	AH4	A26	AL9	$\overline{BE0}$	AM32	A8
V36	V_{SS}	AB36	V_{SS}	AH36	A22	AL11	$\overline{BE2}$	AM34	A4
W1	V_{CC2}	AC1	V_{CC2}	AJ1	BREQ	AL13	$\overline{BE4}$	AM36	A30
W3	$\overline{EWBE}$	AC3	NC	AJ3	HLDA	AL15	$\overline{BE6}$	AN1	INC
W5	$\overline{KEN}$	AC5	PRDY	AJ5	$\overline{ADS}$	AL17	SCYC	AN3	INC
W33	NC	AC33	NMI	AJ33	A31	AL19	NC	AN5	INC
W35	NC	AC35	$\overline{RS}$	AJ35	A25	AL21	A20	AN7	$\overline{FLUSH}$
W37	V_{CC3}	AC37	V_{CC3}	AJ37	V_{SS}	AL23	A18	AN9	V_{CC2}
X2	V_{SS}	AD2	V_{SS}	AK2	AP	AL25	A16	AN11	V_{CC2}
X4	$\overline{BRDY}$	AD4	NC	AK4	$\overline{DC}$	AL27	A14	AN13	V_{CC2}
X34	BF1	AD34	INTR	AK6	$\overline{HIT}$	AL29	A12	AN15	V_{CC2}
X36	V_{SS}	AD36	V_{SS}	AK8	$\overline{A20M}$	AL31	A11	AN17	V_{CC2}
Y1	V_{CC2}	AE1	V_{CC2}	AK10	$\overline{BE1}$	AL33	A7	AN19	V_{CC2}
Y3	NC	AE3	NC	AK12	$\overline{BE3}$	AL35	A3	AN21	V_{CC3}
Y5	$\overline{NA}$	AE5	$\overline{APCHK}$	AK14	$\overline{BE5}$	AL37	V_{SS}	AN23	V_{CC3}
Y33	BF0	AE33	A23	AK16	$\overline{BE7}$	AM2	NC	AN25	V_{CC3}
Y35	NC	AE35	NC	AK18	CLK	AM4	$\overline{EADS}$	AN27	V_{CC3}
Y37	V_{CC3}	AE37	V_{CC3}	AK20	RESET	AM6	W/$\overline{R}$	AN29	V_{CC3}
Z2	V_{SS}	AF2	V_{SS}	AK22	A19	AM8	V_{SS}	AN31	A10
Z4	$\overline{BOFF}$	AF4	$\overline{PCHK}$	AK24	A17	AM10	V_{SS}	AN33	A6
Z34	$\overline{PEN}$	AF34	A21	AK26	A15	AM12	V_{SS}	AN35	NC
Z36	V_{SS}	AF36	V_{SS}	AK28	A13	AM14	V_{SS}	AN37	V_{SS}
AA1	V_{CC2}	AG1	V_{CC2}	AK30	A9	AM16	V_{SS}		
AA3	NC	AG3	$\overline{SMIACT}$	AK32	A5	AM18	V_{SS}		
AA5	W/$\overline{WB}$	AG5	PCD	AK34	A29	AM20	V_{SS}		
AA33	INIT	AG33	A27	AK36	A28	AM22	V_{SS}		

FIGURE 2. Terminal connections - Continued.

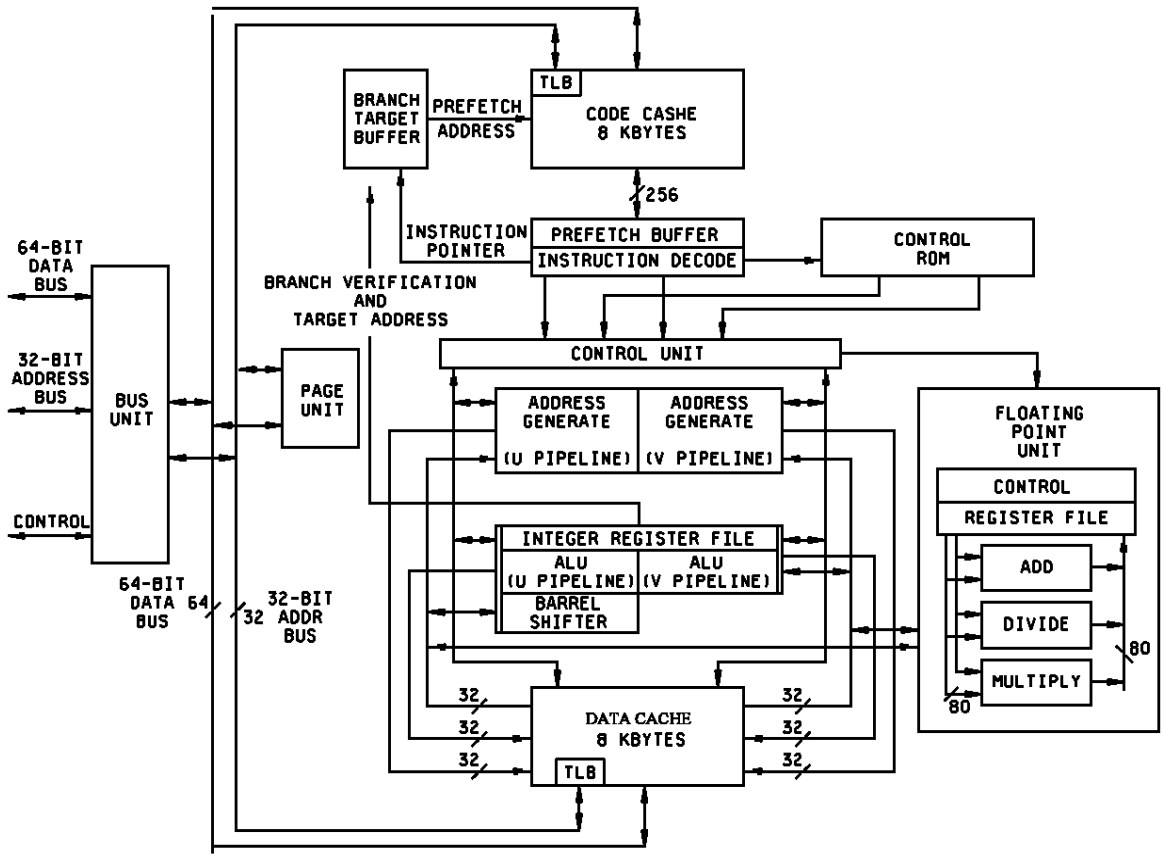
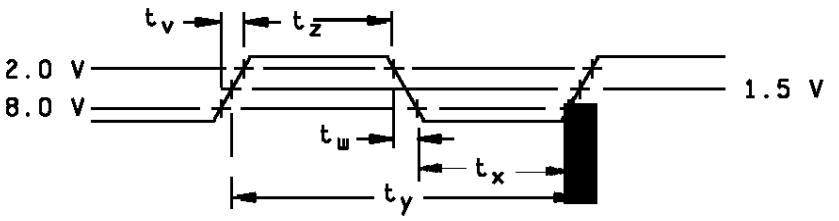
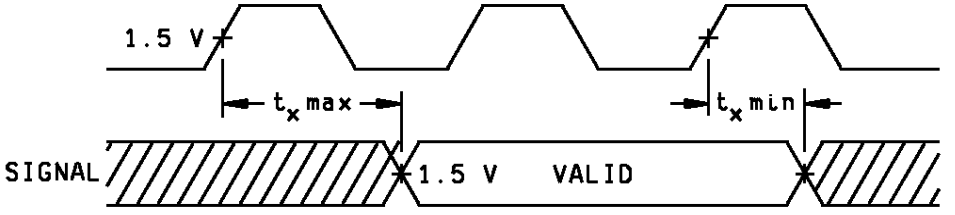


FIGURE 3. Block diagram.



CLOCK WAVEFORM

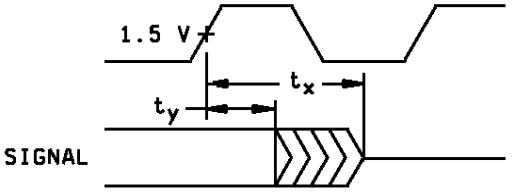
$t_v = t_5, t_{49}$
$t_w = t_4, t_{48}$
$t_x = t_3, t_{47}$
$t_y = t_1, t_{45}$
$t_z = t_2, t_{46}$



VALID DELAY TIMINGS

$t_x = t_6, t_8, t_9, t_{10}, t_{11}, t_{12}$

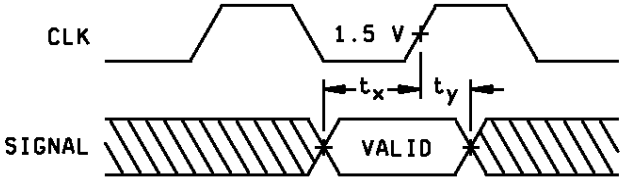
FIGURE 4. Timing waveforms.



FLOAT DELAY TIMINGS

$t_x = t_7, t_{13}$

$t_y = t_{6\ min}, t_{12\ min}$

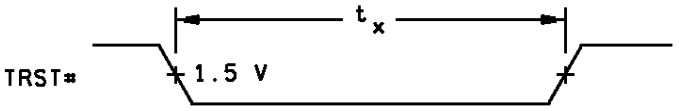


SETUP AND HOLD TIMINGS

$t_x = t_{14}, t_{16}, t_{18}, t_{20}, t_{22}, t_{24}, t_{26}, t_{28}, t_{31}, t_{34}$

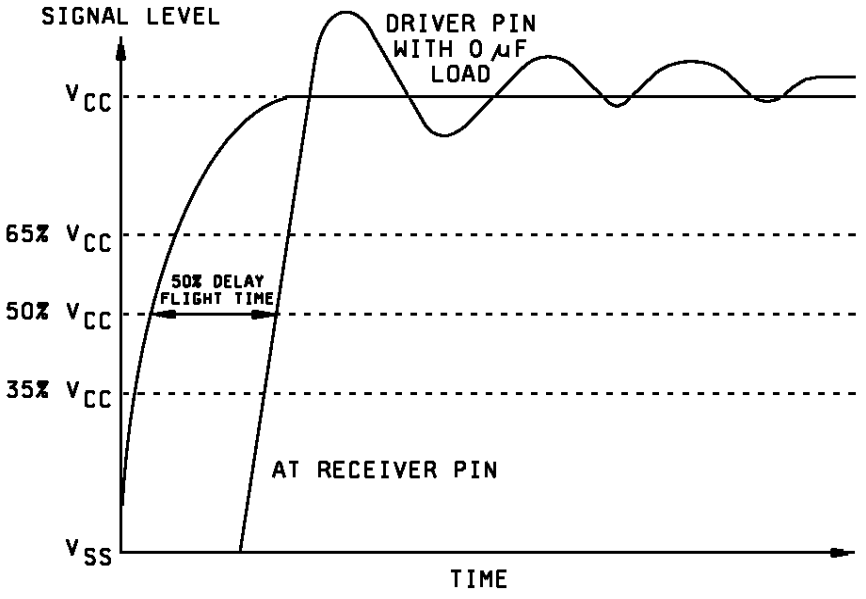
$t_y = t_{15}, t_{17}, t_{19}, t_{21}, t_{23}, t_{25}, t_{27}, t_{29}, t_{32}, t_{35}$

FIGURE 4. Timing waveforms - Continued.



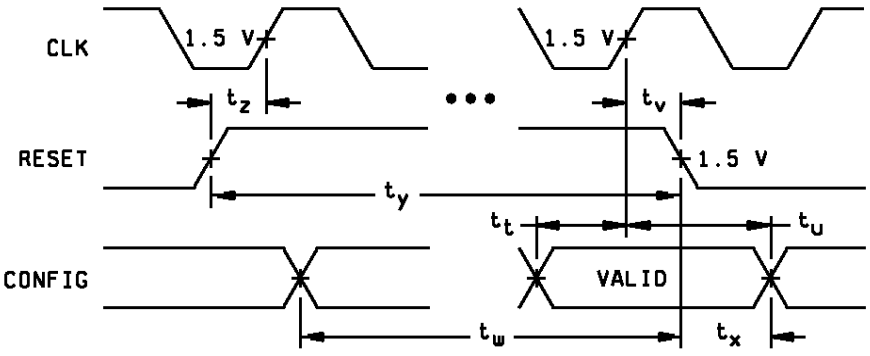
TEST RESET TIMINGS

$t_x = t_{50}$



50% V_{CC} MEASUREMENT OF FLIGHT TIME

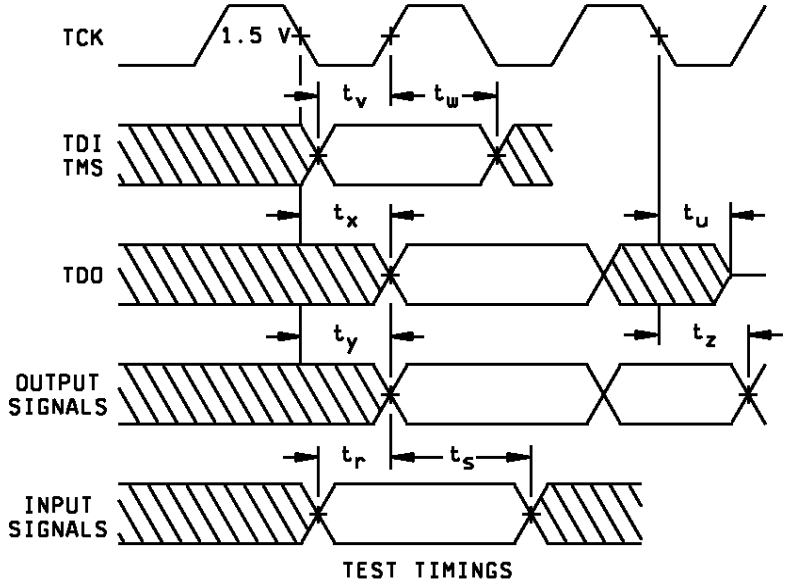
FIGURE 4. Timing waveforms - Continued.



RESET AND CONFIGURATION TIMINGS

$t_t = t_{40}, t_u = t_{41}, t_v = t_{37}, t_w = t_{42}, t_{43a}, t_{43c}$

$t_x = t_{43b}, t_{43d}$ $, t_y = t_{38}, t_{39}, t_z = t_{36}$



TEST TIMINGS

$t_r = t_{57}, t_s = t_{58}, t_u = t_{54}, t_v = t_{51}, t_w = t_{52}, t_x = t_{53}, t_y = t_{55}, t_z = t_{56}$

FIGURE 4. Timing waveforms - Continued.

Instruction Name	Instruction Register Bits 12:4	TAP Command Field [Bits 3:0]
EXTEST		0000
Sample/Preload		0001
IDCODE		0010
Private Instruction		0011
Private Instruction		0100
Private Instruction		0101
Private Instruction		0110
RUNBIST		0111
Private Instruction		1000
Private Instruction		1001
Private Instruction		1010
HI-Z		1011
Private Instruction		1100
BYPASS		1111

The TAP command field encodings not listed in (1101, 1110) are unimplemented and will be interpreted as bypass instructions.

Figure 5. Boundry Scan instruction Codes

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_O, $C_{I/O}$, C_{CLK}, C_{TIN}, C_{TOUT}, and C_{TCK} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	2,3, 8, 10,11 1/	2,3 ,8, 10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	2,5,8,10	2,5,8,10	2,5,8,10	2,5,8,10
Group D end-point electrical parameters (see 4.4)	2,5,8,10	2,5,8,10	2,5,8,10	2,5,8,10
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 2.
2/ PDA applies to subgroups 2 and 8a.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Pin symbol	Type	Description
$\overline{A20M}$	I	When the address bit 20 mask pin is asserted, the device emulates the address wraparound at 1 Mbyte which occurs on the 8086. When $\overline{A20M}$ is asserted, the device masks physical address bit 20(A20) before perfroming a lookup to the internal caches or driving a memory cycle on the bus. The effect of $\overline{A20M}$ is undefined in protected mode. $\overline{A20M}$ must be asserted only when the processor is in real mode. $\overline{A20M}$ is internally masked by the device when configured as a Dual processor.
A31-A3	I/O	As outputs, the address lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
$\overline{ADS}$	O	The address status indicates that a new valid bus cycle is currently being driven by the device.
AHOLD	I	In response to the assertion of address hold, the device will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	Address parity is driven by the device with even parity information on all the device generated cycles in the same clock that the address is driven. Even parity must be driven back to the device during inquire cycles on this pin in the same clock as $\overline{EADS}$ to ensure that correct parity check status is indicated by the device.
$\overline{APCHK}$	O	The address parity check status pin is asserted two clocks after $\overline{EADS}$ is sampled active if the device has detected a parity error on the address bus during inquire cycles. $\overline{APCHK}$ will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
(APICEN) PICD1	I	Advanced programmable interrupt controller enable is a new pin that enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the programmable interrupt contoller data 1 signal.
$\overline{BE7}$-$\overline{BE5}$ $\overline{BE4}$-$\overline{BE0}$	O I/O	The byte enable pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Unlike the 60/66 MHz device, the lower 4-byte enables ($\overline{BE3}$-$\overline{BE0}$) are used on the device as APIC ID inputs and are sampled at RESET. After RESET, these behave exactly lide the 60/66 MHz device byte enables. In dual processing mode, $\overline{BE4}$ is used as an input during flush cycles.
BF(1:0)	I	Bus frequency deternubes the bus-to-core frequency ratio. BF is sampled at RESET, and cannot be changed until another nonwarm (1 ms) assertion of RESET. Additionally, BF must not change values while RESET is active. For proper operation of the device this pin should be strapped high or low. When BF is strapped to V_{CC}, the processor will operate at a 2/3 bus/core frequency ratio. When BF is strapped to V_{SS}, the processor will operate at a 1/2 bus/core frequency ratio. If BF is left floating, the device defaults to a 2/3 bus ratio. Note that core operation at either 75 Mhz or 90 Mhz does not allow 1/2 bus/core frequency, while core operation at 120 Mhz and 133 Mhz does not allow 2/3 bus core frequency.
$\overline{BOFF}$	I	The backoff input is used to abort all outstanding bus cycles that have not yet completed. In response to $\overline{BOFF}$, the device will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until $\overline{BOFF}$ is negated, at which time the device restarts the aborted bus cycle(s) in their entirety.

Pin symbol	Type	Description - Continued.
BP(3:2) PM/BP(1:0)	O	The breakpoint pins (BP3-0) correrpond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the perfromance monitoring pins (PM1 and PM0). The PB1 and PB0 bits in the debug mode control register determine if the pins are configured as breakpoint or perfromance monitoring pins. The pins come out of RESET configured for performance monitoring.
$\overline{\text{BRDY}}$	I	The burst ready input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the device data in response to a write request. This signal is sampled in the T2, T12, and T2P bus states.
BREQ	O	The bus request output indicates to the external system that the device has internally generated a bus request. This signal is always driven whether or not the device is driving its bus.
$\overline{\text{BUSCHK}}$	I	The bus check input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the device will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the device will vector to the machine check exception. NOTE: To assure that the $\overline{\text{BUSCHK}}$ will always be recognized, $\overline{\text{STPCLK}}$ must be deasserted any time $\overline{\text{BUSCHK}}$ is asserted by the system, before the system allows another external bus cycle. If $\overline{\text{BUSCHK}}$ is asserted by the system for a snoop cycle while $\overline{\text{STPCLK}}$ remains asserted, ussually (if MCE = 1) the processor will vector to the exception after $\overline{\text{STPCLK}}$ is deasserted. But if another snoop to the same line occurs during $\overline{\text{STPCLK}}$ assertion, the processor can lose the $\overline{\text{BUSCHK}}$ request.
$\overline{\text{CACHE}}$	O	For the device-initiated cycles the cache pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the device will not chache the returned data, regardless of the state of the $\overline{\text{KEN}}$ pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The clock input provides the fundamental timing for the device. Its frequency is the operating frequency fo the device external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, $\overline{\text{TRST}}$, and PICD0-1 are specified with respect to the rising edge of CLK. NOTE: It is recommended the CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to ensure long-term reliability of the device.
D/$\overline{\text{C}}$	O	The data/code output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the $\overline{\text{ADS}}$ signal is asserted. D/$\overline{\text{C}}$ distinguishes between data and code or special cycles.

Pin symbol	Type	Description - Continued.
D63-d0	I/O	These are the 64 data lines for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY is returned.
DP7-DP0	I/O	These are the data parity pins for the processor. There is one for each byte of the data bus. They are driven by the device with even parity information on writes in the same clock as write data. Even parity information must be driven back to the device on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the device. DP7 applies to D63-56, DP0 applies to D7-0.
EADS	I	This signal indicates that a valid external address has been driven onto the device address pins to be used for an inquire cycle.
EWBE	I	The external write buffer empty input, when inactive (high), indicates that a write cycle is pending in the external system. When the device generates a write, and EWBE is sampled inactive, the device will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE being active.
FERR	O	The floating point error pin is driven active when an unmasked floating point error occurs. FERR is similar to the ERROR pin on the 5962-89534 device math coprocessor. FERR is included for compatibility withe systems using DOS type floating point error reporting. FERR is never driven active by the dual processor.
FLUSH	I	When asserted, the cache flush input forces the device to write back all modified lines in the data cache and invalidate its internal caches. A flush acknowledge special cycle will be generated by the device indicating completion of the write back and invalidation. If FLUSH is sampled low when RESET transitions from high to low, three-state test mode is entered. If two devices are operating in dual processing mode in a system and FLUSH is asserted, the dual processor will perform a flush first (without a flush acknowledge cycle), then the primary processor will perform a flush followed by a flush acknowledge cycle. NOTE: If the FLUSH signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY of the FLUSH acknowledge cycle to avoid DP arbitration problems.

Pin symbol	Type	Description - Continued.
$\overline{\text{HTT}}$	O	The hit indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line ineither the device daa or instruction cache, this pin is asserted two clicks after $\overline{\text{EADS}}$ is sampled asserted. If the inquire cycle misses the device cache, this pin is negated two clocks after $\overline{\text{EADS}}$. This pin chnges its value only as a result of an inquire cycle and retains its value between the cycles.
$\overline{\text{HTTM}}$	O	The hit to a modified line output is driven to relect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HILDA	O	The bus hold acknowledge pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the device has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the device will resume driving the bus. If the device has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the bus hold request, the device will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The device will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The device will recognize HOLD during reset.
$\overline{\text{TERR}}$	O	The internal error pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. If a parity error occurs on a read from an internal array, the device will assert the $\overline{\text{TERR}}$ pin for one clock and then shutdown. If the device is configured as a checker and a mismatch occurs between the value sampled on the pins and the corresponding value computed internally, the device will assert $\overline{\text{TERR}}$ two clocks after the mismatched value is returned.
$\overline{\text{TGNNE}}$	I	This is the ignore numeric error input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the $\overline{\text{TGNNE}}$ pin is asserted, the device will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, $\overline{\text{TGNNE}}$ is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the device will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, $\overline{\text{TGNNE}}$ is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the device will stop execution and wait for an external interrupt. $\overline{\text{TGNNE}}$ is internally masked when the device is configured as a dual processor.
INIT	I	The device initialization input pin forces the device to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating point registers retain the values thay had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the device will perfrom built-in self test prior to the start of program execution.

Pin symbol	Type	Description - Continued.
INTR	I	An active maskable interrupt input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the device will generate two locked interrupt acknowledge bus cycles and vectro to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrup acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The invalidation input determines the final cache line state (S or 1) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock $\overline{EADS}$ is sampled active.
$\overline{KEN}$	I	The cache enable pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the device generates a cycle that can be cached ($\overline{CACHE}$ asserted) and $\overline{KEN}$ is active, the cycle will be transformed into a burst line fill cycle.
$\overline{LOCK}$	O	The bus lock pin indicates that the current bus cycle is locked. The device will not allow a bus hold when $\overline{LOCK}$ is asserted (but AHOLD and $\overline{BOFF}$ are allowed). $\overline{LOCK}$ goes active in the first clock of the first locked bus cycle and goes inactive after the $\overline{BRDY}$ is returned for the last licked bus cycle. $\overline{LOCK}$ is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/$\overline{IO}$	O	The memory/input-output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the $\overline{ADS}$ signal is asserted. M/$\overline{IO}$ distinguishes between memory and I/O cycles.
$\overline{NA}$	I	An active next address input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The device will issue $\overline{ADS}$ for a pending cycle two clocks after $\overline{NA}$ is asserted. The device supports up to two outstanding bus cycles.
NMI	I	The nonmaskable interrupt request signal indicates that an external nonmaskable interrupt has been generated.
PCD	O	The page cache disable pin reflects the state of the PCD bit in CR3, the page directory entry, or the page table entry. The purpose of PCD is to provide an external cacheablity indication on a page by page basis.

Pin symbol	Type	Description - Continued.
$\overline{\text{PCHK}}$	O	The parity check ouput indicates the result of a parity check on a data read. It is driven with parity status two clicks after $\overline{\text{BRDY}}$ is returned. $\overline{\text{PCHK}}$ remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two device are operating in dual processing mode, $\overline{\text{PEN}}$ may be driven two or three clocks after $\overline{\text{BRDY}}$ is returned.
$\overline{\text{PEN}}$	I	The parity enable input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the device will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the device will vector to the machine check exception before the beginning of the next instruction.
PM/BP(1:0)	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the performance monitoring 1-0 pins. The BP1 and PB0 bits in the debug mode control register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The probe ready output pin indicates that the processor has stopped normal execution in response to the $\overline{\text{R/S}}$ pin going active, or probe mode being enter
PWT	O	The page write through pin refects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
$\overline{\text{R/S}}$	I	The run/stop input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the $\overline{\text{R/S}}$ pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	RESET forces the device to begin execution at a known state. All the devices internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. $\overline{\text{FLUSH}}$, $\overline{\text{FRCMC}}$, and INIT are sampled when RESET transitions from high to low to determine if three-state test mode or checker mode will be entered, or if BIST will be run.
SCYC	O	The split cycle output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.

Pin symbol	Type	Description - Continued.
$\overline{SMI}$	I	The system management interrupt causes a system management interrupt request to be latched internally. When the latched $\overline{SMI}$ is recognized on an instruction boundary, the processor enters system management mode.
$\overline{SMIACT}$	O	An active system management interrupt active output indicates that the processor is operating in system management mode.
$\overline{STPCLK}$	I	Assertion of the stop clock input signifies a request to stop the internal clock of the device thereby causing the core to consume less power. When the CPU recognizes $\overline{STPCLK}$, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When $\overline{STPCLK}$ is asserted, the device will still respond to interprocessor and external snoop requests.
TCK	I	The testability clock input provides the clocking function for the device boundary scan in accordance with the IEE Boundary Scan Interface (Standard 1149.1). It is used to clock state information and data into and out of the device during boundary scan.
TDI	I	The test data input is a serial input for the test logic. TAP instructions and data are shifted into the device on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state
TDO	O	The test data output is a serial output of the test logic. TAP instructions and data are shifted out of the device on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the test mode select input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
$\overline{TRST}$	I	When asserted, the test reset input allows the TAP controller to be asynchronously initialized.
V_{CC}	I	The device has 53 3.3 V power inputs.
V_{SS}	I	The device has 53 ground inputs.
W/$\overline{R}$	O	Write/read is one of the primary bus cycle definition pins. It is driven valid in the same clock as the $\overline{ADS}$ signal is asserted. W/$\overline{R}$ distinguishes between write and read cycles.
WB/$\overline{WT}$	I	The write back/write through input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, if determines whether a cache line is initially in the S or E state in the data cache.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-02-05

Approved sources of supply for SMD 5962-94578 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9457801QXC	34369	MG8050250100
5962-9457802NXC	34369	TA8050250100
5962-9457803NXC	34369	MG8050250100
5962-9457804QXC	34369	MG8050260120
5962-9457805NXC	34369	TA8050260120
5962-9457806NXC	34369	MG8050260120
5962-9457807QXC	34369	MG8050266133
5962-9457808NXC	34369	TA8050266133
5962-9457809NXC	34369	MG8050266133

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34369	Intel Corporation 2200 Mission College Boulevard P.O. Box 58119 Santa Clara, CA 95052-8119 Point of contact: 5000 W. Chandler Boulevard Chandler, AZ 85226