REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
SHEET																									
REV																									
SHEET	22	23	24	25	26	27																			
REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY

CHECKED BY

APPROVED BY

DRAWING APPROVAL DATE

91-10-22

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CHMOS BUS CONTROLLER, MONLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90997

SHEET 1 OF 27

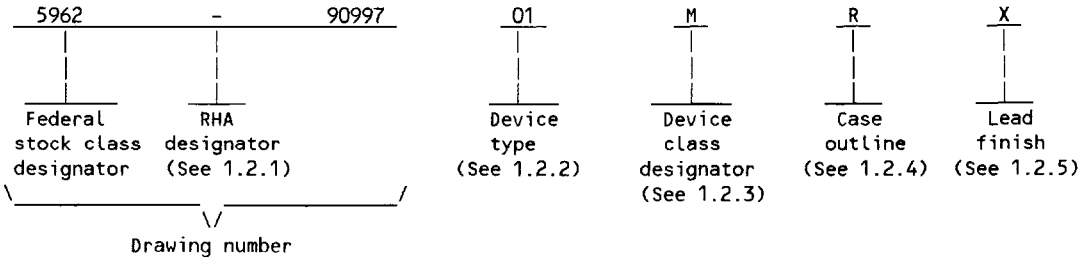
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	M82C288-6	Bus controller	6 MHz
02	M82C288-8	Bus controller	8 MHz
03	M82C288-10	Bus controller	10 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200") dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-0.5 V to +7 V
Power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage (V_{CC})	4.75 V dc to 5.25 V dc 2/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ The approved source of supply is unable to furnish devices with a supply voltage range (V_{SS}) of 4.5 V minimum to 5.5 V maximum, which is desirable for system applications, when the desired V_{CC} range is available it will be incorporated into the next action of the document.
3/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input low voltage	V_{IL}		1,2,3	All	-0.5	0.8	V
Input high voltage	V_{IH}				2.0	$V_{CC}+0.5$	
CLK input low voltage	V_{ILC}				-0.5	0.6	
CLK input high voltage	V_{IHC}				3.8	$V_{CC}+0.5$	
Output low voltage 2/	V_{OL}	Command outputs 3/ I_{OL} = 32 mA				0.45	
		Control outputs 4/ I_{OL} = 16 mA				0.45	
Output high voltage	V_{OH}	Command outputs I_{OH} = -5 mA I_{OH} = -1 mA 3/			2.4 $V_{CC}-0.5$		
		Control outputs I_{OH} = -1 mA I_{OH} = -0.2 mA 4/			2.4 $V_{CC}-0.5$		
Input leakage current	I_{IL1}	$V_{IN} \ge 0.0\ V$			-10		µA
	I_{IL2}	$V_{IN} \le V_{CC}$				+10	
Output leakage current	I_{LO1}	$V_{OUT} \ge 0.45\ V$			-10		
	I_{LO2}	$V_{OUT} \le V_{CC}$				+10	
Power supply current	I_{CC}					75	mA
Power supply current (static)	I_{CCS}	5/				3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK input capacitance	C_{CLK}	FC = 1 MHz, see 4.4.1c	4	All		12	pF
Input capacitance	C_{IN}					10	
Input/output capacitance	C_O					20	
Functional testing		See 4.4.1b	7,8				
CLK period	t_1	See figure 3	9,10,11	01	83	250	ns
				02	62	250	
				03	50	250	
CLK high time	t_2			01	25		
				02	20		
				03	16		
CLK low time	t_3			01	20		
				02	15		
				03	12		
CLK rise time 2/	t_4			01,02		10	
				03		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK fall time 2/	t_5	See figure 3	9,10,11	01,02		10	ns
				03		8	
M/IO and status setup time	t_6			01	28		
				02	22		
				03	18		
M/IO and status hold time	t_7			All	1		
CENL setup time	t_8			01	30		
				02	20		
				03	15		
CENL hold time	t_9			All	1		
READY setup time	t_{10}			01	50		
				02	38		
				03	26		
READY hold time	t_{11}			01	35		
				02,03	25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CMDLY setup time	t_{12}	See figure 3	9,10,11	01	25		ns
				02	20		
				03	15		
CMDLY hold time	t_{13}			All	1		
AEN setup time 6/	t_{14}			01	25		
				02	20		
				03	15		
AEN hold time 6/	t_{15}			All	0		
ALE, MCE active delay from CLK	t_{16}	See figure 3, C_L = 150 pF		01	3	25	
				02	3	20	
				03	3	16	
ALE, MCE inactive delay from CLK 2/	t_{17}			01		35	
				02		25	
				03		19	
DEN (write) inactive from CENL 2/	t_{18}			01		35	
				02		35	
				03		23	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DT/R low from CLK	t_{19}	See figure 3, C_L = 150 pF	9,10,11	01		40	ns
				02		25	
				03		23	
DEN (read) active from DT/R 2/	t_{20}			01	0	50	
				02	0	35	
				03	0	21	
DEN (read) inactive delay from CLK 2/	t_{21}			01	5	40	
				02	5	35	
				03	5	21	
DT/R high from DEN inactive 2/	t_{22}			01	3	45	
				02	3	35	
				03	3	20	
DEN (write) active delay from CLK	t_{23}			01		35	
				02		30	
				03		23	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DEN (write) inactive delay from CLK 2/	t_{24}	See figure 3, C_L = 150 pF	9,10,11	01	3	35	ns
				02	3	30	
				03	3	19	
DEN inactive from CEN	t_{25}			01		40	
				02		30	
				03		25	
DEN active from CEN 2/	t_{26}			01		35	
				02		30	
				03		24	
DT/R high from CLK when CEN = low 2/	t_{27}			01		50	
				02		35	
				03		25	
DEN active from AEN 2/	t_{28}			01		35	
				02		30	
				03		26	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CMD active delay from CLK 2/	t_{29}	See figure 3, C_L = 300 pF	9,10,11	01	3	40	ns
				02	3	25	
				03	3	21	
CMD inactive from CLK 2/	t_{30}			01	5	30	
				02	5	25	
				03	5	20	
CMD inactive from CEN 2/	t_{31}			01		45	
				02,03		25	
CMD active from CEN 2/	t_{32}			01		25	
				02,03		25	
CMD inactive enable from AEN	t_{33}			All		40	
CMD float delay from AEN 7/	t_{34}	See figure 3				40	
MB setup time	t_{35}			01	25		
				02	20		
				03	15		
MB hold time	t_{36}			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55^{\circ}C \le T_C \le +125^{\circ}C$ 4.75 V ≤ V_{CC} ≤ 5.25 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Command inactive enable from MB(L)	t_{37}	See figure 3 C_L = 300 pF	9,10,11	All		40	ns
Command float time from MB(H) 7/	t_{38}	See figure 3				40	
DEN inactive from MB(H)	t_{39}	See figure 3 C_L = 150 pF		01		40	
				02		30	
				03		26	
DEN active from MB(L) 2/	t_{40}			01		35	
				02		30	
				03		26	

1/ The following pins are active low: $\overline{READY}$, $\overline{S_1}$, $\overline{MRDC}$, $\overline{MWTC}$, $\overline{S_0}$, $\overline{IO}$ of M/$\overline{IO}$, $\overline{R}$ of DT/$\overline{R}$, $\overline{AEN}$ of CEN/$\overline{AEN}$, $\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{CMD}$. The approved source of supply is unable to furnish devices with a supply voltage range (V_{CC}) of 4.5 V minimum to 5.5 V maximum, which is desireable for system applications, when the desired V_{CC} range is available it will be incorporated into the next action of the document. Unless otherwise specified all test conditions shall be worst case test conditions.

2/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.

3/ Command outputs are $\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{MRDC}$, $\overline{MWTC}$.

4/ Control outputs are DT/$\overline{R}$, DEN, ALE and MCE.

5/ Tested while outputs are unloaded, and inputs at V_{CC} or GND.

6/ AEN is an asynchronous input. This specification is for testing purposes only, to assure recognition at specific CLK edge.

7/ Float condition occurs when output current is less than I_{LO} in magnitude.

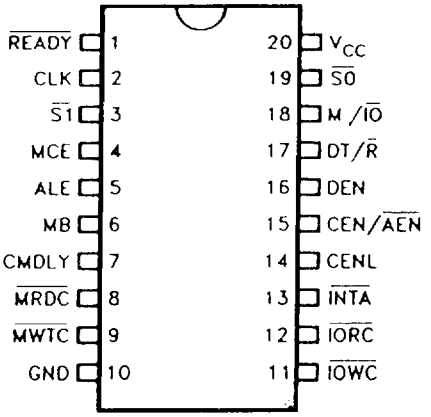


FIGURE 1. Terminal connections.

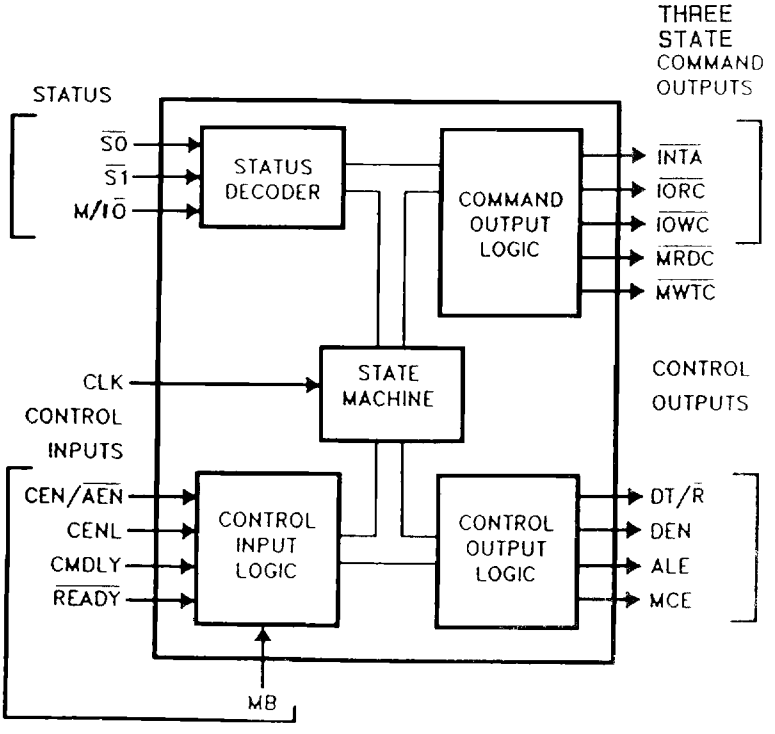
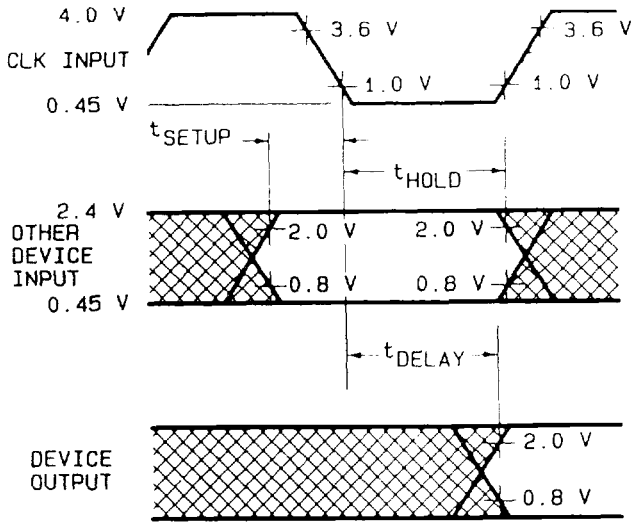
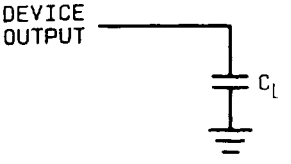


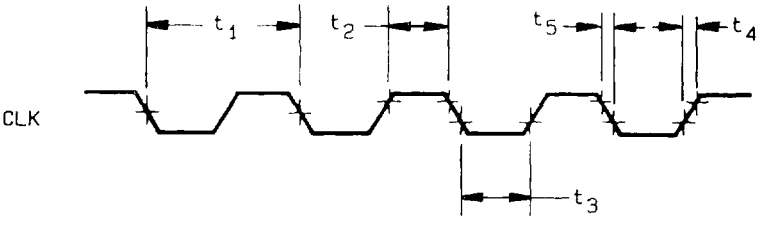
FIGURE 2. Functional block diagram.



AC SETUP, HOLD AND DELAY TIME MEASUREMENT - GENERAL

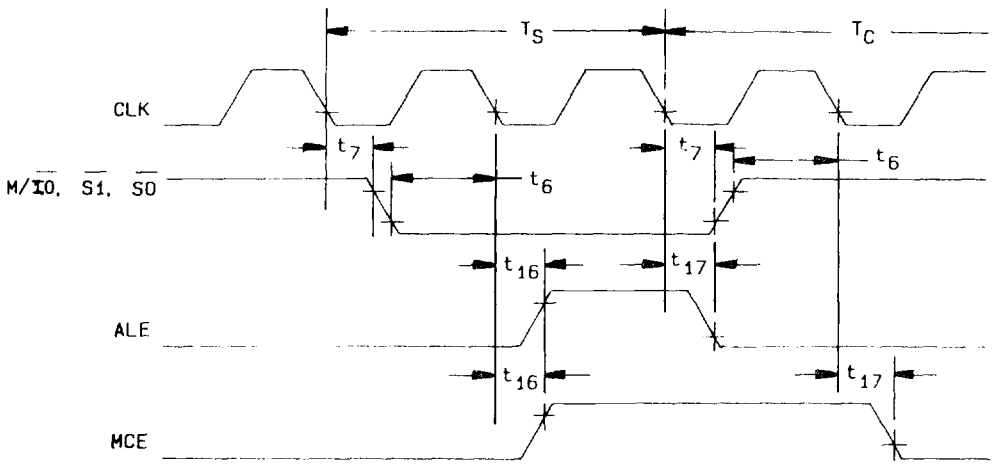


AC TEST LOADING ON OUTPUTS

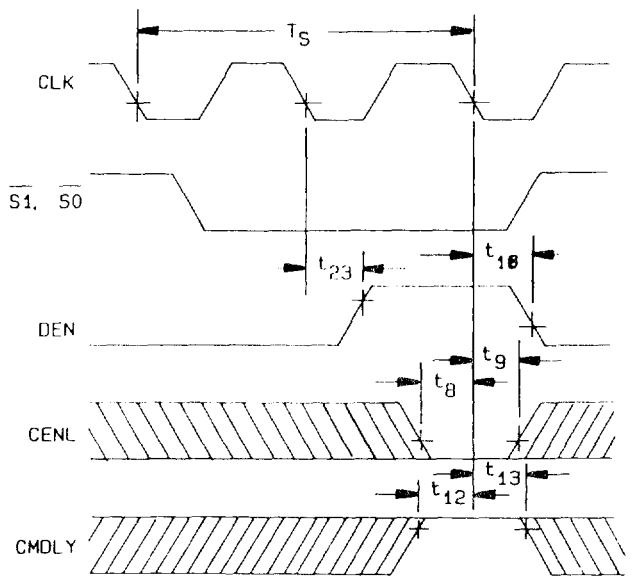


CLK CHARACTERISTICS

FIGURE 3. Switching waveforms and test circuit.

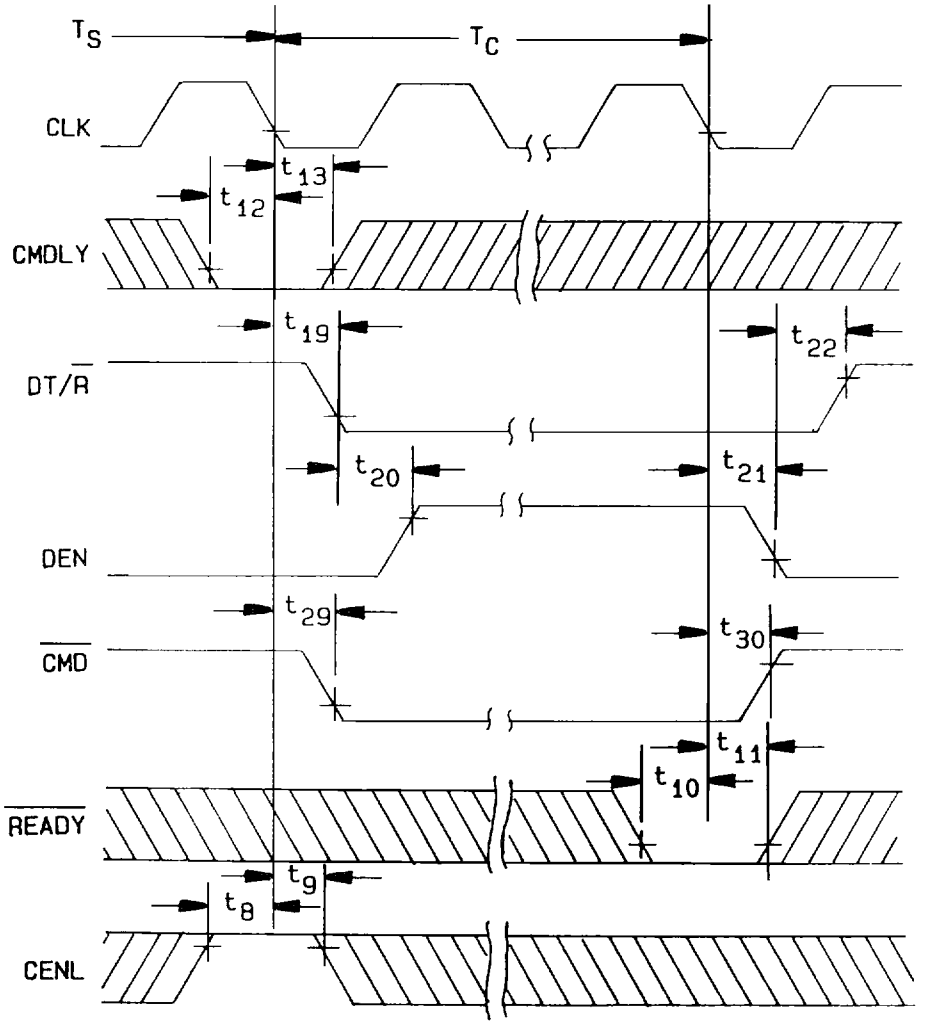


STATUS, ALE, AND MCE CHARACTERISTICS



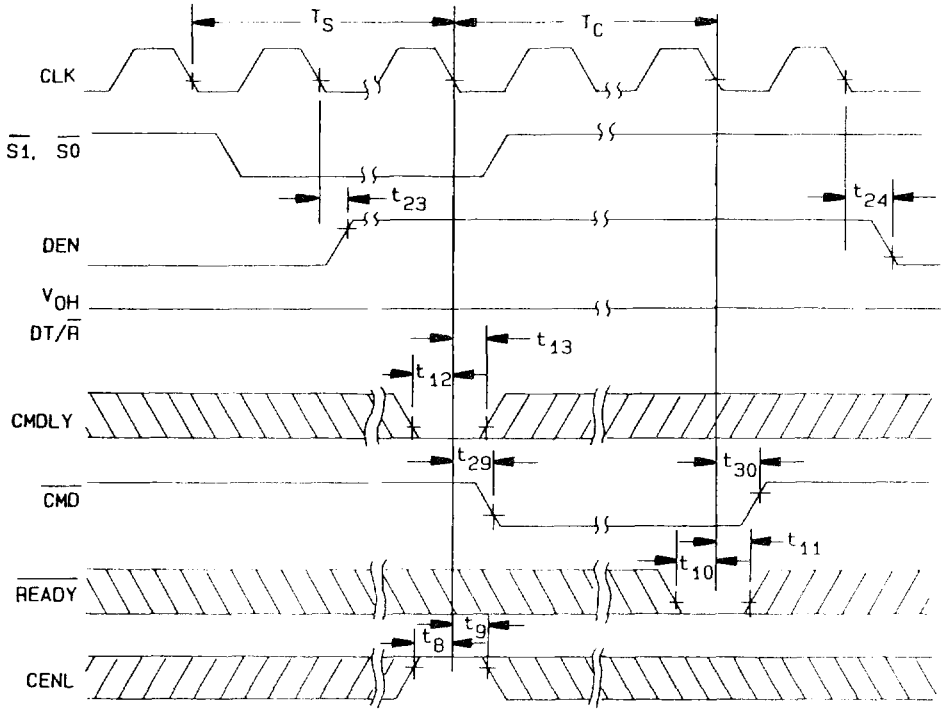
CENL, CMDLY, AND DEN CHARACTERISTICS WITH
MB = 0 AND CEN = 1 DURING WRITE CYCLE

FIGURE 3. Switching waveforms and test circuit - Continued.

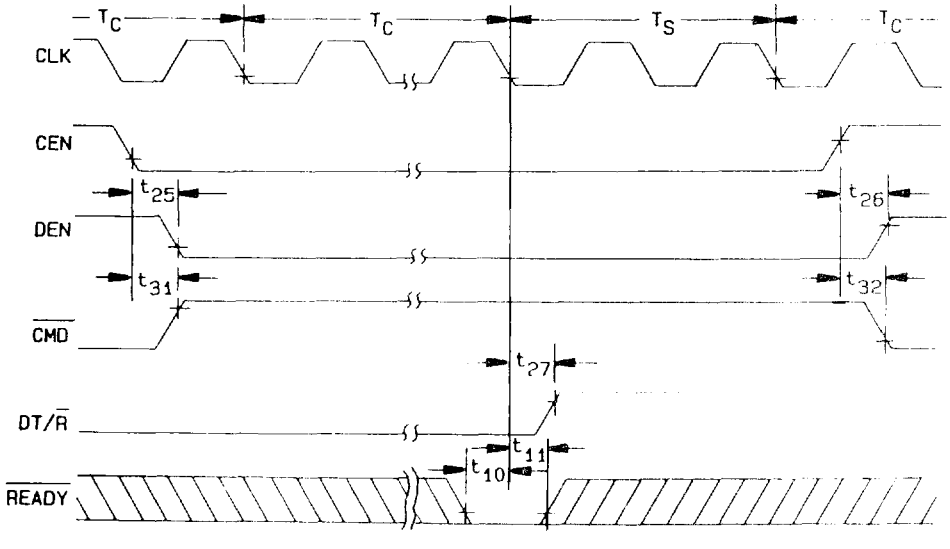


READ CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1

FIGURE 3. Switching waveforms and test circuit - Continued.

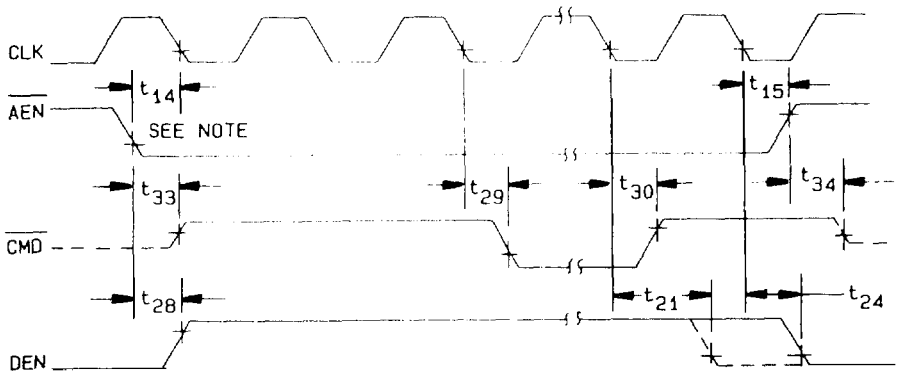


WRITE CYCLE CHARACTERISTIC WITH MB = 0 AND CEN = 1



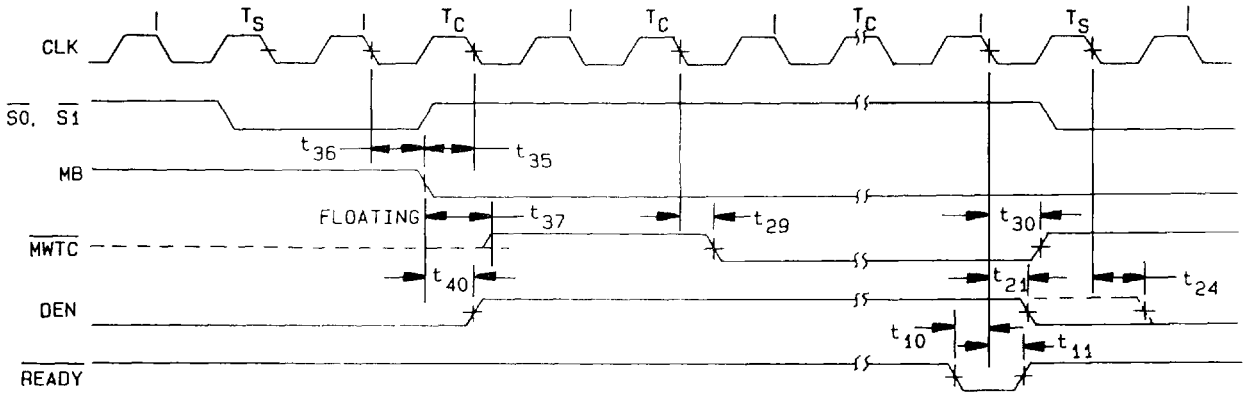
CEN CHARACTERISTICS WITH MB = 0

FIGURE 3. Switching waveforms and test circuit - Continued.



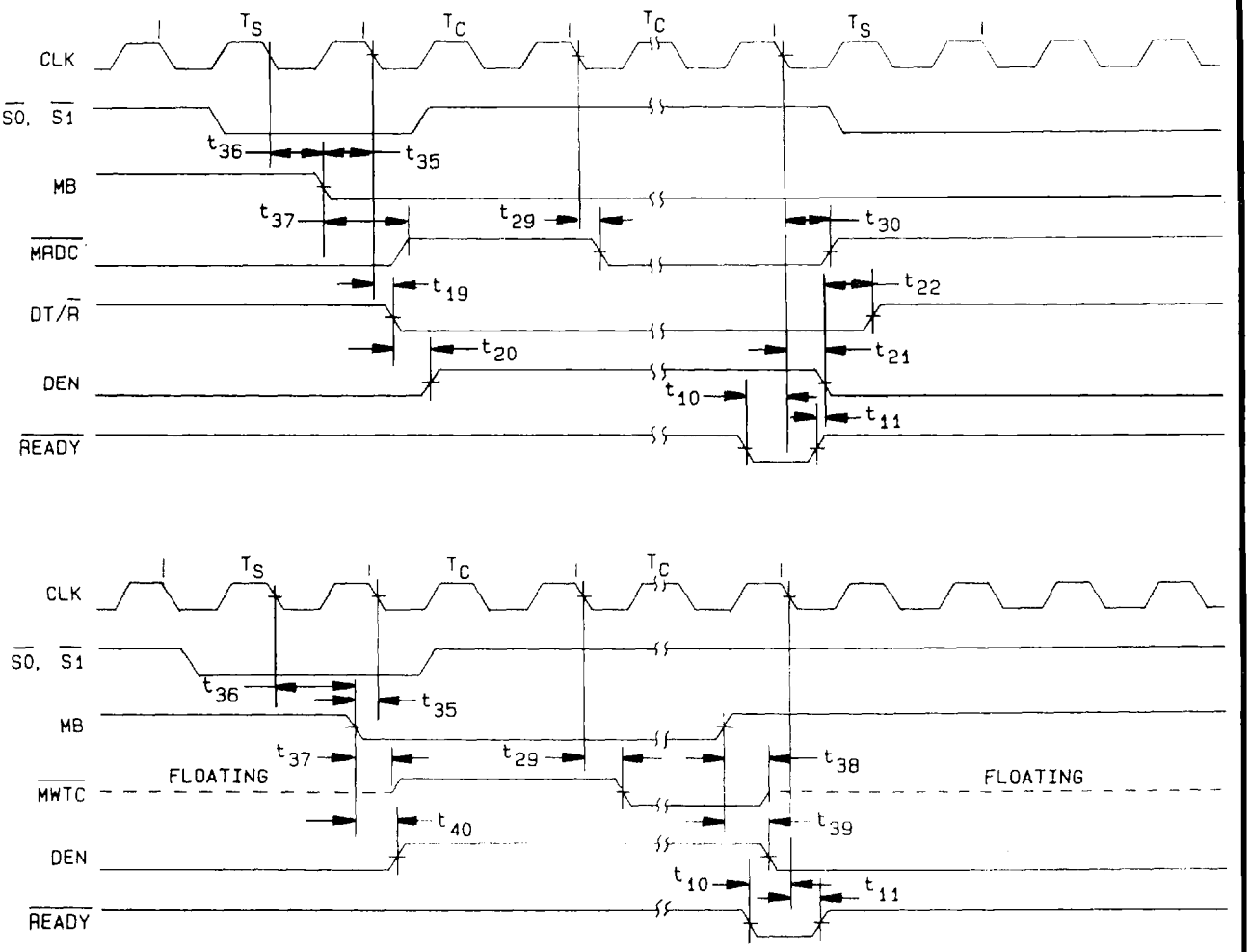
AEN CHARACTERISTICS WITH MB = 1

NOTE: AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.



MB CHARACTERISTICS WITH AEN/CEN = HIGH

FIGURE 3. Switching waveforms and test circuit - Continued.



MB CHARACTERISTICS WITH $\overline{AEN}$/CEN = HIGH (CONTINUED)

NOTES:
1. MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.
2. If the setup time, t35, is met two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

FIGURE 3. Switching waveforms and test circuit - Continued.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall consist of verifying the functionality of the device. These tests form a part of the vendor's test tape and shall be maintained and available from the approved sources of supply. For device classes B and S, subgroups 7 and 8 tests shall include verification of the device functionality as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{CLK}, C_{IN} and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1,7		1,7
Final electrical parameters (see 4.2)	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,2,3,7,8 9,10,11		1,2,3,7,8 9,10,11
Group C end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10		2,8a,10	
Group D end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,7,8a,10	2,8a,10	2,7,8a,10
Group E end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Symbols, definitions, and functional descriptions.

Symbol	Type	Name and function
CLK	1	System clock provides the basic timing control for the device. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.
$\overline{S0}$, $\overline{S1}$	1	Bus cycle status starts a bus cycle and, along with M/$\overline{IO}$, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either $\overline{S1}$ or $\overline{S0}$ is sampled LOW at the falling edge of CLK. Setup and hold times must be met for proper operation.

Bus Cycle Status Definition

$\overline{M/IO}$	$\overline{S1}$	$\overline{S0}$	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None; Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None; Idle

6.5 Symbols, definitions, and functional descriptions - Continued.

Symbol	Type	Name and function
M/$\overline{IO}$	1	Memory or I/O select determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.
MB	1	Multibus mode select determines timing of the command and control outputs. When HIGH, the bus controller operates with MULTIBUS 1 compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/AEN input pin is selected by this signal. This input is typically a strapping option and not dynamically changed.
CENL	1	Command enable latched is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the end of each T_S cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select the device for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.
CMDLY	1	Command delay allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If READY is detected LOW before the command output is activated, the device will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command. This input has no effect on the device control outputs.
$\overline{READY}$	1	READY indicates the end of the current bus cycle. $\overline{READY}$ is an active LOW input. MULTIBUS 1 mode requires at least one wait state to allow the command outputs to become active. READY must be LOW during reset, to force the device into the idle state. Setup and hold times must be met for proper operation.
CEN/$\overline{AEN}$	1	Command enable/address enable controls the command and DEN outputs of the bus controller. CEN/AEN inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is HIGH this pin has the $\overline{AEN}$ function. $\overline{AEN}$ is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). AEN HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not tri-state them.

6.5 Symbols, definitions, and functional descriptions - Continued.

Symbol	Type	Name and function
ALE	O	Address latch enable controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	Master cascade enable signals that a cascade address from a master interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	Data enable controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the MULTIBUS 1 mode.
DT/$\overline{R}$	O	Data transmit/receive establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/R changes states. This output is HIGH when no bus cycle is active. DT/R is not affected by any of the control inputs.
$\overline{IOWC}$	O	I/O write command instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY input control when this output becomes active. READY controls when it becomes inactive.
$\overline{IORC}$	O	I/O read command instructs an I/O device to place the data onto the data bus. This command output is active LOW. The MB and CMDLY input control when this output becomes active. READY controls when it becomes inactive.
$\overline{MWTC}$	O	Memory write command instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
$\overline{MRDC}$	O	Memory read command instructs the memory device to place the data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
$\overline{INTA}$	O	Interrupt acknowledge tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.

6.5 Symbols, definitions, and functional descriptions - Continued.

Symbol	Type	Name and function
V_{CC}		System power: +5 V power supply
GND		System ground: 0 V

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-10-22

Approved sources of supply for SMD 5962-90997 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9099701MRX	34649	MD82C288-6
5962-9099702MRX	34649	MD82C288-8
5962-9099703MRX	34649	MD82C288-10

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 W. Williams Field Road Chandler, AZ 85224