MSH60N35D

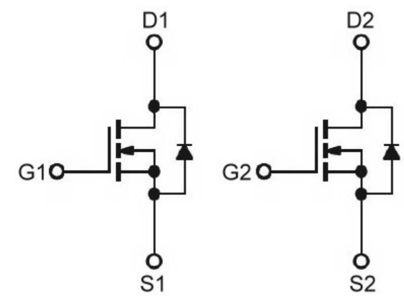
Dual N-Channel 60-V (D-S) MOSFET

Description

The device uses advanced Trench technology and designs to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Graphic Symbol



Features

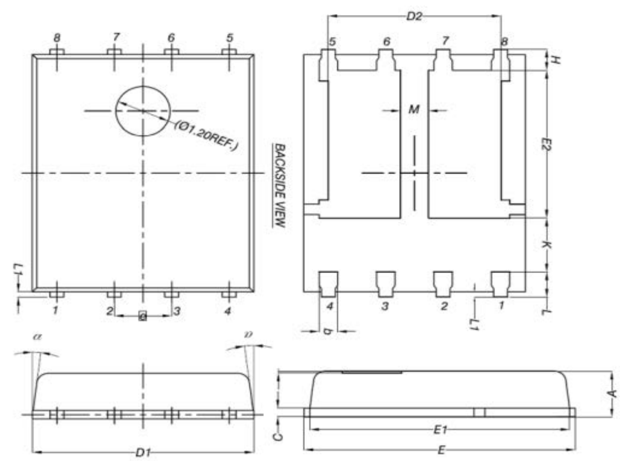
- $R_{DS(ON)}$ =20mΩ@ V_{GS} =10V
- Low Miller Charge
- Low Input Capacitance
- 100% EAS Guaranteed
- Green Device Available

Typical Applications

- Motor Drive
- Power Tools
- LED Lighting

Package type：PDFN 5X6 Dual

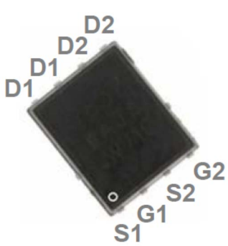
Package Dimension



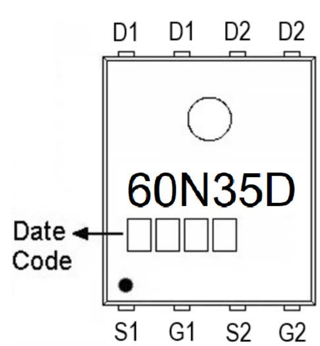
REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.90	1.10	1.10	E2	3.38	3.58	3.78
b	0.33	0.41	0.51	H	0.41	0.51	0.61
C	0.20	0.25	0.30	K	1.10	-	6.20
D1	4.80	4.90	5.00	L	0.51	0.61	0.71
D2	3.61	3.81	3.96	L1	0.06	0.13	0.20
E	5.90	6.00	6.10	M	0.50	-	-
E1	5.70	5.75	5.80	a	0℃	-	12°C
e	1.27 BSC						

Packing & Order Information

3,000/Reel



Marking



RoHS Compliant

Brückewell

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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	35	A
	Continuous Drain Current[1] (T_C =100°C)	22	A
I_{DM}	Pulsed Drain Current[1,2]	80	A
I_{AS}	Single Pulse Avalanche Current, L =0.1mH[3]	28	A
E_{AS}	Single Pulse Avalanche Energy, L =0.1mH[3]	39.2	mJ
P_D	Power Dissipation[4] (T_C =25°C)	45	W
	Power Dissipation[4] (T_A =25°C)	2	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{θJA}$	Maximum Junction-to-Ambient[1]	62	°C/W
$R_{θJC}$	Maximum Junction-to-Case[1]	5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	1.2	1.7	2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	60	-	-	V
g_{fs}	Forward Transconductance	V_{DS} =5V, I_D =15A	-	45	-	S
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =48V, V_{GS} =0V, T_J =25°C V_{DS} =48V, V_{GS} =0V, T_J =125°C	-	-	1 5	μA
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =10V, I_D =20A V_{GS} =4.5V, I_D =15A	- -	- -	20 24	mΩ
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =25V, L =0.1mH, I_{AS} =14A	9.8	-	-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =1A, V_{GS} =0V, T_J =25°C	-	-	1.0	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	35	A
I_{SM}	Pulsed Source Current[2,6]		-	-	80	

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Dynamic						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Q_g	Total Gate Charge[2]	V_{DS} =48V I_D =15A V_{GS} =4.5V	--	19.3	--	nC
Q_{gs}	Gate-Source Charge		--	7.1	--	
Q_{gd}	Gate-Drain (“Miller”) Charge		--	7.6	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DD} =30V I_D =15A V_{GS} =10V R_G =3.3Ω	--	7.2	--	ns
t_r	Rise Time		--	50	--	
$t_{d(off)}$	Turn-Off Delay Time		--	36.4	--	
t_f	Fall Time		--	7.6	--	
C_{ISS}	Input Capacitance	V_{DS} =15V V_{GS} =0V f =1.0MHz	--	2423	--	pF
C_{OSS}	Output Capacitance		--	145	--	
C_{RSS}	Reverse Transfer Capacitance		--	97	--	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	1.7	--	Ω

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=28A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- **Typical Electrical Characteristics**

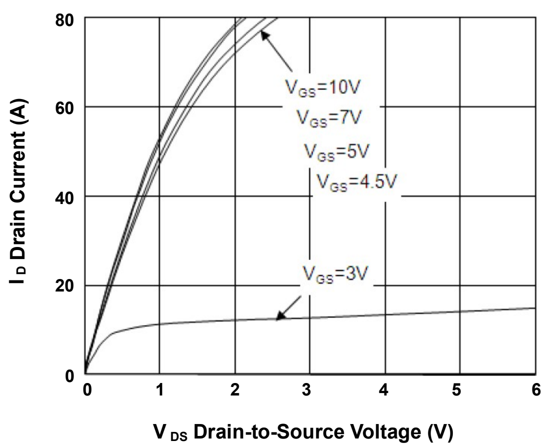

FIG.1-Typical Output Characteristics

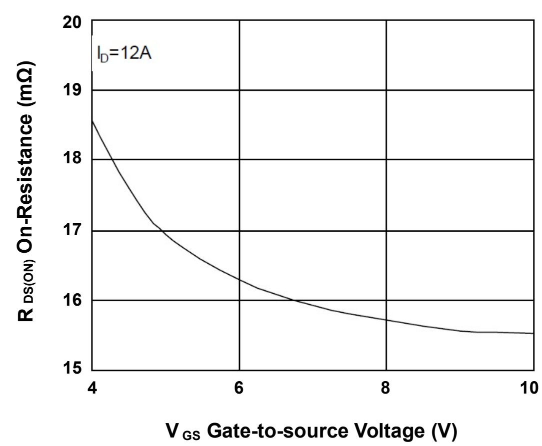

FIG.2-On-Resistance vs. G-S Voltage

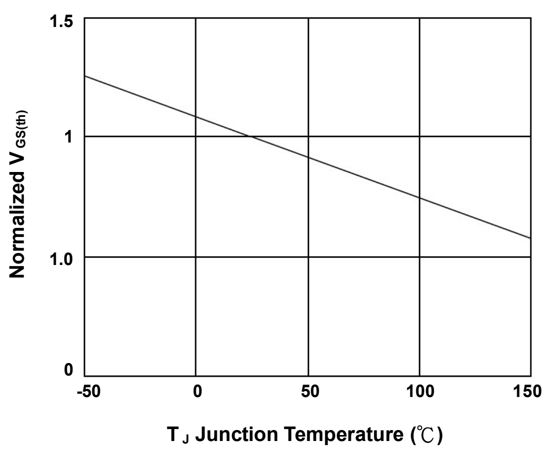

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

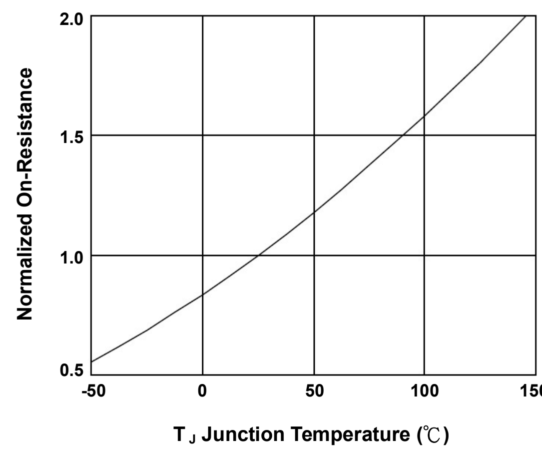

FIG.4-Normalized R_{DSON} vs. T_J

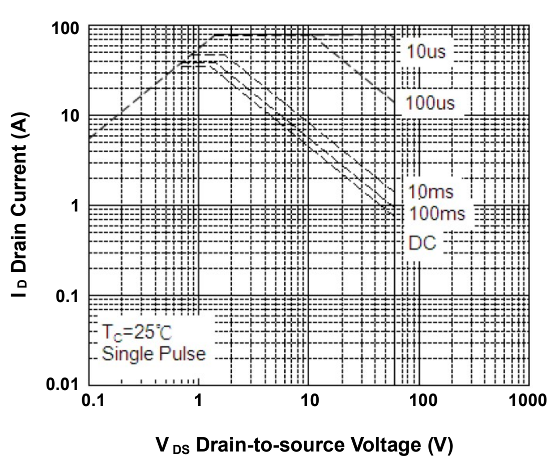

FIG.5-Safe Operating Area

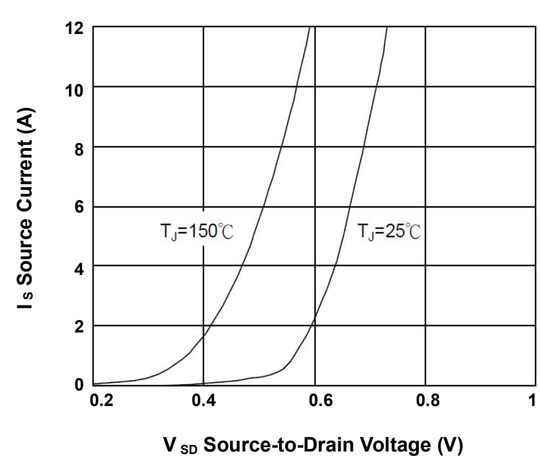

FIG.6-Forward Characteristics of Reverse

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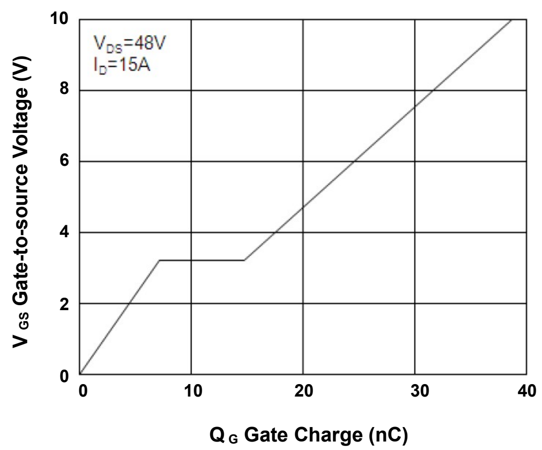

FIG.7-Gate Charge Characteristics

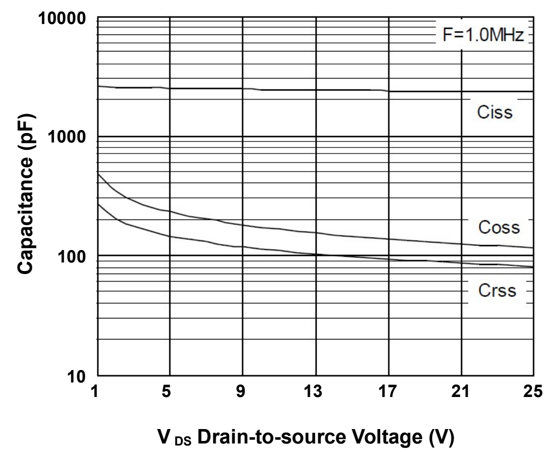

FIG.8-Capacitance Characteristics

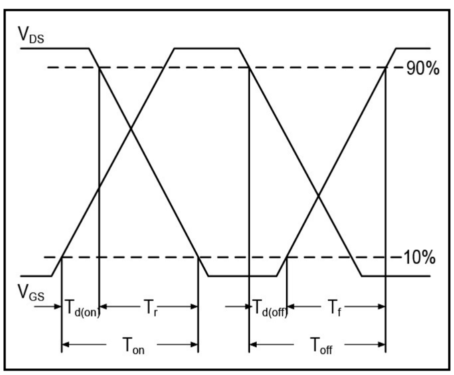

FIG.9-Switching Time Waveform

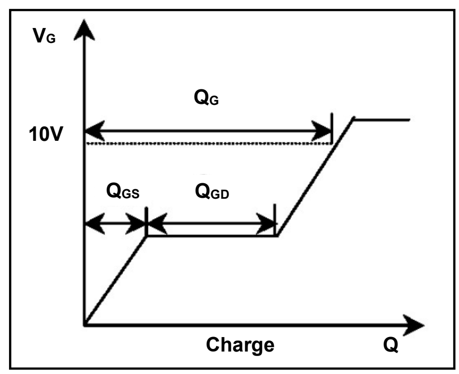

FIG.10-Gate Charge Waveform

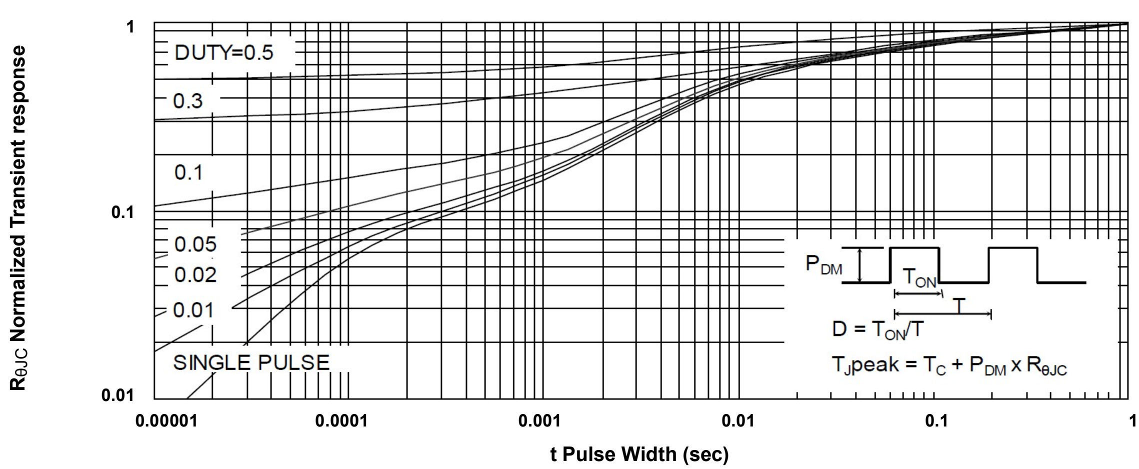

FIG.11-Normalized Maximum Transient Thermal Impedance

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