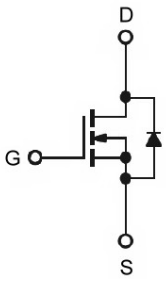
MSB100N023

N-Channel 100-V (D-S) MOSFET

Description

The device is using trench DMOS technology. This advanced technology has been especially tailored to minimize $R_{DS(ON)}$, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Graphic Symbol



Features

- $R_{DS(ON)}$ =2.3mΩ@ V_{GS} =10V
- Fast switching
- Improve dv/dt Capability
- 100% EAS Guaranteed
- Green Device Available

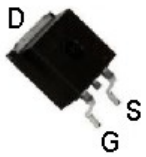
Typical Applications

- Networking
- Load Switch
- Synchronous Rectifier
- BMS Applications

Package type：TO-263

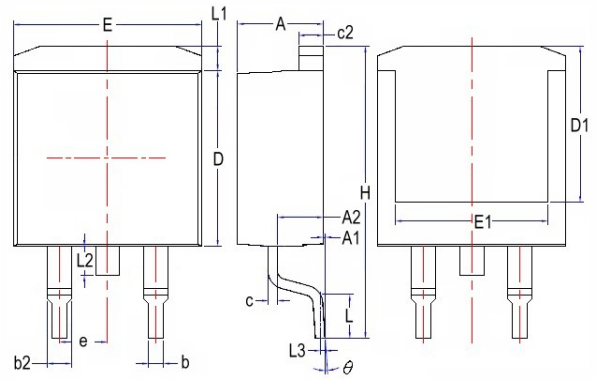
Packing & Order Information

800/Reel



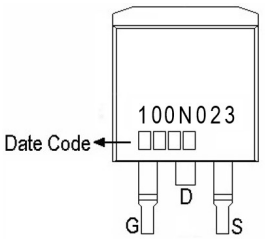
RoHS Compliant

Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.37	4.77	E	9.80	10.36
A1	0.00	0.25	E1	7.06	-
A2	2.20	2.80	e	2.54 BSC	
b	0.70	0.96	H	14.70	15.70
b2	1.17	1.47	L	2.00	2.60
c	0.30	0.60	L1	1.07	1.47
c2	1.22	1.42	L2	1.40	1.75
D	8.50	9.30	L3	0.25 BSC	
D1	6.60	-	θ	0°	9°

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	250	A
	Continuous Drain Current[1] (T_C =100°C)	158	A
I_{DM}	Pulsed Drain Current[1,2]	1000	A
I_{AS}	Single Pulse Avalanche Current, L =0.1mH[3]	137	A
E_{AS}	Single Pulse Avalanche Energy, L =0.1mH[3]	938	mJ
P_D	Power Dissipation[4] (T_C =25°C)	278	W
	Power Dissipation[4] (T_A =25°C)	2	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-50 to +150	°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	62.5	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case[1]	0.45	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	2	2.5	4	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	100	-	-	V
g_{fs}	Forward Transconductance	V_{DS} =10V, I_D =3A	-	20	-	S
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =20V	-	-	100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =100V, V_{GS} =0V, T_J =25°C V_{DS} =80V, V_{GS} =0V, T_J =85°C	-	-	1 10	μA
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =10V, I_D =40A	-	1.9	2.3	mΩ
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =50V, L =0.1mH, I_{AS} =60A	180	-	-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =1A, V_{GS} =0V, T_J =25°C	-	-	1	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	250	A
I_{SM}	Pulsed Source Current[2,6]		-	-	500	

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=60A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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Dynamic						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Q_g	Total Gate Charge[2]	V_{DS} =50V I_D =100A V_{GS} =10V	--	192	--	nC
Q_{gs}	Gate-Source Charge		--	18.5	--	
Q_{gd}	Gate-Drain Charge		--	28.3	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DS} =50V I_D =100A V_{GS} =10V R_G =3.3Ω	--	20.6	--	ns
t_r	Rise Time		--	19.8	--	
$t_{d(off)}$	Turn-Off Delay Time		--	66	--	
t_f	Fall Time		--	117	--	
C_{ISS}	Input Capacitance	V_{DS} =50V V_{GS} =0V f =1.0MHz	--	10100	--	pF
C_{OSS}	Output Capacitance		--	2020	--	
C_{RSS}	Reverse Transfer Capacitance		--	53	--	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	1.1	--	Ω

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- **Typical Electrical Characteristics**

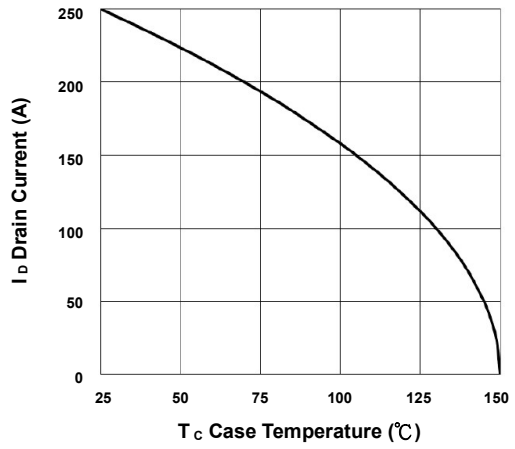

FIG.1-Drain Current vs. T_C

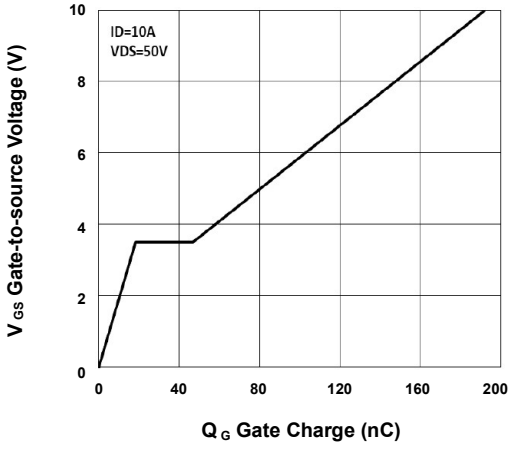

FIG.2-Gate Charge Characteristics

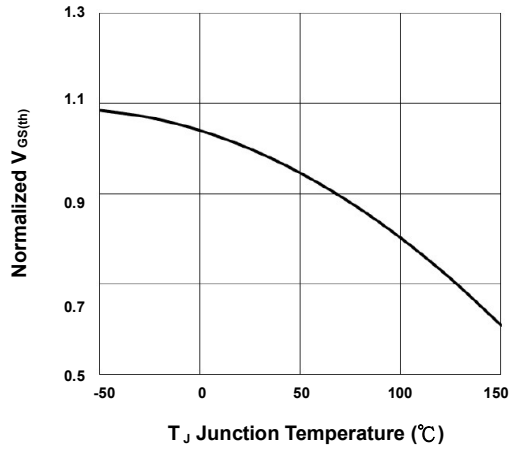

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

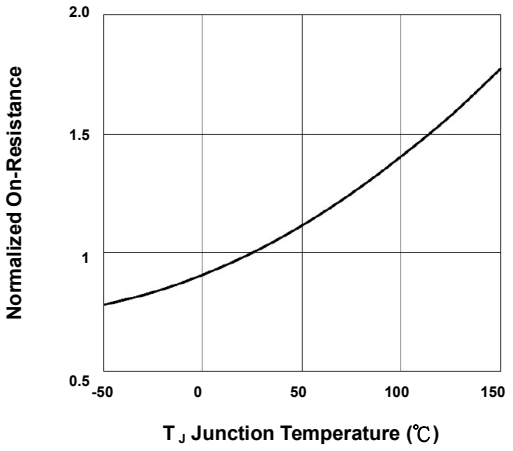

FIG.4-Normalized R_{DSON} vs. T_J

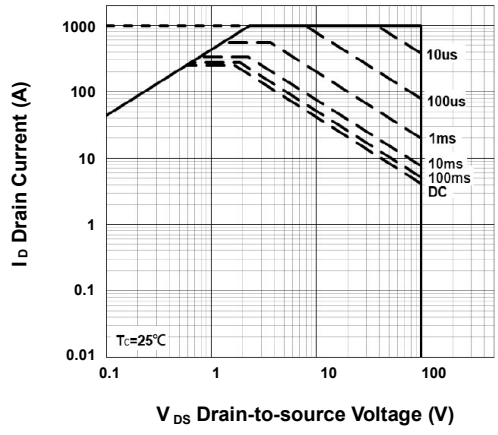

FIG.5-Safe Operating Area

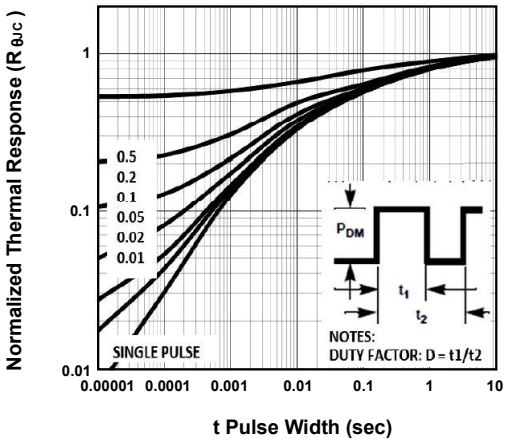

FIG.6-Transient Thermal Impedance

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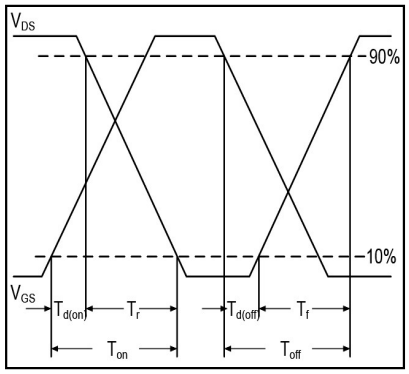

FIG.7-Switching Time Waveform

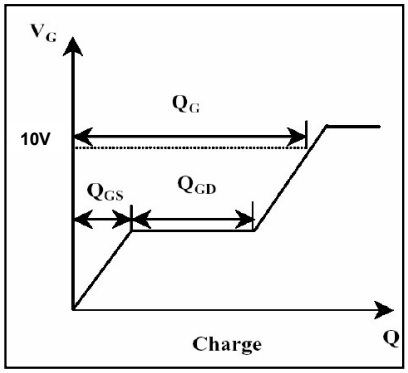

FIG.8-Gate Charge Waveform

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