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T-49-17-34

Intel386™ SL MICROPROCESSOR SuperSet

Highly-Integrated Static Intel386™ SL Microprocessor

Complete ISA Peripheral Subsystem

System-Wide Power Management

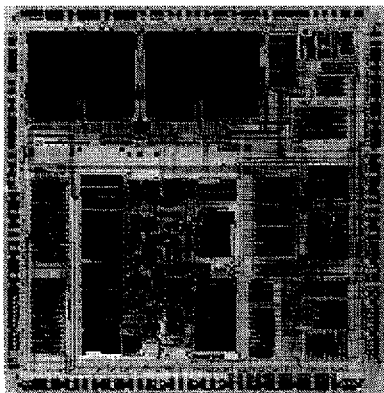
- **Static Intel386™ SL CPU**
 - Runs MS-DOS*, WINDOWS*, OS/2** and UNIX***
 - Object Code Compatible with Intel 8086, 80286 and Intel386 Microprocessors
- **Architecture Extension for Power Management Transparent to Operating Systems and Applications**
- **Complete ISA System, with Extended Support**
 - Full ISA Bus Control, Status and Address and Data Interface Logic
 - Compatible ISA Bus Peripherals
 - System I/O Decoding, Programmable Chip Selects and Support Interfaces
- High-Speed Peripheral Interface Bus (PI-Bus Support)
- New ideaPort Interface for Hardware Expansion
- **Integrated Cache Controller and Tag RAM (Optional)**
 - No-Glue Cache SRAM Interface
 - 16k, 32k, or 64 kByte Cache Size
 - Direct, 2-Way or 4-Way Set Associative Organization
- **Programmable Memory Control**
 - No-Glue, Page-Mode DRAM Interface
 - SRAM Support for Lowest Power
 - 512k to 32 MBytes
 - Full Hardware LIM EMS 4.0

The Intel386 SL Microprocessor SuperSet combines an ISA bus compatible personal computer's microprocessor, memory controller, cache controller and peripheral subsystems into just two Very Large Scale Integration (VLSI) devices. The product's high-integration and power conservation features reduce the size and power consumption typically associated with fully Industry Standard Architecture (ISA) bus compatible systems. In addition, new expandability and flexibility features offer the capability for continued innovation in battery-operated, space-constrained systems. The SL SuperSet brings 100% ISA-Bus compatibility to system designs ranging from the smallest palm-top and notebook PCs to expandable lap-top systems.

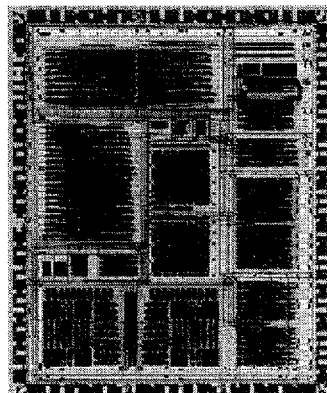
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**OS/2 is a trademark of International Business Machines Corporation.

***UNIX is a trademark of UNIX System Laboratories, Inc.



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Figure 1-1. Die Photograph of the Intel386™ SL Microprocessor (left) and 82360SL ISA Peripheral I/O (right)



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Intel386™ SL MICROPROCESSOR
Intel386™ Microprocessor Core, with
Integrated Memory and Cache Controllers and
System Power Management
Fully-Static CHMOS IV Technology

- **Static Intel386™ SL CPU**
 - Optimized and Compatible with Standard Operating System Software such as:
MS-DOS, WINDOWS, OS/2 and UNIX
 - Object Code Compatible with Intel 8086, 80286 and Intel386™ Microprocessors
 - Runs All Desk-Top Applications, 16- or 32-Bit
 - D.C. to 25 MHz Operation
 - 20 Megabytes Physical Memory/
64 Terabytes Virtual Memory
 - 4 Gigabyte Maximum Segment Size
 - High Integration, Low Power Intel CHMOS IV Process Technology
- **Transparent Power-Management System Architecture**
 - System Management Mode Architecture Extension for Truly Compatible Systems
 - Power Management Transparent to Operating Systems and Application Programs
 - Programmable Hardware Supports Custom Power-Control Methods
- **Direct Drive Bus Interfaces**
 - Full ISA Bus Interface
 - High Speed Peripheral Interface Bus
- **Integrated Cache Controller and Tag RAM**
 - No-Glue Cache SRAM Interface
 - 16k, 32k, or 64 kByte Cache Size
 - Direct, 2-Way or 4-Way Set Associative Organization
 - Write Posting—Posted Memory Writes
 - 16-Bit Line Size—Reduces Bus Utilization for Cache Line Fills
 - Write-Thru, with SmartHit Algorithm for Reduced Main Memory Power Consumption
- **Programmable Memory Control**
 - No-Glue, Page-Mode DRAM Interface
 - SRAM Support for Lowest Power (Standard 5V Mode Only)
 - 1, 2, or 4 Banks Interleaved, with Programmable Wait States
 - 512k to 20 MBytes
 - Advanced, Flexible Address-Map Configuration
 - Full Hardware LIM EMS 4.0 Address Translation to 32 Megabytes without Waitstate Penalty
- **3.3 CPU core with FlexibleVoltage Interfaces (Optional)**
 - Pin-Compatible with Standard 5V CPU
 - Flexible 5V/3.3V ISA/PI Bus Interface
 - 50% Power Savings

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82360SL I/O Subsystem
Complete ISA Peripheral Subsystem
Integrated System Power Management
Fully-Static CHMOS IV Technology

- **Complete ISA System, with Extended Support**
 - Full ISA Bus Control, Status and Address and Data Interface Logic, with Full 24 mA Drive
 - Compatible ISA Bus Peripherals:
 - Two 8237 Direct Memory Access Controllers
 - Two 8254 Programmable Timer Counters (6 Timer/Counter Channels)
 - Two 8259A Programmable Interrupt Controllers (15 Channels)
 - Enhanced LS612 Page Memory Mapper
 - One 146818 Compatible Real Time Clock w/256-byte CMOS RAM
 - Two 16450 Compatible Serial Port Controllers
 - One 8-Bit Parallel I/O Port with High Speed Protocol (Centronics or Bi-Directional)
 - Additional System I/O Decoding, Programmable Chip Selects and Support Interfaces:
 - Full Integrated Drive Electronics (I.D.E.) Hard Disk Interface
 - Floppy Disk Controller
 - Keyboard Controller Chip Selects and Support Logic
- External Real Time Clock Support
- PS/2 and EISA Control/Status Ports
- Local Memory and ISA-Bus Memory Refresh Control
- New IdeaPort Interface for Hardware Expansion
- **Transparent Power-Management System Architecture**
 - Architecture Extension for Truly Compatible Systems
 - Transparent to Operating Systems and Applications Programs
 - Programmable Hardware Supports Custom Power-Control Methods
 - Integrated Power Management Unit Manages Power-Events Safely



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Intel386™ SL MICROPROCESSOR SuperSet

Intel386™ SL CPU and 82360SL I/O

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1.0 INTRODUCTION

This document provides the pinouts, signal descriptions, and D.C./A.C. electrical characteristics of the Intel386™ SL CPU and 82360SL ISA I/O Peripheral device. Consult Intel for the most recent design-in information. For a thorough description of any functional topic, other than the parametric specifications, please consult the latest Intel386 SL Microprocessor SuperSet System Design Guide (Order No. 240816), and the Intel386 SL Microprocessor SuperSet Programmer's Guide (Order No. 240815).

1.1 Overview of System Architecture

The Intel386 SL Microprocessor SuperSet is an extremely flexible pair of components marking a new milestone in microcomputer technology. Included in the pair are an Intel386 Architecture Central Processing Unit (CPU), a memory subsystem controller capable of controlling either DRAM or SRAM, address translation and remapping logic, an optional cache memory controller and an extensive collection of ISA bus compatible peripheral functions.

The SL SuperSet allows the personal computer designer to take advantage of the highest level of system integration, while preserving complete freedom

in selecting system features, power/performance trade-offs, and value-added enhancements.

Essentially, all of the components needed to build an ISA bus compatible personal computer have been combined within just two components: the Intel386 SL Microprocessor and memory control system, and the 82360SL ISA peripheral I/O and power management subsystem. The only other components needed for a complete personal computer are the main DRAM or optional static memory subsystem, optional cache SRAM and a graphics controller. A minimal amount of commodity Small Scale Integration (SSI) logic or Medium Scale Integration (MSI) logic buffers may be required for design-specific interface to peripheral devices on the ISA bus.

Systems based on the SL SuperSet typically include the functional blocks shown in Figure 1.2.

The Intel386 SL CPU is available to operate in **flexible, pin compatible modes: standard 5V and FlexibleVoltage configurations.** The addition of an internal 3.3V plane to power the CPU core and the majority of the internal logic modules is the most substantial difference between the two configurations. Refer to the table below for specific voltage differences.

Table 1.1. Intel386™ SL CPU Voltage Options

Module	Standard (All 5V)	FlexibleVoltage (Low-Voltage)
CPU Core	5V	3.3V
Memory Bus Interface	5V	3.3V
ISA/PI Bus Interface	5V	5V/3.3V*
Math Coprocessor Interface	5V	3.3V

*For more information on 3.3V support, please contact your local Intel Field Sales Office.

For a complete list of products in the Intel386 SL family, refer to the following table.

Table 1.2. Intel386™ SL CPU Family

Features	Options			
	20/25	16/20/25	20	16/20
CPU Frequency (Mhz)	20/25	16/20/25	20	16/20
Cache Support	Cache	Cacheless	Cache	Cacheless
Voltage Options	All 5V	All 5V	FlexibleVoltage	Flexible Voltage
Packaging	PQFP/LGA	PQFP/LGA	PQFP	PQFP

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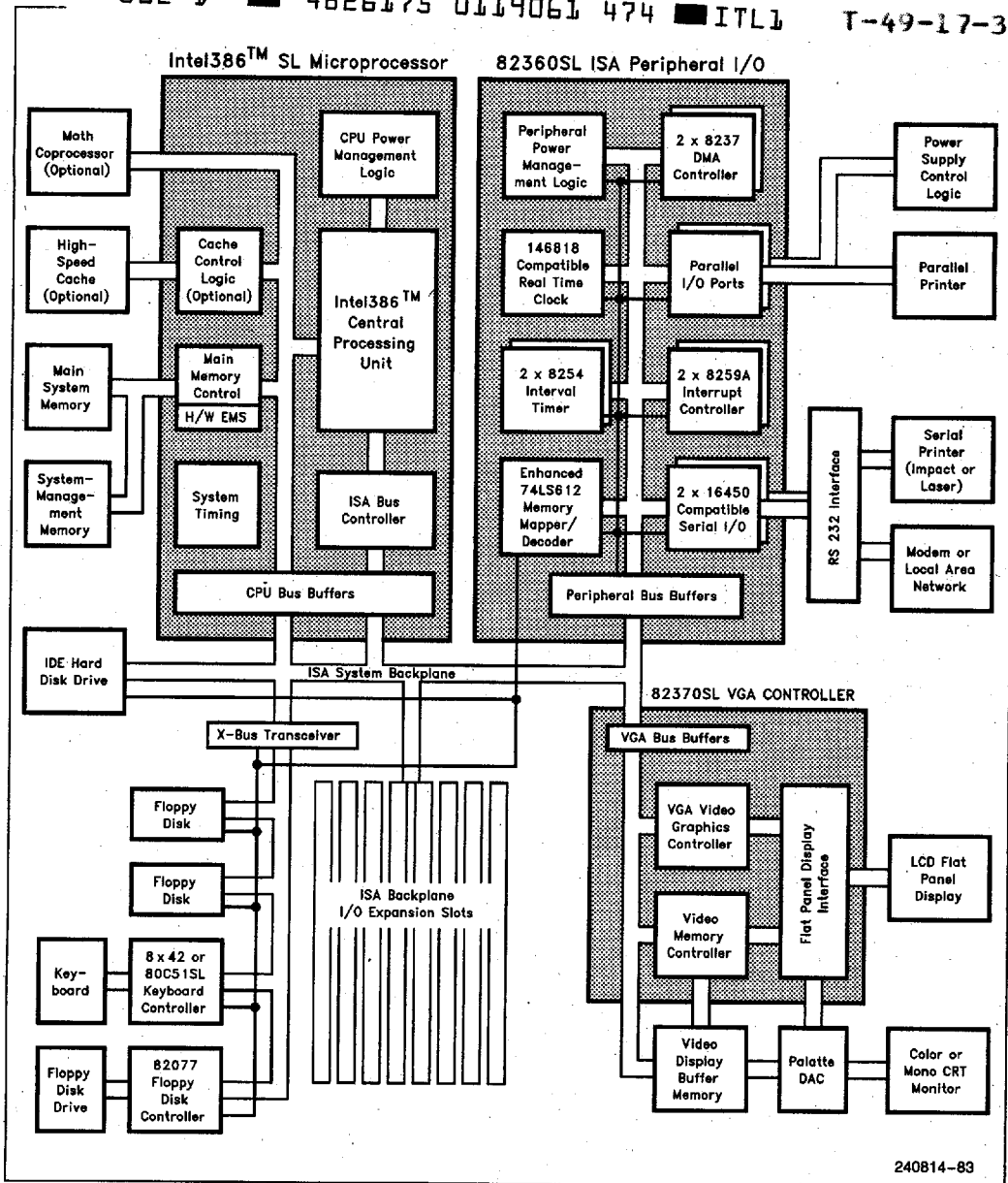
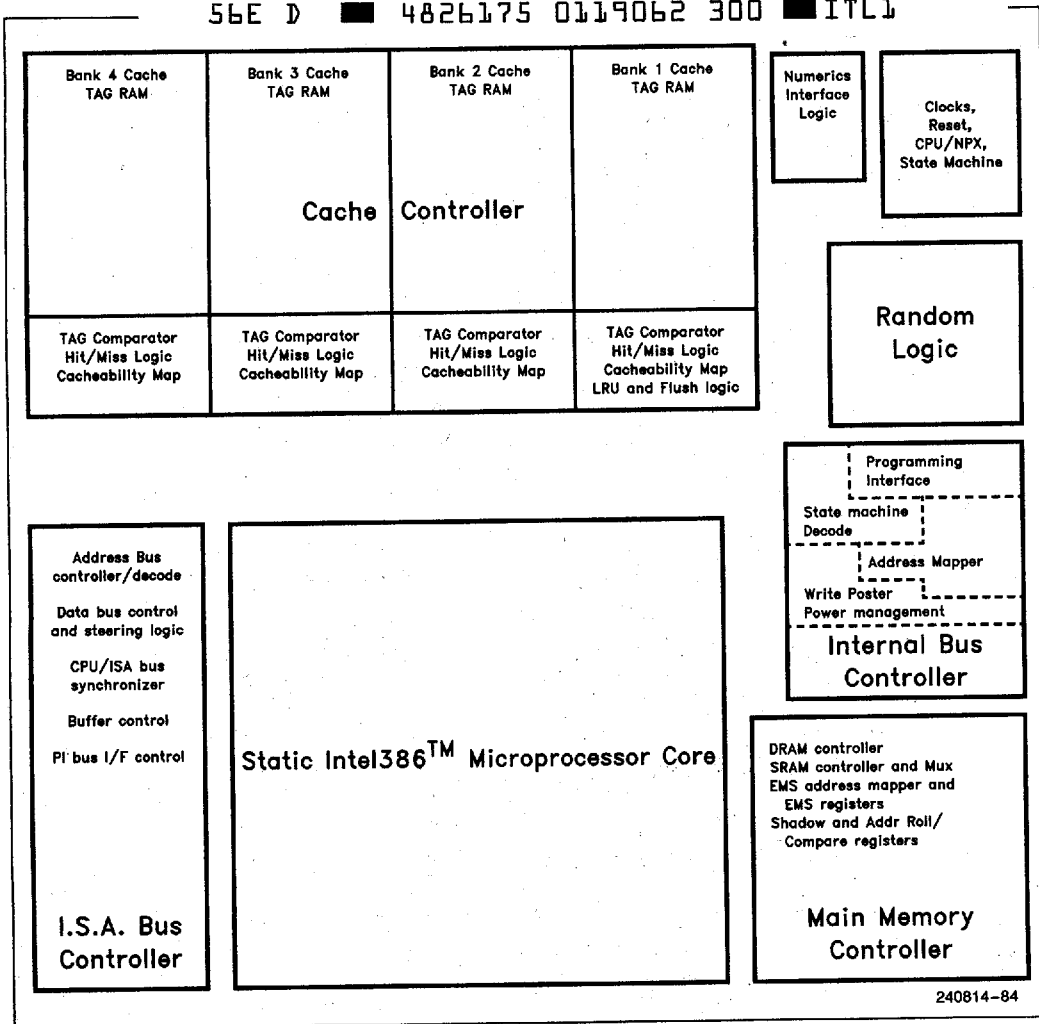


Figure 1.2. Intel386™ SL Microprocessor-Based System Functional Block Diagram

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Figure 1.3a. Intel386™ SL Microprocessor Internal Functional Modules

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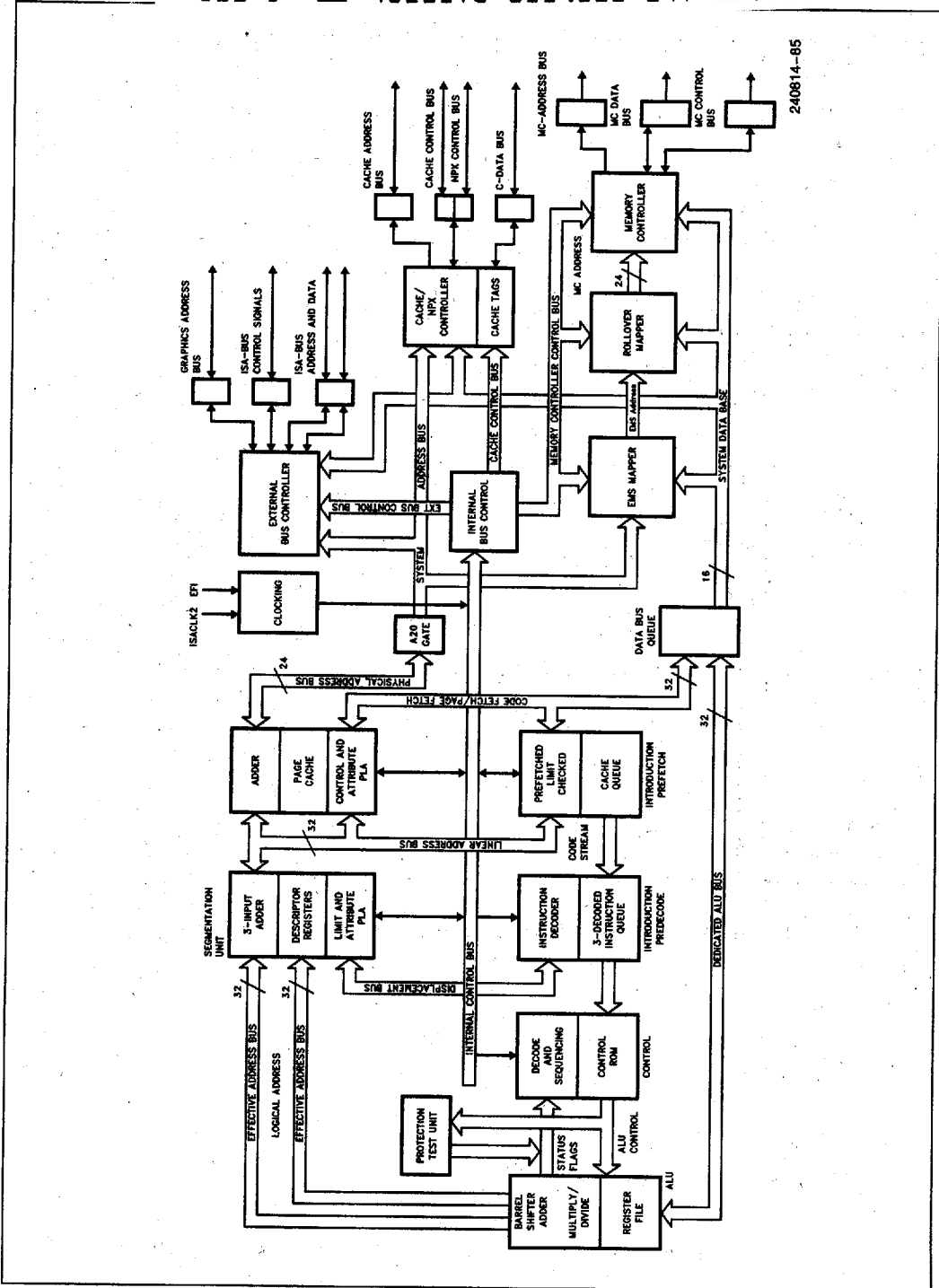


Figure 1.3b. Intel386™ SL Microprocessor Micro-Architecture

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Intel386™ SL SuperSet

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1.2 Intel386™ SL Microprocessor: Central Processing Unit (CPU) and Memory Controller Subsystem

The Intel386 SL Microprocessor is a highly-integrated, complete microprocessor and memory controller subsystem. At the heart of the Intel386 SL Microprocessor is a CHMOS static Intel386 SL CPU core. The Intel386 SL CPU core has been fully optimized to reduce run-time power requirements, and includes a key architectural extension required by battery-operated systems.

The Intel386 SL processor is the first member of the Intel386 Microprocessor product line to implement a CPU with the System Management Mode extension. The System Management Mode is a new CPU operating-mode which allows system vendors to rid their systems of the backwards-compatibility problems that plague battery-operated PCs. This Intel386 architecture extension eliminates portable-system conflicts by providing a safe, new operating level for the battery management firmware developed by system designers. With the Intel386 SL CPU, firmware will execute transparently to every application, operating system and CPU mode, thus avoiding the compatibility conflicts which were once unavoidable.

The Intel386 SL Microprocessor retains the paged memory-management system, and all the other key features which are common to the Intel386 architecture. In addition, on-chip hardware implements the Expanded Memory Specification (E.M.S.) address translation compatible with the current Lotus/Intel/Microsoft (L.I.M.) E.M.S. 4.0 standard. Additional address-mapping and control logic integrated in the Intel386 SL CPU allows BIOS ROMs to be "shadowed" by faster memory devices, and supports a variety of common memory roll-over and back-fill schemes. The Intel386 SL CPU contains all of the control and interface logic needed to directly drive large main memory and an optional cache memory subsystem.

The Intel386 SL CPU contains bus drivers and control circuitry for two expansion interfaces. A Peripheral Interface Bus (PI-Bus) provides high-speed communication with fast devices such as VGA and FLASH Disk. The Industry Standard Architecture (ISA) bus provides a common interface for the wealth of third party ISA bus compatible I/O peripheral and expansion memory add-in boards. On-chip data-byte steering logic, address decoding and mapping logic automatically routes each memory or I/O operation to the appropriate local memory, cache, PI-Bus or ISA expansion bus.

All system configuration logic in the Intel386 SL processor subsystem is initialized under software control.

The system designer only has to program the processor in order to support multiple system hardware designs where many devices of less flexibility were once required. System characteristics such as memory type, size, speed, organization, and mapping; cache size, organization and mapping; and peripheral selection, configuration and mapping are configured under software control. Thereafter, all memory and I/O transfer requests are automatically sent to the appropriate memory space or expansion bus, fully-transparent to existing operating system software and application programs.

Figure 1.3a shows the functional blocks and Figure 1.3b shows the microarchitecture of the Intel386 SL processor.

1.3 Intel386™ SL Microprocessor with FlexibleVoltage Operation

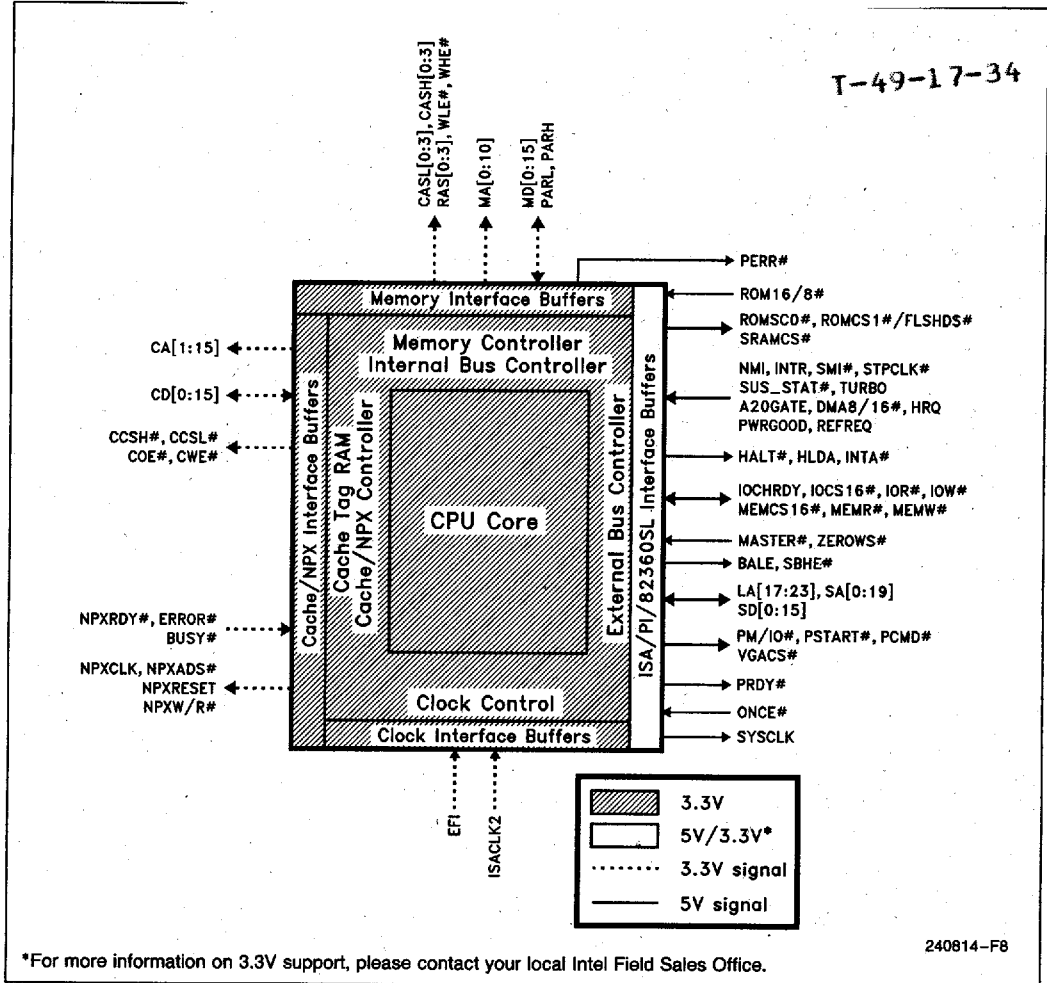
The Intel386 SL CPU in FlexibleVoltage mode achieves low power consumption by supporting lower voltage operation. The majority of the CPU internal logic is powered by 3.3V. The interfaces to local DRAM, Cache SRAM, and Math Coprocessor are also powered by 3.3V. The ISA/PI bus interfaces can be powered by 5V or 3.3V. This ensures the reusability of CPU with existing 5V and future 3.3V ISA bus peripherals and I/O devices. Figure 1.4 shows the internal power plane partitioning of the low-voltage Intel386™ SL CPU.

The Intel386 SL CPU, when combined with 82360SL I/O, provides the majority of the core logic required to design a high integration ISA-Bus compatible personal computer. Other system components not integrated in the CPU or 82360SL include: a Graphics Controller and Display Subsystem, a Keyboard Controller and keyboard/mouse, removable storage (such as floppy disk controller/floppy disk drive or PCMCIA FLASH memory card), fixed storage (such as an I.D.E. hard disk drive), DRAM system memory (such as on-board DRAM or a JEIDA/JEDEC 88-pin DRAM memory card), and BIOS/User/Graphics ROM (such as EPROM or FLASH). The Intel 80C51SL Keyboard Controller, 82365SL PCMCIA I/F Controller, 82077SL Floppy Controller and a third party graphics controller may be used to create a full-function transportable personal computer. A typical system based on the Intel386 SL CPU in FlexibleVoltage mode is shown in Figure 1.5, in which the powering of various interfaces is explicitly depicted.

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*For more information on 3.3V support, please contact your local Intel Field Sales Office.

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Figure 1.4. Power Plane Partitioning of the Intel386™ SL CPU with FlexibleVoltage Operation

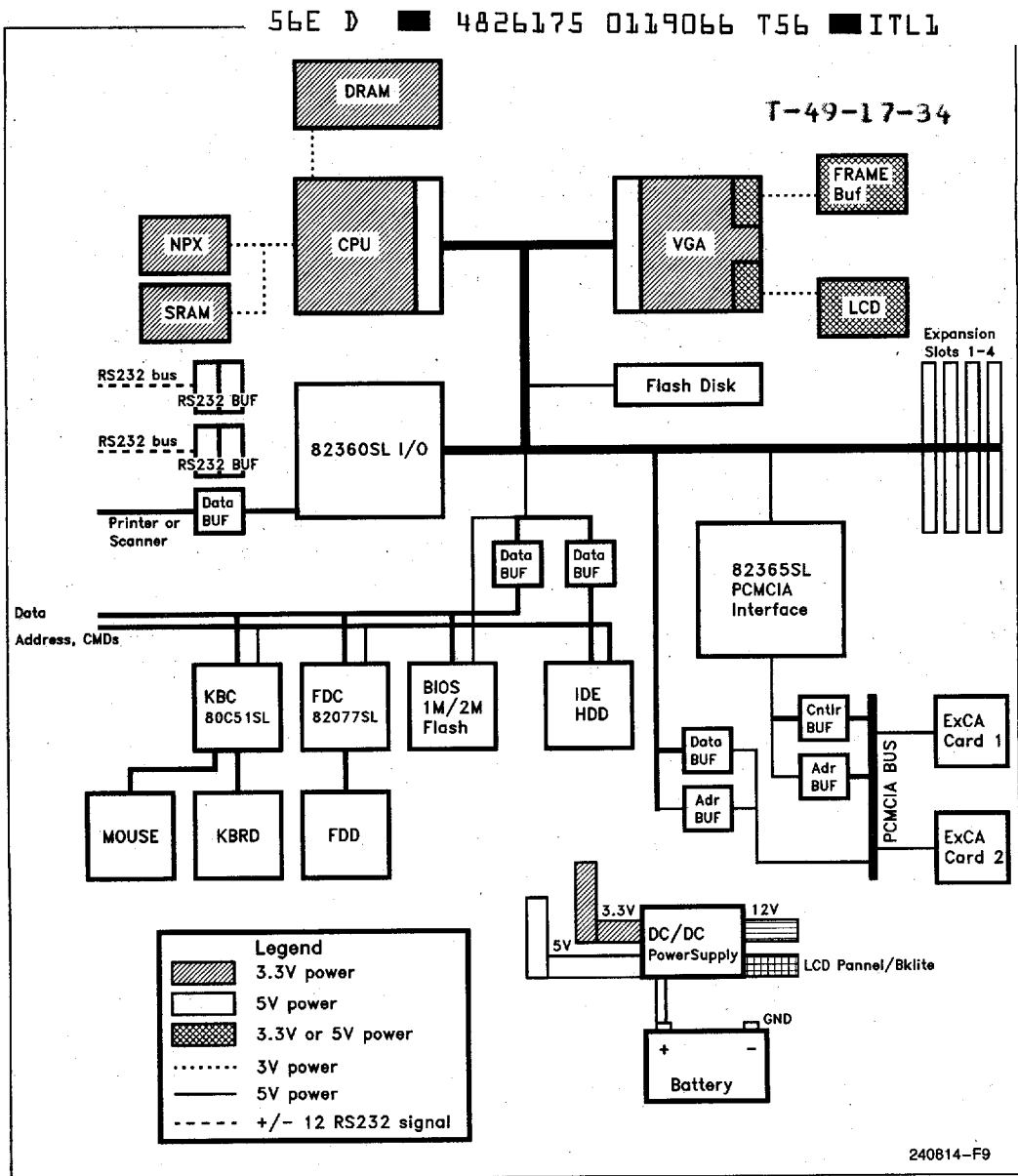


Figure 1.5. Sample Block Diagram of a PC System Based on the low-voltage Intel386™ SL CPU

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1.4 82360SL I/O: Integrated ISA Peripheral and Power Management Device

The 82360SL Peripheral I/O contains dedicated logic to perform a number of CPU, memory, and peripheral support functions. The 82360SL device also contains an extensive set of programmable power management facilities which allow minimized system energy requirements for battery-powered portable computers.

The 82360SL includes a complete set of on-chip peripheral device functions including two 16450 compatible serial ports, one 8-bit Centronics interface or bi-directional parallel port, two 8254 compatible timer counters, two 8259 compatible interrupt controllers, two 8237 compatible DMA controllers, one 74LS612 compatible DMA page register, one 146818 compatible Real-time clock/calendar with an additional 128 bytes of battery backed CMOS RAM and an integrated drive electronics (IDE) hard disk drive interface. The Intel 82360SL also contains highly programmable chip selects and complete peripheral interface logic for direct keyboard and floppy disk controller support. The peripheral registers and functions behave exactly as the discrete components commonly found in industry standard personal computers. The peripheral logic is enhanced for static operation by supporting write only registers as read/write.

The processor and memory support functions contained in the 82360SL device eliminate most of the external random-logic "glue" that might otherwise be required. The 82360SL device provides internal programmable-frequency clock generators for the ISA bus backplane, and video subsystems. A programmable, low-power DRAM refresh timer is also provided to maintain system memory integrity during the power saving suspend state.

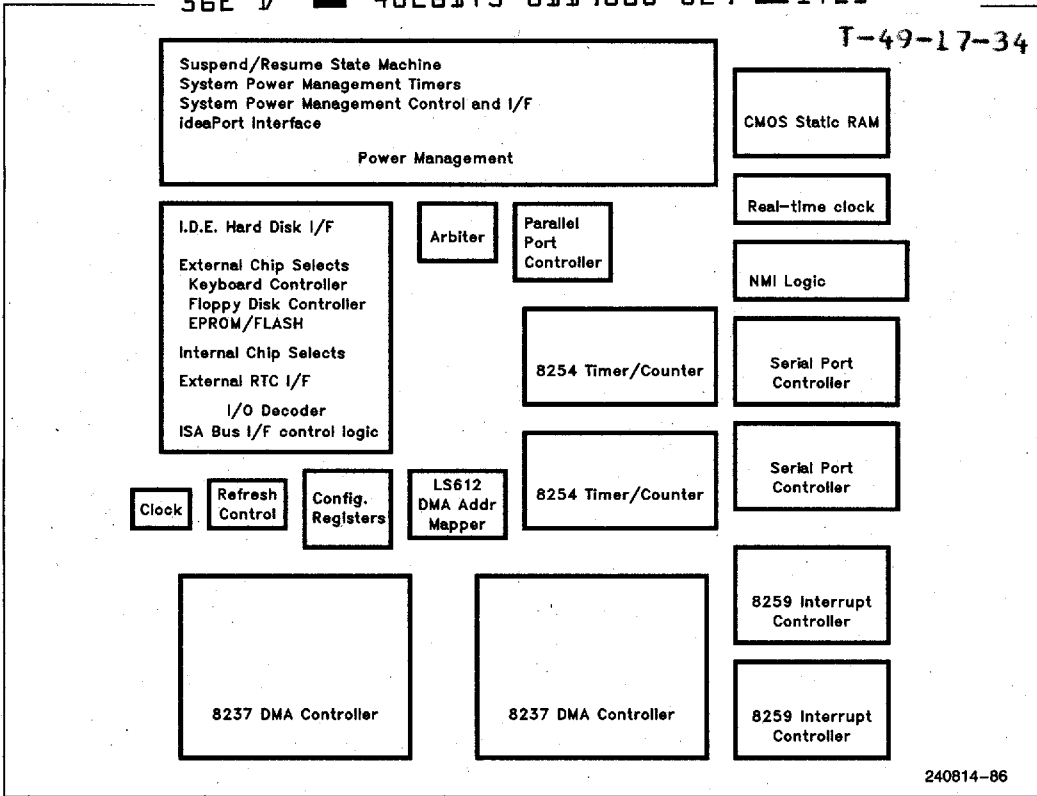
The 82360SL also contains a flexible set of hardware functions to support the growing sophistication in power management schemes required by portable systems. Numerous hardware timers, event monitors and I/O interfaces can programmably monitor and control system activity. Firmware developed by the system designer allocates and directs the hardware to fulfill the unique power management needs of a given system configuration.

All of the standard peripheral registers, clock-generation logic, and power-management facilities have been designed to ensure complete compatibility with existing operating systems and applications software.

Figures 1.6a and 1.6b show the functional blocks and micro-architecture of the 82360SL I/O subsystem.

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Figure 1.6a. 82360SL ISA Peripheral I/O Internal Functional Modules

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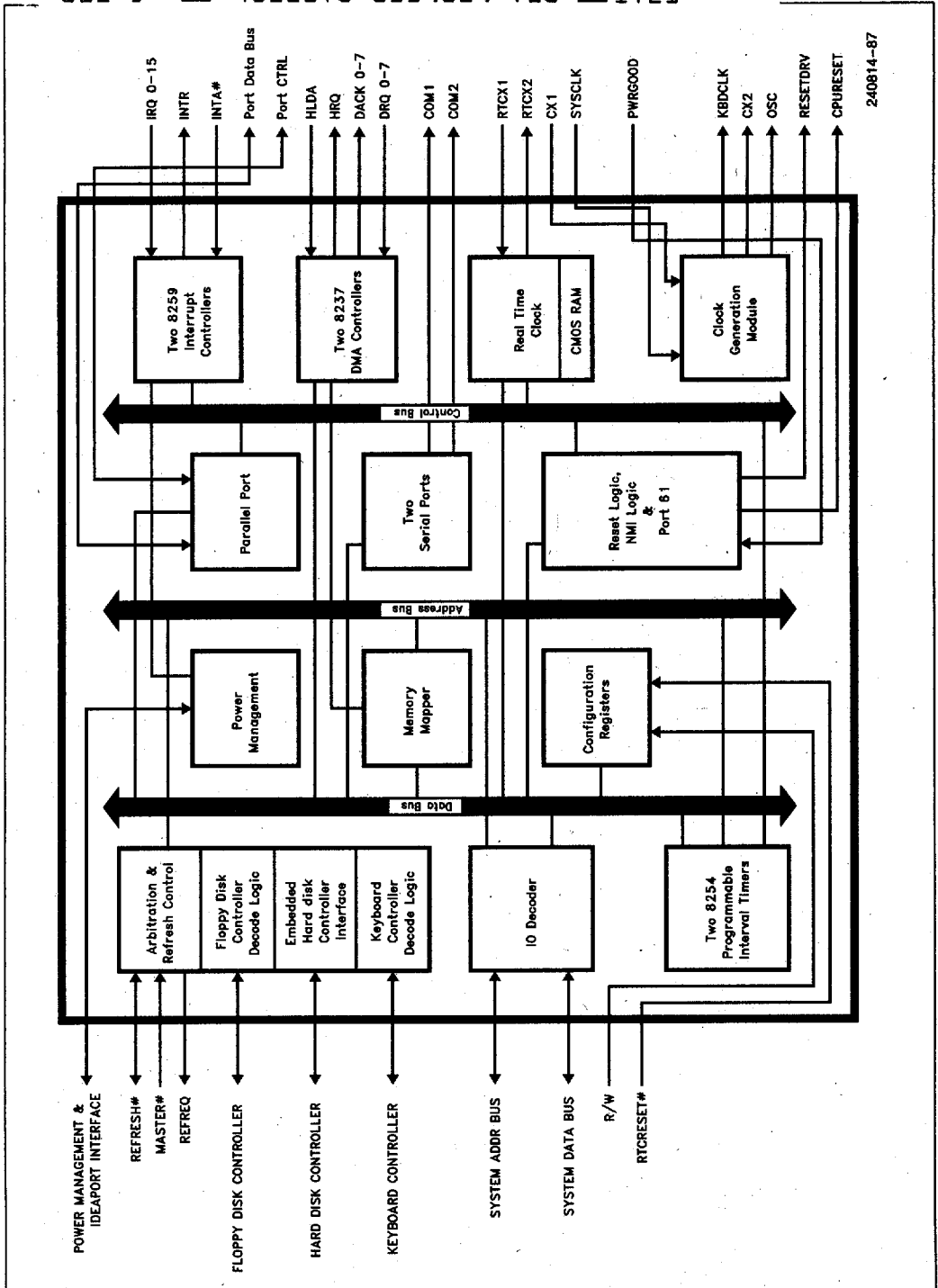


Figure 1.6b. 82360SL Functional Block Diagram



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**2.0 Intel386™ SL MICROPROCESSOR
(Standard 5V Operation)****2.1 Pin Assignments and Signal
Characteristics**

Section 2.1 provides information for the Intel386 SL CPU pin assignment with respect to the signal

mnemonics. In addition to the package pin out diagrams, a table is provided for easy location of signals. Table 2.1-2 lists the Intel386 SL CPU package device pinouts in the 227 pin Land Grid Array (LGA). The table also includes additional information for the signals and associated pin numbers. A brief explanation of each column of the table is given in Table 2.1-1.

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Table 2.1-1. Description of the Columns of Tables 2.1-2

PQFP	This column lists the pin numbers of the Intel386 SL CPU in a Plastic Quad Flat Package.
LGA	This column lists the pin numbers of the Intel386 SL CPU in a Land Grid Array.
Signal Name	This column lists the signal name associated with the package pins.
Type	Indicates whether the pin is an Input (I), an Output (O) or an Input-Output (IO).
Term	Specifies the internal terminator on the pin. This could be an internal pull-up or pull-down resistor value or a hold circuit. To find out whether a pull-up or a pull-down is provided, use the STPCK (Stop Clock) column for the Intel386 SL CPU.
Drive	Specifies the drive current I_{OL} (Current Output Logic Low) and I_{OH} (Current Output Logic High) in milli-Amperes (mA) for output (O), and bi-directional (IO), pins.
Load	This column lists the maximum specified capacitive load which the buffer can directly drive in pico-Farads (pF) for each signal. This is specified for output and input-output pins only.
Susp.	This column specifies the state of the pin during a suspend operation. Input signals have the representation Tri. This indicates that the input is internally isolated and that the internal termination on the pin is tri-stated or disabled. The additional output buffer abbreviations are explained below. Tri - Tristated Actv - Active (Active input signals must be held at valid logic levels) 0 - held low 1 - held high Hold - held at last state
Stpck.	This is a state specific to the Intel386 SL CPU. This column specifies the state of the pin when the clock signal CPUCLK is internally stopped in the Intel386 SL CPU. Pu - Pulled up Pd - Pulled down Drv - Driven high, low or at the last state Actv - Active (Signal is driven and continues to operate or change logic states)
ONCE	This column specifies the state of the pin when the ONCE# (On Circuit Emulator) pin is asserted, allowing in-circuit testing while the device is still populated on the logic board. Tri - Floats Actv - Active 0 - held low 1 - held high Hold - held at last state
Derating Curve	This column specifies which derating curve ⁽¹⁾ is used for each output buffer associated with the pin.

NOTES:

- For more information on derating curves and how to use them, see Section 3.7 (Capacitive Derating Information).
- Typical resistor values are given as guidelines only. Not tested.



THE Intel386™ SL CPU (STANDARD 5V) PINOUT DIAGRAM

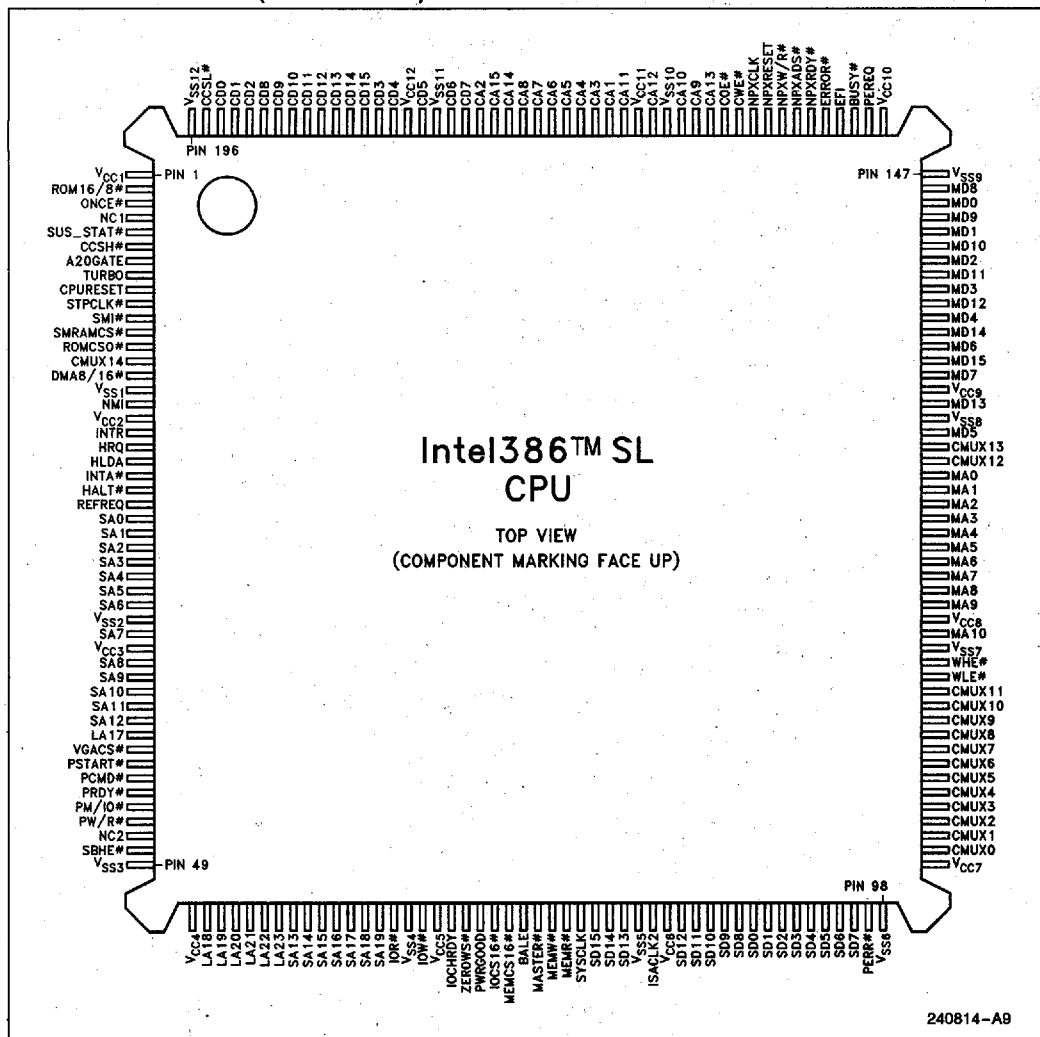
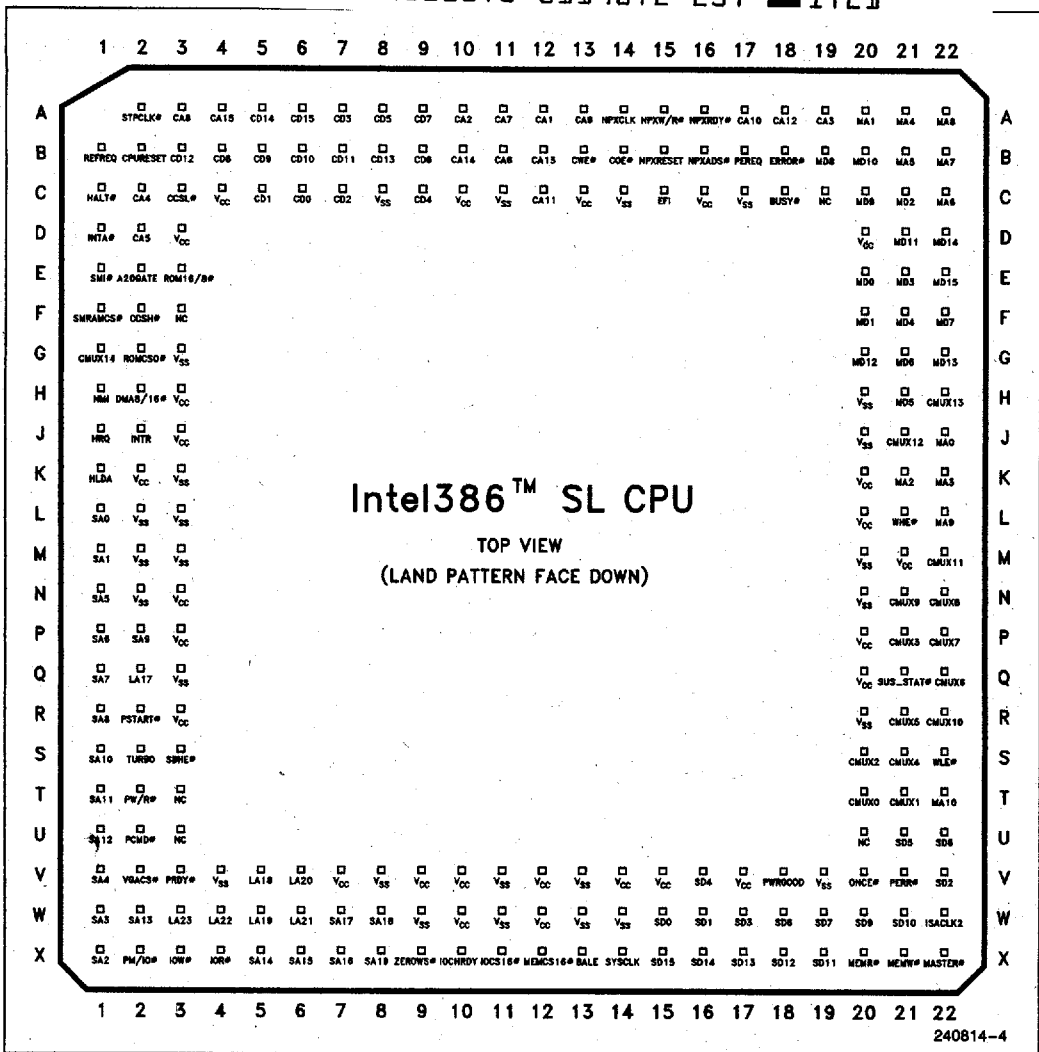


Figure 2.1a. Top View of the Pinout of the Intel386™ SL CPU (Standard 5V) in a PQFP Package



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Figure 2.1b. Pin Assignments of the Intel386™ SL CPU (Standard 5V) in the 227-Lead LGA Package (Top View—Land Pattern Facing Down, Component Marking Facing Up)



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Table 2.1-2. Intel386™ SL CPU (Standard 5V) Pin Characteristics

Signal Name	PQFP Pin #	LGA Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	Stpck	ONCE	Derating Curve
A20GATE	A007	E02	I	60K			Tri	Pu	Tri	
BALE	A073	X13	O	Hold	24, 4	50, 240	Hold	Drv	Hold	A-26
BUSY#	A150	C18	I	60K			Tri	Pu	Tri	
CA1	A167	A12	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA2	A176	A10	O	Hold	4, 2	15, 60	Hold	Drv	Hold	A-5
CA3	A168	A19	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA4	A169	C02	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA5	A170	D02	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA6	A171	B11	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA7	A172	A11	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA8	A173	A03	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA9	A161	A13	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA10	A162	A17	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA11	A166	C12	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA12	A164	A18	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA13	A160	B12	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA14	A174	B10	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CA15	A175	A04	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-4
CCSH#	A006	F02	O	Hold	4, 2	20, 35	Hold	Drv	Hold	A-10
CCSL#	A195	C03	O	Hold	4, 2	20, 35	Hold	Drv	Hold	A-10
CD0	A194	C06	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD1	A193	C05	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD2	A192	C07	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD3	A183	A07	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD4	A182	C09	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD5	A180	A08	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD6	A178	B09	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD7	A177	A09	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD8	A191	B04	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD9	A190	B05	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD10	A189	B06	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD11	A188	B07	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD12	A187	B03	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD13	A186	B08	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11



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Table 2.1-2. Intel386™ SL CPU (Standard 5V) Pin Characteristics (Continued)

Signal Name	PQFP Pin #	LGA Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	Stpck	ONCE	Derating Curve
CD14	A185	A05	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CD15	A184	A06	IO	Hold	4, 2	20, 50	Hold	Drv	Hold	A-11
CMUX0	A100	T20	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX1	A101	T21	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX2	A102	S20	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX3	A103	P21	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX4	A104	S21	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX5	A105	R21	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX6	A106	Q22	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX7	A107	P22	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold	A-6
CMUX8	A108	N22	O	Hold	4, 2	32, 136	Hold(1)	Drv	Hold	A-21
CMUX9	A109	N21	O	Hold	4, 2	32, 136	Hold(1)	Drv	Hold	A-21
CMUX10	A110	R22	O	Hold	4, 2	32, 136	Hold(1)	Drv	Hold	A-21
CMUX11	A111	M22	O	Hold	4, 2	32, 136	Hold(1)	Drv	Hold	A-21
CMUX12	A127	J21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-2
CMUX13	A128	H22	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-2
CMUX14	A014	G01	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
COE#	A159	B14	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-7
CPURESET	A009	B02	I	20K			Actv	Pd	Tri	
CWE#	A158	B13	O	Hold	4, 2	15, 45	Hold	Drv	Hold	A-8
DMA8/16#	A015	H02	I	60K			Tri	Pu	Tri	
EFI	A151	C15	I				Actv		Tri	
ERROR#	A152	B18	I	60K			Tri	Pu	Tri	
HALT#	A023	C01	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
HLDA	A021	K01	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
HRQ	A020	J01	I	20K			Tri	Pd	Tri	
INTA#	A022	D01	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
INTR	A019	J02	I	20K			Tri	Pd	Tri	
IOCHRDY	A068	X10	IO	1K	24, 4	50, 240	Tri	Pu	Tri	A-22
IOCS16#	A071	X11	IO	1K	24, 4	50, 240	Tri	Pu	Tri	A-23
IOR#	A064	X04	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-24
IOW#	A066	X03	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-24
ISACK2	A082	W22	I				Actv		Tri	
LA17	A040	Q02	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
LA18	A051	V05	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
LA19	A052	W05	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25

NOTE:

1. These pins are driven during the suspend state if suspend refresh is enabled.



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Table 2.1-2. Intel386™ SL CPU (Standard 5V) Pin Characteristics (Continued)

Signal Name	PQFP Pin #	LGA Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	Stpck	ONCE	Derating Curve
LA20	A053	V06	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
LA21	A054	W06	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
LA22	A055	W04	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
LA23	A056	W03	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
MA0	A126	J22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA1	A125	A20	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA2	A124	K21	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA3	A123	K22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA4	A122	A21	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA5	A121	B21	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA6	A120	C22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA7	A119	B22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA8	A118	A22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA9	A117	L22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MA10	A115	T22	O	Hold	4, 2	32, 240	Hold ⁽¹⁾	Drv	Hold	A-20
MASTER#	A074	X22	I	1K			Tri	Pu	Tri	
MD0	A145	E20	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD1	A143	F20	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD2	A141	C21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD3	A139	E21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD4	A137	F21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD5	A129	H21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD6	A135	G21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD7	A133	F22	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD8	A146	B19	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD9	A144	C20	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD10	A142	B20	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD11	A140	D21	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD12	A138	G20	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD13	A131	G22	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD14	A136	D22	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MD15	A134	E22	IO	Hold	4, 2	8, 32	Hold	Drv	Hold	A-1
MEMCS16#	A072	X12	IO	1K	24, 4	50, 240	Tri	Pu	Tri	A-23
MEMR#	A076	X20	IO	60K	24, 4	20, 240	Tri	Pu	Tri	A-12
MEMW#	A075	X21	IO	60K	24, 4	20, 240	Tri	Pu	Tri	A-12
NMI	A017	H01	I	20K			Tri	Pd	Tri	

NOTE:

1. These pins are driven in the suspend state if suspend refresh is enabled.



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Table 2.1-2. Intel386™ SL CPU (Standard 5V) Pin Characteristics (Continued)

Signal Name	PQFP Pin #	LGA Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	Stpck	ONCE	Derating Curve
NPXADS#	A154	B16	O	Hold	4, 2	20, 32	Hold	Drv	Hold	A-13
NPXCLK	A157	A14	O	Hold	4, 2	20, 40	Hold	Drv	Tri	A-14
NPXRDY#	A153	A16	I	20K			Tri	Pd	Tri	
NPXRESET	A156	B15	O	Hold	4, 2	20, 32	Hold	Drv	Hold	A-15
NPXW/R#	A155	A15	O	Hold	4, 2	20, 32	Hold	Drv	Tri	A-13
ONCE#	A003	V20	I	60K			Actv	Pu	Actv	
PCMD#	A043	U02	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
PEREQ	A149	B17	I	20K			Tri	Pd	Tri	
PERR#	A097	V21	O	Hold	4, 2	8, 32	Hold	Drv	Hold	A-3
PM/IO#	A045	X02	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
PRDY#	A044	V03	I	60K			Tri	Pu	Tri	
PSTART#	A042	R02	O	Hold	4, 2	20, 65	Hold	Drv	Tri	A-16
PW/R#	A046	T02	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
PWRGOOD	A070	V18	I				Actv	Actv	Tri	
REFREQ	A024	B01	I	Hold			Actv	Actv	Tri	
ROM16/8#	A002	E03	I	60K			Tri	Pu	Tri	
ROMCS0#	A013	G02	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
SA0	A025	L01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA1	A026	M01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA2	A027	X01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA3	A028	W01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA4	A029	V01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA5	A030	N01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA6	A031	P01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA7	A033	Q01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA8	A035	R01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA9	A036	P02	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA10	A037	S01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA11	A038	T01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA12	A039	U01	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA13	A057	W02	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA14	A058	X05	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA15	A059	X06	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA16	A060	X07	IO	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25



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Table 2.1-2. Intel386™ SL CPU (Standard 5V) Pin Characteristics (Continued)

Signal Name	PQFP Pin #	LGA Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	Stpck	ONCE	Derating Curve
SA17	A061	W07	O	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA18	A062	W08	O	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SA19	A063	X08	O	Hold	24, 4	50, 240	Hold	Drv	Hold	A-25
SBHE#	A048	S03	IO	Hold	24, 4	20, 240	Hold	Drv	Hold	A-17
SD0	A089	W15	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD1	A090	W16	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD2	A091	V22	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD3	A092	W17	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD4	A093	V16	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD5	A094	U21	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD6	A095	W18	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD7	A096	W19	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD8	A088	U22	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD9	A087	W20	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD10	A086	W21	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD11	A085	X19	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD12	A084	X18	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD13	A080	X17	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD14	A079	X16	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SD15	A078	X15	IO	60K	24, 4	50, 240	Tri	Pu	Tri	A-26
SMI#	A011	E01	I	60K			Tri	Pu	Tri	
SMRAMCS#	A012	F01	O	Hold	4, 2	20, 65	Drv	Drv	Hold	A-18
STPCLK#	A010	A02	I	60K			Tri	Pu	Tri	
SUS_STAT#	A005	Q21	I				Actv	Actv	Tri	
SYSCLK	A077	X14	O	Hold	4, 2	20, 120	Hold	Drv	Hold	A-19
TURBO	A008	S02	I	60K			Tri	Pu	Tri	
VGACS#	A041	V02	O	Hold	4, 2	20, 65	Hold	Drv	Hold	A-16
WHE#	A113	L21	O	Hold	4, 2	15, 136	Hold ⁽¹⁾	Drv	Hold	A-9
WLE#	A112	S22	O	Hold	4, 2	15, 136	Hold ⁽¹⁾	Drv	Hold	A-9
ZEROWS#	A069	X09	I	700			Tri	Pu	Tri	

Power Pins

V_{CC} PQFP: A001, A018, A034, A050, A067, A083, A099, A116, A132, A148, A165, A181

LGA: C04, C10, C13, C16, D03, D20, H03, J03, K02, K20, L20, M21, N03, P03, P20, Q20, R03, V07, V17, V15, V14, V12, V10, V09, W10, W12

V_{SS} PQFP: A016, A032, A049, A065, A081, A098, A114, A130, A147, A163, A179, A196

LGA: C08, C11, C14, C17, G03, H20, J20, K03, L02, L03, M02, M03, M20, N02, N20, Q03, R20, V04, V08, V19, V13, V11, W09, W11, W13, W14

No Connects

PQFP: A004, A047

LGA: C19, F03, T03, U03, U20

NOTE:

1. These pins are driven inactive in the suspend state if suspend refresh is enabled.



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2.2 Signal Descriptions

T-49-17-34

Intel386™ SL Microprocessor (Standard 5V)

The following table provides a brief description of the signals of the Intel386 SL CPU. Signal names which end with the character “#” indicate that the corresponding signal is low when active.

Symbol	Name and Function																								
A20GATE	A20 Gate: This active HIGH input signal controls the Intel386 SL CPU A20 address line. When LOW this signal forces the Intel386 SL CPU to mask off (force LOW) the internal physical address signal A20. When this signal is HIGH, A20 is available on the System Address (SA) bus. When A20 gate is LOW this allows emulation of the 8086 1 Mbyte address “wrap-around”.																								
BALE	<p>Bus Address Latch Enable (ISA bus signal): This active HIGH output signal is used for two purposes. BALE is used to latch the address lines on the LA bus (LA17–LA23) on the falling edge of BALE. BALE is also used to qualify ISA bus cycles for signals on the Peripheral Interface (PI) bus (PM/IO# and PW/R#). On the falling edge of BALE, PM/IO# and PW/R# can be sampled to determine the type of ISA bus cycle that is going to occur. BALE may be used to qualify and generate buffered control and status signals to the ISA expansion bus. The PI bus signal decoding is as follows:</p> <table border="1" data-bbox="358 673 851 906"> <thead> <tr> <th>Type of Bus Cycle</th> <th>PM/IO#</th> <th>PW/R#</th> </tr> </thead> <tbody> <tr> <td>Memory Read</td> <td>1</td> <td>0</td> </tr> <tr> <td>Memory Write</td> <td>1</td> <td>1</td> </tr> <tr> <td>I/O Read</td> <td>0</td> <td>0</td> </tr> <tr> <td>I/O Write</td> <td>0</td> <td>1</td> </tr> <tr> <td>Interrupt Acknowledge</td> <td>0</td> <td>1</td> </tr> <tr> <td>HALT (address = 2)*</td> <td>1</td> <td>1</td> </tr> <tr> <td>Shutdown (address = 0)*</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>*Note that BALE is not generated for these cycles, however the PM/IO# and PW/R# will reflect these states during HALT and Shutdown bus cycles where BALE is driven in typical ISA bus systems. Memory read/write, IO read/write and interrupt/interrupt acknowledge cycles correspond to the standard ISA bus cycle.</p>	Type of Bus Cycle	PM/IO#	PW/R#	Memory Read	1	0	Memory Write	1	1	I/O Read	0	0	I/O Write	0	1	Interrupt Acknowledge	0	1	HALT (address = 2)*	1	1	Shutdown (address = 0)*	1	1
Type of Bus Cycle	PM/IO#	PW/R#																							
Memory Read	1	0																							
Memory Write	1	1																							
I/O Read	0	0																							
I/O Write	0	1																							
Interrupt Acknowledge	0	1																							
HALT (address = 2)*	1	1																							
Shutdown (address = 0)*	1	1																							
BUSY#	BUSY: This active LOW input signal indicates a busy condition from a math co-processor (MCP).																								
CA[15:1]	Cache Address Bus: This is the address bus output used to select the memory cell in the cache memory. The CA2 signal is also connected to the CMD0# input of the MCP indicating Opcode (when high) or Data (when low) during a write cycle and control/status register (high) or data register (low) during a read. CA2 is used to address the upper or lower DWORD port of the MCP.																								
CCSH#	Cache Chip Select High Byte: This active LOW output is used to enable the upper byte of the cache SRAMs. This signal should be connected to the upper byte cache SRAM chip-select input.																								
CCSL#	Cache Chip Select Low Byte: This active LOW output is used to enable the lower byte of the cache SRAMs. This signal should be connected to the lower byte cache SRAM chip-select input.																								
CD[15:0]	Cache Data Bus: This is the bi-directional data bus used to transfer data between the cache SRAMs and the Intel386 SL CPU. The Cache Data bus is also used to transfer data between the MCP and the Intel386 SL CPU.																								

2



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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
CMUX0 (CASL3# / DIR)	CPU Multiplexed Pin Zero: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller then this pin becomes "CASL3#" and should be connected to the lower byte of DRAM bank 3 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as an SRAM controller this signal becomes the direction control (DIR) and should be connected to the direction control input of the SRAM data transceiver.
CMUX1 (CASH3# / LE)	CPU Multiplexed Pin One: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller then this pin becomes "CASH3#" and should be connected to the upper byte of DRAM bank 3 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this signal becomes "LE" and should be connected to the latch enable input of the SRAM address latch. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX2 (CASL2# / DEN3#)	CPU Multiplexed Pin Two: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL2#" and should be connected to the lower byte of DRAM bank 2 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN3#" and should be connected to the data transceiver enable input for bank 3 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX3 (CASH2# / DEN2#)	CPU Multiplexed Pin Three: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH2#" and should be connected to the upper byte of DRAM bank 2 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN2#" and should be connected to the data transceiver enable input for bank 2 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX4 (CASL1# / DEN1#)	CPU Multiplexed Pin Four: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL1#" and should be connected to the lower byte of DRAM bank 1 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN1#" and should be connected to the data transceiver enable input for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

NOTE:

Pins CMUX4 and CMUX5 both carry the signal DEN1# in the SRAM mode. This is done to provide increased drive capacity on the DEN1# signal.



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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
CMUX5 (CASH1 # / DEN1 #)	<p>CPU Multiplexed Pin Five: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH1 #" and should be connected to the upper byte of DRAM bank 1 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN1 #" and should be connected to the data transceiver enable input for bank 1 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX6 (CASL0 # / DENO #)	<p>CPU Multiplexed Pin Six: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL0 #" and should be connected to the lower byte of DRAM bank 0 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DENO #" and should be connected to the data transceiver enable input for bank 0 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX7 (CASH0 # / DENO #)	<p>CPU Multiplexed Pin Seven: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH0 #" and should be connected to the upper byte of DRAM bank 0 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DENO #" and should be connected to the data transceiver enable input for bank 0 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX8 (RAS3 # / CE3 #)	<p>CPU Multiplexed Pin Eight: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS3 #" and should be connected to the upper and lower byte of DRAM bank 3 RAS# inputs.</p> <p>When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller then this pin becomes "CE3 #" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 3 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX9 (RAS2 # / CE2 #)	<p>CPU Multiplexed Pin Nine: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS2 #" and should be connected to the upper and lower byte of DRAM bank 2 RAS# inputs.</p> <p>When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE2 #" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 2 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>

NOTES:

Pins CMUX4 and CMUX5 both carry the signal DEN1# in the SRAM mode. This is done to provide increased drive capacity on the DEN1# signal.

Pins CMUX6 and CMUX7 both carry the signal DENO# in the SRAM mode. This is done to provide increased drive capacity on the DENO# signal.

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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
CMUX10 (RAS1 #/ CE1 #)	<p>CPU Multiplexed Pin Ten: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS1 #" and should be connected to the upper and lower byte of DRAM bank 1 RAS# inputs.</p> <p>When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE1 #" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 1 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX11 (RAS0 #/ CE0 #)	<p>CPU Multiplexed Pin Eleven: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS0 #" and should be connected to the upper and lower byte of DRAM bank 0 RAS# inputs.</p> <p>When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE0 #" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 0 of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX12 (PARL/ OLE #)	<p>CPU Multiplexed Pin Twelve: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "PARL" and should be connected to the lower byte of DRAM bank 0 data parity bit.</p> <p>When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "OLE #" and should be connected to the lower byte of the SRAM output enable input of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX13 (PARH/ OHE #)	<p>CPU Multiplexed Pin Thirteen: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "PARH" and should be connected to the upper byte of DRAM bank 0 data parity bit.</p> <p>When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "OHE #" and should be connected to the upper byte of the SRAM output enable input of the SRAM memory subsystem.</p> <p>This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".</p>
CMUX14 (ROMCS1 #/ FLSHDCS #)	<p>CPU Multiplexed Pin 14: This output signal has two functions. The Intel386 SL CPU can be configured to use this pin as either a BIOS ROM chip-select (ROMCS1 #), or a FLASH disk chip-select signal (FLSHDCS #). In either case, the signal is driven LOW when an access to the selected interface occurs.</p>
COE #	<p>Cache Output Enable: This active LOW output signal is used to indicate a read access to the CACHE SRAMs, and is used to enable the cache SRAMs' output buffers. This signal should be connected to the output enable signals of the upper and lower byte cache SRAMs.</p>
CPURESET	<p>CPU Reset: This active HIGH input forces the Intel386 SL CPU to execute a reset to the internal CPU core and state machines. The configuration registers are not reset.</p>

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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
CWE#	Cache Write Enable: This active LOW output is used to indicate a write (LOW) access to the cache SRAMs. This signal should be connected to the write enable signal of the upper and lower cache SRAMs.
DMA8/16#	DMA 8-bit or 16-bit Cycle: This input, in conjunction with HRQ, indicates to 386 SL CPU if an 8-bit or 16-bit DMA access is occurring. If an 8-bit DMA access is occurring, the Intel386 SL CPU will swap the upper byte of data to the lower data byte for upper byte accesses.
EFI	External Frequency Input. This is an oscillator input. This clock controls all CPU core and memory controller timings and is equal to twice the desired processor frequency (CPUCLK).
ERROR#	Numerics ERROR: This active LOW input to the Intel386 SL CPU is generated from a math co-processor (MCP). It also indicates to the 82360SL that an unmasked exception has occurred in the MCP. ERROR# is provided to allow numerics error handling compatible with the ISA bus compatible Personal Computer.
HALT#	HALT: This active LOW output indicates to external devices that the Intel386 SL CPU has executed a HALT instruction (address = 2) or a shutdown condition (address = 0). This can be used as an indicator for devices to assert the STPCLK# signal.
HLDA	HoLD Acknowledge: This active HIGH output indicates to external devices that the Intel386 SL CPU has relinquished control of the ISA bus. At this time the Intel386 SL CPU has floated the address and control signals of the ISA bus.
HRQ	Hold ReQuest: This active HIGH input indicates to the Intel386 SL CPU that an external device wishes to take control of the ISA bus.
INTA#	INTerrupt Acknowledge: This active LOW output indicates that the Intel386 SL CPU is executing an interrupt acknowledge bus cycle. During this process an external interrupt device will pass an interrupt vector to the Intel386 SL CPU.
INTR	Interrupt Request: This active HIGH input indicates to the Intel386 SL CPU that an external device is requesting the execution of an interrupt service routine.
IOCHRDY	I/O Channel ReaDY: This active HIGH input/output signal indicates that the I/O Channel, (ISA expansion bus), is ready to terminate the bus cycle. The ISA expansion bus is a normally ready bus and IOCHRDY is active HIGH. When an ISA bus peripheral needs to extend the standard 3 SYSCLK, 16-bit ISA bus cycle the peripheral device asserts IOCHRDY LOW.
IOCS16#	I/O Chip Select 16: This active LOW input/output signal indicates that an ISA bus peripheral wishes to execute a 16-bit I/O cycle. This signal has an active pull-up, when not driven the default I/O bus cycle is 8 bits.
IOR#	I/O Read: This active LOW signal indicates that the ISA bus is executing an I/O read cycle.
IOW#	I/O Write: This active LOW signal indicates that the ISA bus is executing an I/O write cycle.
ISACK2	ISA Clock Two: This is an oscillator input. This clock controls all of the ISA bus timings and is equal to twice the SYSCLK frequency. Normally the ISA bus SYSCLK is 8 MHz, and the ISACK2 oscillator is 16 MHz.

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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
LA[23:17]	Latchable local Address bus: This is the unlatched local address of the ISA bus for access to memory above 1 megabyte. The LA bus is also used by the Peripheral Interface (PI) Bus.
MA[10:0]	Memory controller Multiplexed Address bus: This is the address bus output for the Memory Controller Unit. The 22-bit address is output in a row/column fashion for both DRAM and SRAM memory subsystems. The Memory Controller Unit places the ROW address out first and qualifies it by the RASx# signal going active in DRAM mode or the LE signal going active in the SRAM mode. The column address is then placed on the Memory Address bus and is qualified by the CASXx# signals going active for the DRAM mode. This pin is disabled when SUS_STAT# is active (LOW). When the pin is disabled the output is sustained at the previous state by internal "keepers".
MASTER#	Master: This active LOW input indicates that an ISA bus peripheral is controlling the bus. The peripheral device asserts this signal in conjunction with a DMA request (DRQ) line or the HRQ (hold request) to gain control of the bus. When the MASTER# signal is asserted LOW along with HRQ being asserted HIGH the Intel386 SL CPU will float all address, data and control signals on the ISA bus.
MD[15:0]	Memory controller local Memory Data bus: This is the bi-directional data bus of the Memory Controller Unit. All accesses by the Memory Controller Unit that transfer data between the Intel386 SL CPU and SRAM or DRAM use the Memory Data Bus. This pin is disabled when SUS_STAT# is active (low) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
MEMCS16#	MEMory Chip Select 16: This active LOW input/output signal indicates that an ISA bus peripheral wishes to execute a 16-bit memory cycle. This signal has an active pull-up, when not driven the default memory bus cycle is 8 bits.
MEMR#	MEMory Read: This bi-directional active LOW signal indicates when a memory read access is taking place on the ISA bus. When the Intel386 SL CPU is performing a memory read to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA device or Master drives MEMR#.
MEMW#	MEMory Write: This bi-directional active LOW signal indicates when a memory write access is taking place on the ISA bus. When the Intel386 SL CPU is performing a memory write to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA controller or Bus Master drives MEMW#.
N/C	No connection: These pins must not be connected to any voltage, but must be left floating in order to guarantee proper operation of the Intel386 SL CPU and to maintain compatibility with future Intel Processors.
NMI	Non-Maskable Interrupt: This rising edge sensitive input will latch a request to the Intel386 SL CPU for a non-maskable interrupt on a LOW-to-HIGH transition.
NPXADS#	Numerics Address Strobe: This active LOW output signal indicates the start of a math co-process (MCP) data transfer cycle.
NPXCLK	Numerics Clock: This output signal is used to drive the MCP clock input.
NPXRDY#	Numerics Ready: This active LOW input is used to terminate a MCP bus cycle. This signal is low for I/O and data operand MCP cycles.



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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
NPXRESET	Numerics Reset: This active HIGH output signal is used to reset the MCP.
NPXW/R#	Numerics Write or Read: This output signal indicates the type of data transfer that is being performed between the Intel386 SL CPU and the MCP. When high this signal indicates a MCP write, when low this signal indicates a MCP read.
ONCE#	ON-board Circuit Emulation: This active LOW input signal floats the necessary outputs from the Intel386 SL CPU allowing an in-circuit emulation (ICETM-Intel386 SL) module to drive the Intel386 SL CPU signals. This allows an emulator to be used for system testing and development while the Intel386 SL CPU and the 82360SL are still physically populated on the system motherboard. The state of all Intel386 SL CPU and 82360SL signals when ONCE# is asserted low is summarized in section 2, (Intel386 SL CPU and 82360SL signal characteristics). Note that the ONCE# pin of the Intel386 SL CPU should not be connected to the ONCE# pin of the 82360 SL I/O.
PCMD#	PI-BUS Command: This active LOW output indicates that valid write data is on the System data bus (SD[15:0]) signals, or that the Intel386 SL CPU is ready to sample valid read data from the PI bus for Peripheral Interface bus cycles.
PEREQ	Processor Extension Request: This active HIGH input signal indicates that the MCP has data to transfer to or from the Intel386 SL CPU.
PERR#	Parity ERROR: This active LOW output indicates to an external device that the Intel386 SL CPU Memory Controller Unit has detected a memory parity error. The PERR# signal is used by the 82360SL to generate NMI back to the Intel386 SL CPU.
PM/IO#	PI-BUS Memory or I/O: This output indicates the type of bus cycle the Intel386 SL CPU is executing on the Peripheral Interface Bus (PI-bus): Either a Memory (HIGH) or I/O (LOW) cycle.
PRDY#	PI-BUS Ready: This active LOW input is used to terminate Peripheral Interface bus cycles. The Peripheral Interface Bus is a normally not-ready bus, and will continue the bus cycle until the PRDY# is activated or a Peripheral Interface Time-out occurs.
PSTART#	PI-BUS START: This active LOW output indicates that the address (SA[19:0], LA[23:17] and SBHE#), command signals (PM/IO# and PW/R#) and chip-selects (VGACS# or FLSHDCS#) are valid for a Peripheral Interface Bus cycle.
PW/R#	PI-BUS Write or Read: This output indicates the type of bus cycle the Intel386 SL CPU is executing on the Peripheral Interface Bus: Either a Write (HIGH) or Read (LOW) cycle.
PWRGOOD	Power Good: This active HIGH input indicates that power to the system is good. This signal is generated by the power supply circuitry, and a LOW level on this signal causes the Intel386 SL to totally reset: The CPU core is reset, internal state machines are reset, all configuration registers are reset. Power Good should be low for a specified minimum number of CPU clocks for valid recognition in order to perform a global Intel386 SL CPU reset.
REFREQ	REfresh REQUEST: This active HIGH input indicates that the Intel386 SL CPU should execute an internal DRAM refresh cycle to the on-board local memory.
ROM16/8#	ROM 16-bits or 8-bits: This input configuration signal pin selects if the BIOS interface is a 16-bit (when high) or 8-bit interface (when low). This pin has an internal pull-up resistor defaulting to a 16-bit wide BIOS EPROM.
ROMCS0#	ROM Chip Select 0: This LOW true output provides the chip select for the System BIOS EPROM.
SA[19:0]	System Address Bus: This is the bi-directional system address of the ISA bus, as well as the Peripheral Interface Bus. SA[16:0] are inputs during DMA and Master operation. SA[19:17] are outputs only since a 8237 compatible DMA controller accesses up to 64 kBytes at a time. The 74LS612 module in the 82360SL is used to furnish the DMA upper addresses for DMA access to 16 Megabyte.



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Intel386™ SL Microprocessor (Standard 5V) Signal Descriptions (Continued)

Symbol	Name and Function
SBHE#	System Byte High Enable: When this output signal is LOW, it indicates that data is being transferred on the upper byte of the 16-bit data bus (SD[15:8]).
SD[15:0]	System Data Bus: This 16-bit bi-directional data bus is used to transfer data between the Intel386 SL CPU and the ISA bus. The system data bus is also used to transfer data between the Intel386 SL CPU and the Peripheral Interface (PI-BUS).
SMI#	System power Management Interrupt: This falling edge sensitive input latches a Power Management interrupt request with a High-to-Low edge. The SMI# is the highest priority interrupt in the Intel386 SL processor.
SMRAMCS#	System power Management RAM Chip Select: This active LOW output is used to select an external system power management SM-RAM, and to indicate to the 82360SL device when accesses to the system power management SM-RAM are occurring.
STPCLK#	Stop Clock: This active LOW input stops the clock to the internal Intel386 SL CPU core. (This signal is functionally tested by the execution of HALT or I/O read instructions.)
SYSClk	System Clock: This is a clock output equal to one half of the ISAClk2 input frequency.
SUS_STAT#	SUSpend STATUS: This active LOW input indicates to the Intel386 SL CPU that system power is being turned off. The Intel386 SL CPU will respond by electrically isolating selected pins as indicated in Section 2, (Intel386 SL CPU signal characteristics).
TURBO	Turbo: This active HIGH input signal indicates to Intel386 SL CPU when to enter "Turbo Mode". Turbo Mode is defined as the CPU executing at full speed, the default speed for the system. When this signal is forced inactive LOW, the Intel386 SL CPU executes from a divide by two or a divide by four clock as defined by the De-turbo bit in the CPUPWRMODE register. When this signal is HIGH, the CPU executes from a clock as defined by the Fast CPU clock field in the CPUPWRMODE register.
V _{CC}	System Power: Provides the +5V nominal D.C. supply inputs.
VGACS#	VGA Chip-select: This active LOW output is asserted anytime an access occurs to the user defined VGA address space.
V _{SS}	System Ground: Provides the 0V connection from which all inputs and outputs are referenced.
WHE#	Write High Enable: This active LOW output indicates that a write access to the upper byte of the Intel386 SL CPU memory bus is occurring when the Memory Controller Unit is configured for SRAM mode. When in DRAM mode, the signal is active anytime a write access occurs. This output should be connected to the write enable of the upper byte for either DRAM or SRAM memory subsystems. This pin is driven inactive during a suspend operation.
WLE#	Write Low Enable: This active LOW output indicates that a write access to the lower byte of the Intel386 SL CPU memory bus is occurring when the Memory Controller Unit is configured for SRAM mode. When in DRAM mode, the signal is active anytime a write access occurs. This output should be connected to the write enable of the lower byte for either DRAM or SRAM memory subsystems. This pin is driven inactive during a suspend operation.
ZEROWS#	ZERO Wait State (ISA bus signal): This active LOW input indicates that an ISA bus peripheral wishes to execute a zero wait state bus cycle (the normal default 16-bit ISA bus memory or I/O cycle is 3 SYSClks or one PC/AT equivalent wait state). When ZEROWS# is driven low, a 16-bit bus cycle will occur in two SYSClks. When ZEROWS# is driven low for an 8-bit memory cycle the default 6 SYSClks bus cycle is shortened to 4 SYSClks.

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2.3 D.C. Specifications

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2.3.1 Intel386™ SL CPU D.C. SPECIFICATIONS

Functional operating range: $V_{CC} = 5V \pm 10\%$; $T_{CASE} = 0^{\circ}C$ to $90^{\circ}C$

Table 2.3-1. D.C. Voltage Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	0.8	V	Tested at 4 MHz. Min value for system design reference only.
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V	Tested at 4 MHz. Min value for system design reference only.
V_{ILC}	EFI/ISACKL2 Input Low Voltage	-0.3	0.8	V	Tested at 4 MHz, CMOS Logic Levels. Min value for system design reference only.
V_{IHC}	EFI/ISACKL2 Input High Voltage	$V_{CC} - 0.8$	$V_{CC} - 0.5$	V	At 4 MHz, CMOS Logic Levels. Min value for system design reference only.
V_{OL}	Output Low Voltage $I_{OL} = 4$ mA $I_{OL} = 24$ mA		0.5	V	At 4 MHz (Note 1)
				V	At 4 MHz (Note 2)
V_{OH}	Output High Voltage $I_{OH} = -1.6$ mA $I_{OH} = -2$ mA $I_{OH} = -0.2$ mA $I_{OH} = -4$ mA $I_{OH} = -0.18$ mA	2.4 $V_{CC} - 0.5$ 2.4 $V_{CC} - 0.5$		V	For IOCHRDY, IOCS16# and MEMCS16#
				V	At 4 MHz (Note 1)
				V	At 4 MHz (Note 2)
				V	At 4 MHz (Note 2)
				V	At 4 MHz (Note 1)

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Table 2.3-2. Leakage Current and Sustaining Current Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I _{IL}	Input Leakage Current Condition 1: When SUS_STAT# and/or ONCE# not active. Pins with internal 60k PU Pins with internal 20k PD Pins with internal 1K PU Other Input Pins		-120 300 -15 ±1	μA μA mA μA	V _{IL} = 0.45V V _{IH} = 2.4V V _{IL} = 0.45V 0V < V _{IN} < V _{CC}
	Condition 2: When SUS_STAT# and/or ONCE# active.		±15	μA	0V < V _{IN} < V _{CC}
I _{LO}	Output Leakage Current Condition 1: When SUS_STAT# and/or ONCE# not active Pins with internal 60k PU Pins with internal 1K PU Other Output Pins		±24 ±15	μA mA μA	V _{OUT} = 0.45V V _{OUT} = 0.45V 0.45V < V _{OUT} < V _{CC}
	Condition 2: When SUS_STAT# and/or ONCE# active.		±15	μA	0.45V < V _{OUT} < V _{CC}
I _{BHL}	Input Sustaining Current (Bus Hold Low)		38	μA	V _{IN} = 0.8V (Note 3)
I _{BHH}	Input Sustaining Current (Bus Hold High)		-60	μA	V _{IN} = 3.0V (Note 4)
I _{BHLO}	Bus Hold Low Overdrive	300		μA	(Note 5)
I _{BHHO}	Bus Hold High Overdrive	-550		μA	(Note 6)

Table 2.3-3. Capacitance D.C. Specifications

Symbol	Parameter	Min	Max	Unit	Notes
C _{IN}	Input Capacitance		10	pF	EFI = 1 MHz (Note 7)
C _{OUT}	Output or I/O Capacitance		20	pF	EFI = 1 MHz (Note 7)
C _{CLK}	EFI Capacitance		15	pF	EFI = 1 MHz (Note 7)

NOTES:

- List of pins which have 24 mA/4 mA I_{OL}/I_{OH} specification, (reference section 2), except IOCHRDY, IOCS16# and MEMCS16#.
- Other output pins which do not belong to list in Note 1, (reference Section 2).
- This is the maximum current the bus hold circuit can sink without raising the node above 0.8V. I_{BHL} should be measured after lowering V_{IN} to Ground (0V) and then raising to 0.8V.
- This is the maximum current the bus hold circuit can source without lowering the node voltage below 3.0V. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V.
- An external driver must source at least I_{BHLO} to switch this node from low to high.
- An external driver must sink at least I_{BHHO} to switch this node from high to low.
- Guaranteed by design characterization.

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FUNCTIONAL OPERATING RANGE: $V_{CC} = 5V \pm 10\%$; $T_{CASE} = 0^{\circ}C$ to $90^{\circ}C$.Table 2.3-4. Intel386™ SL CPU I_{CC} Specifications

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Symbol	Parameter	Typ	Max	Unit	Notes
I_{CC} (16 MHz)	Supply Current		450	mA	(Note 1a)
	Notebook Configuration	50		mA	(Note 2)
	Desktop Configuration	50		mA	(Note 3)
I_{CC} (20 MHz)	Supply Current		525	mA	(Note 1b)
	Notebook Configuration	50		mA	(Note 2)
	Desktop Configuration	50		mA	(Note 3)
I_{CC} (25 MHz)	Supply Current		600	mA	(Note 1c)
	Notebook Configuration	50		mA	(Note 2)
	Desktop Configuration	570		mA	(Note 3)
I_{CCS1}	Supply Current with the STPCLK Signal Asserted	50		mA	(Note 4)
I_{CCS2}	Supply Current in Suspend Mode with Oscillators OFF and Suspend Refresh ON	0.3		mA	(Note 5)
I_{CCS3}	Supply Current in Suspend Mode with Oscillators OFF and Suspend Refresh OFF	0.2	2	mA	(Note 6)

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NOTES:

- 1a. Tested with $V_{CC} = 5.5V$, $EFI = 32$ MHz, $ISACKL = 16$ MHz, 50 pF capacitive loads and no resistive load on the outputs.
- 1b. Tested with $V_{CC} = 5.5V$, $EFI = 40$ MHz, $ISACKL2 = 16$ MHz, 50 pF capacitive loads and no resistive load on the outputs.
- 1c. Tested with $V_{CC} = 5.5V$, $EFI = 50$ MHz, $ISACKL2 = 16$ MHz, 50 pF capacitive loads and no resistive load on the outputs.
2. Notebook system configuration consists of 1 bank of 1 MB \times 4 DRAMs with 1 MB \times 1 DRAMs for parity (2 MB total memory with Cache enabled. 25 pF capacitive loading on PI-bus control/status signals, 100 pF capacitive loading on the ISA bus signals and SYSCLK.
3. Desktop system configuration consists of 4 banks of DRAM in the configuration ((1 MB \times 4) \times 2 + 1 MB \times 1) for banks 0 and 1 and (1 MB \times 9) for banks 3 and 4 (20 MB total memory). Cache is enabled with 2 \times (16K \times 16) SRAMs and 240 pF on the ISA bus signals including SYSCLK from 8 ISA slots.
4. STPCLK signal asserted, all external oscillators free running, no cycles on cache, memory or ISA bus. Typically with $V_{CC} = 5V$, $EFI = 40$ MHz, $ISACKL2 = 16$ MHz, 50 pF capacitive loads and no resistive loads on the outputs.
5. Suspend mode and all external oscillators turned OFF (in a fixed logic state), no cycles on cache, memory or ISA bus. The REFREQ signal is active causing memory refreshes to the on-board DRAM memory during suspend. Typically with $V_{CC} = 5V$, 50 pF capacitive loads and no resistive loads on the outputs.
6. Tested with $V_{CC} = 5.5V$, 50 pF capacitive loads and no resistive load on the outputs. The 386 SL CPU is in suspend mode and all external oscillators turned OFF (in a fixed logic state), no cycles on cache, memory or ISA bus. The REFREQ signal is turned OFF (Refresh is not required if the on-board memory consists of battery backed SRAMs).

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2.3.2 Intel386™ SL CPU I_{CC} SPECIFICATIONS: SPECIAL TOPICS

2.3.2.1 Determining I_{CC} with Slow Clock Control

The Intel386 SL CPU supports CPU clock division which reduces power consumption of the CPU core logic. The EFI clock input is similar to the CLK2 input found on the Intel386 SL CPU. However, the internal CPUCLK signal in the Intel386 SL CPU is not always one half of the frequency of the EFI input. An internal clock divider and synchronizer allows the CPU core clock to be slowed down and even stopped. However, additional internal logic such as the memory controller and cache controller continue to use half the EFI frequency. Therefore, when calculating the theoretical power consumption with CPU clock division it is important to recognize that a fixed constant (K) value of power is required by the Intel386 SL CPU.

The value K is constant only if the ISA bus loading is constant. Figure 2.2 shows the value of K for different values of ISA bus capacitance.

$$I_{CC}(\text{divided clock}) = \left[\frac{I_{CC}(\text{normal clock}) - nI}{K} \right]$$

I_{CC}(normal clock) = The I_{CC} value calculated from the following section.

n = The fractional value that the clock is divided (e.g., divide by 2 = 0.5)

K = Is a constant in MilliAmps which determined by reading the value in Figure 2.2.

To determine the maximum current for the Intel386 SL CPU with EFI divider perform the following steps:

1. Sum the total capacitive load of all active ISA bus output signals from the Intel386 SL CPU to all devices.
2. From Figure 2.2 draw a line from the horizontal axis (capacitance) where it intersects the diagonal line.
3. From Figure 2.2 draw a perpendicular line to the vertical axis to determine K.
4. Solve the equation for I_{CC} (divided clock).

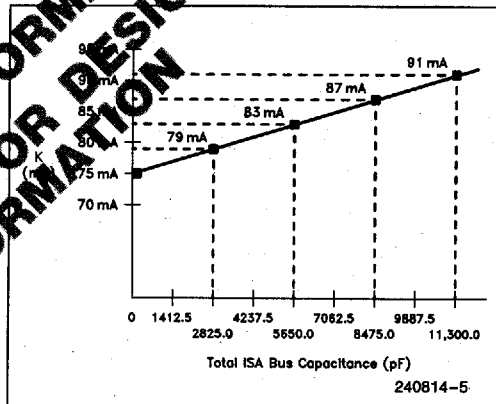


Figure 2.2. Variation of the constant current (K) with respect to the total ISA bus capacitance

POWER VARIATIONS WITH CAPACITIVE LOADS AT VARIOUS VOLTAGES

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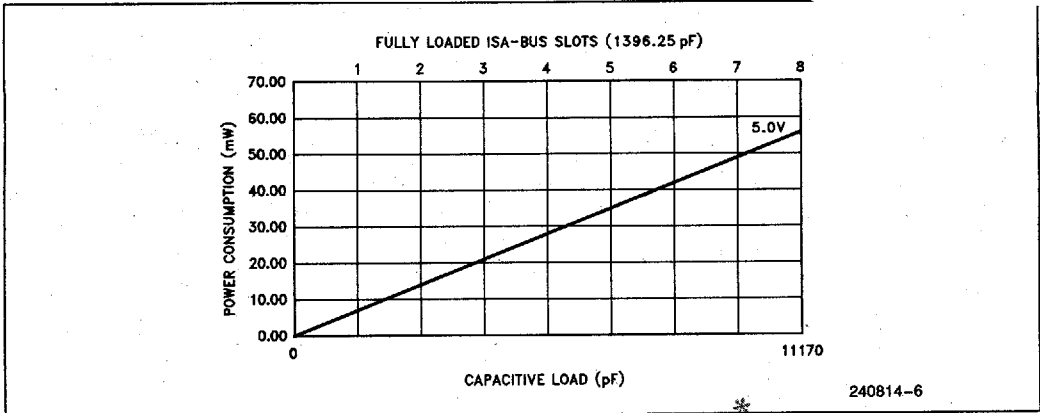


Figure 2.3. ISA Bus

2

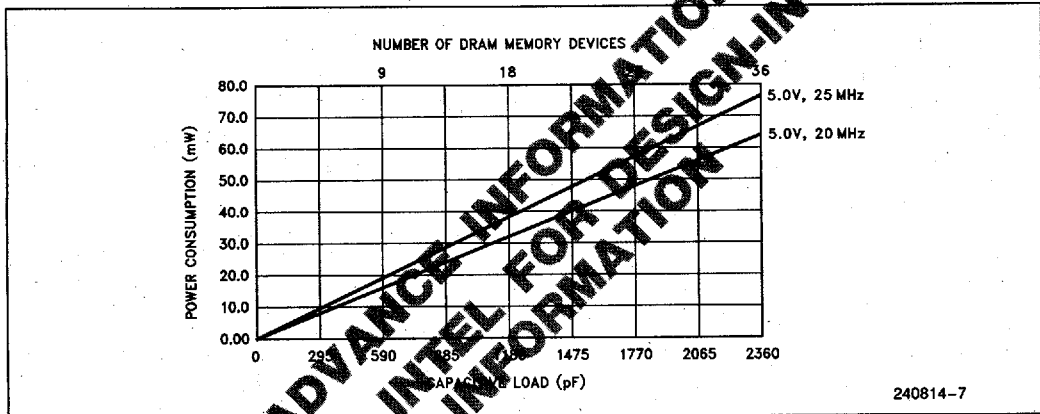


Figure 2.4a. Memory Bus without Cache

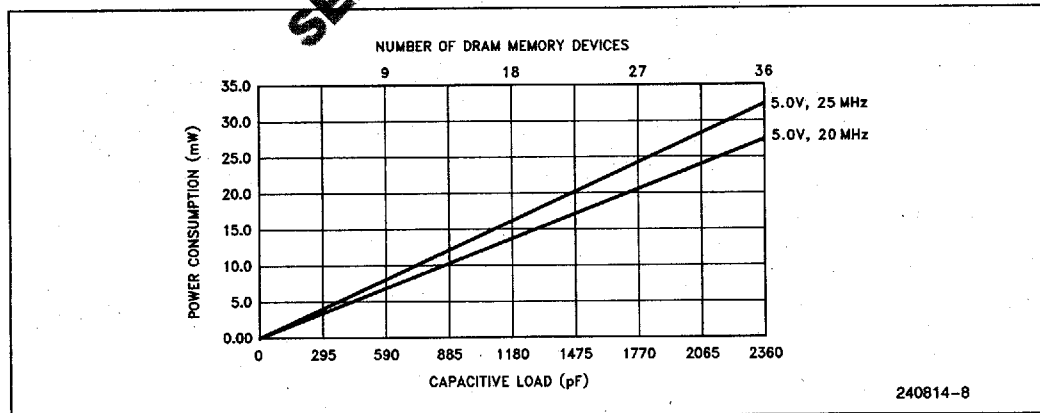


Figure 2.4b. Memory Bus with Cache



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2.3.2.2 Calculation of I_{CC} for Various SL SuperSet System Configurations

Figure 2.3 illustrates the power consumption in milliWatts with respect to the capacitive loading on the ISA bus signals of the Intel386 SL CPU. A set of two curves with V_{CC} at 5V and CPUCLK frequencies at 20 and 25 MHz are plotted in Figure 2.4a. This set of curves is provided for the memory bus without a cache subsystem in Figure 2.4a. The power consumption with respect to load capacitance for the memory bus with a cache subsystem is illustrated in Figure 2.4b. To find the Power (P in milliWatts) of the Intel386 SL CPU for the configuration of your system, use the following method.

1. Prepare a configuration list for your system including how many ISA-bus connectors, how many memory chips will be used and whether a cache will be connected or not.
2. From the curves in Figure 2.3, use the voltage of your system and the total capacitive load of all of the Intel386 SL CPU ISA signals to find the power consumed by the ISA-bus interface.
3. If a cache is connected to the Intel386 SL CPU in your system, use Figure 2.4b to find memory bus power. If cache is not connected, use Figure 2.4a.
4. Find the internal power consumption of the Intel386 SL CPU from Table 2.3-5 and the cache internal power and cache bus power from Tables 2.3-6 and 2.3-7.
5. For a system with no cache, add the ISA-bus interface power, the memory bus interface power without cache and the internal power. This gives the power consumption of the Intel386 SL CPU without cache.
6. For a system with cache, add the ISA bus interface power, the memory interface power with cache, the cache internal power, the cache bus interface power and the internal power. This gives the power consumption of the Intel386 SL CPU with cache.

NOTE:

Data provided in Figures 2.2 through 2.4b and in Tables 2.3-5 through 2.3-7 is based on engineering approximation and is given as an evaluation tool only.

Table 2.3-5. Internal Power

Frequency (MHz)	Power (mW)
20	1220
25	1525

Table 2.3-6. Cache Bus Power (mW)

Freq. (MHz)	5.0V
20	30
25	38

Table 2.3-7. Cache Internal Power

Frequency (MHz)	Power (mW)
20	170
25	215

As an example, the power consumed by the Intel386 SL CPU when it is used in a 20 MHz system with 8 memory chips and 2 fully loaded ISA bus expansion slots will be calculated. The system voltage is assumed to be 5V.

From Figure 2.3, the power consumed by the ISA expansion bus interface is found to be 15 mW (the total capacitance of all the pins of a fully loaded AT-bus slot is 1396.25 pF). For a system with no cache, the power consumed by the memory bus for 8 chips is about 15 mW from Figure 2.4a. The internal power at 20 MHz is 1220 mW from Table 2.3-5. The power consumed by Intel386 SL CPU is the sum of the power for the internal power (ISA bus and CPU core) and memory bus. The total power consumed by the Intel386 SL CPU for this system is 1250 mW.

For a system with cache, the ISA bus interface power is 15 mW as previously determined. The memory bus interface power is determined from Figure 2.4b is found to be 8 mW. The internal power remains 1220 mW. The cache bus power is read off from Table 2.3-6 to be 30 mW and the cache internal power from Table 2.3-7 is 170 mW. Hence, in this system, the Intel386 SL CPU consumes a total of 1443 mW.

2.4 Timing Specifications

A.C. Specification Definitions

The A.C. specifications given in the tables of the following pages consist of output delays, input setup and hold requirements. They may be relative to a clock edge or another signal edge. ALL CPU clock

related specifications reference EFl except ISA bus timings which reference ISACK2. A.C. specifications are defined in Figure 2.4.1. All clock related specifications are tested at the voltage levels shown. Output specifications are derived from tested clock related timings.

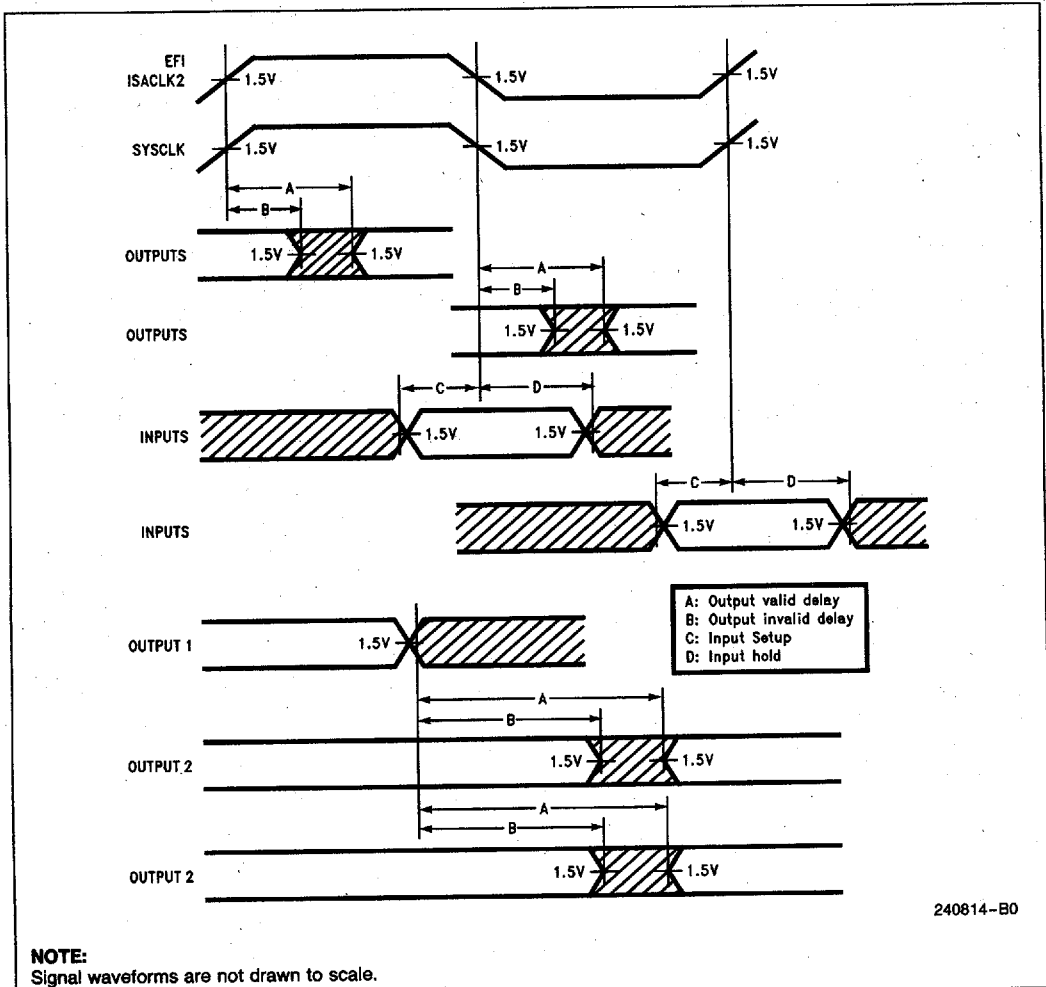


Figure 2.4.1. Drive Levels and Measurement Points for A.C. Specifications



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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
ISA-Bus Clock Timings							
Ct 201	ISACK2 Period	62.5		ns	*	2.5.2	(Note 1)
Ct 202	ISACK2 High Time at 2V	28	32.5	ns		2.5.2	(Note 1)
Ct 203	ISACK2 Low Time at 2V	28	32.5	ns		2.5.2	(Note 1)
Ct 204	ISACK2 Fall Time from (V _{CC} - 0.8V) to 0.8V		8	ns		2.5.2	(Note 1)
Ct 205	ISACK2 Rise Time from 0.8V to (V _{CC} - 0.8V)		8	ns		2.5.2	(Note 1)
Ct 206	ISACK2 to SYSCLK Delay, Falling to Rising Edge	2	30	ns	FR; SR	2.5.2	
Ct 207	ISACK2 to SYSCLK Delay, Falling to Falling Edge	2	32	ns	FF; SF	2.5.2	
Ct 211	SYSCLK Period	165		ns		2.5.2	(Note 2)
Ct 212	SYSCLK High Time at 1.5V			ns		2.5.2	(Note 2)
Ct 213	SYSCLK Low Time at 1.5V	57		ns		2.5.2	(Note 2)
Ct 214	SYSCLK Fall Time from (V _{CC} - 0.8V) to 0.8V			ns		2.5.2	(Note 2)
Ct 215	SYSCLK Rise Time from 0.8V to (V _{CC} - 0.8V)		10	ns		2.5.2	(Note 2)
Ct 272a	A20GATE Setup to EFI (ns)	11		ns			(Note 3)
Ct 272b	A20GATE Hold Time (ns)	16		ns			(Note 3)

NOTES:

- ISACK2 minimum period, high and low times are specified with ISACK2 input = 16 MHz and SYSCLK output = 8 MHz. The ISACK2 input specifications are provided to ensure that the SYSCLK output, period, minimum high and low time, rise and fall time and ISACK2 to SYSCLK skew are met.
- SYSCLK period, low and high time are tested at 1.5V thresholds. All other parameters are guaranteed by design characterization.
- A20GATE is an asynchronous input to the Intel386 SL CPU. Setup and hold times with respect to EFI are provided for test purposes only.



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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
ISA-Bus Timings							
Ct 221	BALE Active Delay from T _S phi 2 Low		52	ns	SR	2.5.12	NT1
Ct 222	BALE Inactive Delay from T _C phi 1 Low	5	52	ns	FF; SF	2.5.12	
Ct 223	LA17-23 Valid Delay from T _C or T _C phi 2 Low		52	ns	S	2.5.12	
Ct 224	LA17-23 Invalid Delay from T _C phi 2 Low	0		ns	F	2.5.12	
Ct 225	SA1-19 Valid Delay from T _S phi 2 Low		44	ns	S	2.5.12	
Ct 226	SA0-19, SBHE#, LA17-23 Valid Setup to phi 1 Low (External Master)	18		ns	*	2.5.27	
Ct 227	SA1-19 Invalid Delay from T _S or Ti phi 2 Low	0				2.5.12	
Ct 228	SA0, SBHE# Valid Delay from T _S phi 2 Low		52			2.5.12	
Ct 229	SA0, SBHE# Invalid Delay from T _S or Ti phi 2 Low	0	45	ns	FR; SR	2.5.12	
Ct 230	MEMR#, MEMW# Active from T _C phi 1 Low (16-bit MEMR#/MEMW#, HALT# Cycles)	7			FF; SF	2.5.18	
Ct 231	Command Active Setup to phi 1 Low (External Master)			ns		2.5.27	
Ct 232	HALT# Valid Delay from phi 1 Low				SF		NT8
Ct 233	Command Inactive to Float Delay from Ti phi 1 Low (External Master)		45	ns	S	2.5.27	
Ct 234	Command Active Delay from T _C phi 2 Low (IOR#/IOW# 8-, 16-Bit; MEMR#/MEMW# 8-Bit)		5	ns	FF; SF	2.5.12	
Ct 235	Command Inactive Delay from Teoc phi 1 Low (MEMR#/MEMW#, IOR#/IOW# and HALT#)		45	ns	FR; SR	2.5.12	NT2
Ct 238	MEMCS16# Setup to T _C phi 1 Low	0		ns		2.5.13	NT6, NT12
Ct 239	MEMCS16# Hold from phi 1 Low	25		ns		2.5.13	NT6, NT12
Ct 240	IOCS16# Setup to T _C phi 1 Low		45	ns		2.5.15	NT7
Ct 241	IOCS16# Hold from Teoc phi 1 Low	0		ns		2.5.21	NT7
Ct 242	ZEROWS# Setup to T _C phi 1 Low	0		ns		2.5.21	NT7, NT9
Ct 244	ZEROWS# Hold from T _C phi 2 Low	10		ns		2.5.15	NT7, NT9
Ct 245	MEMCS16# Active Delay from Valid Address (External Master Cycles)		64	ns	SF	2.5.28b	
Ct 246	SD0-15 Valid Setup to IOR#/MEMR#, INTA# Inactive	63		ns		2.5.13	
Ct 247	SD0-15 Hold from IOR#/MEMR#, INTA# Inactive	0				2.5.12	Read Cycle
Ct 248	SD0-7 Valid Delay from T _S phi 2 Low	30	65	ns	F; S	2.5.12	Write Cycle
Ct 249	SD8-15 Valid Delay from T _S phi 2 Low	37	65	ns	F; S		Write Cycle
Ct 250	SD0-15 Invalid Delay from Teoc phi 2 Low	12		ns		2.5.12	Write Cycle

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
ISA-Bus Timings (Continued)							
Ct 251	IOCHRDY Setup to T _C phi 1 Low	6		ns		2.5.14	
Ct 251a	IOCHRDY Inactive Setup to T _C phi 2 Low	45		ns		2.5.20	
Ct 252	IOCHRDY Hold from T _C phi 1 Low	8		ns	*	2.5.14	NT11
Ct 259	INTA# Active Delay from T _C phi 2 Low		45	ns		2.5.23	NT16
Ct 260	INTA# Inactive Delay from Teoc phi 1 Low		60	ns	FR	2.5.23	NT17
Ct 261	HRQ Setup to T _C or T _I phi 2 Low	15		ns		2.5.24	
Ct 262	HRQ Hold from Th phi 2 Low	5		ns		2.5.24	
Ct 263	HLDA Active Delay from Th phi 1 Low	0	38	ns	FF; SR	2.5.24	NT9
Ct 264	HLDA Inactive Delay from Th phi 1 Low	7	38	ns	FF; SF	2.5.24	
Ct 265	DMA8/16# Setup to Th phi 2 Low	15		ns		2.5.24	NT13, NT14, NT15
Ct 266	MASTER# Setup to Th phi 2 Low	15		ns		2.5.26	NT15
Ct 267	REFREQ Setup to T _I or T _C phi 2 Low			ns		2.5.25	
Ct 268	VGACS# Active Delay from LA[23:17]			ns	SF	2.5.10	
Ct 269	VGACS# Inactive Delay from LA[23:17]			ns	SR	2.5.10	
Ct 269a	VGACS# Active Delay from T _C phi 2 Low			ns	SF	2.5.19	
Ct 269b	VGACS# Inactive Delay from T _C phi 2 Low			ns	SR	2.5.19	
Ct 270	ROMCSO#/CMUX14# Active Delay from T _S phi 2 Low		41	ns	SF	2.5.11	NT18
Ct 271	ROMCSO#/CMUX14# Inactive Delay from T _S phi 2 Low		25	ns	FR	2.5.11	NT18
Ct 272	ROMCSO#/CMUX14# Active Delay from Address		41	ns	SF	2.5.9	NT19
Ct 273	ROMCSO#/CMUX14# Inactive Delay from Address		41	ns	SR	2.5.9	NT19
Ct 274	SMRAMCS# Active Delay from T _S phi 2 Low	5	49	ns	FF; SF	2.5.11	NT18
Ct 275	SMRAMCS# Inactive Delay from T _S or T _I phi 2 Low	5	49	ns	FR; SR	2.5.11	NT18
Ct 275a	TURBO Setup	16		ns			Asynch

2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
ISA-Bus Timings (Continued)							
Ct 276	SD15-0 Valid Delay from IOCHRDY Asserted (External Master)		48	ns	SR, S	2.5.28b	
Ct 277	SD15-0 Data Invalid Delay from MEMR# Inactive (External Master)	7		ns	F	2.5.28b	
Ct 278	SD15-0 Data Invalid Delay from IOR# Inactive (External Master)	7		ns	F	2.5.28a	
Ct 279	SD15-0 Data Setup to MEMW# Active (External Master)	-45		ns	*	2.5.28b	
Ct 280	SD15-0 Data Hold from MEMW# Inactive (External Master)	0		ns		2.5.28b	
Ct 281	SD15-0 Setup to IOW# Active (External Master)	0				2.5.28a	
Ct 282	BALE Active Delay from Th phi 1 Low (External Master)		45	ns	SR	2.5.26	
Ct 283	BALE Inactive from Th phi 1 Low (External Master)		45		SF	2.5.26	
Ct 284	LA23-17, SA19-0, SBHE# Float to Invalid Delay from Th phi 2 (External Master)		45		S	2.5.26	
Ct 285	LA23-17, SA19-0, SBHE# Invalid to Float Delay from Th phi 1 (External Master)		50	ns	S	2.5.26	
Ct 286	SA19-17 Delay from LA19-17 (DMA Cycle)	10	46	ns	F, S	2.5.24	
Ct 287	Command Float to Inactive from Th phi 2 Low (External Master)		45	ns	S	2.5.24	
Ct 288	Address Setup to Command Inactive (External Master)	28		ns		2.5.28a	
Ct 289	SA15-0 Hold after A15# or IOW# Inactive (External Master)	15		ns		2.5.28a	
Ct 290	IOCS16# Active Delay to Valid Address (External Master)		64	ns	SF	2.5.28a	
Ct 291	SD15-0 Delay from IOR# Active (External Master Read from CPU I/O Ports)		65	ns	S	2.5.28a	
Ct 292	SD15-0 Valid Delay from phi 1 Low (External Master Read from On Board Memory)		95	ns	S	2.5.28a	
Ct 293	SD15-0 Hold from IOW# Inactive (External Master)	15		ns		2.5.28a	
Ct 294	Byte Swap Delay (External Master)	10	72	ns	F, S	2.5.26	NT5

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
ISA-Bus Timings (Continued)							
Ct 295	IOCHRDY Invalid from Command Active (External Master)		44	ns	SF	2.5.28b	
Ct 296	IOCHRDY Active Delay from phi 1 Low (External Master)		85	ns	SR	2.5.28b	
Ct 298	IOCS16# Inactive Delay from Address (External Master)		110	ns	*SR	2.5.28a	NT20
Ct 299	IOCS16#/MEMCS16#/MASTER# Float to High Delay		78	ns			NT20

NOTES:

- NT1. The ISA bus timings are specified in a synchronous manner with respect to the ISACKL2 input. ISACKL2 input is 16 MHz, which is twice the frequency of the SYSCLK output. Each SYSCLK period represents one T-state and each T-state corresponds to either the beginning of a bus cycle (T_{S} —Setup Status), middle of a bus cycle (T_C —execute command), end of cycle (T_{Eoc}), hold (T_H) or idle (T_I). States (T_{S} , T_C , T_H , and T_I) are comprised of two ISACKL2 periods (Phi 1 and Phi 2). The ISACKL2 Periods or Phases, (Phi 1 and Phi 2) falling or rising edge are used to reference the synchronous ISA parameters. ISACKL2 Phi 1 rising edge leads SYSCLK rising edge, ISACKL2 Phi 2 falling edge leads SYSCLK falling edge.
- NT2. T_{Eoc} represents the End of Cycle. The falling edge of ISACKL2 Phi 2 during T_C indicates T_{Eoc} .
- NT3. After HLDA (Hold Acknowledge) is de-asserted, the Intel386 SL CPU drives the address bus with the previous address that was latched prior to the beginning of the HLDA cycle. The term "invalid" refers to this latched address. The latched address may or may not be valid for the next CPU bus cycle. At the start of the next CPU bus cycle on an external bus a valid address will be placed on the address bus.
- NT4. INTR, NMI, SMI#, and TURBO are asynchronous inputs with respect to ISACKL2 and SYSCLK. These are input signals to the Intel386 SL CPU. Setup and hold times with respect to the ISACKL2 input are provided for reference. The minimum setup and hold times are specified for valid recognition at a specific clock edge in other timing diagrams with the EFI clock input.
- NT5. The setup time is required to ensure that byte swapping is not delayed when an external master reads from an 8-bit device on an odd byte address boundary.
- NT6. MEMCS16# is sampled on the falling edge of ISACKL2 Phi 2.
- NT7. IOCS16# and ZEROWS# are sampled on the falling edge of ISACKL2 Phi 1.
- NT8. HALT timing is identical to a 16-bit ISA bus default memory bus cycle except that no BALE or Status Signal is asserted.
- NT9. ZEROWS# and IOCHRDY should not both be driven LOW during the same bus cycle.
- NT11. IOCHRDY de-asserted (LOW) is sampled on the falling edge of ISACKL2 Phi 2 when Command is active (LOW). De-asserting IOCHRDY# adds incremental wait-states (1 SYSCLK long). IOCHRDY should not be held LOW longer than 17 SYSCLKs (2.1 μ s).
- NT12. ROM read bus cycles are similar to 8-/16-bit ISA bus memory read bus cycles except that MEMCS# is ignored. The strapping pin ROM16/8# is sampled to determine if the ROM read is an 8-bit or 16-bit memory read. Additionally ROMCS0# and/or ROMCS1# are asserted during a ROM read.
- NT13. DMA bus cycles are not supported to On-Board I/O ports. AEN is HIGH during MASTER, DMA and access to the configuration registers.
- NT14. Byte swap timing for 8-bit DMA bus cycles is identical to that of an external master.
- NT15. During DMA cycles the Intel386 SL CPU drives SA17-19 with the values of LA17-19 while HLDA is active. During other Slave cycles (i.e., Refresh and External Master) the Intel386 SL CPU does not drive SA17-19.
- NT16. During the INTA# cycle, SD8-15 should not change state. During the first INTA# pulse SD0-16 are ignored. The second INTA# pulse in an INTA# bus cycle indicates a bus cycle that is similar to an 8-bit I/O read in which the interrupt vector is read from SD0-7.
- NT17. The 8259 INTA# minimum pulse width is 160 ns.
- NT18. ROMCS0#, ROMCS1# and SMRAMCS# are specified with respect to ISACKL2 when the CPU is the bus master.
- NT19. ROMCS0#, ROMCS1# and SMRAMCS# are specified with respect to valid address when an external master controls the bus.
- NT20. The low to high or float to high delays on these signals are guaranteed for four ISA slots with a total of 160 pF capacitive load. The 386 SL CPU will pull these signals high at a slew rate of $(160/C) \cdot 0.021$ V/ns where C is the total capacitive load on the signal pin. To use 8 slots, these signals must be pulled up with 300 Ω resistors.



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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
General: 16 MHz							
Ct 101	EFI Period	31.25	500	ns		2.5.1	(Note 1)
Ct 102a	EFI High Time at 2V	9		ns		2.5.1	
Ct 102b	EFI High Time at 3.7V	6		ns		2.5.1	
Ct 103a	EFI Low Time at 2V	9		ns	*	2.5.1	
Ct 103b	EFI Low Time at 0.8V	7		ns		2.5.1	
Ct 104	EFI Fall Time from (V _{CC} - 0.8V) to 0.8V		8	ns		2.5.1	
Ct 105	EFI Rise Time from 0.8V to (V _{CC} - 0.8V)		8	ns		2.5.1	
Ct 111	PWRGOOD Minimum Pulse Width	1		ns	EFI		
Ct 111a	PWRGOOD Setup to EFI	12					(Note 2)
Ct 111b	PWRGOOD Hold Time	4					
Ct 112	CPURESET Minimum Pulse Width	1		ns	EFI		
Ct 112a	CPURESET—Setup to EFI	15					(Note 2)
Ct 112b	CPURESET Hold Time	4		ns			
Ct 113a	STPCLK# Setup to EFI	12			ns		(Note 2)
Ct 113b	STPCLK# Hold Time	6			ns		
Ct 114a	SUS_STAT# Setup to EFI	15			ns		(Note 2)
Ct 114b	SUS_STAT# Hold Time	15			ns		
Ct 115	ONCE# Minimum Pulse Width	15			ns		
Ct 115a	ONCE# Setup to EFI	20			ns		(Note 2)
Ct 115b	ONCE# Hold Time	15			ns		
Ct 116a	SMI# Setup to EFI	21			ns		(Note 2)
Ct 116b	SMI# Hold Time	21			ns		
Ct 117a	INTR Setup to EFI	15			ns		(Note 2)
Ct 117b	INTR Hold Time	45			ns		
Ct 118a	NMI Setup to EFI	11			ns		(Note 2)
Ct 118b	NMI Hold Time	16			ns		

NOTES:

1. EFI maximum period is specified only for the case where an MCP (Math co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.
2. A20GATE, CPURESET, INTR, NMI, ONCE#, PWRGOOD, SMI#, STPCLK#, and SUS_STAT# are asynchronous inputs to the Intel386 SL CPU. Setup and hold times with respect to the EFI input are provided for test purposes only. The minimum setup and hold times are specified for valid recognition at a specific clock edge. The minimum valid pulse width can be extrapolated from the setup and hold times with respect to EFI.



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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
PI-Bus Timings: 16 MHz							
Ct 301	Min. Chip Select and Command Setup to PSTART# Active	42.5		ns	SF, SF	2.5.7	C _R = Min, C _T = Max
Ct 302	Min. Chip Select and Command Hold from PSTART# Active	80		ns	FF, FR	2.5.7	C _R = Max, C _T = Min
Ct 304	Min. Read Data Setup Time to PCMD# Inactive	48		ns	*	2.5.7	
Ct 305	Min. Read Data Hold Time from PCMD# Inactive	12		ns		2.5.7	
Ct 307	Maximum Write Data Valid Delay from PSTART# Active		64			2.5.7	C _R = Min, C _T = Max
Ct 308	Min. Write Data Invalid Delay from PCMD# Inactive	31		ns	FF, F	2.5.7	C _R = Max, C _T = Min
Ct 309	Min Address Setup Time to PSTART# Active	32.5			SF, S	2.5.7	C _R = Min, C _T = Max
Ct 310	Min Address Hold Time from PSTART# Active			ns	FF, F	2.5.7	C _R = Max, C _T = Min
Ct 311	PSTART# Pulse Width	55		ns		2.5.7	
Ct 312	Min Delay from PSTART# Active to PCMD# Active			ns	SF, SF	2.5.7	C _R = Max, C _T = Min
Ct 313	Min Delay from PRDY# Active to PCMD# Inactive	37		ns	FR	2.5.7	
Ct 314	Min Delay from PCMD# Inactive to PSTART# Active			ns	FR, FF	2.5.7	C _R = Max, C _T = Max
Ct 315	PRDY# Hold from PCMD# Inactive	0	40	ns		2.5.7	
External Master Timings: SYSCLK at 8 MHz (Slave CPU)							
Ct 321	PW/R# Valid Delay		35	ns	SF	2.5.8	
Ct 321	PM/IO# Valid Delay		35	ns	SF	2.5.8	
Ct 321	VGACS# Valid Delay		35	ns	SF	2.5.8	
Ct 325	PSTART# Valid Delay		34	ns	SF	2.5.8	
Ct 326	PCMD# Valid Delay		34	ns	SF	2.5.8	
Ct 327a	PRDY# Set-up	5		ns		2.5.8	
Ct 327b	PRDY# Hold	25		ns		2.5.8	

NOTES:

1. VGACS#, FLSHDCS#, PW/R#, PM/IO# and Addresses change for each subsequent read or write.
2. PSTART# indicates a new cycle in which address, status and chip selects are valid before PSTART# is asserted LOW. PRDY# terminates each bus cycle and a new PSTART# is driven if a new address and status signals are available.
3. C_R is the capacitive load on the reference signal.
4. C_T is the capacitive load on the target signal.



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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes	
Math Coprocessor Timings: 16 MHz								
Ct 421	CA2 Valid Delay (NPX Cyc)	3	25	ns	FR, F; SR, S	2.5.3		
Ct 422	NPXADS# Valid Delay	5	27	ns	FR, FF; SR, SF	2.5.3		
Ct 423	NPXW/R# Valid Delay	5	27	ns	FR, FF; SR, SF	2.5.3		
Ct 424	CD Valid Delay (NPX Cycle)	2	35	ns	FR, F; SR, S	2.5.4		
Ct 425a	NPXRDY# Setup	16		ns		2.5.5		
Ct 425b	NPXRDY# Hold	3		ns		2.5.5		
Ct 426a	BUSY#, PEREQ, ERROR# Setup to NPXCLK phi1 high	23		ns		*2.5.5		
Ct 426b	BUSY#, PEREQ, ERROR# Hold from NPXCLK phi1 high	5		ns		2.5.5		
Ct 427a	CD Setup (NPX Cycle)	12		ns		2.5.3		
Ct 427b	CD Hold (NPX Cycle)	6		ns		2.5.3		
Ct 441	NPXCLK Period	31.25	500	ns		2.5.1	(Note 1)	
Ct 442a	NPXCLK High Time 2V	8		ns		2.5.1	(Note 1)	
Ct 442b	NPXCLK High Time 3.7V	5		ns		2.5.1		
Ct 443a	NPXCLK Low Time 2V	8		ns		2.5.1	(Note 1)	
Ct 443b	NPXCLK Low Time 0.8V	6		ns		2.5.1		
Ct 444	NPXCLK Fall Time (V _{CC} - 0.8V) to 0.8V		8	ns		2.5.1		
Ct 445	NPXCLK Rise Time 0.8V to (V _{CC} - 0.8V)		8	ns		2.5.1		
Ct 446	NPXCLK to NPXRESET inactive delay		18	ns	FR, FF; SR, SF			
SRAM Mode: 16 MHz Timings								
Ct 501	Access Time from OE#	50		ns		2.5.30	2 Wait State	
Ct 502	Access Time from OE#	60		ns			3 Wait State	
Ct 503	CE# Setup to OE# Active	50		ns	SF, SF		2 Wait State	C _R = 10 pF, C _T = 10 pF
Ct 504	CE# Setup to OE# Active	50		ns	SF, SF		3 Wait State	
Ct 505	Addr Setup to OE# Active	50		ns	SF, S		2 Wait State	C _R = 10 pF, C _T = 40 pF
Ct 506	Addr Setup to OE# Active	50		ns	SF, S		3 Wait State	
Ct 507	CE# Setup to WE# Active	0		ns	SF, SF		2 Wait State	C _R = 80 pF, C _T = 10 pF
Ct 508	CE# Setup to WE# Active	0		ns	SF, SF		3 Wait State	
Ct 509	Addr Setup to WE# Active	0		ns	SF, S		2 Wait State	C _R = 80 pF, C _T = 40 pF
Ct 510	Addr Setup to WE# Active	0		ns	SF, S		3 Wait State	
Ct 511	WE# Active Pulse Width	90		ns	S		2 Wait State	C _R = 80 pF
Ct 512	WE# Active Pulse Width	100		ns	S		3 Wait State	

NOTE:

- NPXCLK maximum period is specified only for the case where a MCP (Math Co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
SRAM Mode: 16 MHz Timings (Continued)							
Ct 513	WE# Recovery Time	10		ns	SR, S	2 Wait State	$C_R = 80$ pF, $C_T = 40$ pF
Ct 514	WE# Recovery Time	10		ns	SR, S		3 Wait State
Ct 515	Write Data Setup to WE# Inactive	40		ns	SR, S	2 Wait State	$C_R = 80$ pF, $C_T = 40$ pF
Ct 516	Write Data Setup to WE# Inactive	50		ns	SR, S		3 Wait State
Ct 517	Write Data Hold from WE# Inactive	0		ns	FR, F	2 Wait State	$C_R = 80$ pF, $C_T = 40$ pF
Ct 518	Write Data Hold from WE# Inactive	0		ns	FR, F		3 Wait State
Ct 519	DIR Setup to OE# Active	0		ns	SF, S	2 Wait State	$C_R = 10$ pF, $C_T = 10$ pF
Ct 520	DIR Setup to OE# Active	0		ns	SF, S		3 Wait State
Ct 523	OE# Inactive Setup to DEN# Active	40		ns	SF, S	2 Wait State	$C_R = 20$ pF, $C_T = 10$ pF
Ct 524	OE# Inactive Setup to DEN# Active	50		ns	SF, S		3 Wait State
Ct 525	DIR Inactive Setup to WE# Active	0		ns	SF, S	2 Wait State	$C_R = 80$ pF, $C_T = 10$ pF
Ct 526	DIR Inactive Setup to WE# Active	0		ns	SF, S		3 Wait State
Ct 527	DEN# Hold from WE# Inactive	0		ns	SR, SR	2 Wait State	$C_R = 80$ pF, $C_T = 20$ pF
Ct 528	DEN# Hold from WE# Inactive	0		ns	SR, SR		3 Wait State
Ct 529	DIR Inactive Setup to DEN# Active	0		ns	SF, S	2 Wait State	$C_R = 20$ pF, $C_T = 10$ pF
Ct 530	DIR Inactive Setup to DEN# Active	0		ns	SF, S		3 Wait State
Ct 531	DIR Hold from DEN# Inactive	0		ns	SR, S	2 Wait State	$C_R = 20$ pF, $C_T = 10$ pF
Ct 532	DIR Hold from DEN# Inactive	0		ns	SR, S		3 Wait State
Ct 533	DIR Setup to DEN# Active	0		ns	SF, S; SF, S	2 Wait State	$C_R = 20$ pF, $C_T = 10$ pF
Ct 534	DIR Setup to DEN# Active	0	73	ns	SF, S; SF, S		3 Wait State
Ct 535	Upper Addr Setup to LE Inactive	8		ns	SF, S	2 Wait State	$C_R = 20$ pF, $C_T = 40$ pF
Ct 536	Upper Addr Setup to LE Inactive	8		ns	SF, S		3 Wait State
Ct 537	Upper Addr Hold from LE Inactive	4		ns	SF, S	2 Wait State	$C_R = 20$ pF, $C_T = 40$ pF
Ct 538	Upper Addr Hold from LE Inactive	4		ns	SF, S		3 Wait State
Ct 539	LE Active Pulse Width	8		ns	S	2 Wait State	$C_R = 20$ pF
Ct 540	LE Active Pulse Width	8		ns	S		3 Wait State
Ct 541	Addr Valid Delay from LE Inactive		60	ns	SF, S	2 Wait State	$C_R = 20$ pF, $C_T = 40$ pF
Ct 542	Addr Valid Delay from LE Inactive		80	ns	SF, S		3 Wait State
Ct 543	Read Data Hold from OE# Inactive	0		ns		2 Wait State	
Ct 544	Read Data Hold from OE# Inactive	0		ns			3 Wait State

ADVANCE INFORMATION
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2.5.30



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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes	
DRAM Mode: 16 MHz Timings									
Ct 601	tASR	Row Addr Setup to RAS# Active	0		ns	SF, S	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 602		Row Addr Setup to RAS# Active	7		ns			F2 Mode	
Ct 603		Row Addr Setup to RAS# Active	7		ns			P1 Mode	
Ct 605	tRAH	Row Addr Hold from RAS# Active	25		ns	SF, S	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 606		Row Addr Hold from RAS# Active	25		ns			F2 Mode	
Ct 607		Row Addr Hold from RAS# Active	25		ns			P1 Mode	
Ct 609	tASC	Col Addr Setup to CAS# Active	0		ns	* SF, S	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 610		Col Addr Setup to CAS# Active	0		ns			F2 Mode	
Ct 611		Col Addr Setup to CAS# Active	0		ns			P1 Mode	
Ct 613	tCAH	Col Addr Hold from CAS# Active	20		ns	S	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 614		Col Addr Hold from CAS# Active	20		ns			F2 Mode	
Ct 615		Col Addr Hold from CAS# Active	25		ns			P1 Mode	
Ct 617	tRCD	RAS# to CAS# Delay	25		ns	SF, SF	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 618		RAS# to CAS# Delay	25		ns			F2 Mode	
Ct 619		RAS# to CAS# Delay	25		ns			P1 Mode	
Ct 621	tCSH	CAS# Hold Time from RAS# Active	100		ns	SF, SR	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 622		CAS# Hold Time from RAS# Active	20		ns			F2 Mode	
Ct 623		CAS# Hold Time from RAS# Active	100		ns			P1 Mode	
Ct 625	tRSH	RAS# Hold Time from CAS# Active	45		ns	SF, SR	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 626		RAS# Hold Time from CAS# Active	45		ns			F2 Mode	
Ct 627		RAS# Hold Time from CAS# Active	45		ns			P1 Mode	
Ct 629	tWCS	WE# Setup to CAS# Active (Write)	0		ns	SF, SF	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 630		WE# Setup to CAS# Active (Write)	0		ns			F2 Mode	
Ct 631		WE# Setup to CAS# Active (Write)	0		ns			P1 Mode	
Ct 633	tWCH	WE# Hold from CAS# Active (Write)	25		ns	SF, SR	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 634		WE# Hold from CAS# Active (Write)	25		ns			F2 Mode	
Ct 635		WE# Hold from CAS# Active (Write)	25		ns			P1 Mode	
Ct 637	tRCS	WE# Inactive Setup to CAS# Active (Read)	0		ns	SF, SR	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 638		WE# Inactive Setup to CAS# Active (Read)	0		ns			F2 Mode	
Ct 639		WE# Inactive Setup to CAS# Active (Read)	0		ns			P1 Mode	
Ct 641	tRCH	WE# Inactive Hold from CAS# Inactive (Read)	0		ns	SR, SF	2.5.29	F1 Mode	C _R = Max, C _T = Max
Ct 642		WE# Inactive Hold from CAS# Inactive (Read)	0		ns			F2 Mode	
Ct 643		WE# Inactive Hold from CAS# Inactive (Read)	0		ns			P1 Mode	

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
DRAM Mode: 16 MHz Timings (Continued)								
Ct 645	tWDS	Write Data Setup to CAS# Active	0		ns	SF, S	2.5.29	F1 Mode C _R = Max, C _T = Max
Ct 646		Write Data Setup to CAS# Active	0		ns			F2 Mode
Ct 647		Write Data Setup to CAS# Active	0		ns			P1 Mode
Ct 649	tWDH	Write Data Hold from CAS# Active	20		ns	SF, S	2.5.29	F1 Mode C _R = Max, C _T = Max
Ct 650		Write Data Hold from CAS# Active	20		ns			F2 Mode
Ct 651		Write Data Hold from CAS# Active	20		ns			P1 Mode
Ct 653	tRAC	Access Time from RAS# Active	100		ns	*	2.5.29	F1 Mode
Ct 654		Access Time from RAS# Active	100		ns			F2 Mode
Ct 655		Access Time from RAS# Active	100		ns			P1 Mode
Ct 657	tCAC	Access Time from CAS# Active	30		ns		2.5.29	F1 Mode
Ct 658		Access Time from CAS# Active	30		ns			F2 Mode
Ct 659		Access Time from CAS# Active	50		ns			P1 Mode
Ct 661	tRDH	Read Data Hold from CAS# Inactive	0		ns		2.5.29	F1 Mode
Ct 662		Read Data Hold from CAS# Inactive	0		ns			F2 Mode
Ct 663		Read Data Hold from CAS# Inactive	0		ns			P1 Mode
Ct 665	tRAS	RAS# Active Pulse Width	100		ns		2.5.29	F1 Mode
Ct 666		RAS# Active Pulse Width	100		ns			F2 Mode
Ct 667		RAS# Active Pulse Width	200		ns			P1 Mode
Ct 669	tCAS	CAS# Active Pulse Width	30		ns		2.5.29	F1 Mode
Ct 670		CAS# Active Pulse Width	30		ns			F2 Mode
Ct 671		CAS# Active Pulse Width	30		ns			P1 Mode
Ct 673	tRP	RAS# Precharge Pulse Width	90		ns		2.5.29	F1 Mode
Ct 674		RAS# Precharge Pulse Width	90		ns			F2 Mode
Ct 675		RAS# Precharge Pulse Width	90		ns			P1 Mode
Ct 677	tCP	CAS# Precharge Pulse Width	20		ns		2.5.29	F1 Mode
Ct 678		CAS# Precharge Pulse Width	20		ns			F2 Mode
Ct 679		CAS# Precharge Pulse Width	25		ns			P1 Mode
Ct 681	tPSW	PARx Setup to CAS# Active (Write)	0		ns	SF, S	2.5.29	F1 Mode C _R = Max, C _T = Max
Ct 682		PARx Setup to CAS# Active (Write)	0		ns			F2 Mode
Ct 683		PARx Setup to CAS# Active (Write)	0		ns			P1 Mode
Ct 685	tPHW	PARx Hold from CAS# Active (Write)	20		ns	SF, S	2.5.29	F1 Mode C _R = Max, C _T = Max
Ct 686		PARx Hold from CAS# Active (Write)	20		ns			F2 Mode
Ct 687		PARx Hold from CAS# Active (Write)	20		ns			P1 Mode



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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 16 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating*	Figure	Notes
DRAM Mode: 16 MHz Timings (Continued)								
Ct 689	tPVR	PARx Valid from CAS# Active (Read)	30		ns		2.5.29	F1 Mode
Ct 690		PARx Valid from CAS# Active (Read)	30		ns	SF, S		F2 Mode
Ct 691		PARx Valid from CAS# Active (Read)	50		ns			P1 Mode
Ct 693	tPHR	PARx Hold from CAS# Inactive (Read)	0		ns		2.5.29	F1 Mode
Ct 694		PARx Hold from CAS# Inactive (Read)	0		ns	SR, S		F2 Mode
Ct 695		PARx Hold from CAS# Inactive (Read)						P1 Mode
Other DRAM Timings								
Ct 701	tPED	PERR# Delay from SYSCLK		38		SR, SF	2.5.34	C _R = Max C _T = Max
Ct 702	tCSR	CAS# Setup to RAS# Active (DRAM Refresh)			ns	SF, SF	2.5.31	C _R = Max C _T = Max
Ct 703	tCHR	CAS# Hold from RAS# Active (DRAM Refresh)			ns	FF, FR	2.5.31	C _R = Min C _T = Min
Ct 704	tWSR	WE# Inactive Setup to RAS# Active (DRAM Refresh)	15		ns	SF, SF	2.5.31	C _R = Min, C _T = Max
Ct 705	tWHR	WE# Inactive Hold from RAS# Inactive (DRAM Refresh)	15		ns	FF, FR	2.5.31	C _R = Min C _T = Min
Ct 706	tRDS	RAS# Active Delay from SYSCLK (DRAM DMA/Master)		55	ns	SF	2.5.33	
Ct 707	tADS	Address Valid Delay from SYSCLK (DRAM DMA/Master)		65	ns	S	2.5.32	

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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
General: 20 MHz							
Ct 101	EFI Period	25	500	ns		2.5.1	(Note 1)
Ct 102a	EFI High Time at 2V	8		ns		2.5.1	
Ct 102b	EFI High Time at 3.7V	5		ns		2.5.1	
Ct 103a	EFI Low Time at 2V	8		ns	*	2.5.1	
Ct 103b	EFI Low Time at 0.8V	6		ns		2.5.1	
Ct 104	EFI Fall Time from (V _{CC} - 0.8V) to 0.8V		8	ns		2.5.1	
Ct 105	EFI Rise Time 0.8V to (V _{CC} - 0.8V)		8	ns		2.5.1	
Ct 111	PWRGOOD Minimum Pulse Width	1		ns			
Ct 111a	PWRGOOD Setup to EFI	12		ns			(Note 2)
Ct 111b	PWRGOOD Hold Time	4		ns			
Ct 112	CPURESET Minimum Pulse Width	1		ns			
Ct 112a	CPURESET—Setup to EFI	12		ns			(Note 2)
Ct 112b	CPURESET Hold Time	4		ns			
Ct 113a	STPCLK# Setup to EFI	15		ns			(Note 2)
Ct 113b	STPCLK# Hold Time			ns			
Ct 114a	SUS_STAT# Setup to EFI	20		ns			(Note 2)
Ct 114b	SUS_STAT# Hold Time			ns			
Ct 115	ONCE# Minimum Pulse Width			ns			
Ct 115a	ONCE# Setup to EFI	20		ns			(Note 2)
Ct 115b	ONCE# Hold Time	15		ns			
Ct 116a	SMI# Setup to EFI	15		ns			(Note 2)
Ct 116b	SMI# Hold Time	21		ns			
Ct 117a	INTR Setup to EFI	15		ns			(Note 2)
Ct 117b	INTR Hold Time	45		ns			
Ct 118a	NMI Setup to EFI	11		ns			(Note 2)
Ct 118b	NMI Hold Time	16		ns			

NOTES:

1. EFI maximum period is specified only for the case where a MCP (Math co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.
2. A20GATE, CPURESET, INTR, NMI, ONCE#, PWRGOOD, SMI#, STPCLK# and SUS_STAT# are asynchronous inputs to the Intel386 SL CPU. Setup and hold times with respect to the EFI input are provided for test purposes only. The minimum setup and hold times are specified for valid recognition at a specific clock edge. The minimum valid pulse width can be extrapolated from the setup and hold times with respect to EFI.

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
PI-Bus Timings: 20 MHz							
Ct 301	Min. Chip Select and Command Setup to PSTART # Active	30		ns	SF, SF	2.5.7	C _R = Min, C _T = Max
Ct 302	Min. Chip Select and Command Hold from PSTART # Active	48		ns	FF, FR	2.5.7	C _R = Max, C _T = Min
Ct 304	Min. Read Data Setup Time to PCMD # Inactive	48		ns	*	2.5.7	
Ct 305	Min. Read Data Hold Time from PCMD # Inactive	12		ns		2.5.7	
Ct 307	Maximum Write Data Valid Delay from PSTART # Active		57			2.5.7	C _R = Min, C _T = Max
Ct 308	Min. Write Data Invalid Delay from PCMD # Inactive	25		ns	FF, F	2.5.7	C _R = Max, C _T = Min
Ct 309	Min Address Setup Time to PSTART # Active	20			SF, S	2.5.7	C _R = Min, C _T = Max
Ct 310	Min Address Hold Time from PSTART # Active			ns	FF, F	2.5.7	C _R = Max, C _T = Min
Ct 311	PSTART # Pulse Width	45		ns		2.5.7	
Ct 312	Min Delay from PSTART # Active to PCMD # Active			ns	SF, SF	2.5.7	C _R = Max, C _T = Min
Ct 313	Min Delay from PRDY # Active to PCMD # Inactive	32		ns	FR	2.5.7	
Ct 314	Min Delay from PCMD # Inactive to PSTART # Active	0		ns	FR, FF	2.5.7	C _R = Max, C _T = Max
Ct 315	PRDY # Hold from PCMD # Inactive	0	40	ns		2.5.7	
External Master Timings: PYSCL# at 8 MHz (Slave CPU)							
Ct 321	PW/R# Valid Delay		35	ns		2.5.8	
Ct 321	PM/IO# Valid Delay		35	ns		2.5.8	
Ct 321	VGACS# Valid Delay		35	ns		2.5.8	
Ct 325	PSTART # Valid Delay		34	ns		2.5.8	
Ct 326	PCMD # Valid Delay		34	ns		2.5.8	
Ct 327a	PRDY # Set-up	5		ns		2.5.8	
Ct 327b	PRDY # Hold	25		ns		2.5.8	

NOTES:

1. VGACS#, FLSDHCS#, PW/R#, PM/IO# and Addresses change for each subsequent read or write.
2. PSTART # indicates a new cycle in which address, status and chip selects are valid before PSTART # is asserted LOW.
3. PRDY # terminates each bus cycle and a new PSTART # is driven if a new address and status signals are available.
4. C_R is the capacitive load on the reference signal.
5. C_T is the capacitive load on the target signal.

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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications **20 MHz** (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Cache Bus Timing: 20 MHz							
Ct 401	CABUS Valid to CD Bus Valid		36	ns		2.5.6	
Ct 402	COE# Pulse Width	60		ns	SF, SR	2.5.6	
Ct 403	CSSH#, CCSL# Active to CD Bus Valid		36	ns		2.5.6	
Ct 404a	COE# Active to CD Bus Valid		25	ns		2.5.6	
Ct 404b	CDBUS Hold from COE# Inactive	0		ns		2.5.6	
Ct 405	CABUS Valid Setup to CWE# Active	1		ns	FF, F	2.5.6	C _R = Min, C _T = Max
Ct 406	CWE# Active Width	35		ns	SF, SR	2.5.6	
Ct 407	CDBUS Setup to CWE# Inactive	25		ns	SR, S	2.5.6	C _R = Min, C _T = Max
Ct 408	CDBUS Hold to CWE# Inactive	0		ns	.SR, S	2.5.6	C _R = Max, C _T = Max
Ct 409	CABUS Hold to CWE# Inactive	0		ns	FR, F	2.5.6	C _R = Max, C _T = Min
Math Coprocessor Timings: 20 MHz							
Ct 421	CA2 Valid Delay (NPX Cycle)		25	ns	FR, F; SR, S	2.5.3	
Ct 422	NPXADS# Valid Delay		27	ns	FR, FF; SR, SF	2.5.3	
Ct 423	NPXW/R# Valid Delay	5	27	ns	FR, FF; SR, SF	2.5.3	
Ct 424	CD Valid Delay (NPX Cycle)	2	35	ns	FR, F; SR, S	2.5.4	
Ct 425a	NPXRDY# Setup	16		ns		2.5.5	
Ct 425b	NPXRDY# Hold	3		ns		2.5.5	
Ct 426a	BUSY#, PEREQ, ERROR# Setup to NPXCLK phi1 high	19		ns		2.5.5	
Ct 426b	BUSY#, PEREQ, ERROR# Hold from NPXCLK phi1 high	4		ns		2.5.5	
Ct 427a	CD Setup (NPX Cycle)	12		ns		2.5.3	
Ct 427b	CD Hold (NPX Cycle)	6		ns		2.5.3	

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes	
Math Coprocessor Timings: 20 MHz (Continued)								
Ct 441	NPXCLK Period	25	500	ns		2.5.1	(Note 1)	
Ct 442a	NPXCLK High Time 2V	7		ns		2.5.1	(Note 1)	
Ct 442b	NPXCLK High Time 3.7V	4		ns		2.5.1		
Ct 443a	NPXCLK Low Time 2V	7		ns		2.5.1	(Note 1)	
Ct 443b	NPXCLK Low Time 0.8V	5		ns		2.5.1		
Ct 444	NPXCLK Fall Time (V _{CC} - 0.8V) to 0.8V		8	ns		2.5.1		
Ct 445	NPXCLK Rise Time 0.8V to (V _{CC} - 0.8V)		8	ns		2.5.1		
Ct 446	NPXCLK to NPXRESET inactive delay	3	14	ns	FR, F, SF			
SRAM Mode: 20 MHz Timings								
Ct 501	Access Time from OE#	40		ns		2.5.30	2 Wait State	
Ct 502	Access Time from OE#	50		ns			3 Wait State	
Ct 503	CE# Setup to OE# Active	40		ns	SF, SF		2 Wait State	C _R = 10 pF, C _T = 10 pF
Ct 504	CE# Setup to OE# Active	40		ns	SF, SF		3 Wait State	
Ct 505	Addr Setup to OE# Active	40		ns	SF, S		2 Wait State	C _R = 10 pF, C _T = 40 pF
Ct 506	Addr Setup to OE# Active	40		ns	SF, S		3 Wait State	
Ct 507	CE# Setup to WE# Active	40		ns	SF, SF		2 Wait State	C _R = 80 pF, C _T = 10 pF
Ct 508	CE# Setup to WE# Active	0		ns	SF, SF		3 Wait State	
Ct 509	Addr Setup to WE# Active	0		ns	SF, S		2 Wait State	C _R = 80 pF, C _T = 40 pF
Ct 580	Addr Setup to WE# Active	0		ns	SF, S		3 Wait State	
Ct 511	WE# Active Pulse Width	70		ns	S		2 Wait State	C _R = 80 pF
Ct 512	WE# Active Pulse Width	90		ns	S		3 Wait State	
Ct 513	WE# Recovery Time	10		ns	SR, S		2 Wait State	C _R = 80 pF, C _T = 40 pF
Ct 514	WE# Recovery Time	10		ns	SR, S		3 Wait State	
Ct 515	Write Data Setup to WE# Inactive	39		ns	SR, S		2 Wait State	C _R = 80 pF, C _T = 40 pF
Ct 516	Write Data Setup to WE# Inactive	44		ns	SR, S		3 Wait State	
Ct 517	Write Data Hold from WE# Inactive	0		ns	FR, F		2 Wait State	C _R = 80 pF, C _T = 40 pF
Ct 518	Write Data Hold from WE# Inactive	0		ns	FR, F		3 Wait State	

NOTE:

- NPXCLK maximum period is specified only for the case where a MCP (Math Co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
SRAM Mode: 20 MHz Timings (Continued)							
Ct 519	DIR Setup to OE# Active	0		ns	SF, S	*	2 Wait State C _R = 10 pF,
Ct 520	DIR Setup to OE# Active	0		ns	SF, S		3 Wait State C _T = 10 pF
Ct 523	OE# Inactive Setup to DEN# Active	30		ns	SF, SR	2.5.30	2 Wait State C _R = 20 pF,
Ct 524	OE# Inactive Setup to DEN# Active	40		ns	SF, S		3 Wait State C _T = 10 pF
Ct 525	DIR Inactive Setup to WE# Active	0		ns	SF, S	2.5.30	2 Wait State C _R = 80 pF,
Ct 526	DIR Inactive Setup to WE# Active	0		ns	SF, S		3 Wait State C _T = 10 pF
Ct 527	DEN# Hold from WE# Inactive	0		ns	SR, SF	2.5.30	2 Wait State C _R = 80 pF,
Ct 528	DEN# Hold from WE# Inactive	0		ns	SF, S		3 Wait State C _T = 20 pF
Ct 529	DIR Inactive Setup to DEN# Active	0		ns	SF, S	2.5.30	2 Wait State C _R = 20 pF,
Ct 530	DIR Inactive Setup to DEN# Active	0		ns	SF, S		3 Wait State C _T = 10 pF
Ct 531	DIR Hold from DEN# Inactive	0		ns	SF, S	2.5.30	2 Wait State C _R = 20 pF,
Ct 532	DIR Hold from DEN# Inactive	0		ns	SR, S		3 Wait State C _T = 10 pF
Ct 533	DIR Setup to DEN# Active	0	60	ns	SF, S; SF, S	2.5.30	2 Wait State C _R = 20 pF,
Ct 534	DIR Setup to DEN# Active	0	60	ns	SF, S; SF, S		3 Wait State C _T = 10 pF
Ct 535	Upper Addr Setup to LE Inactive	8		ns	SF, S	2.5.30	2 Wait State C _R = 20 pF,
Ct 536	Upper Addr Setup to LE Inactive	8		ns	SF, S		3 Wait State C _T = 40 pF
Ct 537	Upper Addr Hold from LE Inactive	4		ns	SF, S	2.5.30	2 Wait State C _R = 20 pF,
Ct 538	Upper Addr Hold from LE Inactive	4		ns	SF, S		3 Wait State C _T = 40 pF
Ct 539	LE Active Pulse Width	8		ns	S	2.5.30	2 Wait State C _R = 20 pF
Ct 540	LE Active Pulse Width	8		ns	S		3 Wait State
Ct 541	Addr Valid Delay from LE Inactive		50	ns	SF, S	2.5.30	2 Wait State C _R = 20 pF,
Ct 542	Addr Valid Delay from LE Inactive		70	ns	SF, S		3 Wait State C _T = 40 pF
Ct 543	Read Data Hold from OE# Inactive	0		ns		2.5.30	2 Wait State
Ct 544	Read Data Hold from OE# Inactive	0		ns			3 Wait State

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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
DRAM Mode: 20 MHz Timings								
Ct 601	tASR	Row Addr Setup to RAS# Active	0		ns			F1 Mode C _R = Max, C _T = Max
Ct 602		Row Addr Setup to RAS# Active	7		ns	SF, S		F2 Mode
Ct 603		Row Addr Setup to RAS# Active	7		ns			P1 Mode
Ct 605	tRAH	Row Addr Hold from RAS# Active	20		ns			F1 Mode
Ct 606		Row Addr Hold from RAS# Active	20		ns	SF, S		F2 Mode C _R = Max, C _T = Max
Ct 607		Row Addr Hold from RAS# Active	20		ns			P1 Mode
Ct 609	tASC	Col Addr Setup to CAS# Active	0		ns			F1 Mode
Ct 610		Col Addr Setup to CAS# Active	0		ns	SF		F2 Mode C _R = Max, C _T = Max
Ct 611		Col Addr Setup to CAS# Active	0		ns			P1 Mode
Ct 613	tCAH	Col Addr Hold from CAS# Active	15		ns			F1 Mode
Ct 614		Col Addr Hold from CAS# Active	15		ns	SF, S		F2 Mode C _R = Max, C _T = Max
Ct 615		Col Addr Hold from CAS# Active	25		ns			P1 Mode
Ct 617	tRCD	RAS# to CAS# Delay	25		ns			F1 Mode
Ct 618		RAS# to CAS# Delay	25		ns	SF, SF		F2 Mode C _R = Max, C _T = Max
Ct 619		RAS# to CAS# Delay	25		ns			P1 Mode
Ct 621	tCSH	CAS# Hold Time from RAS# Active			ns		2.5.29	F1 Mode
Ct 622		CAS# Hold Time from RAS# Active			ns	SF, SR		F2 Mode C _R = Max, C _T = Max
Ct 623		CAS# Hold Time from RAS# Active	100		ns			P1 Mode
Ct 625	tRSH	RAS# Hold Time from CAS# Active	25		ns			F1 Mode
Ct 626		RAS# Hold Time from CAS# Active	30		ns	SF, SR		F2 Mode C _R = Max, C _T = Max
Ct 627		RAS# Hold Time from CAS# Active	45		ns			P1 Mode
Ct 629	tWCS	WE# Setup to CAS# Active (Write)	0		ns			F1 Mode
Ct 630		WE# Setup to CAS# Active (Write)	0		ns	SF, SF		F2 Mode C _R = Max, C _T = Max
Ct 631		WE# Setup to CAS# Active (Write)	0		ns			P1 Mode
Ct 633	tWCH	WE# Hold from CAS# Active (Write)	20		ns			F1 Mode
Ct 634		WE# Hold from CAS# Active (Write)	20		ns	SF, SR		F2 Mode C _R = Max, C _T = Max
Ct 635		WE# Hold from CAS# Active (Write)	20		ns			P1 Mode
Ct 637	tRCS	WE# Inactive Setup to CAS# Active (Read)	0		ns			F1 Mode
Ct 638		WE# Inactive Setup to CAS# Active (Read)	0		ns	SF, SR		F2 Mode C _R = Max, C _T = Max
Ct 639		WE# Inactive Setup to CAS# Active (Read)	0		ns			P1 Mode
Ct 641	tRCH	WE# Inactive Hold from CAS# Inactive (Read)	0		ns			F1 Mode
Ct 642		WE# Inactive Hold from CAS# Inactive (Read)	0		ns	SR, SF		F2 Mode C _R = Max, C _T = Max
Ct 643		WE# Inactive Hold from CAS# Inactive (Read)	0		ns			P1 Mode

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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
DRAM Mode: 20 MHz Timings (Continued)								
Ct 645	tWDS	Write Data Setup to CAS# Active	0		ns	SF, S	2.5.29	F1 Mode
Ct 646		Write Data Setup to CAS# Active	0		ns			F2 Mode
Ct 647		Write Data Setup to CAS# Active	0		ns			P1 Mode
Ct 649	tWDH	Write Data Hold from CAS# Active	20		ns	SF, S	2.5.29	F1 Mode
Ct 650		Write Data Hold from CAS# Active	20		ns			F2 Mode
Ct 651		Write Data Hold from CAS# Active	20		ns			P1 Mode
Ct 653	tRAC	Access Time from RAS# Active	80		ns	*	2.5.29	F1 Mode
Ct 654		Access Time from RAS# Active	100		ns			F2 Mode
Ct 655		Access Time from RAS# Active	100		ns			P1 Mode
Ct 657	tCAC	Access Time from CAS# Active	25		ns	2.5.29	2.5.29	F1 Mode
Ct 658		Access Time from CAS# Active	30		ns			F2 Mode
Ct 659		Access Time from CAS# Active	40		ns			P1 Mode
Ct 661	tRDH	Read Data Hold from CAS# Inactive	0		ns	2.5.29	2.5.29	F1 Mode
Ct 662		Read Data Hold from CAS# Inactive	0		ns			F2 Mode
Ct 663		Read Data Hold from CAS# Inactive	0		ns			P1 Mode
Ct 665	tRAS	RAS# Active Pulse Width	80		ns	2.5.29	2.5.29	F1 Mode
Ct 666		RAS# Active Pulse Width	100		ns			F2 Mode
Ct 667		RAS# Active Pulse Width	200		ns			P1 Mode
Ct 669	tCAS	CAS# Active Pulse Width	25		ns	2.5.29	2.5.29	F1 Mode
Ct 670		CAS# Active Pulse Width	30		ns			F2 Mode
Ct 671		CAS# Active Pulse Width	40		ns			P1 Mode
Ct 673	tRP	RAS# Precharge Pulse Width	70		ns	2.5.29	2.5.29	F1 Mode
Ct 674		RAS# Precharge Pulse Width	90		ns			F2 Mode
Ct 675		RAS# Precharge Pulse Width	90		ns			P1 Mode
Ct 677	tCP	CAS# Precharge Pulse Width	15		ns	2.5.29	2.5.29	F1 Mode
Ct 678		CAS# Precharge Pulse Width	15		ns			F2 Mode
Ct 679		CAS# Precharge Pulse Width	25		ns			P1 Mode
Ct 681	tPSW	PARx Setup to CAS# Active (Write)	0		ns	SF, SF	2.5.29	F1 Mode
Ct 682		PARx Setup to CAS# Active (Write)	0		ns			F2 Mode
Ct 683		PARx Setup to CAS# Active (Write)	0		ns			P1 Mode
Ct 685	tPHW	PARx Hold from CAS# Active (Write)	20		ns	SF, SF	2.5.29	F1 Mode
Ct 686		PARx Hold from CAS# Active (Write)	20		ns			F2 Mode
Ct 687		PARx Hold from CAS# Active (Write)	20		ns			P1 Mode



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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 20 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
DRAM Mode: 20 MHz Timings (Continued)								
Ct 689	tPVR	PARx Valid from CAS# Active (Read)	25		ns		2.5.29	F1 Mode
Ct 690		PARx Valid from CAS# Active (Read)	30		ns			F2 Mode
Ct 691		PARx Valid from CAS# Active (Read)	45		ns			P1 Mode
Ct 693	tPHR	PARx Hold from CAS# Inactive (Read)	0		ns		2.5.29	F1 Mode
Ct 694		PARx Hold from CAS# Inactive (Read)	0		ns			F2 Mode
Ct 695		PARx Hold from CAS# Inactive (Read)	0		ns			P1 Mode
Other DRAM Timings								
Ct 701	tPED	PERR# Delay from SYSCLK		38	ns	FF, SF	2.5.34	C _R = Max C _T = Max
Ct 702	tCSR	CAS# Setup to RAS# Active (DRAM Refresh)	10		ns	SF, SF	2.5.31	C _R = Max, C _T = Max
Ct 703	tCHR	CAS# Hold from RAS# Active (DRAM Refresh)	30		ns	FF, FR	2.5.31	C _R = Min, C _T = Min
Ct 704	tWSR	WE# Inactive Setup to RAS# Active (DRAM Refresh)			ns	SF, SF	2.5.31	C _R = Min, C _T = Max
Ct 705	tWHR	WE# Inactive Hold from RAS# Active (DRAM Refresh)	15		ns	FF, FR	2.5.31	C _R = Min, C _T = Min
Ct 706	tRDS	RAS# Active Delay from SYSCLK (DRAM DMA Master)		55	ns	SF	2.5.33	
Ct 707	tADS	Address Valid Delay from SYSCLK (DRAM DMA Master)		65	ns	S	2.5.32	

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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
General: 25 MHz							
Ct 101	EFI Period	20	500	ns		2.5.1	(Note 1)
Ct 102a	EFI High Time at 2V	7		ns		2.5.1	
Ct 102b	EFI High Time at 3.7V	4		ns		2.5.1	
Ct 103a	EFI Low Time at 2V	7		ns		2.5.1	
Ct 103b	EFI Low Time at 0.8V	5		ns		2.5.1	
Ct 104	EFI Fall Time from (V _{CC} - 0.8V) to 0.8V		7	ns		2.5.1	
Ct 105	EFI Rise Time 0.8V to (V _{CC} - 0.8V)		7	ns		2.5.1	
Ct 111	PWRGOOD Minimum Pulse Width	2		ns	EFI		
Ct 111a	PWRGOOD Setup to EFI	10		ns			(Note 2)
Ct 111b	PWRGOOD Hold Time	3		ns			
Ct 112	CPURESET Minimum Pulse Width	1		ns			
Ct 112a	CPURESET—Setup to EFI	10		ns			(Note 2)
Ct 112b	CPURESET Hold Time	3		ns			
Ct 113a	STPCLK# Setup to EFI	10		ns			(Note 2)
Ct 113b	STPCLK# Hold Time	3		ns			
Ct 114a	SUS_STAT# Setup to EFI	10		ns			(Note 2)
Ct 114b	SUS_STAT# Hold Time			ns			
Ct 115	ONCE# Minimum Pulse Width			ns			
Ct 115a	ONCE# Setup to EFI	10		ns			(Note 2)
Ct 115b	ONCE# Hold Time			ns			
Ct 116a	SMI# Setup to EFI	11		ns			(Note 2)
Ct 116b	SMI# Hold Time	15		ns			
Ct 117a	INTR Setup to EFI	11		ns			(Note 2)
Ct 117b	INTR Hold Time	16		ns			
Ct 118a	NMI Setup to EFI	11		ns			(Note 2)
Ct 118b	NMI Hold Time	16		ns			

NOTES:

1. EFI maximum period is specified only for the case where a MCP (Math co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.
2. A20GATE, CPURESET, INTR, NMI, ONCE#, PWRGOOD, SMI#, STPCLK# and SUS_STAT# are asynchronous inputs to the Intel386 SL CPU. Setup and hold times with respect to the EFI input are provided for test purposes only. The minimum setup and hold times are specified for valid recognition at a specific clock edge. The minimum valid pulse width can be extrapolated from the setup and hold times with respect to EFI.



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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
PI-Bus Timings: 25 MHz							
Ct 301	Min. Chip Select and Command Setup to PSTART# Active	20		ns	SF, SF	2.5.7	C _R = Min, C _T = Max
Ct 302	Min. Chip Select and Command Hold from PSTART# Active	38		ns	FF, FR	2.5.7	C _R = Max, C _T = Min
Ct 304	Min. Read Data Setup Time to PCMD# Inactive	48		ns		2.5.7	
Ct 305	Min. Read Data Hold Time from PCMD# Inactive	12		ns		2.5.7	
Ct 307	Maximum Write Data Valid Delay from PSTART# Active		52			2.5.7	C _R = Min, C _T = Max
Ct 308	Min. Write Data Invalid Delay from PCMD# Inactive	20		ns	FF, F	2.5.7	C _R = Max, C _T = Min
Ct 309	Min Address Setup Time to PSTART# Active	10			SF, S	2.5.7	C _R = Min, C _T = Max
Ct 310	Min Address Hold Time from PSTART# Active				FF, F	2.5.7	C _R = Max, C _T = Min
Ct 311	PSTART# Pulse Width	35		ns		2.5.7	
Ct 312	Min Delay from PSTART# Active to PCMD# Active			ns	SF, SF	2.5.7	C _R = Max, C _T = Min
Ct 313	Min Delay from PRDY# Active to PCMD# Inactive	26		ns	FR	2.5.7	
Ct 314	Min Delay from PCMD# Inactive to PSTART# Active			ns	FR, FF	2.5.7	C _R = Max, C _T = Max
Ct 315	PRDY# Hold from PCMD# Inactive	0	40	ns		2.5.7	
External Master Timings: SYSCLK at 8 MHz (Slave CPU)							
Ct 321	PW/R# Valid Delay		35	ns	SF	2.5.8	
Ct 321	PM/IO# Valid Delay		35	ns	SF	2.5.8	
Ct 321	VGACS# Valid Delay		35	ns	SF	2.5.8	
Ct 325	PSTART# Valid Delay		34	ns	SF	2.5.8	
Ct 326	PCMD# Valid Delay		34	ns	SF	2.5.8	
Ct 327a	PRDY# Set-up	5		ns		2.5.8	
Ct 327b	PRDY# Hold	25		ns		2.5.8	

NOTES:

1. VGACS#, FLSDCS#, PW/R#, PM/IO# and Addresses change for each subsequent read or write.
2. PSTART# indicates a new cycle in which address, status and chip selects are valid before PSTART# is asserted LOW. PRDY# terminates each bus cycle and a new PSTART# is driven if a new address and status signals are available.
3. C_R is the capacitive load on the reference signal.
4. C_T is the capacitive load on the target signal.



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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Cache Bus Timing: 25 MHz							
Ct 401	CABUS Valid to CD Bus Valid		25	ns		2.5.6	
Ct 402	COE# Pulse Width	45		ns	SF, SR	2.5.6	
Ct 403	COSH#, CCSL# Active to CD Bus Valid		25	ns		2.5.6	
Ct 404a	COE# Active to CD Bus Valid		15	ns	*	2.5.6	
Ct 404b	CDBUS Hold from COE# Inactive	0		ns		2.5.6	
Ct 405	CABUS Valid Setup to CWE# Active	1		ns	FF, F	2.5.6	C _R = Min, C _T = Max
Ct 406	CWE# Active Width	25		ns	SR	2.5.6	
Ct 407	CDBUS Setup to CWE# Inactive	15		ns	SR, S	2.5.6	C _R = Min, C _T = Max
Ct 408	CDBUS Hold to CWE# Inactive	0		ns	SR, S	2.5.6	C _R = Max, C _T = Max
Ct 409	CABUS Hold to CWE# Inactive	0		ns	FR, F	2.5.6	C _R = Max, C _T = Min
Math Coprocessor Timings: 25 MHz							
Ct 421	CA2 Valid Delay (NPX Cyc)	2	23	ns	FR, F; SR, S	2.5.3	
Ct 422	NPXADS# Valid Delay	4		ns	FR, FF; SR, SF	2.5.3	
Ct 423	NPXW/R# Valid Delay	4		ns	FR, FF; SR, SF	2.5.3	
Ct 424	CD Valid Delay (NPX Cycle)	8	35	ns	FR, F; SR, S	2.5.4	
Ct 425a	NPXRDY# Setup	3		ns		2.5.5	
Ct 425b	NPXRDY# Hold	3		ns		2.5.5	
Ct 426a	BUSY#, PEREQ, ERROR# Setup to NPXCLK phi1 high	19		ns		2.5.5	
Ct 426b	BUSY#, PEREQ, ERROR# Hold from NPXCLK phi1 high	4		ns		2.5.5	
Ct 427a	CD Setup (NPX Cycle)	9		ns		2.5.3	
Ct 427b	CD Hold (NPX Cycle)	5		ns		2.5.3	

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications **25 MHz** (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Math Coprocessor Timings: 25 MHz (Continued)							
Ct 441	NPXCLK Period	20	500	ns		2.5.1	(Note 1)
Ct 442a	NPXCLK High Time 2V	6		ns		2.5.1	(Note 1)
Ct 442b	NPXCLK High Time 3.7V	3		ns		2.5.1	
Ct 443a	NPXCLK Low Time 2V	6		ns		2.5.1	(Note 1)
Ct 443b	NPXCLK Low Time 0.8V	4		ns		2.5.1	
Ct 444	NPXCLK Fall Time (V _{CC} - 0.8V) to 0.8V		7	ns		2.5.1	
Ct 445	NPXCLK Rise Time 0.8V to (V _{CC} - 0.8V)		7	ns		2.5.1	
Ct 446	NPXCLK to NPXRESET inactive delay	3	12	ns	FF, S		
SRAM Mode: 25 MHz Timings							
Ct 501	Access Time from OE#	30		ns			2 Wait State
Ct 502	Access Time from OE#	40		ns			3 Wait State
Ct 503	CE# Setup to OE# Active	30		ns	SF, SF		2 Wait State C _R = 10 pF,
Ct 504	CE# Setup to OE# Active			ns	SF, SF		3 Wait State C _T = 10 pF
Ct 505	Addr Setup to OE# Active			ns	SF, S		2 Wait State C _R = 10 pF,
Ct 506	Addr Setup to OE# Active	30		ns	SF, S		3 Wait State C _T = 40 pF
Ct 507	CE# Setup to WE# Active			ns	SF, SF		2 Wait State C _R = 80 pF,
Ct 508	CE# Setup to WE# Active	0		ns	SF, SF		3 Wait State C _T = 10 pF
Ct 509	Addr Setup to WE# Active	0		ns	SF, S		2 Wait State C _R = 80 pF,
Ct 510	Addr Setup to WE# Active	0		ns	SF, S		3 Wait State C _T = 40 pF
Ct 511	WE# Active Pulse Width	55		ns	S		2 Wait State C _R = 80 pF
Ct 512	WE# Active Pulse Width	70		ns	S		3 Wait State
Ct 513	WE# Recovery Time	5		ns	SR, S		2 Wait State C _R = 80 pF,
Ct 514	WE# Recovery Time	10		ns	SR, S		3 Wait State C _T = 40 pF
Ct 515	Write Data Setup to WE# Inactive	35		ns	SR, S		2 Wait State C _R = 80 pF,
Ct 516	Write Data Setup to WE# Inactive	40		ns	SR, S		3 Wait State C _T = 40 pF
Ct 517	Write Data Hold from WE# Inactive	0		ns	SR, S		2 Wait State C _R = 80 pF,
Ct 518	Write Data Hold from WE# Inactive	0		ns	SR, S		3 Wait State C _T = 40 pF

NOTE:

1. NPXCLK maximum period is specified only for the case where a MCP (Math Co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.

SEE INTEL FOR DESIGN-IN INFORMATION

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
SRAM Mode: 25 MHz Timings (Continued)							
Ct 519	DIR Setup to OE# Active	0		ns	SF, S	*	2 Wait State $C_R = 10 \text{ pF}$
Ct 520	DIR Setup to OE# Active	0		ns	SF, S		3 Wait State $C_T = 10 \text{ pF}$
Ct 523	OE# Inactive Setup to DEN# Active	25		ns	SF, SR	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 524	OE# Inactive Setup to DEN# Active	30		ns	SF, S		3 Wait State $C_T = 10 \text{ pF}$
Ct 525	DIR Inactive Setup to WE# Active	0		ns	SF, S	2.5.30	2 Wait State $C_R = 80 \text{ pF}$
Ct 526	DIR Inactive Setup to WE# Active	0		ns	SF, S		3 Wait State $C_T = 10 \text{ pF}$
Ct 527	DEN# Hold from WE# Inactive	0		ns	SR, SF	2.5.30	2 Wait State $C_R = 80 \text{ pF}$
Ct 528	DEN# Hold from WE# Inactive	0		ns	SF		3 Wait State $C_T = 20 \text{ pF}$
Ct 529	DIR Inactive Setup to DEN# Active	0		ns	SF, S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 530	DIR Inactive Setup to DEN# Active	0		ns	SF		3 Wait State $C_T = 10 \text{ pF}$
Ct 531	DIR Hold from DEN# Inactive	0		ns	SF, S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 532	DIR Hold from DEN# Inactive	0		ns	SR, S		3 Wait State $C_T = 10 \text{ pF}$
Ct 533	DIR Setup to DEN# Active	0	50	ns	SF, S; SF, S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 534	DIR Setup to DEN# Active	0	50	ns	SF, S; SF, S		3 Wait State $C_T = 10 \text{ pF}$
Ct 535	Upper Addr Setup to LE Inactive	8		ns	SF, S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 536	Upper Addr Setup to LE Inactive	8		ns	SF, S		3 Wait State $C_T = 40 \text{ pF}$
Ct 537	Upper Addr Hold from LE Inactive	4		ns	SF, S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 538	Upper Addr Hold from LE Inactive	4		ns	SF, S		3 Wait State $C_T = 40 \text{ pF}$
Ct 539	LE Active Pulse Width	8		ns	S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 540	LE Active Pulse Width	8		ns	S		3 Wait State $C_T = 20 \text{ pF}$
Ct 541	Addr Valid Delay from LE Inactive		40	ns	SF, S	2.5.30	2 Wait State $C_R = 20 \text{ pF}$
Ct 542	Addr Valid Delay from LE Inactive		60	ns	SF, S		3 Wait State $C_T = 40 \text{ pF}$
Ct 543	Read Data Hold from OE# Inactive	0		ns		2.5.30	2 Wait State
Ct 544	Read Data Hold from OE# Inactive	0		ns			3 Wait State

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating Figure	Notes
DRAM Mode: 25 MHz Timings							
Ct 601	tASR	Row Addr Setup to RAS# Active	0		ns	SF, S	F1 Mode
Ct 602		Row Addr Setup to RAS# Active	7		ns		F2 Mode
Ct 603		Row Addr Setup to RAS# Active	7		ns		P1 Mode
Ct 605	tRAH	Row Addr Hold from RAS# Active	15		ns	SF, S	F1 Mode
Ct 606		Row Addr Hold from RAS# Active	15		ns		F2 Mode
Ct 607		Row Addr Hold from RAS# Active	15		ns		P1 Mode
Ct 609	tASC	Col Addr Setup to CAS# Active	0		ns	* SF, S	F1 Mode
Ct 610		Col Addr Setup to CAS# Active	0		ns		F2 Mode
Ct 611		Col Addr Setup to CAS# Active	0		ns		P1 Mode
Ct 613	tCAH	Col Addr Hold from CAS# Active	15		ns	SF, S	F1 Mode
Ct 614		Col Addr Hold from CAS# Active	15		ns		F2 Mode
Ct 615		Col Addr Hold from CAS# Active	20		ns		P1 Mode
Ct 617	tRCD	RAS# to CAS# Delay			ns	SF, SF	F1 Mode
Ct 618		RAS# to CAS# Delay	20		ns		F2 Mode
Ct 619		RAS# to CAS# Delay	20		ns		P1 Mode
Ct 621	tCSH	CAS# Hold Time from RAS# Active	0		ns	SF, SR	F1 Mode
Ct 622		CAS# Hold Time from RAS# Active	0		ns		F2 Mode
Ct 623		CAS# Hold Time from RAS# Active	0		ns		P1 Mode
Ct 625	tRSH	RAS# Hold Time from RAS# Active			ns	SF, SR	F1 Mode
Ct 626		RAS# Hold Time from RAS# Active	30		ns		F2 Mode
Ct 627		RAS# Hold Time from RAS# Active	45		ns		P1 Mode
Ct 629	tWCS	WE# Setup to CAS# Active (Write)	0		ns	SF, SF	F1 Mode
Ct 630		WE# Setup to CAS# Active (Write)	0		ns		F2 Mode
Ct 631		WE# Setup to CAS# Active (Write)	0		ns		P1 Mode
Ct 633	tWCH	WE# Hold from CAS# Active (Write)	20		ns	SF, SR	F1 Mode
Ct 634		WE# Hold from CAS# Active (Write)	20		ns		F2 Mode
Ct 635		WE# Hold from CAS# Active (Write)	20		ns		P1 Mode
Ct 637	tRCS	WE# Inactive Setup to CAS# Active (Read)	0		ns	SF, SR	F1 Mode
Ct 638		WE# Inactive Setup to CAS# Active (Read)	0		ns		F2 Mode
Ct 639		WE# Inactive Setup to CAS# Active (Read)	0		ns		P1 Mode
Ct 641	tRCH	WE# Inactive Hold from CAS# Inactive (Read)	0		ns	SF, SF	F1 Mode
Ct 642		WE# Inactive Hold from CAS# Inactive (Read)	0		ns		F2 Mode
Ct 643		WE# Inactive Hold from CAS# Inactive (Read)	0		ns		P1 Mode

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2.4 Timing Specifications (Continued)

Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
DRAM Mode: 25 MHz Timings (Continued)								
Ct 645	tWDS	Write Data Setup to CAS# Active	0		ns	SF, S	2.5.29	F1 Mode
Ct 646		Write Data Setup to CAS# Active	0		ns			F2 Mode
Ct 647		Write Data Setup to CAS# Active	0		ns			P1 Mode
Ct 649	tWDH	Write Data Hold from CAS# Active	15		ns	SF, S	2.5.29	F1 Mode
Ct 650		Write Data Hold from CAS# Active	15		ns			F2 Mode
Ct 651		Write Data Hold from CAS# Active	20		ns			P1 Mode
Ct 653	tRAC	Access Time from RAS# Active	60		ns	*	2.5.29	F1 Mode
Ct 654		Access Time from RAS# Active	80		ns			F2 Mode
Ct 655		Access Time from RAS# Active	80		ns			P1 Mode
Ct 657	tCAC	Access Time from CAS# Active	23		ns		2.5.29	F1 Mode
Ct 658		Access Time from CAS# Active	23		ns			F2 Mode
Ct 659		Access Time from CAS# Active	40		ns			P1 Mode
Ct 661	tRDH	Read Data Hold from CAS# Inactive	0		ns		2.5.29	F1 Mode
Ct 662		Read Data Hold from CAS# Inactive	0		ns			F2 Mode
Ct 663		Read Data Hold from CAS# Inactive	0		ns			P1 Mode
Ct 665	tRAS	RAS# Active Pulse Width	60		ns		2.5.29	F1 Mode
Ct 666		RAS# Active Pulse Width	8		ns			F2 Mode
Ct 667		RAS# Active Pulse Width	8		ns			P1 Mode
Ct 669	tCAS	CAS# Active Pulse Width	25		ns		2.5.29	F1 Mode
Ct 670		CAS# Active Pulse Width	15		ns			F2 Mode
Ct 671		CAS# Active Pulse Width	10		ns			P1 Mode
Ct 673	tRP	RAS# Precharge Pulse Width	50		ns		2.5.29	F1 Mode
Ct 674		RAS# Precharge Pulse Width	70		ns			F2 Mode
Ct 675		RAS# Precharge Pulse Width	70		ns			P1 Mode
Ct 677	tCP	CAS# Precharge Pulse Width	15		ns		2.5.29	F1 Mode
Ct 678		CAS# Precharge Pulse Width	15		ns			F2 Mode
Ct 679		CAS# Precharge Pulse Width	25		ns			P1 Mode
Ct 681	tPSW	PARx Setup to CAS# Active (Write)	0		ns	SF, SF	2.5.29	F1 Mode
Ct 682		PARx Setup to CAS# Active (Write)	0		ns			F2 Mode
Ct 683		PARx Setup to CAS# Active (Write)	0		ns			P1 Mode
Ct 685	tPHW	PARx Hold from CAS# Active (Write)	20		ns	SF, SR	2.5.29	F1 Mode
Ct 686		PARx Hold from CAS# Active (Write)	20		ns			F2 Mode
Ct 687		PARx Hold from CAS# Active (Write)	20		ns			P1 Mode

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2.4 Timing Specifications (Continued)

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Table 2.4-1. Intel386™ SL CPU (Standard 5V) A.C. Specifications 25 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
DRAM Mode: 25 MHz Timings (Continued) *								
Ct 689	tPVR	PARx Valid from CAS# Active (Read)	23		ns		2.5.29	F1 Mode
Ct 690		PARx Valid from CAS# Active (Read)	23		ns	SF, S		F2 Mode
Ct 691		PARx Valid from CAS# Active (Read)	40					P1 Mode
Ct 693	tPHR	PARx Hold from CAS# Inactive (Read)	0				2.5.29	F1 Mode
Ct 694		PARx Hold from CAS# Inactive (Read)	0		ns	S, S		F2 Mode
Ct 695		PARx Hold from CAS# Inactive (Read)	0					P1 Mode
Other DRAM Timings								
Ct 701	tPED	PERR# Delay from SYSCLK		38	ns	SR, SF	2.5.34	C _R = Max C _T = Max
Ct 702	tCSR	CAS# Setup to RAS# Active (DRAM Refresh)		0	ns	SF, SF	2.5.31	C _R = Max, C _T = Max
Ct 703	tCHR	CAS# Hold from RAS# Active (DRAM Refresh)	30		ns	FF, FR	2.5.31	C _R = Min, C _T = Min
Ct 704	tWSR	WE# Inactive Setup to RAS# Active (DRAM Refresh)		0	ns	SF, SF	2.5.31	C _R = Min, C _T = Max
Ct 705	tWHR	WE# Inactive Hold from RAS# Active (DRAM Refresh)	-15		ns	FF, FR	2.5.31	C _R = Min, C _T = Min
Ct 706	tRDS	RAS# Active Setup from SYSCLK (DRAM DMA/Master)		55	ns	SF	2.5.33	
Ct 707	tADS	Address Valid Delay from SYSCLK (DRAM DMA/Master)		65	ns	S	2.5.32	

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2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams

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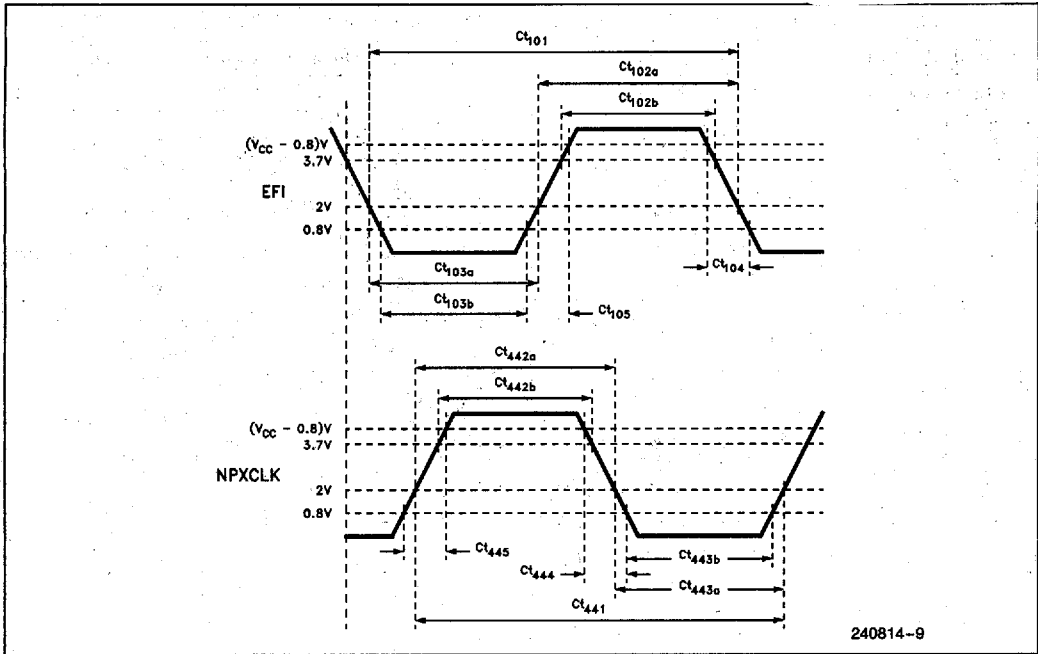


Figure 2.5.1 Clocks

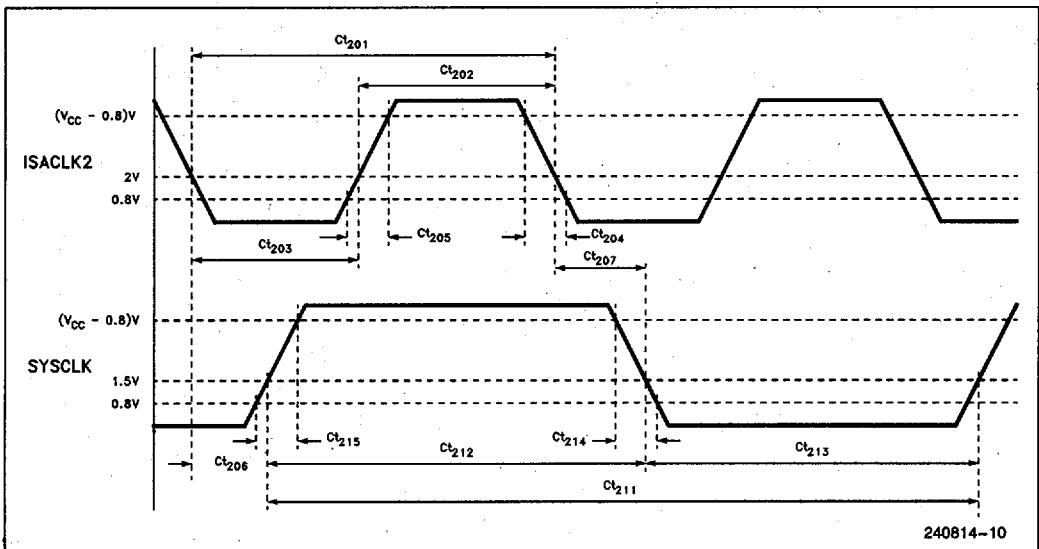


Figure 2.5.2. Clocks

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

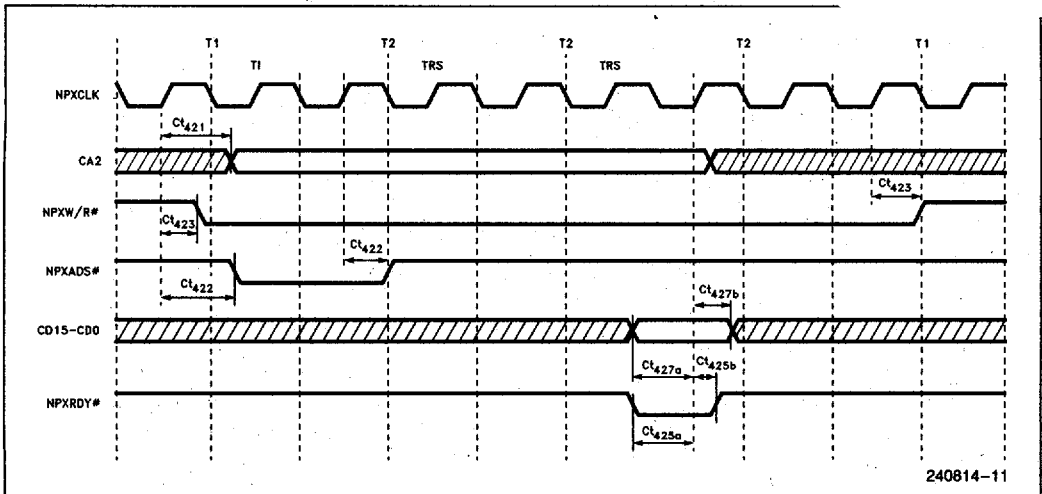


Figure 2.5.3. Intel386™ SL CPU Read from MCP

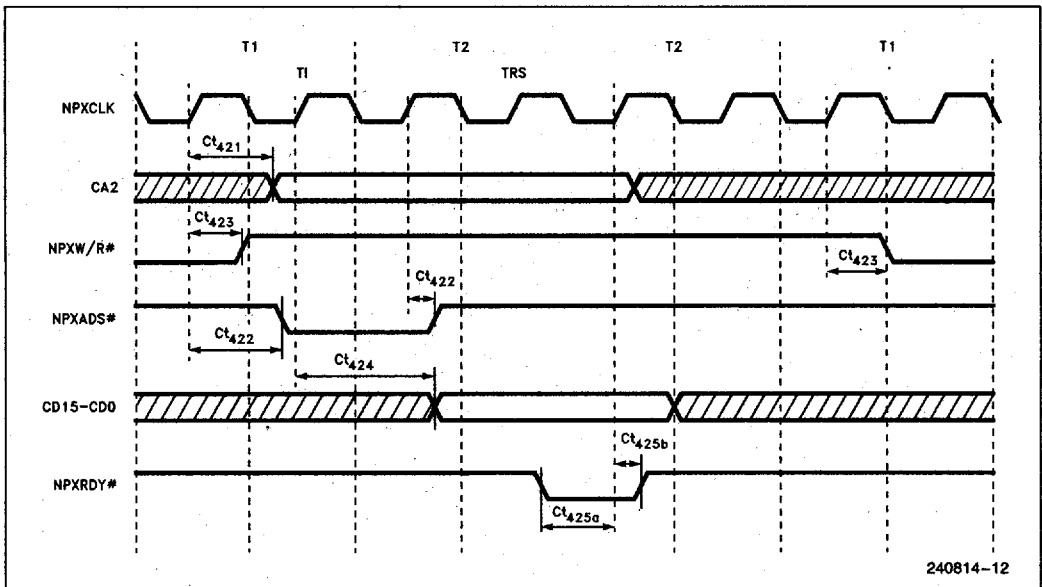


Figure 2.5.4. Intel386™ SL CPU Write to MCP

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2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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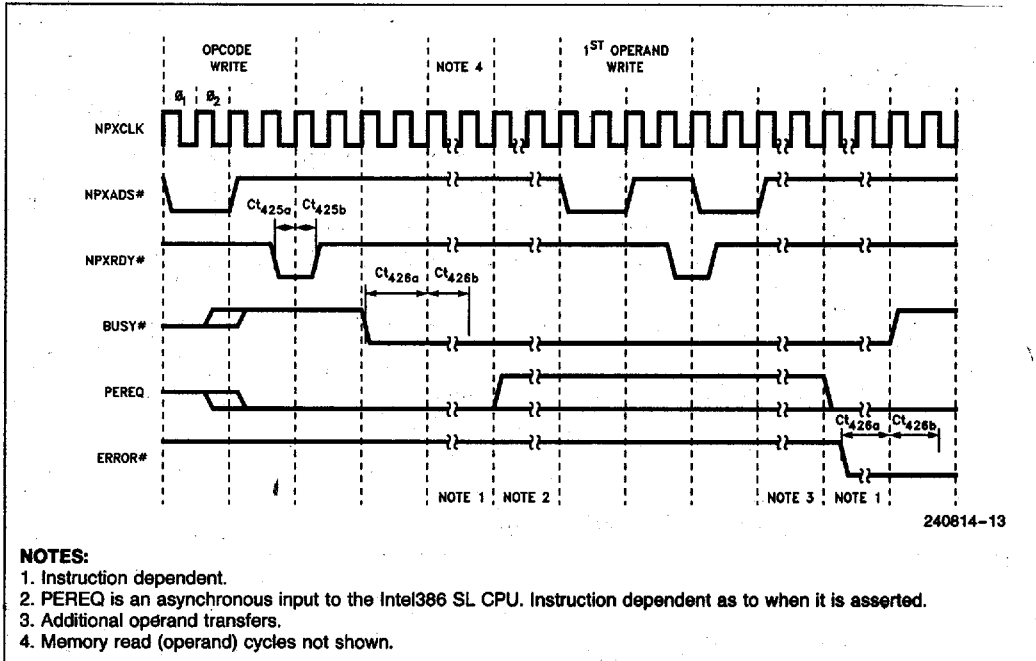


Figure 2.5.5. MCP BUSY#, PEREQ and ERROR# Timings

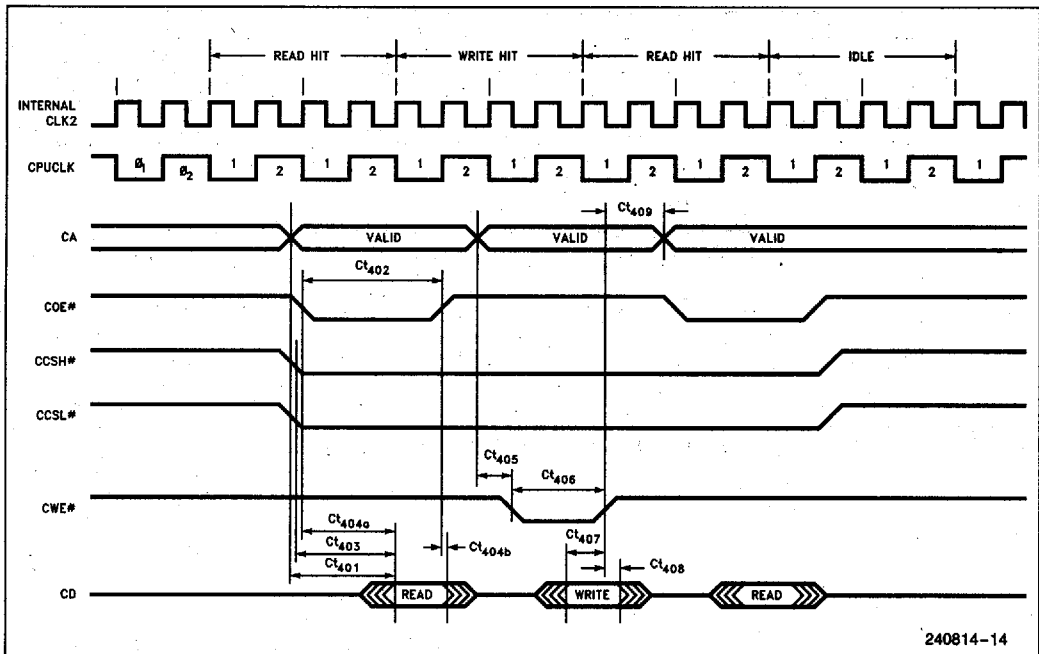


Figure 2.5.6. Cache Read/Write Hit Cycles

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

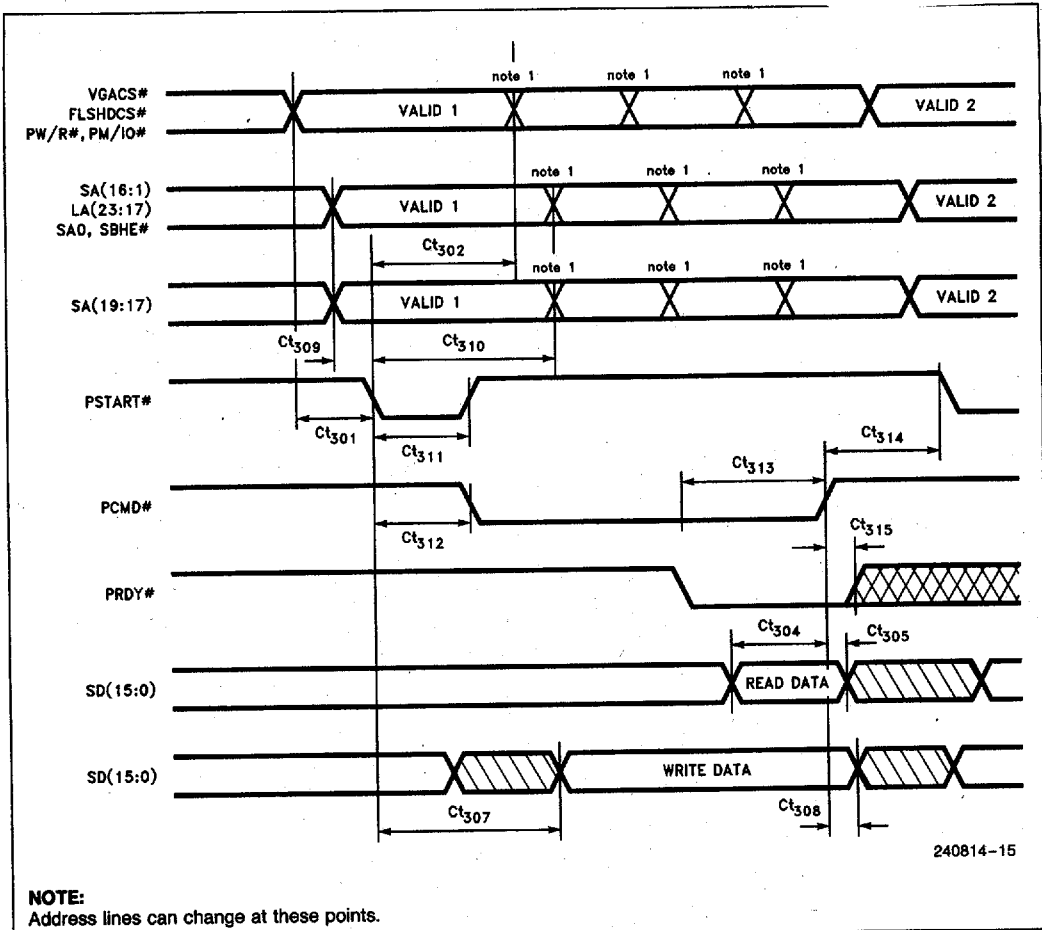


Figure 2.5.7. PI-Bus Timings

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

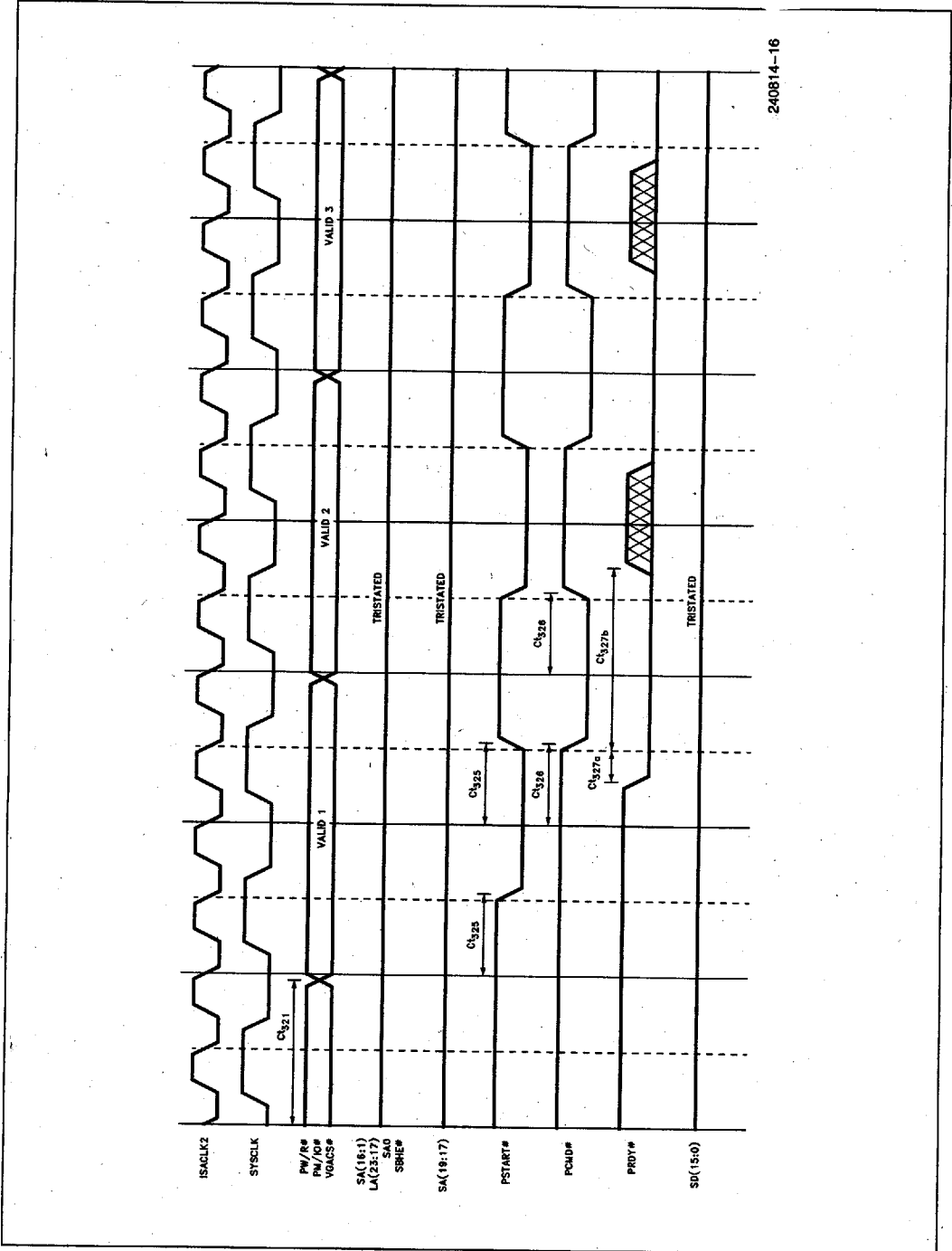


Figure 2.5.8. PI-Bus Slave Controller Generated Timings

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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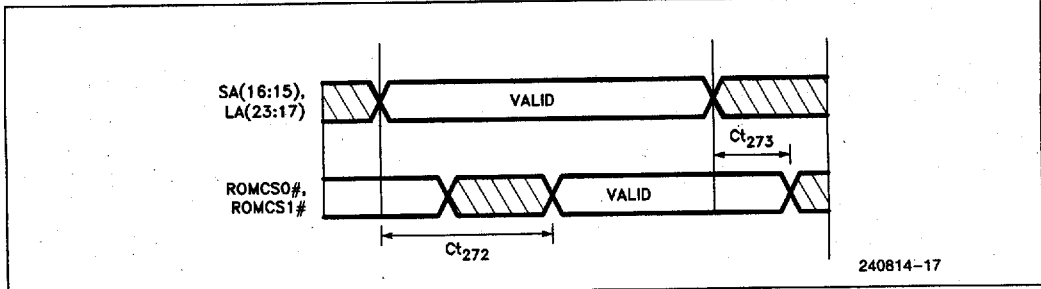


Figure 2.5.9. ISA Bus Slave Controller Generated Timings (ROMCS0#/CS1# with respect to Address)

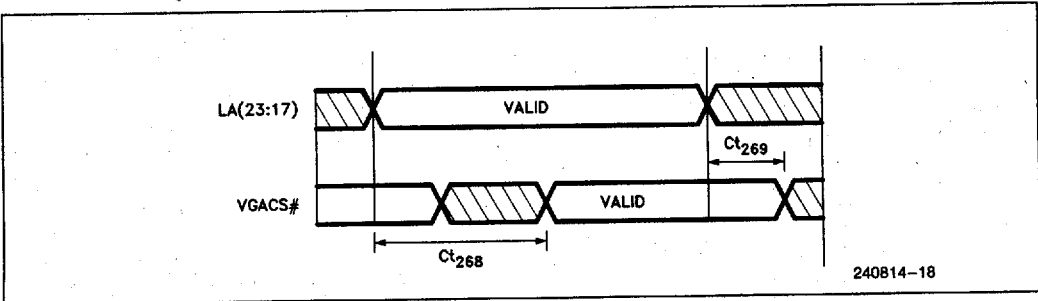


Figure 2.5.10. ISA Bus Master Controller Generated Timings (VGACS# with respect to Address)

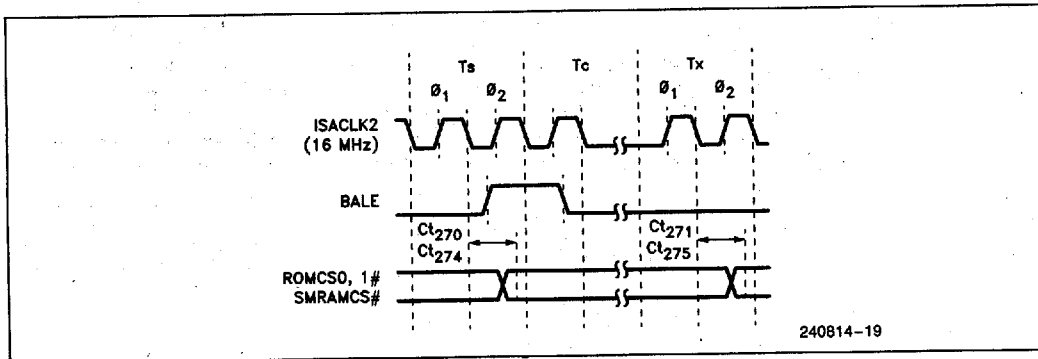


Figure 2.5.11. ROMCS0, ROMCS1, SMRAMCS# Propagation Delays

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2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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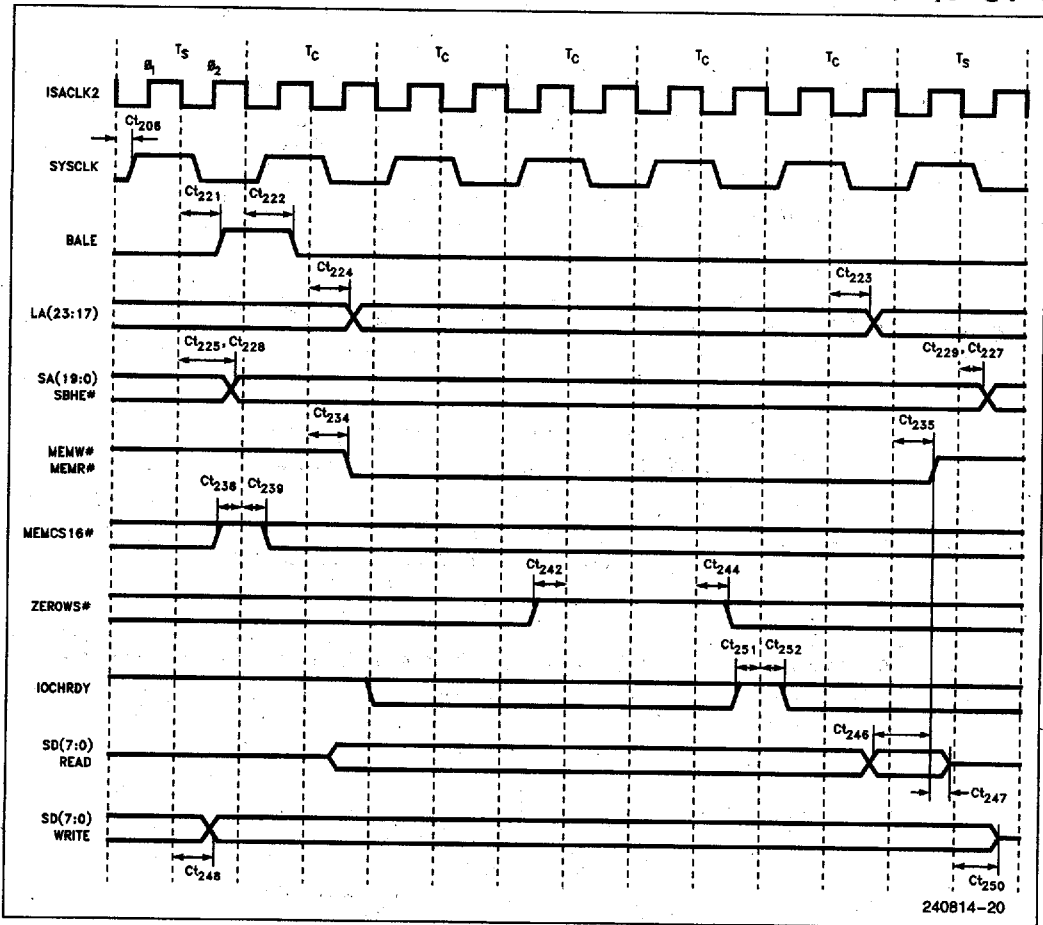


Figure 2.5.12. ISA Bus 8-Bit Memory Read/Write Standard ISA BUS Cycle (6 SYCLKs)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

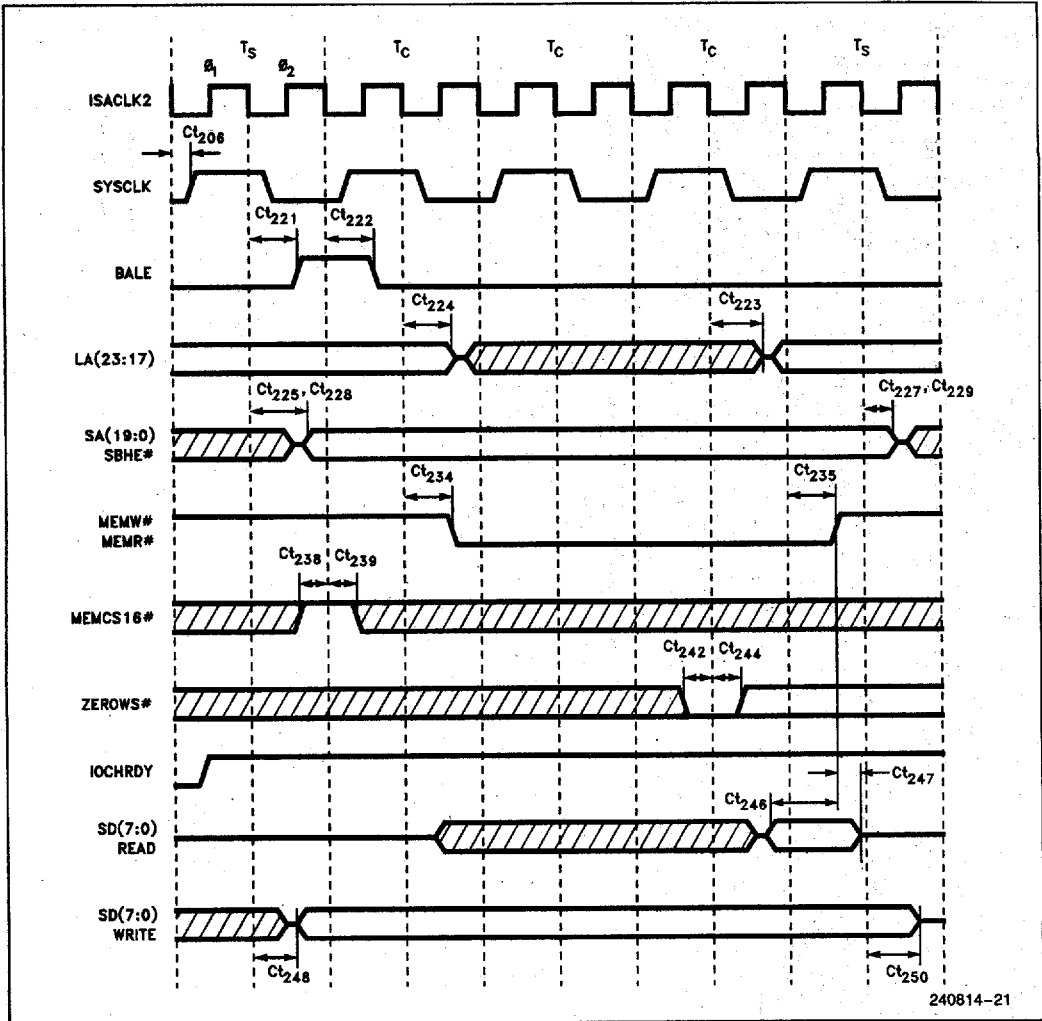


Figure 2.5.13. ISA Bus 8-Bit Memory Read/Write with ZEROWS# Asserted (4 SYSCLKs)

56E D ■ 4826175 0119129 T6T ■ ITL1

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

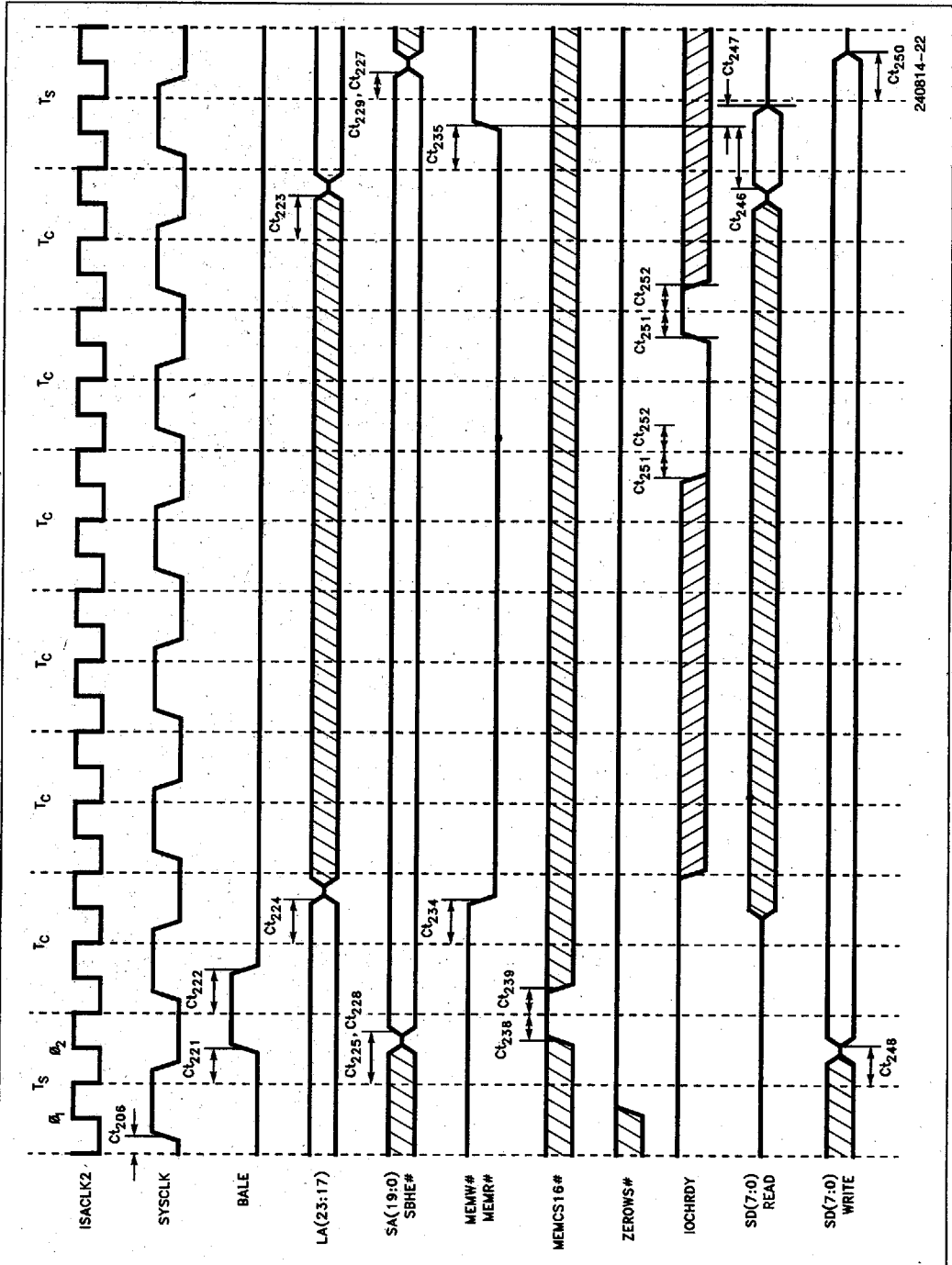


Figure 2.5.14. ISA Bus 8-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

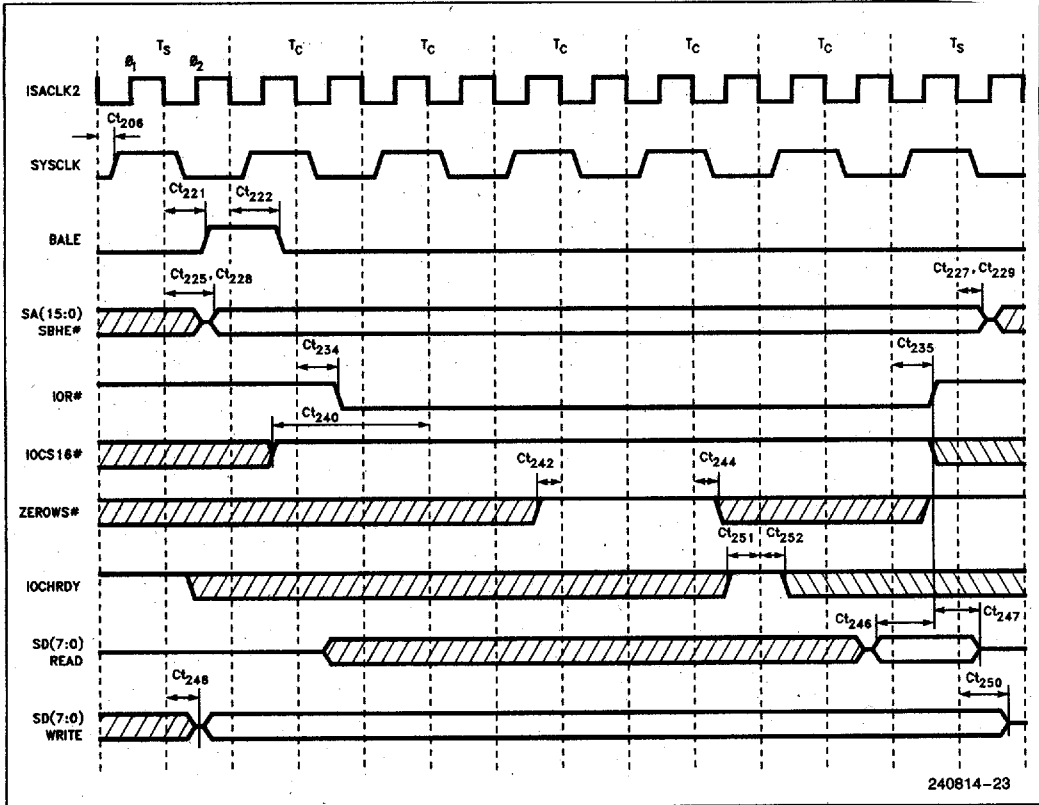


Figure 2.5.15. ISA Bus 8-Bit I/O Read/Write Standard ISA BUS Cycle (6 SYSCLKs)

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56E D ■ 4826175 0119131 618 ■ ITL1

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

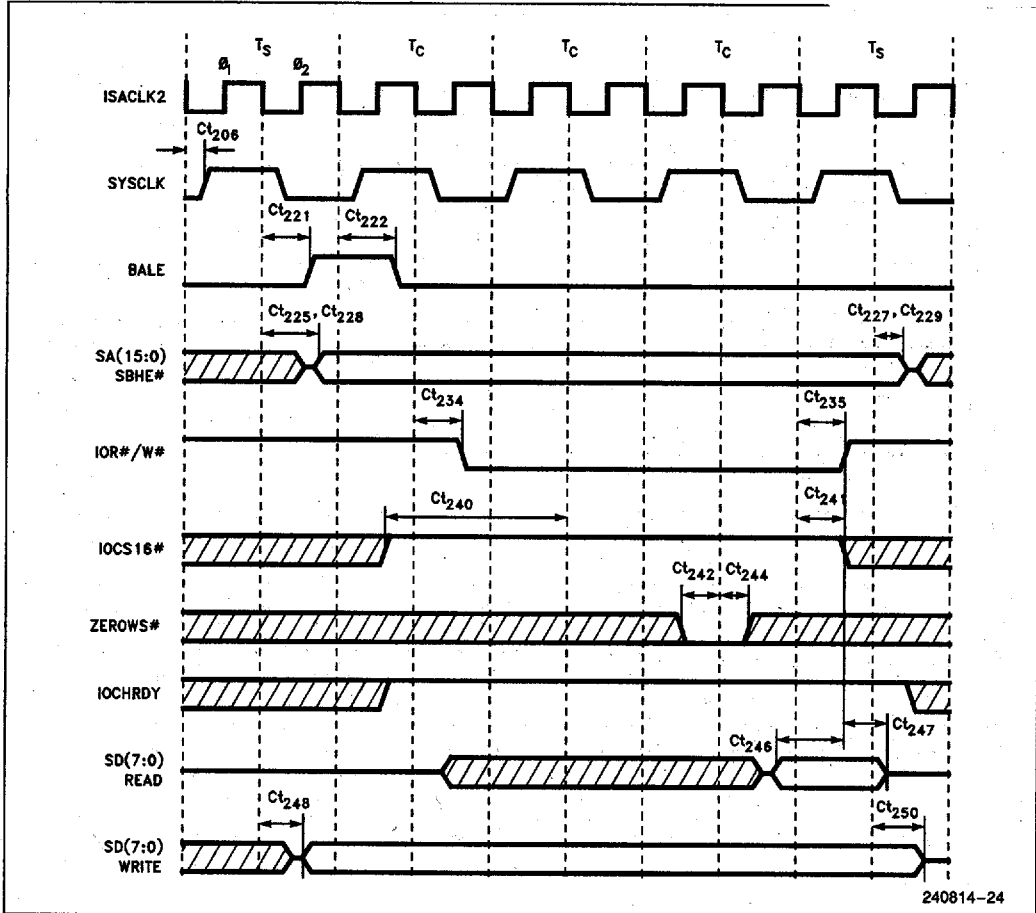


Figure 2.5.16. ISA Bus 8-Bit I/O Read/Write with ZEROWS# Asserted (4 SYSCLKs)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

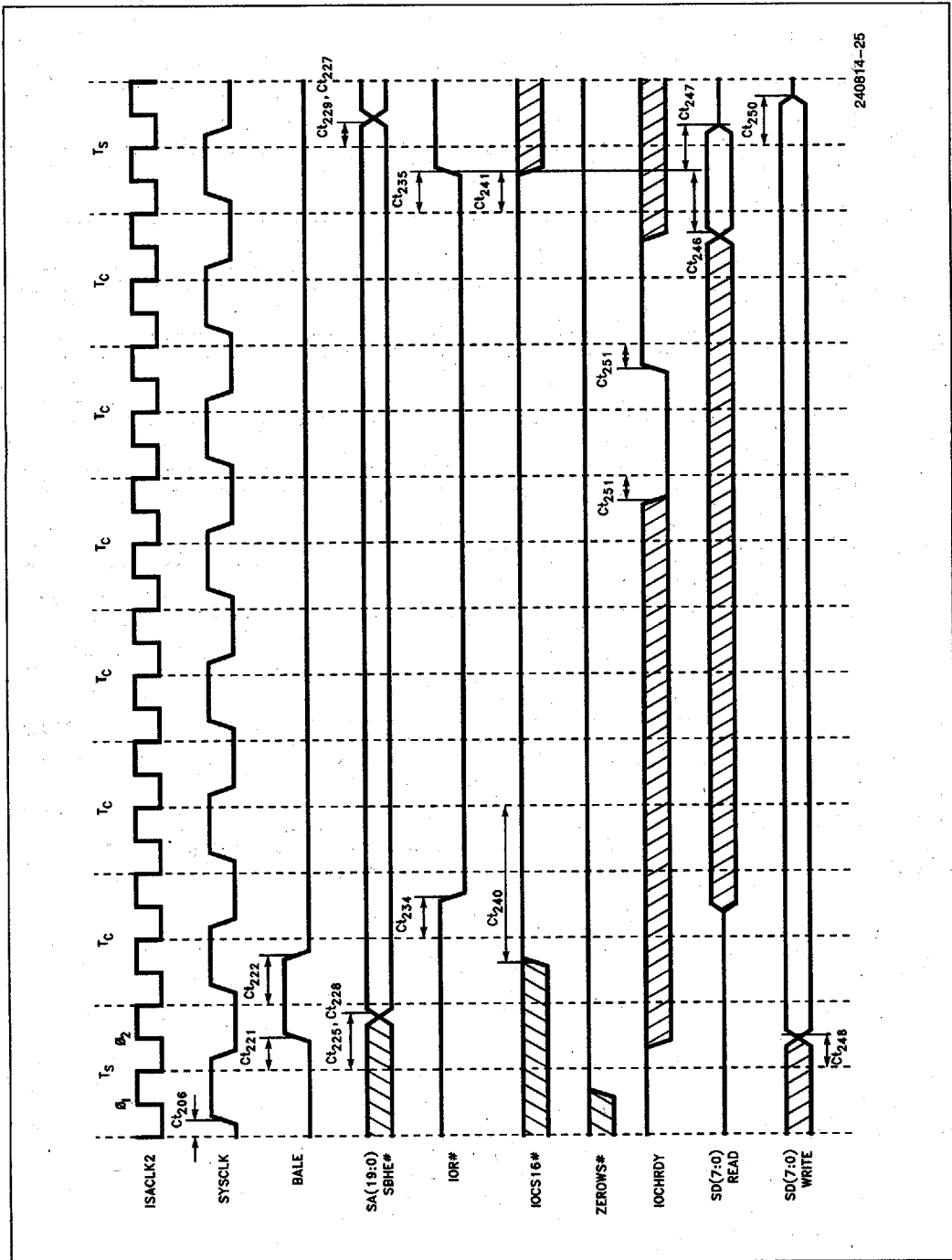
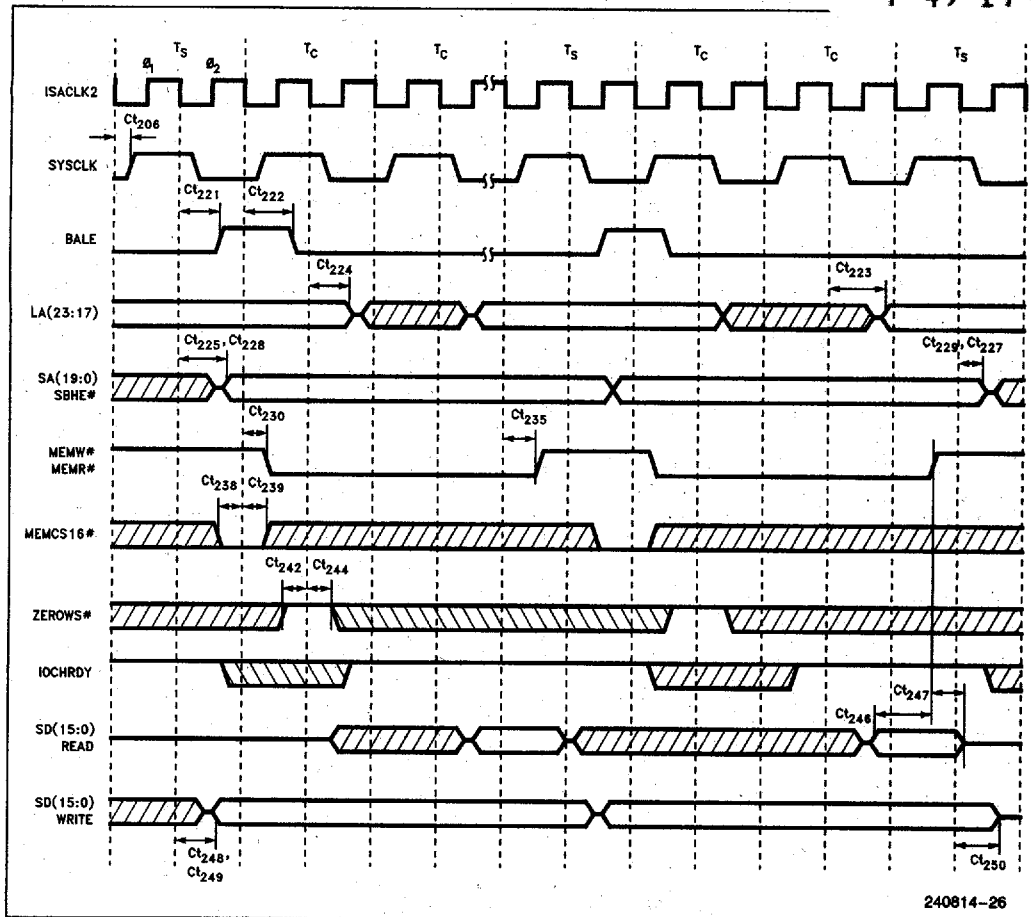


Figure 2.5.17. ISA Bus 8-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

56E D ■ 4826175 0119133 490 ■ ITL1

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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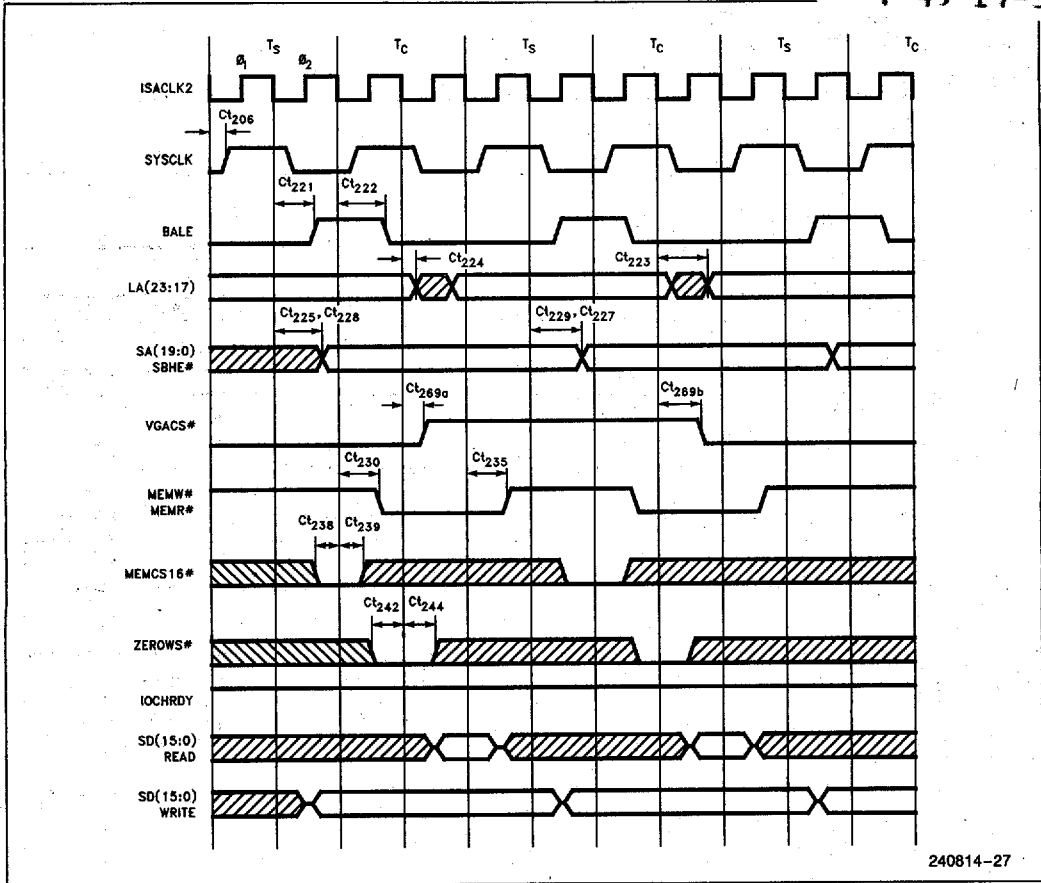


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Figure 2.5.18. ISA Bus 16-Bit Memory Read/Write Standard ISA BUS Cycle (3 SYSCLKs)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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Figure 2.5.19. ISA Bus 16-Bit Memory Read/Write with ZEROWS# Asserted (2 SYSCLKs)

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56E D ■ 4826175 0119135 263 ■ ITL1

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

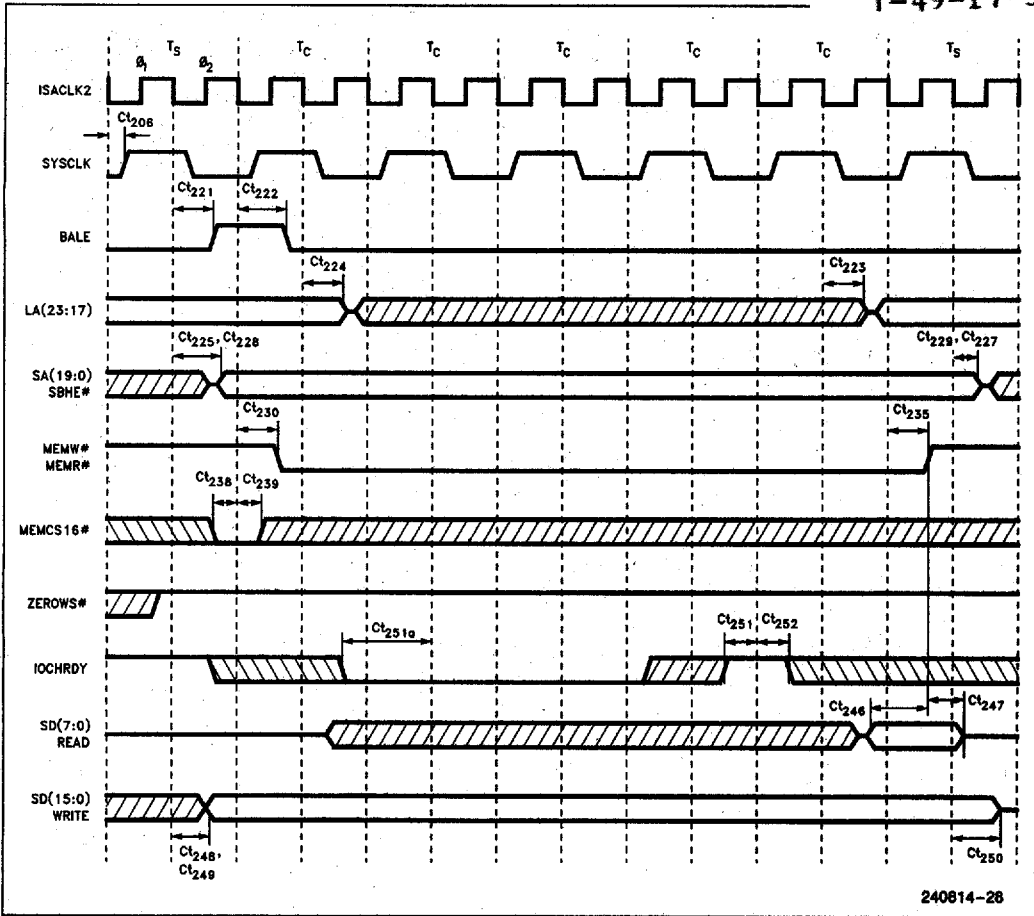


Figure 2.5.20. ISA Bus 16-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

56E D ■ 4826175 0119136 1TT ■ ITL1

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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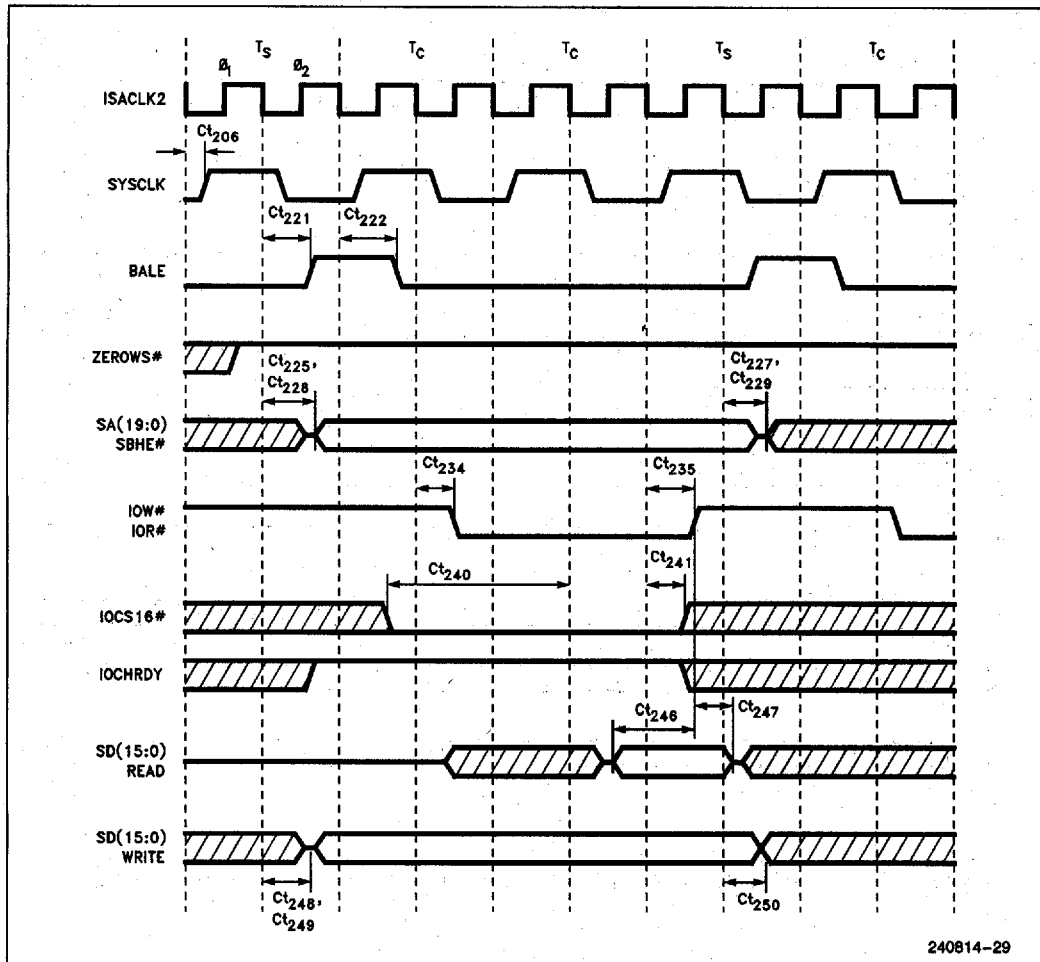


Figure 2.5.21. ISA Bus 16-Bit I/O Read/Write Standard ISA BUS Cycle (3 SYSCLKs)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

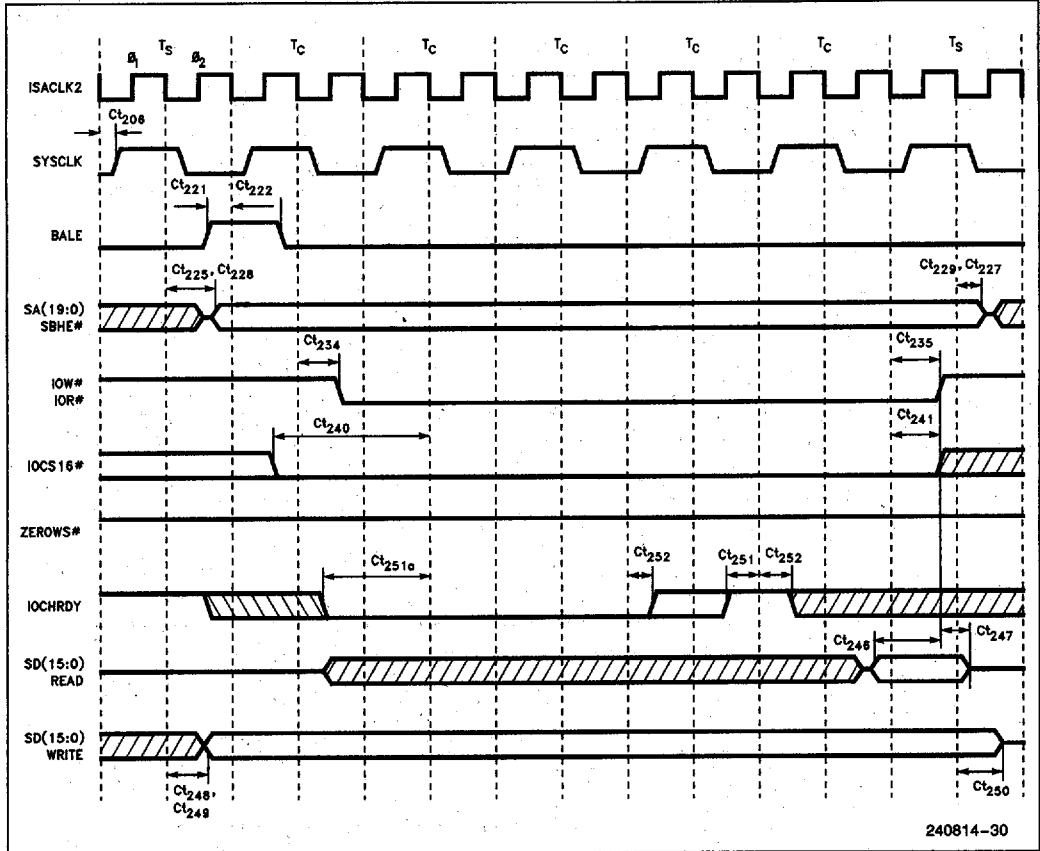


Figure 2.5.22. ISA Bus 16-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

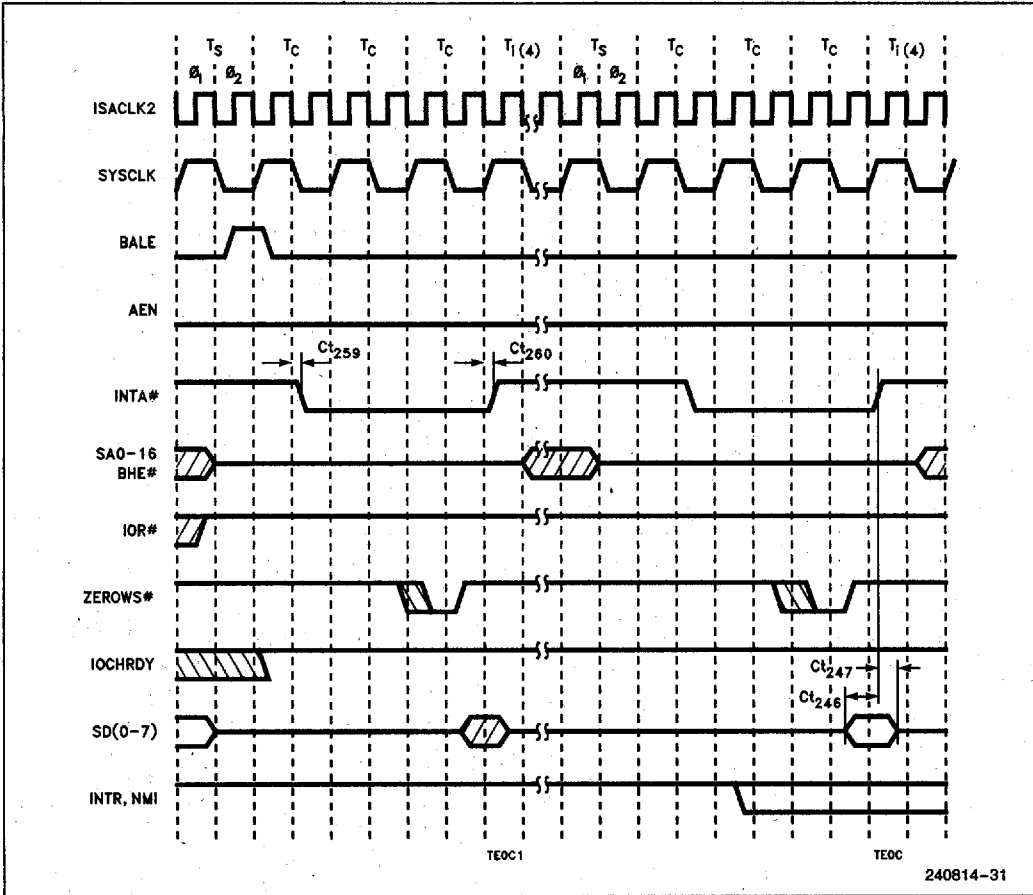
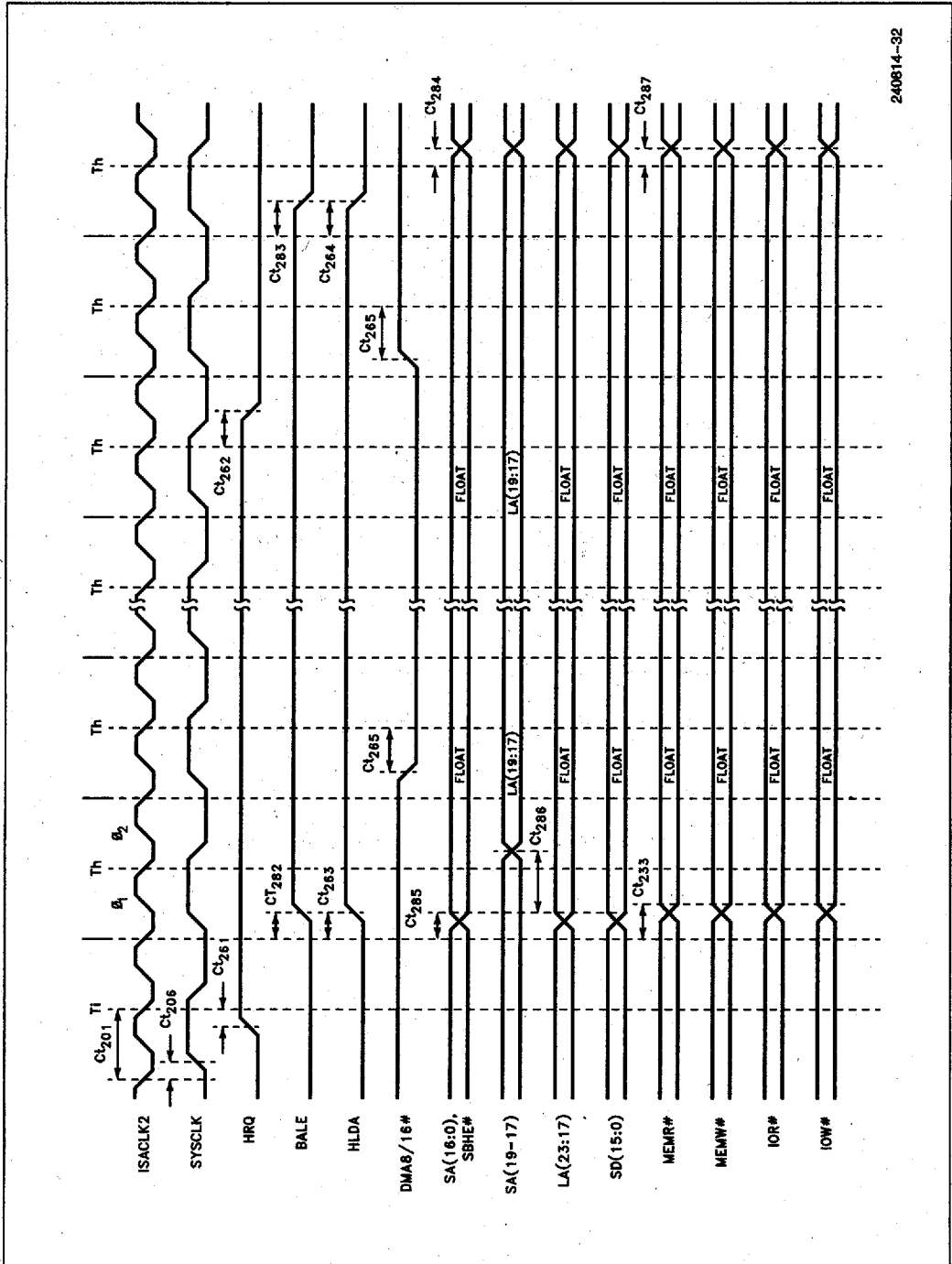


Figure 2.5.23. ISA Bus Interrupt Acknowledge Bus Cycle

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2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)



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Figure 2.5.24. ISA Bus Controller DMA Cycle

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

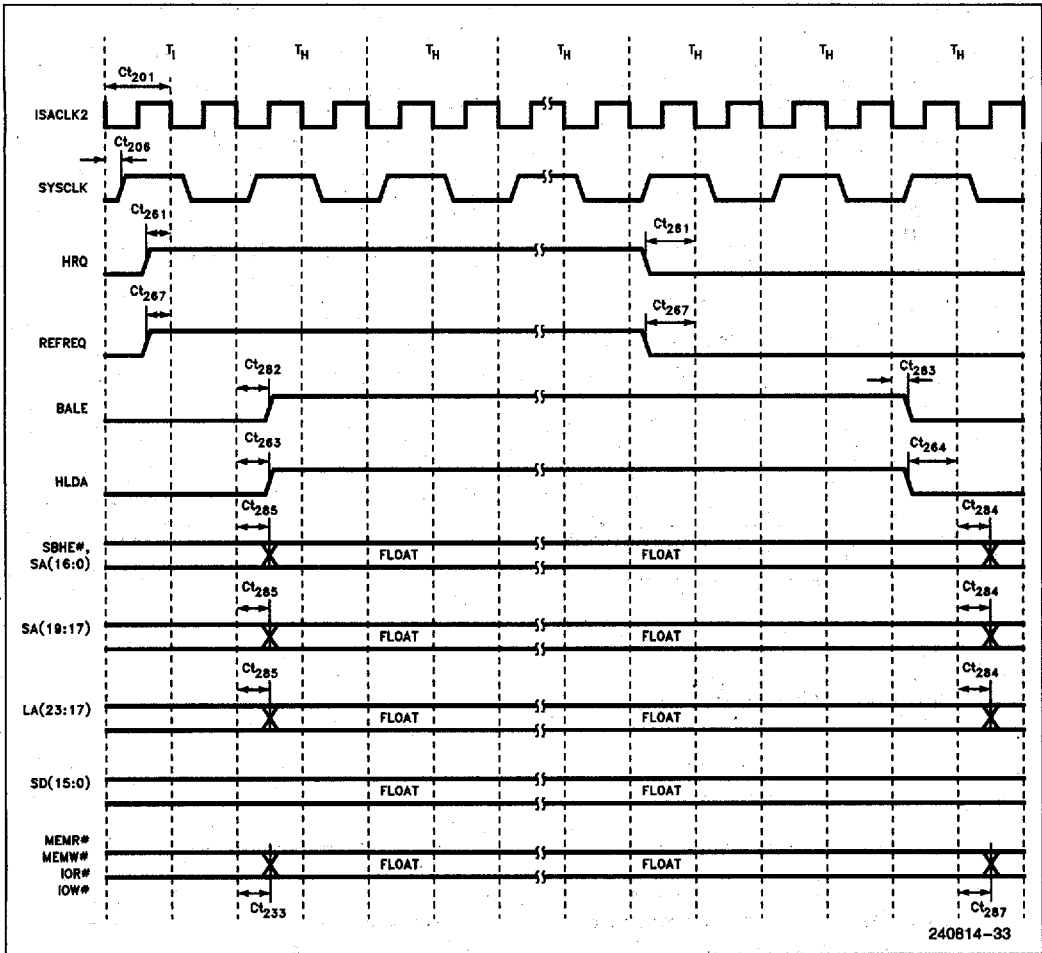


Figure 2.5.25. ISA Bus Controller Refresh Cycle

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2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

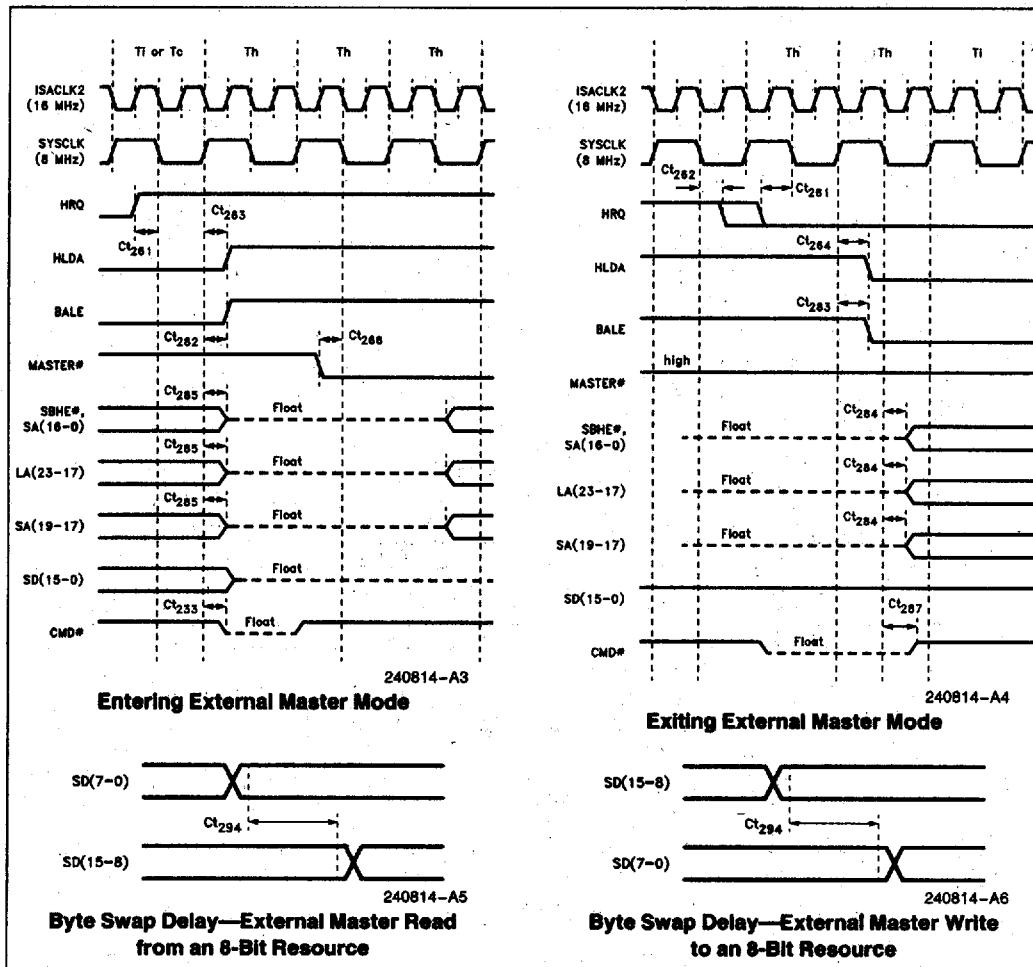


Figure 2.5.26. ISA Bus External Bus Master

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

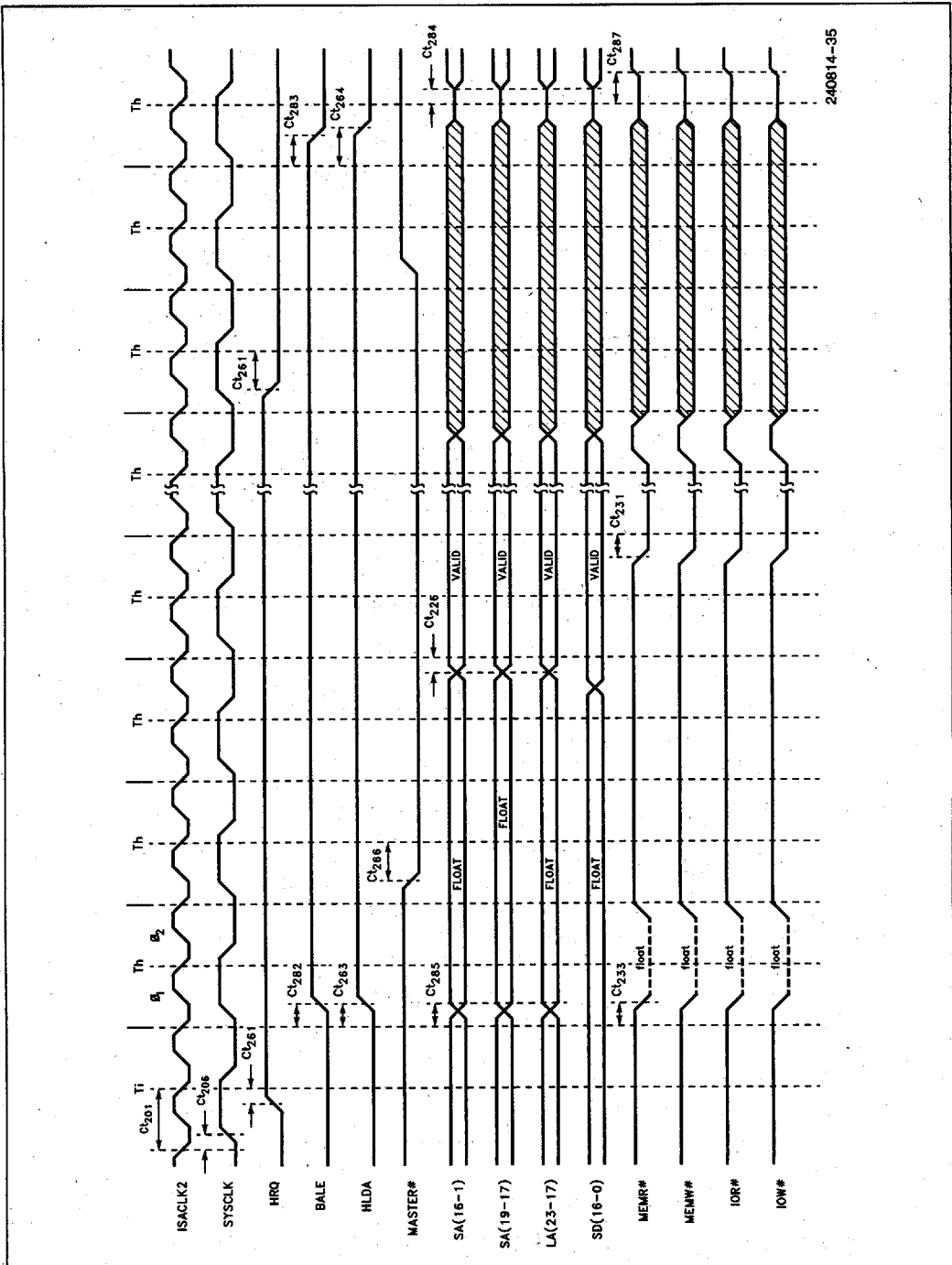
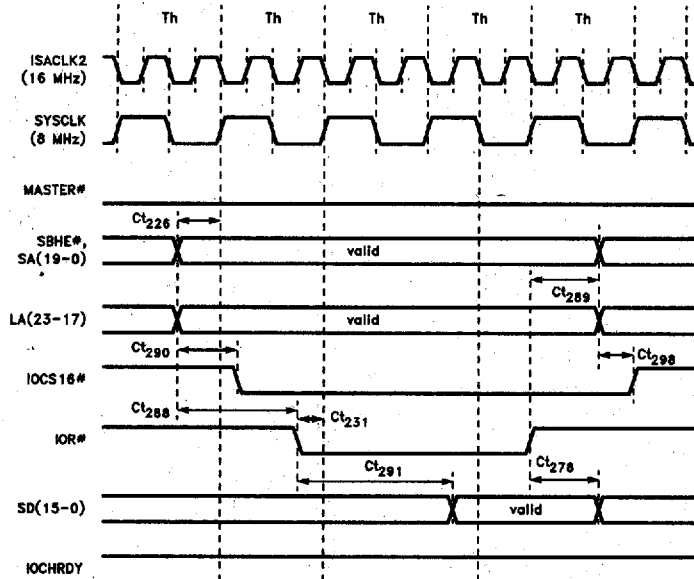


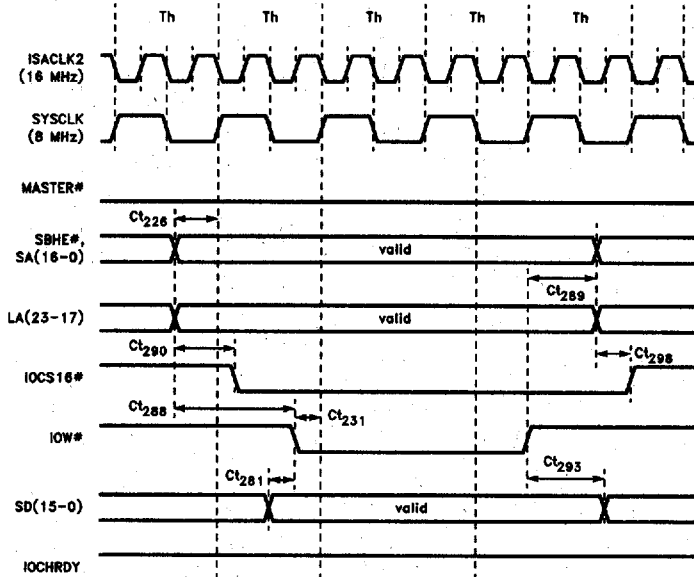
Figure 2.5.27. ISA Bus External Bus Master to Off-Board I/O Ports (No Byte-Swapping)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

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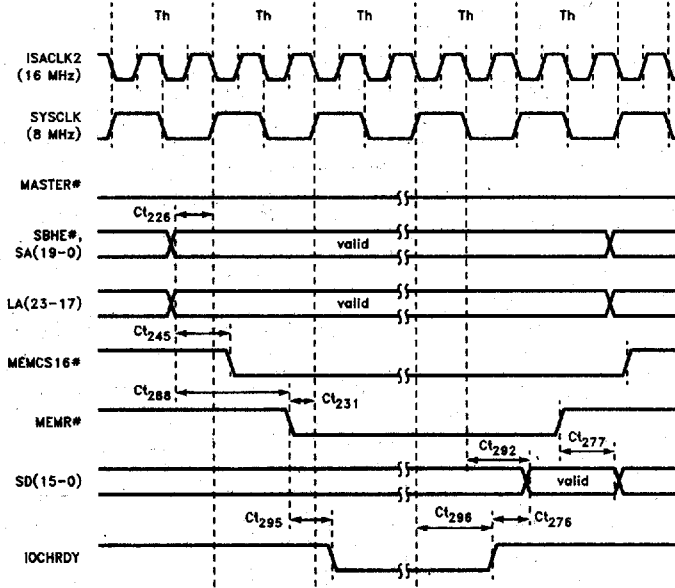
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Figure 2.5.28a. ISA Bus External Bus Master to On-Board I/O Ports (Read/Write)

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

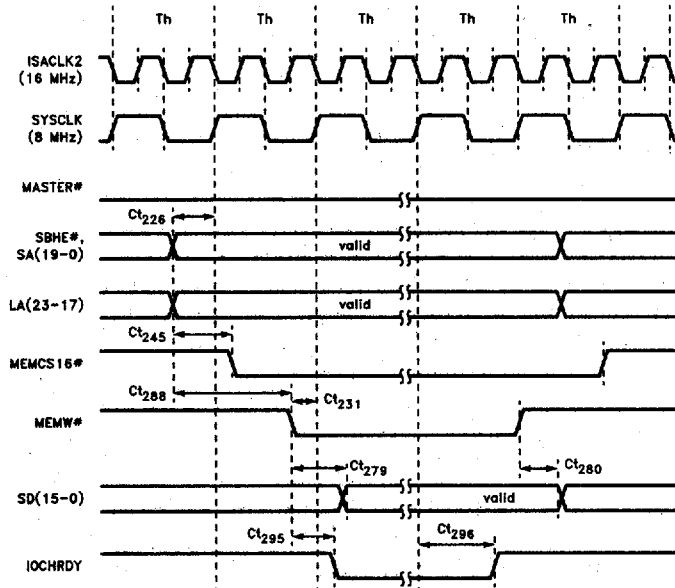
T-49-17-34

2



240814-34

External Master Read from On-Board Memory



240814-A7

External Master Write to On-Board Memory

Figure 2.5.28b. ISA Bus External Bus Master Accesses to On-Board Memory

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2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

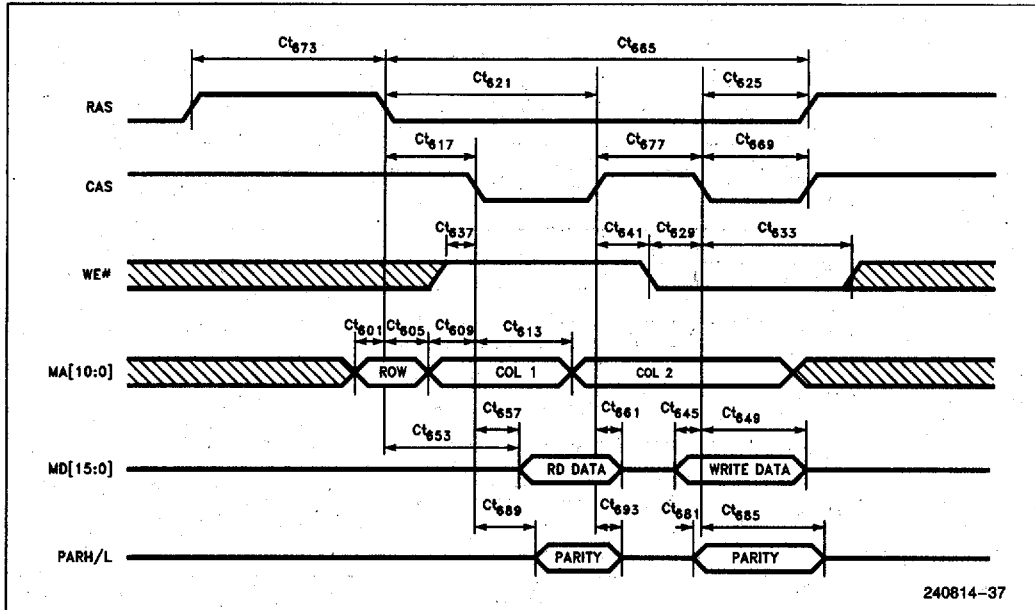
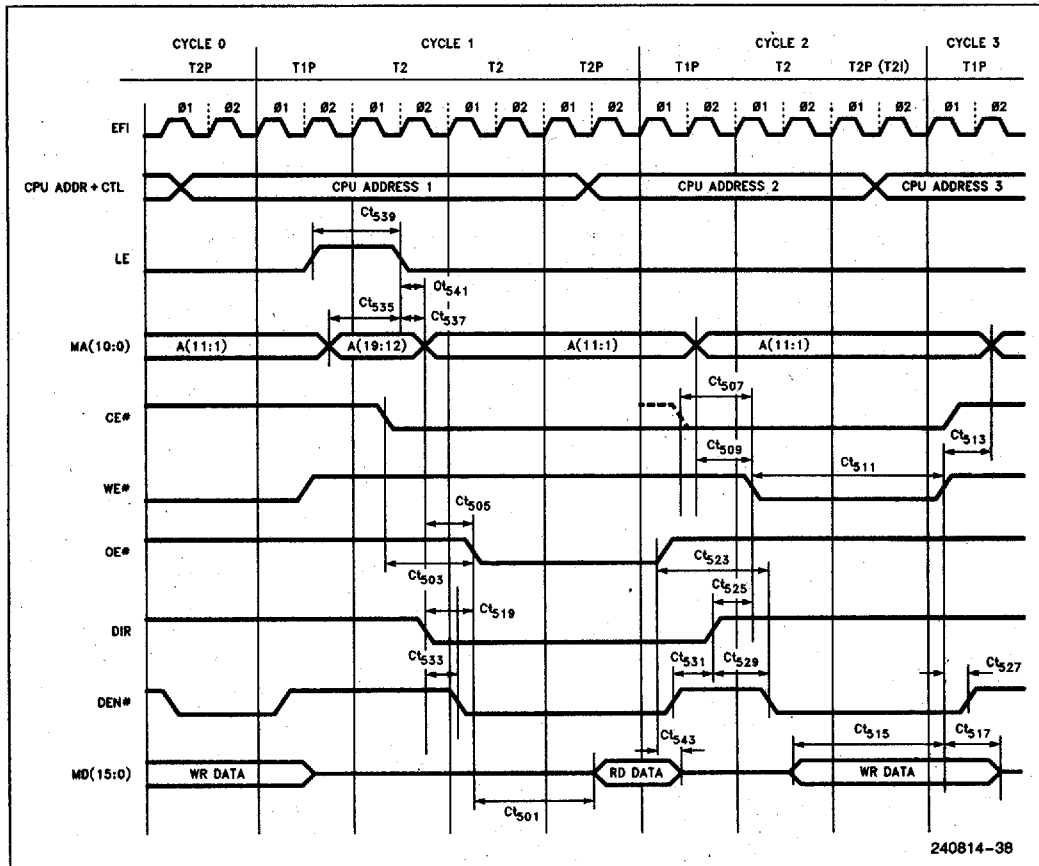


Figure 2.5.29. Intel386™ SL CPU Memory Controller Timings
(DRAM Timing Parameters)

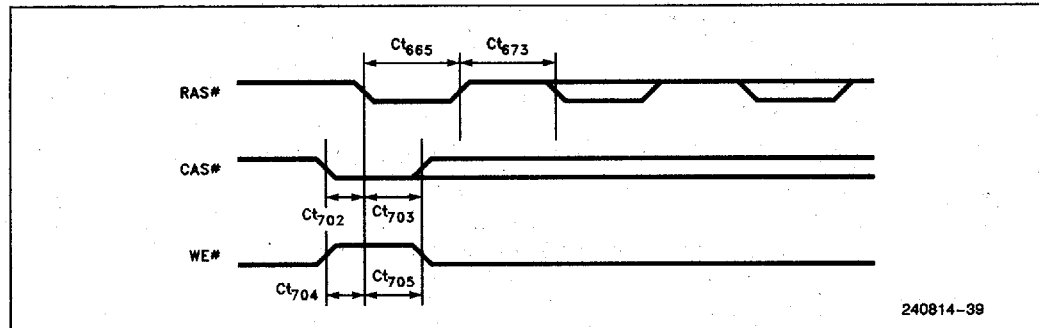
2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34



240814-38

Figure 2.5.30. Intel386™ SL CPU Memory Controller Timings (SRAM Mode Timing Parameters; 2 Wait States)



240814-39

Figure 2.5.31. Intel386™ SL CPU Memory Controller Timings (CAS# before RAS# Refresh Timings)

2

2.5 Intel386™ SL CPU (Standard 5V) Timing Diagrams (Continued)

T-49-17-34

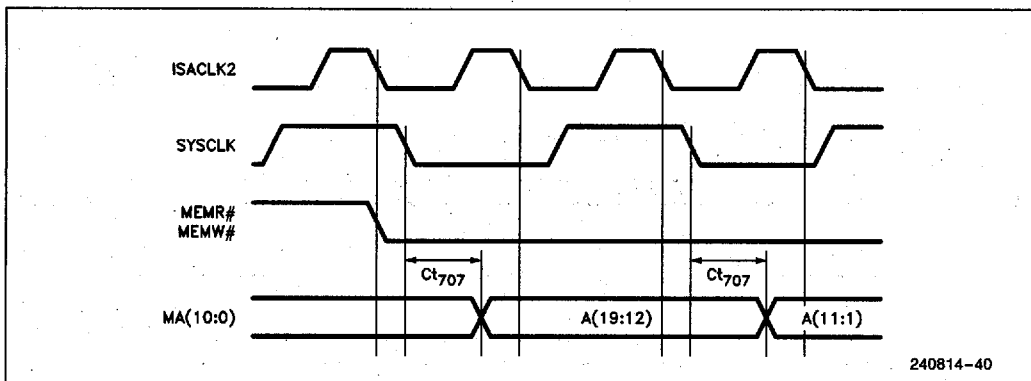


Figure 2.5.32. REFRESH, DMA/MASTER Timing Diagrams (Address Active Delay from SYSCLK)

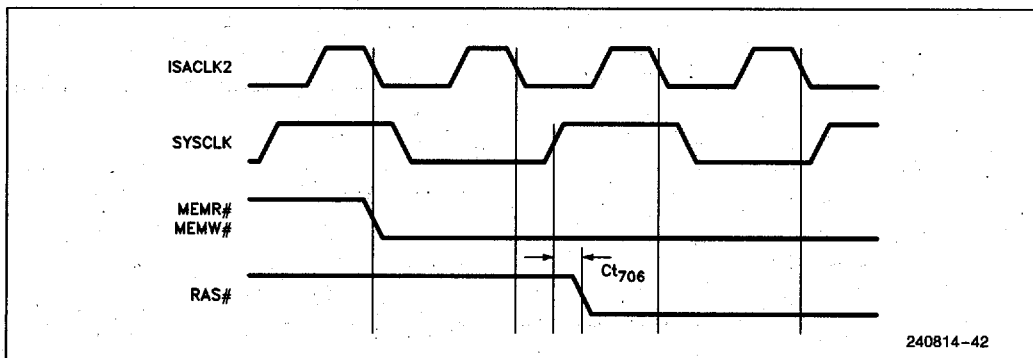


Figure 2.5.33. REFRESH, DMA/MASTER Timing Diagrams (RAS# Active Delay from SYSCLK)

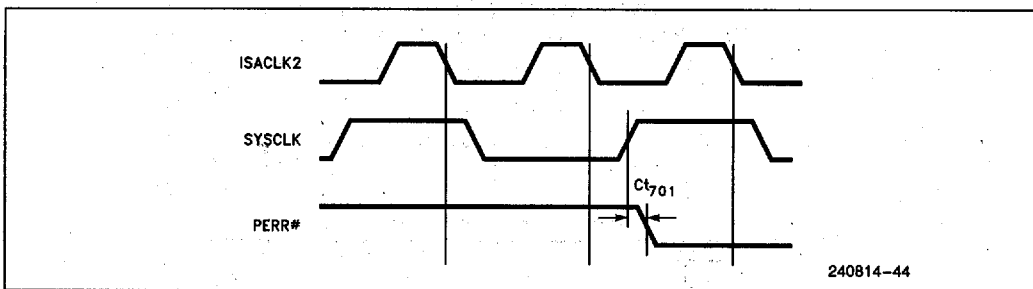


Figure 2.5.34. PERR# Timing Diagram (PERR# Active Delay from SYSCLK)

2.6 Capacitive Derating Information

In the A.C. timing table presented in Section 2.4, all max and min timings are tested at a load of 50 pF. All max timings are specified at the maximum load condition for the pin and all min timings are specified for the minimum load conditions for the pin.

If the load on a pin falls within the range of the min and max capacitance specified, no derating calculations need to be done for synchronous timings. If a lighter or heavier capacitive load is connected to any pin, signal delay will change. To allow the system designer to account for such loading differences in a system, a family of capacitive derating curves are provided in this section.

The derating curves are divided into four groups—Fast rise, fast fall, slow rise and slow fall curves. Each group has one curve for the buffer type associated with the pin corresponding to a signal. Depending upon the parameter for which the timing is being specified, curves of different groups should be used to derate the specification. The group to be used is given in the column "Derating" associated with each specification. The nomenclature used in this column is as follows: FR = Fast Rise, SR = Slow Rise, FF = Fast Fall, SF = Slow Fall. The curve corresponding to the signal in question may be found from the "Derating curve" column of the pin assignment table in Section 2.1.

In the case of output timing specifications, two group notations appear in the "Derating" column. The first of these corresponds to the reference signal and the second corresponds to the target signal.

When a specification is made about a bus or the specification is valid for both rise and fall times, only the type of derating is specified. For instance, F = Fast curve, S = Slow curve. Either the rise or the fall time derating may be used. To make a conservation calculation, use the smaller derating value among rise and fall for fast curves and the larger derating value for the slow curves.

When a specification has both a min and a max time, the derating curves for the min and the max times are separated by a semi-colon.

If loading conditions are not specified in the notes column, the timing parameter is specified for the worst case loading possible.

The rationale in the assignment of derating curves to specifications is as follows.

1. For synchronous (Clock related) specifications, all maximum timings are derated from slow curves. This is the worst case situation.

2. For synchronous (Clock related) specifications, all minimum timings are derated from fast curves. The reasoning here is that fast parts cause the worst case for minimum timings since the signal transition occurs earlier than for slow parts. Since these fast parts have fast buffers, the fast derating curves are used.

3. For output to output timings, the derating curve to be chosen depends on a combination of internal delays and buffer delays in fast and slow parts. From an analysis of the worst case situation, appropriate curves are selected for the system designer.

To use the derating curves, follow the procedure outlined here.

1. From the "Derating" column of A.C. timing table in Section 2.4, find the group of curves that must be used for a particular specification.
2. From the Pin assignment chart in Section 2.1, find the letter corresponding to the signal(s) under consideration from the column "Derating Curve".
3. In this section, find the derating curve of the correct group and letter.
4. Calculate the capacitive loading on the signal(s) under consideration.
5. Find this load point on the capacitive load axis of the derating curve.
6. Project a vertical line to the derating curve from the load point and draw a horizontal line and from the point the vertical line intersects the curve.
7. Estimate the amount of time from the Nominal point to the point where the horizontal line meets the delay axis. This is the derating value for the signal under consideration.

8. If the point where the horizontal meets the delay axis is **above** the nominal value, then

If the signal under consideration is **the reference signal** (in output to output timings) the derating value should be **subtracted** from the timing specification.

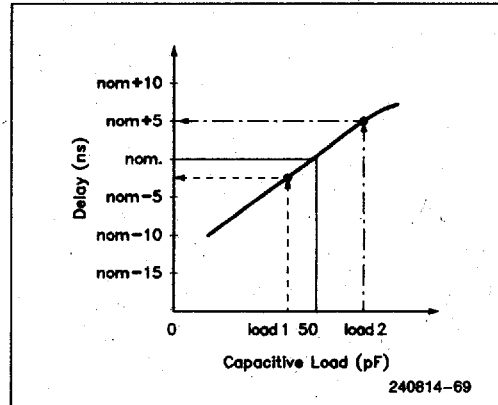
If the signal under consideration is **the target signal** (in all timings) the derating value should be **added** to the timing specification.

9. If the point where the horizontal meets the delay axis is **below** the nominal value, then

If the signal under consideration is **the reference signal** (in output to output timings) the derating value should be **added** to the timing specification.

If the signal under consideration is **the target signal** (in all timings) the derating value should be **subtracted** from the timing specification.

In some output to output specifications, the loads are not at the nominal points for the curves specified. The loads at which the specifications are made are indicated in the notes column. The same procedure as above may be used for derating except that a nominal point corresponding to the load specified must first be found on the curve specified.



Using the Capacitive Derating Curves

Intel386™ SL CPU (Standard 5V) Maximum Timing Derating Curves

FALLING

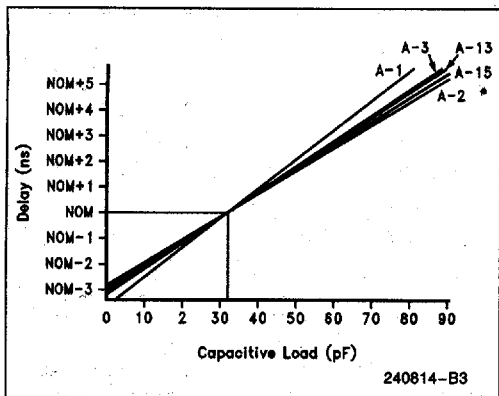


Figure 2.6.1a

RIISING

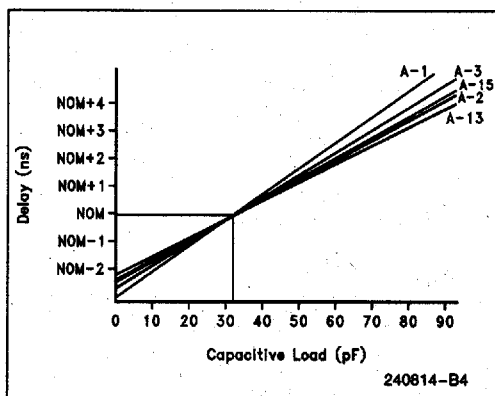


Figure 2.6.1b

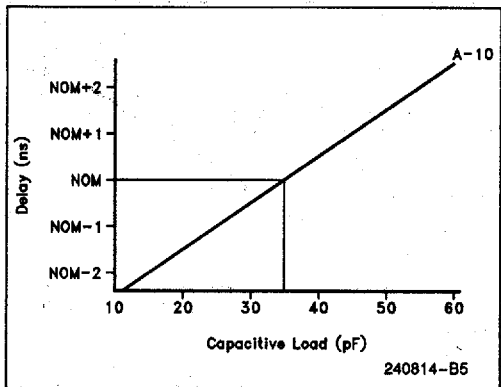


Figure 2.6.2a

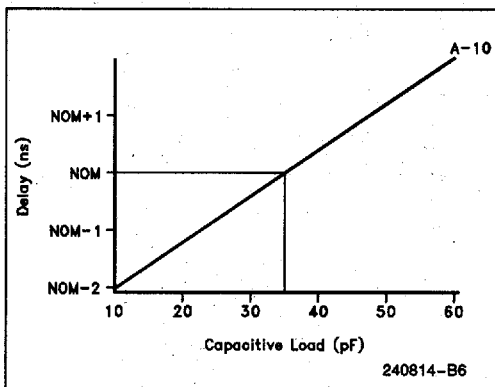


Figure 2.6.2b

2

Intel386™ SL CPU (Standard 5V) Maximum Timing Derating Curves (Continued)

FALLING

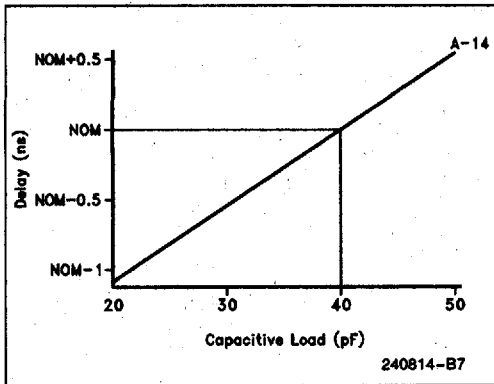


Figure 2.6.3a

RISING

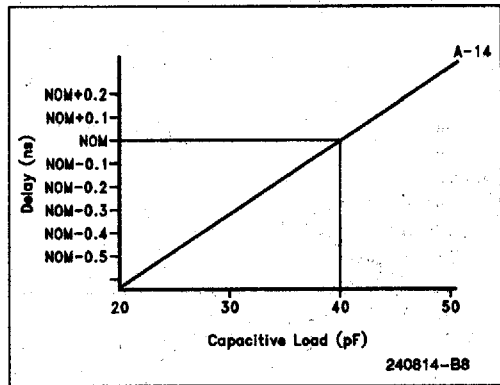


Figure 2.6.3b

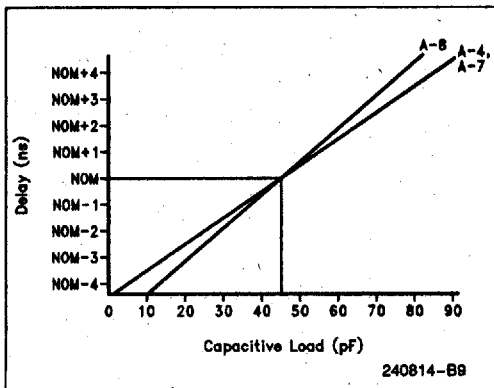


Figure 2.6.4a

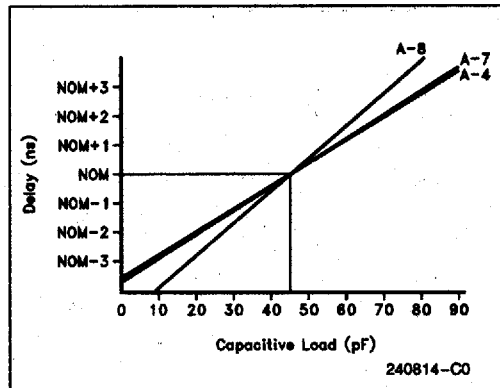


Figure 2.6.4b

Intel386™ SL CPU (Standard 5V) Maximum Timing Derating Curves (Continued)

FALLING

RISING

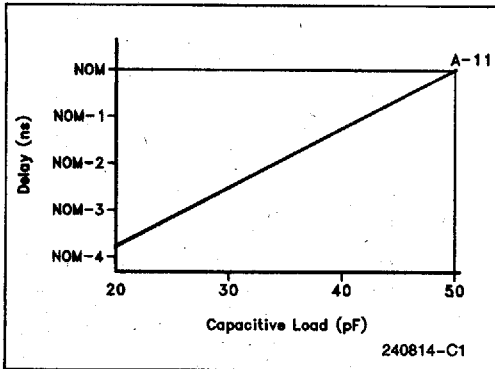


Figure 2.6.5a

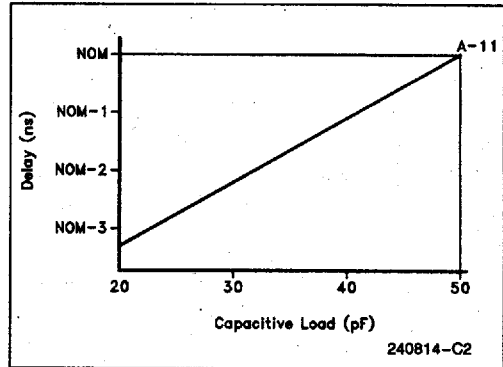


Figure 2.6.5b

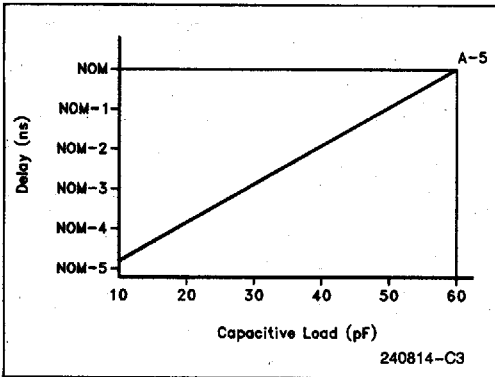


Figure 2.6.6a

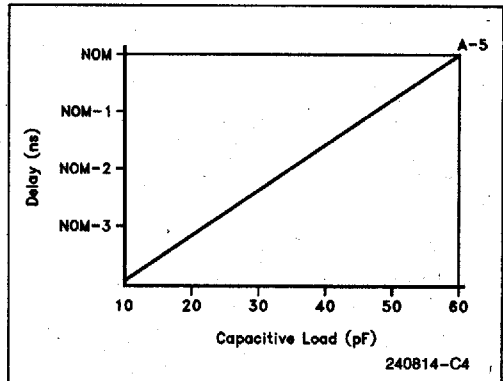


Figure 2.6.6b

2

Intel386™ SL CPU (Standard 5V) Maximum Timing Derating Curves (Continued)

FALLING

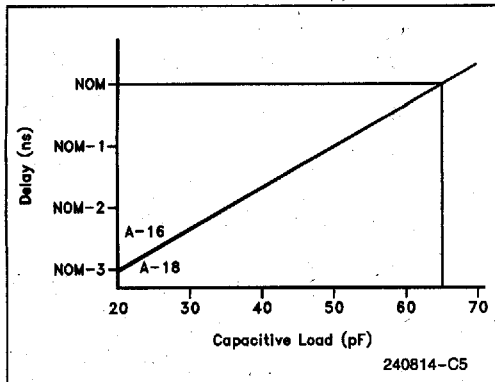


Figure 2.6.7a

RISING

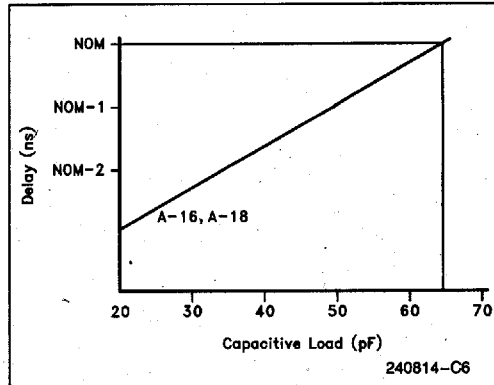


Figure 2.6.7b

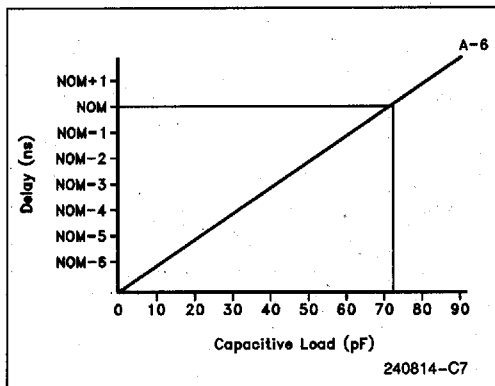


Figure 2.6.8a

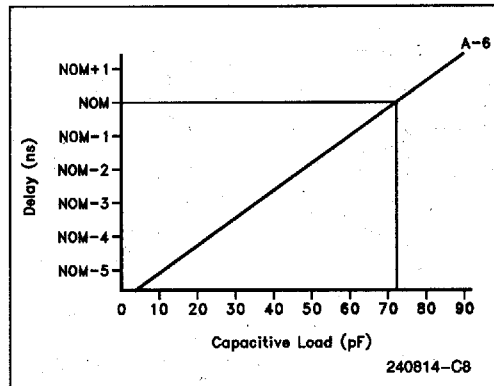


Figure 2.6.8b

Intel386™ SL CPU (Standard 5V) Maximum Timing Derating Curves (Continued)

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FALLING

RIISING

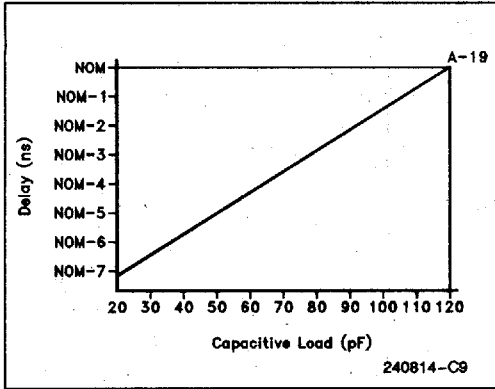


Figure 2.6.9a

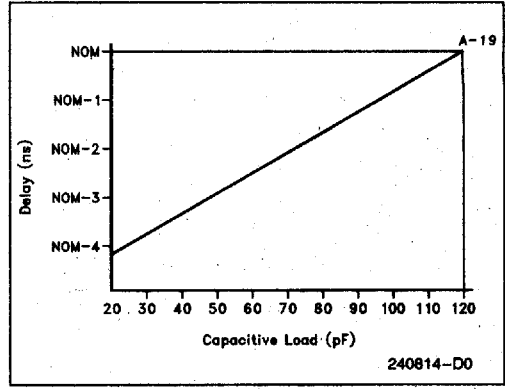


Figure 2.6.9b

2

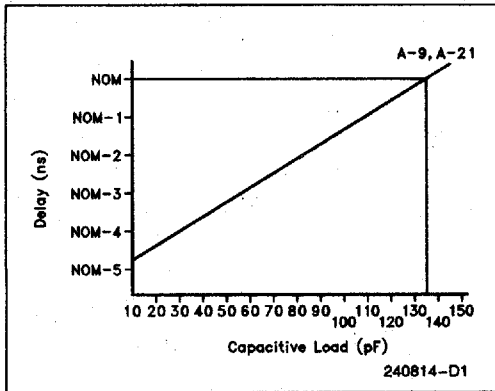


Figure 2.6.10a

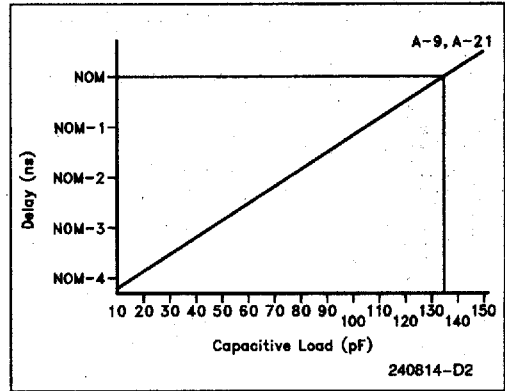


Figure 2.6.10b

Intel386™ SL CPU (Standard 5V) Maximum Timing Derating Curves (Continued)

FALLING

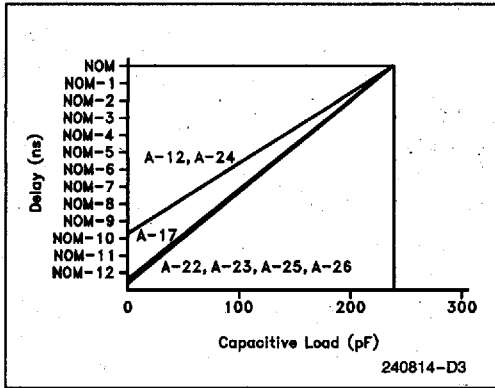


Figure 2.6.11a

RISING

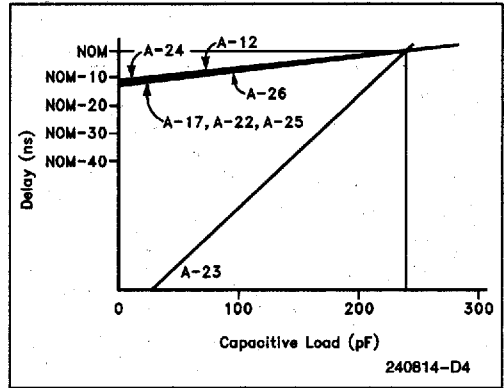


Figure 2.6.11b

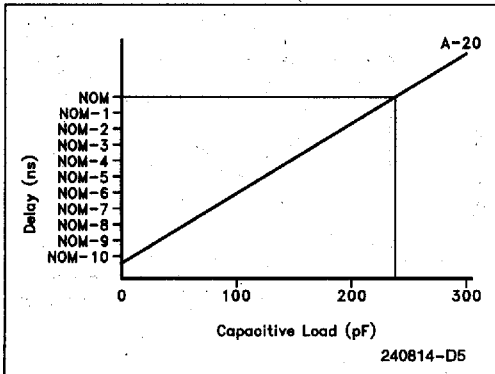


Figure 2.6.12a

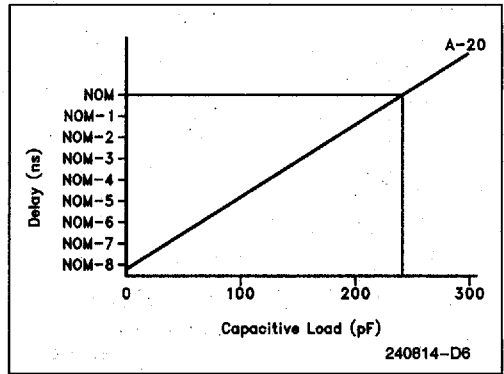


Figure 2.6.12b



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Intel386™ SL CPU (Standard 5V) Minimum Timing Derating Curves

FALLING

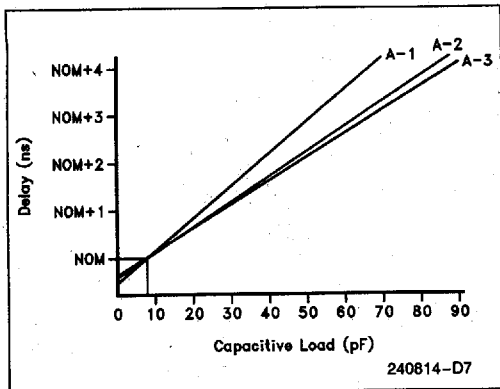


Figure 2.6.13a

RISING

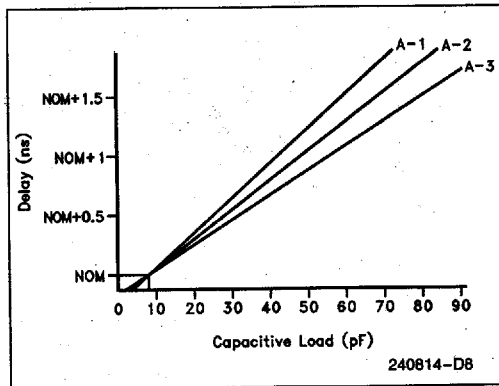


Figure 2.6.13b

2

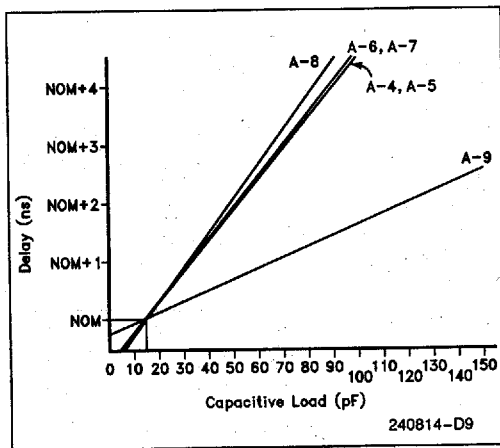


Figure 2.6.14a

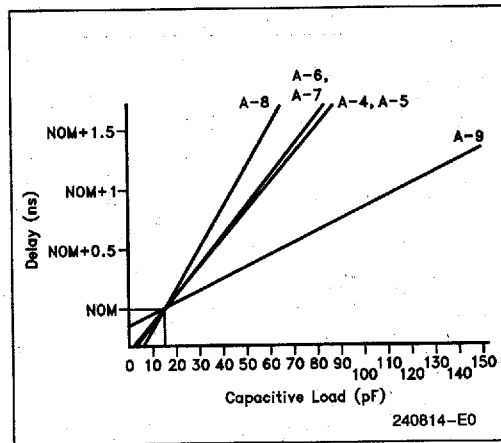


Figure 2.6.14b

Intel386™ SL CPU (Standard 5V) Minimum Timing Derating Curves (Continued)

FALLING

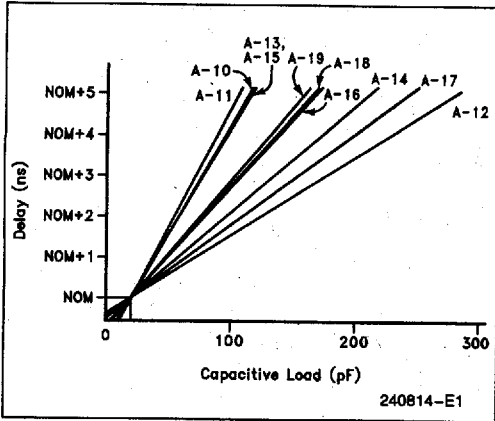


Figure 2.6.15a

RISING

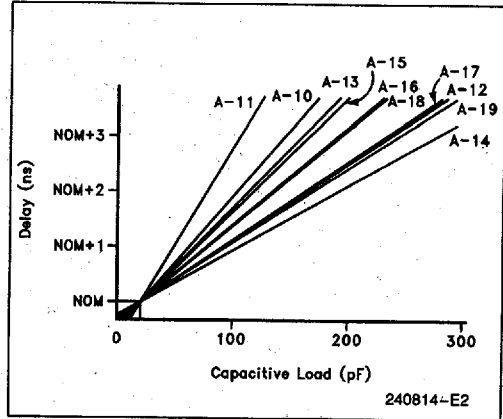


Figure 2.6.15b

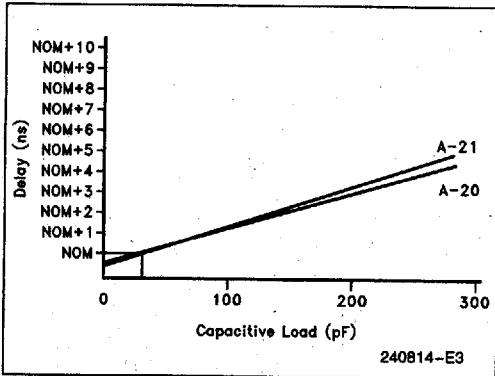


Figure 2.6.16a

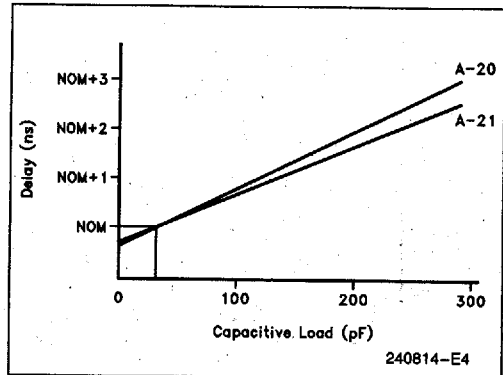


Figure 2.6.16b

Intel386™ SL CPU (Standard 5V) Minimum Timing Derating Curves (Continued)

FALLING

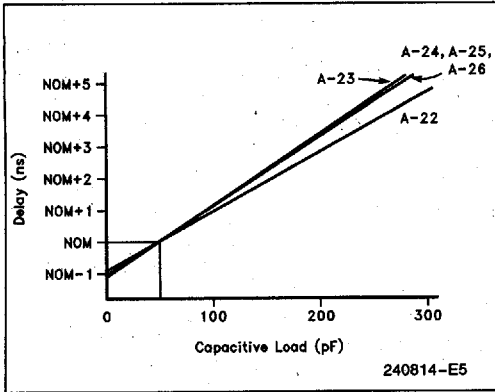


Figure 2.6.17a

RISING

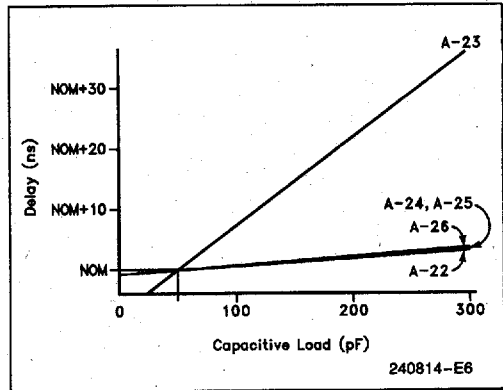


Figure 2.6.17b

3.0 Intel386™ SL MICROPROCESSOR (FlexibleVoltage Operation)

3.1 Pin Assignments and Signal Characteristics

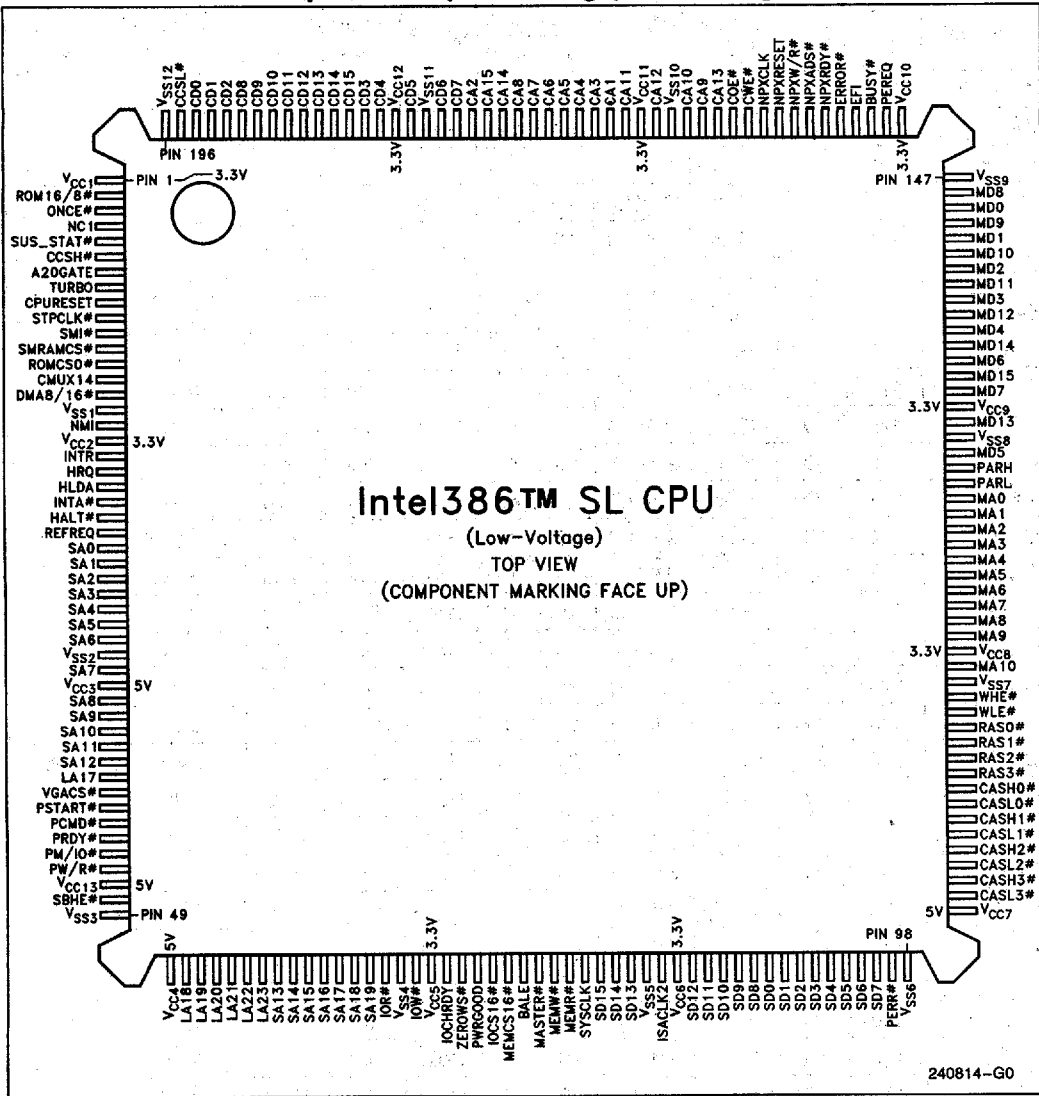
Section 3.1 provides information for the CPU pin assignment with respect to the signal mnemonics. In addition to the package pin out diagrams, a table is provided for easy location of signals. The table lists

the device pinouts in the 196 lead JEDEC PQFP and also includes additional information for the signals and associated pin numbers. A brief explanation of each column of the table is given in Table 3.1-1.

Table 3.1-1. Description of the Columns of CPU Pin Characteristics

PQFP	This column lists the pin numbers of the CPU in a Plastic Quad Flat Package.
Signal mnemonics	This column lists the signal name associated with the Package pins.
Type	Indicates whether the pin is an Input (I), an Output (O) or an Input-Output (IO).
Termination	Specifies the internal termination resistor on the pin. This could be an internal pull-up or pull-down resistor value or a hold circuit. To find out whether a pull-up or a pull-down is provided, use the STPCLK (Stop Clock) column for the CPU.
Drive	Specifies the drive current I_{OL} and I_{OH} in mA for output (O), and bi-directional (IO) pins.
Load	This column lists the maximum and minimum specified capacitive loads which the buffer can directly drive in pF for each signal. This is specified for output and input-output pins only.
Susp.	This column specifies the state of the pin during a suspend operation. Input signals have the representation Tri. This indicates that input is internally isolated and that the internal termination on the pin is tri-stated or disabled. The additional output buffers abbreviations are explained below. Tri — Tristated Actv — Active 0 — held low 1 — held high Hold — held at last state
Stpclk.	This column specifies the state of the pin when the clock signal CPUCLK is internally stopped in the CPU. Pu — Pulled up Pd — Pulled down Drv — Driven high, low, or at the last state Actv — Active (Signal is driven and continues to operate or change logic states)
ONCE	This column specifies the state of the pin when the ONCE# pin is asserted, allowing in-circuit testing while the device is still populated on the logic board. Tri — Floats Actv — Active 0 — held low 1 — held high Hold — held at last state pin
3.3 or 5V	This column specifies the named pin is powered by 3.3V or 5V.

The Intel386™ SL Microprocessor (Low-Voltage) Pinout Diagram



2

Table 3.1-2. Intel386™ SL CPU (Low-Voltage) Pin Characteristics (Continued)

Mnemonic	PQFP Pin#	Type	Termination	Drive IOL/IOH	Load		SUSP	STOP CLK	ONCE	3.3 or 5V ⁽³⁾ (power)	Derating Curve
					Min	Max					
A20GATE	007	I	60K				Tri	Pu	Tri	5V	
BALE	073	O	Hold	12/2	50	160	Hold	Drv	Hold	5V	A-1
BUSY#	150	I	60K				Tri	Pu	Tri	3.3V	
CA1	167	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	A-15
CA2	176	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	A-16
CA3	168	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	A-15
CA4	169	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA5	170	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA6	171	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA7	172	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA8	173	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA9	161	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA10	162	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA11	166	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA12	164	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA13	160	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA14	174	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CA15	175	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	
CSSH#	006	O	Hold	2.6/1.3	20	35	Hold	Drv	Hold	3.3V	A-20
CCSL#	195	O	Hold	2.6/1.3	20	35	Hold	Drv	Hold	3.3V	A-21
CD0	194	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	A-12
CD1	193	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD2	192	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD3	183	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD4	182	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD5	180	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD6	178	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD7	177	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD8	191	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD9	190	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	

NOTES:

1. All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend. (V_{CC5V} pins are ramping up from 3.3V to 5.0V).

2. During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWRGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.

3. For all 3.3V support, please consult your local Intel Sales Office.



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Table 3.1-2. Intel386™ SL CPU (Low-Voltage) Pin Characteristics (Continued)

Mnemonic	PQFP Pin #	Type	Termination	Drive I _{OL} /I _{OH}	Load		SUSP	STOP CLK	ONCE	3.3 or 5V ⁽⁴⁾ (power)	Derating Curve
					Min	Max					
CD10	189	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	A-12
CD11	188	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD12	187	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD13	186	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD14	185	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CD15	184	IO	Hold	2.6/1.3	20	50	Hold	Drv	Hold	3.3V	
CASL3#	100	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	A-19
CASH3#	101	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
CASL2#	102	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
CASH2#	103	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
CASL1#	104	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
CASH1#	105	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
CASL0#	106	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
CASH0#	107	O	Hold	2.6/1.3	12	30	Hold ⁽¹⁾	Drv	Hold	3.3V	
RAS3#	108	O	Hold	2.6/1.3	12	60	Hold ⁽¹⁾	Drv	Hold	3.3V	A-18
RAS2#	109	O	Hold	2.6/1.3	12	60	Hold ⁽¹⁾	Drv	Hold	3.3V	
RAS1#	110	O	Hold	2.6/1.3	12	60	Hold ⁽¹⁾	Drv	Hold	3.3V	
RAS0#	111	O	Hold	2.6/1.3	12	60	Hold ⁽¹⁾	Drv	Hold	3.3V	
PARL	127	IO	Hold	2.6/1.3	12	55	Hold	Drv	Hold	3.3V	A-11
PARH	128	IO	Hold	2.6/1.3	12	55	Hold	Drv	Hold	3.3V	
CMUX14 (ROMCS1# / FLSHDS#)	014	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6
COE#	159	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	A-14
CPURESET	009	I	20K				Actv	Pd	Tri	5V	
CWE#	158	O	Hold	2.6/1.3	15	45	Hold	Drv	Hold	3.3V	A-15a
DMA8/16#	015	I	60K				Tri	Pu	Tri	5V	
EFI	151	I					Actv		Tri	3.3V	
ERROR#	152	I	60K				Tri	Pu	Tri	3.3V	
HALT#	023	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6
HLDA	021	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	

NOTES:

- These pins are driven active in the suspend state if suspend refresh is enabled.
- All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend. (V_{CC5V} pins are ramping up from 3.3V to 5.0V).
- During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWRGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.
- For all 3.3V support, please contact your local Intel Field Sales Office.

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Table 3.1-2. Intel386™ SL CPU (Low-Voltage) Pin Characteristics (Continued)

Mnemonic	PQFP Pin #	Type	Termination	Drive I _{OL} /I _{OH}	Load		SUSP	STOP CLK	ONCE	3.3 or 5V ⁽⁵⁾ (power)	Derating Curve
					Min	Max					
HRQ	020	I	20K				Tri	Pd	Tri	5V	
INTA#	022	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6
INTR	019	I	20K				Tri	Pd	Tri	5V	
IOCHRDY	068	IO	1K	12/2(4)	50	160	Tri	Pu	Tri	5V	A-2
IOCS16#	071	IO	1K	12/2(4)	50	160	Tri	Pu	Tri	5V	A-5
IOR#	064	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	A-3
IOW#	065	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
ISACKL2	082	I					Actv		Tri	3.3V	
LA17	040	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	A-4
LA18	051	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
LA19	052	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
LA20	053	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
LA21	054	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
LA22	055	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
LA23	056	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
MA0	126	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	A-17
MA1	125	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA2	124	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA3	123	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA4	122	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA5	121	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA6	120	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA7	119	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA8	118	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA9	117	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MA10	115	O	Hold	2.6/1.3	12	130	Hold ⁽¹⁾	Drv	Hold	3.3V	
MASTER#	074	I	1K				Tri	Pu	Tri	5V	
MD0	145	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V	A-8
MD1	143	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V	
MD2	141	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V	

NOTES:

1. These pins are driven active in the suspend state if suspend refresh is enabled.
2. All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend. (V_{CC5V} pins are ramping up from 3.3V to 5.0V).
3. During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWARGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.
4. For I_{OH} value when the 1K pull-up is active, refer to Table 3.3-2.
5. For all 3.3V support, please consult your local Intel Sales Office.



56E D ■ 4826175 0119164 064 ■ ITL1

Table 3.1-2. Intel386™ SL CPU (Low-Voltage) Pin Characteristics (Continued)

Mnemonic	PQFP Pin #	Type	Termination	Drive I _{OL} /I _{OH}	Load		SUSP	STOP CLK	ONCE	3.3 or 5V ⁽⁵⁾ (power)	Derating Curve	
					Min	Max						
MD3	139	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V	A-8	
MD4	137	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD5	129	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD6	135	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD7	133	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD8	146	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD9	144	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD10	142	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD11	140	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD12	138	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD13	131	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD14	136	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MD15	134	IO	Hold	2.6/1.3	12	32	Hold	Drv	Hold	3.3V		
MEMCS16#	072	IO	1K	12/2 ⁽⁴⁾	50	160	Tri	Pu	Tri	5V		A-5
MEMR#	076	IO	60K	12/2	50	160	Tri	Pu	Tri	5V		A-3
MEMW#	075	IO	60K	12/2	50	160	Tri	Pu	Tri	5V		
NMI	017	I	20K				Tri	Pd	Tri	5V		
NPXADS#	154	O	Hold	2.6/1.3	20	32	Hold	Drv	Hold	3.3V	A-10	
NPXCLK	157	O	Hold	2.6/1.3	20	40	Hold	Drv	Hold	3.3V	A-13	
NPXRY#	153	I	20K				Tri	Pd	Tri	3.3V		
NPXRESET	156	O	Hold	2.6/1.3	20	32	Hold	Drv	Hold	3.3V	A-9	
NPXW/R#	155	O	Hold	2.6/1.3	20	32	Hold	Drv	Hold	3.3V	A-10	
ONCE#	003	I	60K				Actv	Pu	Actv	5V		
PCMD#	043	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6	
PEREQ	149	I	20K				Tri	Pd	Tri	3.3V		
PERR#	097	O	Hold	4/2	12	20	Hold	Drv	Hold	5V	A-22	
PM/IO#	045	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6	
PRDY#	044	I	60K				Tri	Pu	Tri	5V		
PSTART#	042	O	Hold	4/2	20	65	Hold	Drv	Tri	5V	A-6	
PW/R#	046	O	Hold	4/2	20	65	Hold	Drv	Hold	5V		
PWRGOOD	070	I					Actv	Actv	Tri	5V		

NOTES:

1. These pins are driven active in the suspend state if suspend refresh is enabled.
2. All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend. (V_{CC5V} pins are ramping up from 3.3V to 5.0V).
3. During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWRGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.
4. For I_{OH} value when the 1K pull-up is active, refer to Table 3.3-2.
5. For all 3.3V support, please consult your local Intel Sales Office.



56E D ■ 4826175 0119165 TTD ■ ITL1

Table 3.1-2. Intel386™ SL CPU (Low-Voltage) Pin Characteristics (Continued)

Mnemonic	PQFP Pin #	Type	Termination	Drive IOL/IOH	Load		SUSP	STOP CLK	ONCE	3.3 or 5V(4) (power)	Derating Curve
					Min	Max					
REFREQ	024	I	Hold				Actv	Actv	Tri	5V	
ROM16/8#	002	I	60K				Tri	Pu	Tri	5V	
ROMCS0#	013	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6
SA0	025	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	A-4
SA1	026	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA2	027	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA3	028	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA4	029	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA5	030	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA6	031	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA7	033	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA8	035	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA9	036	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA10	037	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA11	038	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA12	039	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA13	057	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA14	058	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA15	059	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA16	060	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA17	061	O	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA18	062	O	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SA19	063	O	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SBHE#	048	IO	Hold	12/2	50	160	Hold	Drv	Hold	5V	
SD0	089	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	A-1

NOTES:

1. These pins are driven active in the suspend state if suspend refresh is enabled.
2. All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend (V_{CC5V} pins are ramping up from 3.3V to 5.0V).
3. During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.
4. For all 3.3V support, please consult your local Intel Sales Office.



56E D ■ 4826175 0119166 937 ■ ITL1 T-49-17-34

Table 3.1-2. Intel386™ SL CPU (Low-Voltage) Pin Characteristics (Continued)

Mnemonic	PQFP Pin#	Type	Termination	Drive IOL/I _{OH}	Load		SUSP	STOP CLK	ONCE	3.3 or 5V(4) (power)	Derating Curve
					Min	Max					
SD1	090	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	A-1
SD2	091	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD3	092	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD4	093	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD5	094	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD6	095	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD7	096	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD8	088	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD9	087	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD10	086	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD11	085	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD12	084	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD13	080	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD14	079	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SD15	078	IO	60K	12/2	50	160	Tri	Pu	Tri	5V	
SMI#	011	I	60K				Tri	Pu	Tri	5V	
SMRAMCS#	012	O	Hold	4/2	20	65	Drv	Drv	Hold	5V	A-6
STPCLK#	010	I	60K				Tri	Pu	Tri	5V	
SUS_STAT#	005	I					Actv	Actv	Tri	5V	
SYSCLK	077	O	Hold	4/2	20	120	Hold	Drv	Hold	5V	A-7
TURBO	008	I	60K				Tri	Pu	Tri	5V	
VGACS#	041	O	Hold	4/2	20	65	Hold	Drv	Hold	5V	A-6
WHE#	113	O	Hold	2.6/1.3	12	100	Hold(1)	Drv	Hold	3.3V	A-18
WLE#	112	O	Hold	2.6/1.3	12	100	Hold(1)	Drv	Hold	3.3V	
ZEROWS#	069	I	1K				Tri	Pu	Tri	5V	

Power PinsV_{CC} (3.3V) PQFP: Pin 001, 018, 067, 083, 116, 132, 148, 165, 181V_{CC} (5V) PQFP: Pin 034, 047, 050, 099V_{SS} PQFP: Pin 016, 032, 049, 065, 081, 098, 114, 130, 147, 163, 179, 196**No Connects**

PQFP: Pin 004

NOTES:

- These pins are driven active in the suspend state if suspend refresh is enabled.
- All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend. (V_{CC5V} pins are ramping up from 3.3V to 5.0V).
- During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWRGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.
- For all 3.3V support, please consult your local Intel Sales Office.



56E D ■ 4826175 0119167 873 ■ ITL1

3.2 Signal Descriptions

T-49-17-34

Intel386™ SL Microprocessor (Low-Voltage)

The following table provides a brief description of the signals of the CPU. Signal names which end with the character “#” indicate that the corresponding signal is low when active.

Symbol	Name and Function																								
A20GATE	A20 GATE: This active HIGH input signal controls the CPU A20 address line. When LOW this signal forces the CPU to mask off (force LOW) the internal physical address signal A20. When this signal is HIGH, A20 is available on the System Address (SA) bus. When A20 gate is LOW this allows emulation of the 8086 1 Mbyte address “wrap-around”.																								
BALE	<p>BUS ADDRESS LATCH ENABLE (ISA BUS SIGNAL): This active HIGH output signal is used for two purposes. BALE is used to latch the address lines on the LA bus (LA17-LA23) on the falling edge of BALE. BALE is also used to qualify ISA bus cycles for signals on the Peripheral Interface (PI) bus (PM/IO# and PW/R#). On the falling edge of BALE, PM/IO# and PW/R# can be sampled to determine the type of ISA bus cycle that is going to occur. BALE may be used to qualify and generate buffered control and status signals to the ISA expansion bus. The PI bus signal decoding is as follows:</p> <table border="1"> <thead> <tr> <th>Type of Bus Cycle</th> <th>PM/IO#</th> <th>PW/R#</th> </tr> </thead> <tbody> <tr> <td>Memory Read</td> <td>1</td> <td>0</td> </tr> <tr> <td>Memory Read</td> <td>1</td> <td>1</td> </tr> <tr> <td>I/O Read</td> <td>0</td> <td>0</td> </tr> <tr> <td>I/O Write</td> <td>0</td> <td>1</td> </tr> <tr> <td>Interrupt Acknowledge</td> <td>0</td> <td>1</td> </tr> <tr> <td>HALT (address = 2)*</td> <td>1</td> <td>1</td> </tr> <tr> <td>Shutdown (address = 0)*</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>*Note that BALE is not generated for these cycles, however the PM/IO# and PW/R# reflect these states during HALT and Shutdown bus cycles where BALE is driven in typical ISA bus systems. Memory read/write, IO read/write and interrupt acknowledge cycles correspond to the standard ISA bus cycle.</p>	Type of Bus Cycle	PM/IO#	PW/R#	Memory Read	1	0	Memory Read	1	1	I/O Read	0	0	I/O Write	0	1	Interrupt Acknowledge	0	1	HALT (address = 2)*	1	1	Shutdown (address = 0)*	1	1
Type of Bus Cycle	PM/IO#	PW/R#																							
Memory Read	1	0																							
Memory Read	1	1																							
I/O Read	0	0																							
I/O Write	0	1																							
Interrupt Acknowledge	0	1																							
HALT (address = 2)*	1	1																							
Shutdown (address = 0)*	1	1																							
BUSY#	BUSY: This active LOW input signal indicates a busy condition from a math coprocessor (MCP).																								
CA[15: 1]	CACHE ADDRESS BUS: This is the address bus output used to select the memory cell in the cache memory. The CA2 signal is also connected to the CMDO# input of the MCP indicating Op code (when high) or Data (when low) during a write cycle and control/status register (high) or data register (low) during a read. CA2 is used to address the upper or lower DWORD port of the MCP.																								
CCSH#	CACHE CHIP SELECT HIGH BYTE: This active LOW output is used to enable the upper byte of the cache SRAMs. This signal should be connected to the upper byte cache SRAM chip-select input.																								
CCSL#	CACHE CHIP SELECT LOW BYTE: This active LOW output is used to enable the lower byte of the cache SRAMs. This signal should be connected to the lower byte cache SRAM chip-select input.																								



56E D ■ 4826175 0119168 70T ■ ITL1

Intel386™ SL Microprocessor (Low-Voltage) Signal Descriptions (Continued)

Symbol	Name and Function
CD[15:0]	CACHE DATA BUS: This is the bi-directional data bus used to transfer data between the cache SRAMs and the CPU. The Cache Data bus is also used to transfer data between the MCP and the CPU.
CASL3#	COLUMN ADDRESS STROBE BANK 3, LOW BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 3 and should be connected to the CAS# input of the lower byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CASH3#	COLUMN ADDRESS STROBE BANK 3, HIGH BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 3 and should be connected to the CAS# input of the upper byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CASL2#	COLUMN ADDRESS STROBE BANK 2, LOW BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 2 and should be connected to the CAS# input of the lower byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CASH2#	COLUMN ADDRESS STROBE BANK 2, HIGH BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 2 and should be connected to the CAS# input of the upper byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CASL1#	COLUMN ADDRESS STROBE BANK 1, LOW BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 1 and should be connected to the CAS# input of the lower byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CASH1#	COLUMN ADDRESS STROBE BANK 1, HIGH BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 1 and should be connected to the CAS# input of the upper byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CASL0#	COLUMN ADDRESS STROBE BANK 0, LOW BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 0 and should be connected to the CAS# input of the lower byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".



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Intel386™ SL Microprocessor (Low-Voltage) Signal Descriptions (Continued)

Symbol	Name and Function
CASH0#	COLUMN ADDRESS STROBE BANK 0, HIGH BYTE: This Low output signal of the CPU Memory Controller is a column address strobe for the physical DRAM bank 0 and should be connected to the CAS# input of the upper byte. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX14 (ROMCS1#/ FLSHDCS#)	CPU MULTIPLEXED PIN 14: This output signal has two functions. The CPU can be configured to use this pin as either a BIOS ROM chip-select (ROMCS1#), or a FLASH disk chip-select signal (FLSHDCS#). In either case, the signal is driven LOW when an access to the selected interface occurs.
COE#	CACHE OUTPUT ENABLE: This active LOW output signal is used to indicate a read access to the cache SRAMs, and is used to enable the cache SRAMs' output buffers. This signal should be connected to the output enable signals of the upper and lower byte cache SRAMs.
CPURESET	CPU RESET: This active HIGH input forces the CPU to execute a reset to the internal CPU core and state machines. The configuration registers are not reset.
CWE#	CACHE WRITE ENABLE: This active LOW output is used to indicate a write (LOW) access to the cache SRAMs. This signal should be connected to the write enable signal of the upper and lower byte cache SRAMs.
DMA8/16#	DMA 8-BIT OR 16-BIT CYCLE: This input, in conjunction with HRQ, indicates to CPU if an 8-bit or 16-bit DMA access is occurring. If an 8-bit DMA access is occurring, the CPU will swap the upper byte of data to the lower data byte for upper byte accesses.
EFI	EXTERNAL FREQUENCY INPUT. This is an oscillator input. This clock controls all CPU core and memory controller timings and is equal to twice the desired processor frequency (CPUCLK).
ERROR#	NUMERICS ERROR: This active LOW input to the CPU is generated from a math coprocessor (MCP). It also indicates to the 82360SL that an unmasked exception has occurred in the MCP. ERROR# is provided to allow numerics error handling compatible with the ISA bus compatible personal computer.
HALT#	HALT: This active LOW output indicates to external devices that the CPU has executed a HALT instruction (address = 2) or a Shutdown condition (address = 0) This can be used as an indicator for devices to assert the STCLK# signal.
HLDA	HOLD ACKNOWLEDGE: This active HIGH input indicates to the CPU has relinquished control of the ISA bus. At this time the CPU has floated the address and control signals of the ISA bus.
HRQ	HOLD REQUEST: This active HIGH input indicates to the CPU that an external device wishes to take control of the ISA bus.
INTA#	INTERRUPT ACKNOWLEDGE: This active LOW output indicates that the CPU is executing an interrupt acknowledge bus cycle. During this process an external interrupt device will pass an interrupt vector to the CPU.
INTR	INTERRUPT REQUEST: This active HIGH input indicates to the CPU that an external device is requesting the execution of an interrupt service routine.

**Intel386™ SL Microprocessor (Low-Voltage) Signal Descriptions** (Continued)

Symbol	Name and Function
IOCHRDY	I/O CHANNEL READY: This active HIGH input/output signal indicates that the I/O Channel, (ISA expansion bus), is ready to terminate the bus cycle. The ISA expansion bus is a normally ready bus and IOCHRDY is active HIGH. When an ISA bus peripheral needs to extend the standard 3 SYSCLK, 16-bit ISA bus cycle the peripheral device asserts IOCHRDY LOW.
IOCS16#	I/O CHIP SELECT 16: This active LOW input/output signal indicates that an ISA bus peripheral wishes to execute a 16-bit I/O cycle. This signal has an active pull-up, when not driven the default I/O bus cycle is 8-bit.
IOR#	I/O READ: This active LOW signal indicates that the ISA bus is executing an I/O read cycle.
IOW#	I/O WRITE: This active LOW signal indicates that the ISA bus is executing an I/O write cycle.
ISACK2	ISA CLOCK TWO: This is an oscillator input. This clock controls all of the ISA bus timings and is equal to twice the SYSCLK frequency. Normally the ISA bus SYSCLK is 8 MHz, and the ISACK2 oscillator is 16 MHz.
LA[23:17]	LATCHABLE LOCAL ADDRESS BUS: This is the unlatched local address of the ISA bus for access to memory above 1 Mbyte. The LA bus is also used by the Peripheral Interface (PI) Bus.
MA[10:0]	MEMORY CONTROLLER MULTIPLEXED ADDRESS BUS: This is the address bus output for the Memory Controller Unit. The 22-bit address is output in a row/column fashion for the DRAM memory subsystems. The Memory Controller Unit places the ROW address out first and qualifies it by the RASx# signal going active. The column address is then placed on the Memory Address bus and is qualified by the CASx# signals going active. This pin is disabled when SUS_STAT# is active (LOW). When the pin is disabled the output is sustained at the previous state by internal "keepers".
MASTER#	MASTER: This active LOW input indicates that an ISA bus peripheral is controlling the bus. The peripheral device asserts this signal in conjunction with a DMA request (DRQ) line or the HRQ (hold request) to gain control of the bus. When the MASTER# signal is asserted LOW along with HRQ being asserted HIGH the CPU will float all address, data and control signals on the ISA bus.
MD[15:0]	MEMORY CONTROLLER LOCAL MEMORY DATA BUS: This is the bi-directional data bus of the Memory Controller Unit. All accesses by the Memory Controller Unit that transfer data between the CPU and DRAM use the Memory Data Bus. This pin is disabled when SUS_STAT# is active (low) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
MEMCS16#	MEMORY CHIP SELECT 16: This active LOW input/output signal indicates that an ISA bus peripheral wishes to execute a 16-bit memory cycle. This signal has an active pull-up, when not driven the default memo bus cycle is 8 bits.
MEMR#	MEMORY READ: This bi-directional active LOW signal indicates that a memory read access is taking place on the ISA bus. When the CPU is performing a memory read to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA device or Master drives MEMR#.
MEMW#	MEMORY WRITE: This bi-directional active LOW signal indicates that a memory write access is taking place on the ISA bus. When the CPU is performing a memory write to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA device or Master drives MEMW#.



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Intel386™ SL Microprocessor (Low-Voltage) Signal Descriptions (Continued)

Symbol	Name and Function
N/C	NO CONNECTION: These pins must not be connected to any voltage, but must be left floating in order to guarantee proper operation of the CPU and to maintain compatibility with future Intel Processors.
NMI	NON-MASKABLE INTERRUPT: This rising edge sensitive input will latch a request to the CPU for a non-maskable interrupt on a LOW-to-High transition.
NPXADS#	NUMERICS ADDRESS STROBE: This active LOW output signal indicates the start of a math coprocessor (MCP) data transfer cycle.
NPXCLK	NUMERICS CLOCK: This output signal is used to drive the MCP clock input.
NPXRDY#	NUMERICS READY: This active LOW input is used to terminate a MCP bus cycle. This signal is low for I/O and data operand MCP cycles.
NPXRESET	NUMERICS RESET: This active HIGH output signal is used to reset the MCP.
NPXW/R#	NUMERICS WRITE OR READ: This output signal indicates the type of data transfer that is being performed between the CPU and the MCP. When high this signal indicates a MCP write, when low this signal indicates a MCP read.
ONCE#	ON-BOARD CIRCUIT EMULATION: This active LOW input signal floats the necessary outputs from the CPU allowing an in-circuit emulation (ICETM 386 SL) module to drive the CPU signals. This allows an emulator to be used for system testing and development while the CPU and the 82360SL are still physically populated on the system motherboard. The state of all CPU and 82360SL signals when ONCE# is asserted low is summarized in Section 2, (CPU signal characteristics). Note that the ONCE# pin of the CPU should not be connected to the ONCE# pin of the 82360SL I/O.
PARL#	PARITY LOW BYTE: This Low output signal of the CPU Memory Controller Unit is for the CPU to read or write the low byte DRAM parity bit and should be connected to the lower byte of DRAM bank 0 data parity bit. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
PARH#	PARITY HIGH BYTE: This Low output signal of the CPU Memory Controller Unit is for the CPU to read or write the high byte DRAM parity bit and should be connected to the upper byte of DRAM bank 0 data parity bit. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
PCMD#	PI-BUS COMMAND: This active LOW output indicates that valid write data is on the system data bus (SD[15:0]) signals, or that the CPU is ready to sample valid read data from the PI-Bus for Peripheral Interface bus cycles.
PEREQ	PROCESSOR EXTENSION REQUEST: This active HIGH input signal indicates that the MCP has data to transfer to or from the CPU.
PERR#	PARITY ERROR: This active LOW output indicates to an external device that the CPU Memory Controller Unit has detected a memory parity error. The PERR# signal is used by the 82360 SL to generate NMI back to the CPU.
PM/IO#	PI-BUS MEMORY OR I/O: This output indicates the type of bus cycle the CPU is executing on the Peripheral Interface Bus (PI-bus): Either a Memory (HIGH) or I/O (LOW) cycle.
PRDY#	PI-BUS READY: This active LOW input is used to terminate Peripheral Interface bus cycles. The Peripheral Interface Bus is a normally not-ready bus, and will continue the bus cycle until the PRDY# is activated or a Peripheral Interface Timeout occurs.



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Intel386™ SL Microprocessor (Low-Voltage) Signal Descriptions (Continued)

Symbol	Name and Function
PSTART #	PI-BUS START: This active LOW output indicates that the address (SA[19:0], LA[23:17] and SBHE #), command signals (PM/IO # and PW/R #) and chip-selects (VGACS # or FLSDCS #) are valid for a Peripheral Interface Bus cycle.
PW/R #	PI-BUS WRITE OR READ: This output indicates the type of bus cycle the CPU is executing on the Peripheral Interface Bus: Either a Write (HIGH) or a Read (LOW).
PWRGOOD	POWER GOOD: This active HIGH input indicates that power to the system is good. This signal is generated by the power supply circuitry, and a LOW level on this signal causes the CPU to totally reset: The CPU core is reset, internal state machines are reset, all configuration registers are reset. Power Good should be low for a specified minimum number of CPU clocks for valid recognition in order to perform a global CPU reset.
RAS3 #	ROW ADDRESS STROBE BANK 3: This Low output signal of the CPU Memory Controller Unit is a row address strobe for the physical DRAM Bank 3 and should be connected to the upper and lower byte of DRAM bank 3 RAS # inputs. This pin is disabled when SUS_STAT # is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS2 #	ROW ADDRESS STROBE BANK 2: This Low output signal of the CPU Memory Controller Unit is a row address strobe for the physical DRAM Bank 2 and should be connected to the upper and lower byte of DRAM bank 2 RAS # inputs. This pin is disabled when SUS_STAT # is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS1 #	ROW ADDRESS STROBE BANK 1: This Low output signal of the CPU Memory Controller Unit is a row address strobe for the physical DRAM Bank 1 and should be connected to the upper and lower byte of DRAM bank 1 RAS # inputs. This pin is disabled when SUS_STAT # is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
RAS0 #	ROW ADDRESS STROBE BANK 0: This Low output signal of the CPU Memory Controller Unit is a row address strobe for the physical DRAM Bank 0 and should be connected to the upper and lower byte of DRAM bank 0 RAS # inputs. This pin is disabled when SUS_STAT # is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
REFREQ	REFRESH REQUEST: This active HIGH input indicates that the CPU should execute an internal DRAM refresh cycle to the on-board local memory.
ROM16/8 #	ROM 16 BITS OR 8 BITS: This input configuration signal pin selects if the BIOS interface is a 16-bit (when high) or 8-bit interface (when low). This pin has an internal pull-up resistor defaulting to a 16-bit wide BIOS EPROM.
ROMCS0 #	ROM CHIP SELECT 0: This LOW true output provides the chip select for the System BIOS EPROM.
SA[19:0]	SYSTEM ADDRESS BUS: This is the bi-directional system address of the ISA bus, as well as the Peripheral Interface Bus. SA[16:0] are inputs during DMA and Master operation. SA[19:17] are outputs only since a 8237 compatible DMA controller accesses up to 64 Kbytes at a time. The 74LS612 module in the 82360SL is used to furnish the DMA upper addresses for DMA access to 16 Mbyte.



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Intel386™ SL Microprocessor (Low-Voltage) Signal Descriptions (Continued)

Symbol	Name and Function
SBHE#	SYSTEM BYTE HIGH ENABLE: When this output signal is LOW, it indicates that data is being transferred on the upper byte of the 16-bit data bus (SD[15:8]).
SD[15:0]	SYSTEM DATA BUS: This 16-bit bi-directional data bus is used to transfer data between the CPU and the ISA bus. The system data bus is also used to transfer data between the CPU and the Peripheral Interface Bus PI-BUS.
SMI#	SYSTEM POWER MANAGEMENT INTERRUPT: This falling edge sensitive input latches a Power Management interrupt request with a High-to-Low edge. The SMI# is the highest priority interrupt in the CPU processor.
SMRAMCS#	SYSTEM POWER MANAGEMENT RAM CHIP SELECT: This active LOW output is used to select an external system power management SM-RAM, and to indicate to the 82360SL device when accesses to the system power management SM-RAM are occurring.
STPCLK#	STOP CLOCK: This active LOW input stops the clock to the internal CPU core. (This signal is functionally tested by the execution of HALT or I/O read instructions.)
SYSCLK	SYSTEM CLOCK: This is a clock output equal to one half of the ISACKL2 input frequency.
SUS_STAT#	SUSPEND STATUS: This active LOW input indicates to the CPU that system power is being turned off. The CPU will respond by electrically isolating selected pins as indicated in Section 2, (CPU signal characteristics).
TURBO	TURBO: This active HIGH input signal indicates to CPU when to enter "Turbo Mode". Turbo Mode is defined as the CPU executing at full speed, the default speed for the system. When this signal is forced inactive LOW, the CPU executes from a divide by two or a divide by four clock as defined by the De-turbo bit in the CPUPWRMODE register. When this signal is HIGH, the CPU executes from a clock as defined by the Fast CPU clock field in the CPUPWRMODE register.
V _{CC}	SYSTEM POWER: Provides the +5V or 3.3V nominal D.C. supply inputs.
VGACS#	VGA CHIP-SELECT: This active LOW output is asserted anytime an access occurs to the user defined VGA address space.
V _{SS}	SYSTEM GROUND: Provides the 0V connection from which all inputs and outputs are referenced.
WHE#	WRITE HIGH ENABLE: This active LOW output signal is active anytime a write access to DRAM memory subsystem occurs. This output should be connected to the write enable of the upper byte for the DRAM memory subsystems. This pin is driven inactive during a suspend operation.
WLE#	WRITE LOW ENABLE: This active LOW output signal is active anytime a write access to DRAM memory subsystem occurs. This output should be connected to the write enable of the lower byte for the DRAM memory subsystems. This pin is driven inactive during a suspend operation.
ZEROWS#	ZERO WAIT STATE (ISA BUS SIGNAL): This active LOW input indicates that an ISA bus peripheral wishes to execute a zero wait state bus cycle (the normal default 16-bit ISA bus memory or I/O cycle is 3 SYSCLKS or one PC/AT equivalent wait state). When ZEROWS# is driven low, a 16-bit bus cycle will occur in two SYSCLKs. When ZEROWS# is driven low for an 8-bit memory or I/O cycle the default 6 SYSCLK bus cycle is shortened to 3 SYSCLKs.

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3.3 D.C. Specifications

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3.3.1 CAPACITANCE D.C. SPECIFICATIONS**Table 3.3-1. Capacitance D.C. Specifications**

Symbol	Parameter	Min	Max	Unit	Notes
C _{IN}	Input Capacitance		10	pF	
C _{OUT}	Output or I/O Capacitance		20	pF	
C _{CLK}	EFI or ISACKL2		15	pF	

3.3.2 5V SIGNAL CURRENT AND VOLTAGE D.C. SPECIFICATIONS**3.3.2.1 Five (5.0) Volt Signal Pins D.C. Specifications****Table 3.3-2. 5V Signal Pins D.C. Voltage Specifications**

Symbol	Parameter	Min	Max	Unit	Notes
V _{CC5V}	Supply Voltage	4.5	5.5	V	Pins 34, 47, 50, 99
V _{CC5V}	Supply Voltage	3.0	3.6	V	Pins 34, 47, 50, 99 Only during 3.3V-Suspend Mode. (Notes 3, 4)
V _{IL}	Input Low Voltage	-0.3	+0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.3	V	
V _{OL}	Output Low Voltage I _{OL} = 12 mA I _{OL} = 4 mA		0.45 0.45	V V	(Note 1) (Note 2)
V _{OH}	Output High Voltage I _{OH} = -2 mA	2.4		V	All pins except IOCHRDY, IOCS16# and MEMCS16#
V _{OH}	I _{OH} = -0.8 mA	2.4		V	For IOCHRDY, IOCS16# and MEMCS16# (Note 6)

NOTES:

- List of 5V Output signal pins which have 12 mA/-2 mA I_{OL}/I_{OH} specifications in the CPU pin characteristics Table 3.1-2.
- Other 5V Output signal pins which do not belong to list in Note 1.
- All 5V signals should not exceed 0.3V above voltage of V_{CC5V} pins when the system is entering 3.3V-Suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V-Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-Suspend. (V_{CC} 5V pins are ramping up from 3.3V to 5.0V).
- During 5V- or 3.3V-Suspend, all input signals except CPURESET, REFREQ, PWRGOOD, EFI, ISACKL2, ONCE# and SUS_STAT# are disabled by CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.
- All voltages are tested at 4 MHz.
- This spec is only applicable when the 1K pull-up is active.



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3.3.2.2 Five (5.0) Volt Signal Pins D.C. Sustaining & Leakage Current Specifications

Table 3.3-3. 5V Signal Pins Sustaining Current and Leakage Current Specifications

Symbol	Parameter	Min	Max	Unit	Notes
VCC5V	Supply Voltage	4.5	5.5	V	Pins 34, 47, 50, 99
I _{SI}	Input Sustaining Current When SUS_STAT# and/or ONCE# not active				
	Pins with internal 60K PU		-140	μA	V _{IL} = 0.45V
	Pins with internal 20K PD Pins with internal 1K PU		320 -20	μA mA	V _{IH} = 2.4V V _{IL} = 0.45V
I _{LI}	Input Leakage Current When SUS_STAT# and/or ONCE# active		±15	μA	0V < V _{IN} < VCC5V (Note 5)
I _{SO}	Output Sustaining Current When SUS_STAT# and/or ONCE# not active				
	Pins with internal 60K PU		-150	μA	V _{OUT} = 0.45V
	Pins with internal 1K PU		-24	mA	V _{OUT} = 0.45V
I _{LO}	Output Leakage Current When SUS_STAT# and/or ONCE# active		±15	μA	0.45V < V _{OUT} < VCC5V (Note 5)
I _{BHL}	Bus Hold Low Sustaining Current		33	μA	V _{IN} = 0.8V (Note 1)
I _{BHH}	Bus hold High Sustaining Current		-80	μA	V _{IN} = 2.0V (Note 2)
I _{BHLO}	Bus Hold Low Overdrive Current	300		μA	(Note 3)
I _{BHHO}	Bus Hold High Overdrive Current	-550		μA	(Note 4)

NOTES:

1. This is the maximum current the bus hold circuit can sink without raising the node above V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to ground and then raising to V_{IL}max.
2. This is the maximum current the bus hold circuit can source without lowering the node voltage below V_{IH}min. I_{BHH} should be measured after raising V_{IN} to VCC5V and then lowering to V_{IH}min.
3. An external driver must source at least I_{BHLO} to switch this node from low to high.
4. An external driver must sink at least I_{BHHO} to switch this node from high to low.
5. This spec is applicable only to the list of pins that can float when SUS_STAT# and/or ONCE# is active. Refer to CPU Pin Characteristics in Table 3.1-2 for details.

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3.3.2.3 Five (5.0) Volt Power Pins I_{CC} Specifications

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Table 3.3-4. 5V Power I_{CC} Specifications

Symbol	Parameter	Typ	Max	Unit	Notes
V _{CC5V}	Supply Voltage	5.0	5.5	V	Pins 34, 47, 50, 99
I _{CC5V}	Supply Current	15	30	mA	(Note 4)
I _{CCS1_5V}	Supply Current with the STPCLK# Signal Asserted	2		mA	(Note 1)
I _{CCS2_5V}	Supply Current in Suspend Mode with Oscillators OFF and RTC Suspend Refresh ON	0.3		mA	(Note 2)
I _{CCS3_5V}	Supply Current in Suspend Mode with Oscillators OFF and Self Suspend Refresh ON	0.2		mA	(Note 3)

NOTES:

1. STPCLK# Signal is active, all external Oscillators free running, no cycles on cache, memory or ISA Bus. Typically with V_{CC5V} = 5.0V, EFI = 40 MHz, ISACK2 = 16 MHz, 50 pF capacitive loads and no resistive loads on the outputs.
2. RTC Suspend Refresh Mode and all external oscillators turned OFF (in a fixed logic states), no cycles on cache, memory or ISA bus. CASx# are driven active (LOW) and RASx# are toggled during Suspend Mode. Typically with V_{CC5V} = 5.0V, 50 pF capacitive loads and no resistive load on the outputs. Same specification applies in 3.3V—suspend where V_{CC5V} = 3.3V.
3. Self Suspend Refresh Mode and all external oscillators turned OFF (In a fixed logic states), no cycles on cache, memory or ISA bus. The REFREQ signal is active causing memory refreshes to the on-board memory during Suspend. CASx# and RASx# are driven active (LOW) during Suspend Mode. Typically with V_{CC5V} = 5.0V, 50 pF capacitive loads and no resistive load on the outputs. Same specification applies in 3.3V—suspend where V_{CC5V} = 3.3V.
4. The values are theoretical estimates for a typical notebook configuration based on an ISA load of 160 pF @ 8 MHz and ISA-Bus utilization of 10%. For I_{CC} in a maximum configuration system, please refer to Section 3.3.4.

3.3.3 3.3V SIGNAL CURRENT AND VOLTAGE D.C. SPECIFICATIONS

3.3.3.1 Three (3.3) Volt Signal Pins D.C. Specifications

Table 3.3-5. 3.3V Signal Pins D.C. Voltage Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V _{CC3.3V}	Supply Voltage	3.0	3.6	V	Pins 1, 18, 67, 83, 116, 132, 148, 165, 181
V _{IL}	Input Low Voltage	-0.3	+0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.3	V	
V _{ILC}	Input Clock Low Voltage	-0.3	+0.3	V	
V _{IHC}	Input Clock High Voltage	V _{CC} - 0.3	V _{CC} + 0.3	V	
V _{OL}	Output Low Voltage I _{OL} = 2.6 mA		0.40	V	(Note 1)
V _{OH}	Output High Voltage I _{OH} = -1.3 mA	2.4		V	(Note 1)

NOTE:

1. List of 3.3V output signal pins which have 2.6/-1.3 mA I_{OL}/I_{OH} specifications in the CPU Pin Characteristics Table 3.1-2.



3.3.3.2 Three (3.3) Volt Signal Pins D.C. Leakage and Sustaining Current Specifications

Table 3.3-6. 3.3V Signal Pins Sustaining Current and Leakage Current Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V _{CC3.3V}	Supply Voltage	3.0	3.6	V	Pins 1, 18, 67, 83, 116, 132, 148, 165, 181
I _{SI}	Input Sustaining Current When SUS_STAT# and/or ONCE# not active				
	Pins with internal 60K PU Pins with internal 20K PD		-140 320	μ A μ A	V _{IL} = 0.4V V _{IH} = 2.4V
I _{LI}	Input Leakage Current When SUS_STAT# and/or ONCE# active		±15	μ A	0V < V _{IN} < V _{CC3.3V} (Note 5)
I _{SO}	Output Sustaining Current When SUS_STAT# and/or ONCE# not active				
	Pins with internal 60K PU		-150	μ A	V _{OUT} = 0.4V
I _{LO}	Output Leakage Current When SUS_STAT# and/or ONCE# active		±15	μ A	0.4V < V _{OUT} < V _{CC3.3V} (Note 5)
I _{BHL}	Bus Hold Low Sustaining Current		17	μ A	V _{IN} = 0.8V (Note 1)
I _{BHH}	Bus hold High Sustaining Current		-20	μ A	V _{IN} = 2.0V (Note 2)
I _{BHLO}	Bus Hold Low Overdrive Current	210		μ A	(Note 3)
I _{BHHO}	Bus Hold High Overdrive Current	-350		μ A	(Note 4)

NOTES:

1. This is the maximum current the bus hold circuit can sink without raising the node above V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to ground and then raising to V_{IL}max.
2. This is the maximum current the bus hold circuit can source without lowering the node voltage below V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC3.3V} and then lowering to V_{IH}min.
3. An external driver must source at least I_{BHLO} to switch this node from low to high.
4. An external driver must sink at least I_{BHHO} to switch this node from high to low.
5. This spec is only applicable to the list of pins that can float when SUS_STAT# and/or ONCE# is active. Refer to CPU Pin Characteristics in Table 3.1-2 for details.



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3.3.3.3 Three (3.3) Volt Power Pins I_{CC} Specifications

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Table 3.3-7. 3.3V I_{CC} Specifications

Symbol	Parameter	Typ	Max	Unit	Notes
V _{CC3.3V}	Supply Voltage	3.3	3.6	V	Pins 1, 18, 67, 83, 116, 132, 148, 165, 181
I _{CC3.3V} (16 MHz)	Supply Current Notebook Configuration	170	270	mA mA	(Note 1a) (Note 2)
I _{CC3.3V} (20 MHz)	Supply Current Notebook Configuration	190	325	mA mA	(Note 1b) (Note 2)
I _{CCS1_3.3V}	Supply Current with the STPCLK# Signal Asserted	37		mA	(Note 3)
I _{CCS2_3.3V}	Supply Current in Suspend Mode with Oscillators OFF and RTC Suspend Refresh ON	0.3		mA	(Note 4)
I _{CCS3_3.3V}	Supply Current in Suspend Mode with Oscillators OFF and Self Suspend Refresh ON	0.2	2	mA	(Note 5)

NOTES:

1a. Tested with V_{CC} = 3.6V, EFI = 32 MHz, ISACK2 = 16 MHz, 50 pF capacitive loads and no resistive load on the outputs.

1b. Tested with V_{CC} = 3.6V, EFI = 40 MHz, ISACK2 = 16 MHz, 50 pF capacitive loads and no resistive load on the outputs.

2. Notebook system configuration consists of 1 bank of 1 MB x 4 with 1 MB x 1 DRAMs for parity (2 MB total memory with Cache enabled. 25 pF capacitive loading on PI-bus control/status signals, 100 pF capacitive loading on the ISA bus signals and SYSClk).

3. STPCLK# Signal is active, all external Oscillators free running, no cycles on cache, memory or ISA Bus. Typically with V_{CC3.3V} = 3.3V, EFI = 40 MHz, ISACK2 = 16 MHz, 50 pF capacitive loads and no resistive loads on the outputs.

4. RTC Suspend Refresh Mode and all external oscillators turned OFF (in a fixed logic states), no cycles on cache, memory or ISA bus. CASx# are driven active (LOW) and RASx# are toggled during Suspend Mode. Typically with V_{CC3.3V} = 3.3V, 50 pF capacitive loads and no resistive load on the outputs.

5. Self Suspend Refresh Mode and all external oscillators turned OFF (in a fixed logic states), no cycles on cache, memory or ISA bus. CASx# and RASx# are driven active (LOW) during Suspend Mode. Typically with V_{CC3.3V} = 3.3V, 50 pF capacitive loads and no resistive load on the outputs.

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ADVANCE INFORMATION

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3.3.4 CPU I_{CC} SPECIFICATIONS**3.3.4.1 Determine I_{CC} with Slow Clock Control**

The CPU supports CPU clock division which reduces power consumption of the CPU core logic. The EFI clock input is similar to the CLK2 input found on the CPU. However, the internal CPUCLK signal in the CPU is not always one half of the frequency of the EFI input. An internal clock divider and synchronizer allows the CPU core clock to be slowed down and even stopped. However, additional internal logic such as the memory controller and cache controller continue to use half the EFI frequency. Therefore, when calculating the theoretical power consumption with CPU clock division it is important to recognize that a fixed constant (K) value of power is required by the CPU.

The value K is a constant for CPU since its core is powered by 3.3V and has nothing to do with ISA-Bus loading. Following is the equation for calculating CPU I_{CC} when the clock is divided.

$$I_{CC}(\text{divide clock}) = (I_{CC}(\text{normal clock}) - K) n + K$$

I_{CC} (normal clock) = The I_{CC} value calculated from the following section

n = The fractional value that the clock is divided (e.g. divide by 2 = 0.5)

K = 37 mA @ V_{CC} = 3.3V and EFI = 40 MHz.

3.3.4.2 Calculation of I_{CC} for Various System Configurations

Figure 3.3.1 illustrates the 5V power consumption in milli-Watts with respect to the capacitive loading on the ISA bus signals of the CPU. A set of two curves with V_{CC} at 3.3V and CPUCLK frequencies at 16 MHz and 20 MHz are plotted in Figure 3.3.2a. The power consumption with respect to load capacitance for the memory bus with a cache subsystem is illustrated in Figure 3.3.2b. To find the power (P in milli-Watts) of the CPU for the configuration of your system, use the following method.

1. Prepare a configuration list for your system including how many ISA-Bus connectors, how many memory chips will be used and whether a cache will be connected or not
2. From the curves in Figure 3.3.2a, use the total capacitive load of all of the CPU ISA signals to find the 5V power consumed by the ISA-Bus interface.
3. If a cache is connected to the CPU in your system, use Figure 3.3.2b to find memory bus power. If cache is not connected, use Figure 3.3.2a.
4. Find the internal power consumption of the CPU from Table 3.3-8 and the cache internal power and cache bus power from Tables 3.3-9 and 3.3-10.
5. For a system with no cache, add the memory bus interface power without cache and internal power. This gives the 3.3V power consumption of the CPU without cache.
6. For a system with cache, add the memory interface power with cache, the cache internal power. This gives the 3.3V power consumption of the CPU with cache.

Power Variations with Capacitive Loads at Various Voltages

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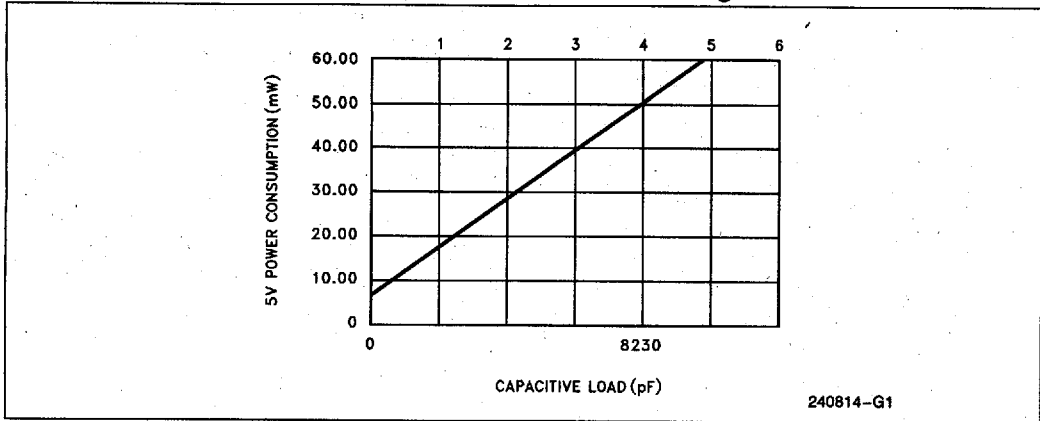


Figure 3.3.1. ISA Bus Power Consumption

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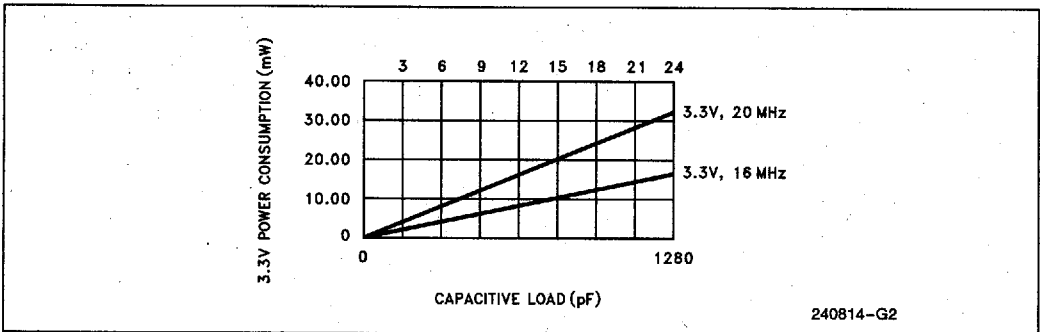


Figure 3.3.2a. Memory Bus without Cache

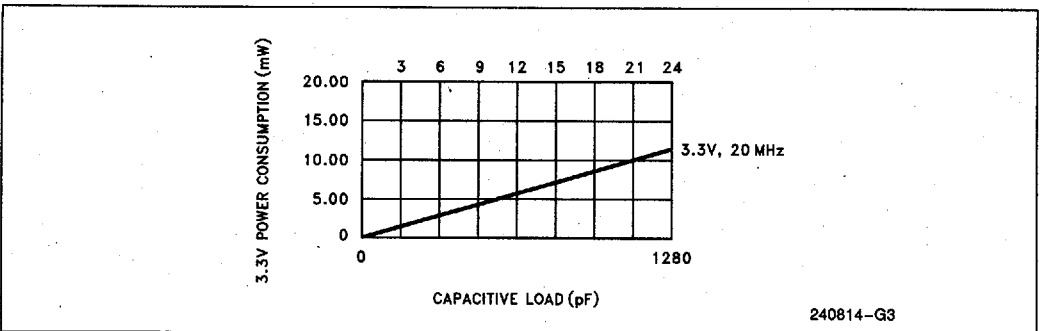


Figure 3.3.2b. Memory Bus with Cache

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Table 3.3-8. Internal Power at 3.3V

Frequency (MHz)	Power (mW)
16	475
20	585

Table 3.3-9. Cache Bus Power at 3.3V

Frequency (MHz)	Power (mW)
20	15

Table 3.3-10. Cache Internal Power at 3.3V

Frequency (MHz)	Power (mW)
20	82

NOTE:

Data provided in Figures 3.3.1 through 3.3.2b and in Tables 3.3-8 through 3.3-10 is based on engineering approximation and is given as an evaluation tool only.

As an example, the power consumed by the CPU when it is used in a 20 MHz system with 8 memory chips and 2 fully loaded ISA expansion slots will be calculated. The system voltages are assumed to be 5V and 3.3V.

From Figure 3.3.1, the 5V power consumed by the ISA expansion interface is found to be 28 mW (the total capacitance of all the pins of a fully loaded AT-bus slot is 2057.5 pF). For a system with no cache, the power consumed by the memory bus for 8 chips is about 12 mW from Figure 3.3.2a. The internal power at 20 MHz is 585 mW from Table 3.3-8. The power consumed by CPU is the sum of the power for the internal power (ISA and CPU core) and memory bus. The total power consumed by the CPU for this system is 625 mW.

For a system with cache, the ISA bus interface power is 28 mW as previously determined. The memory bus interface power determined from Figure 3.3.2b is found to be 4 mW. The internal power remains 585 mW. The cache bus power is read off from Table 3.3-9 to be 15 mW and the cache internal power from Table 3.3-10 is 82 mW. Hence, in this system, the CPU consumes a total of 714 mW.

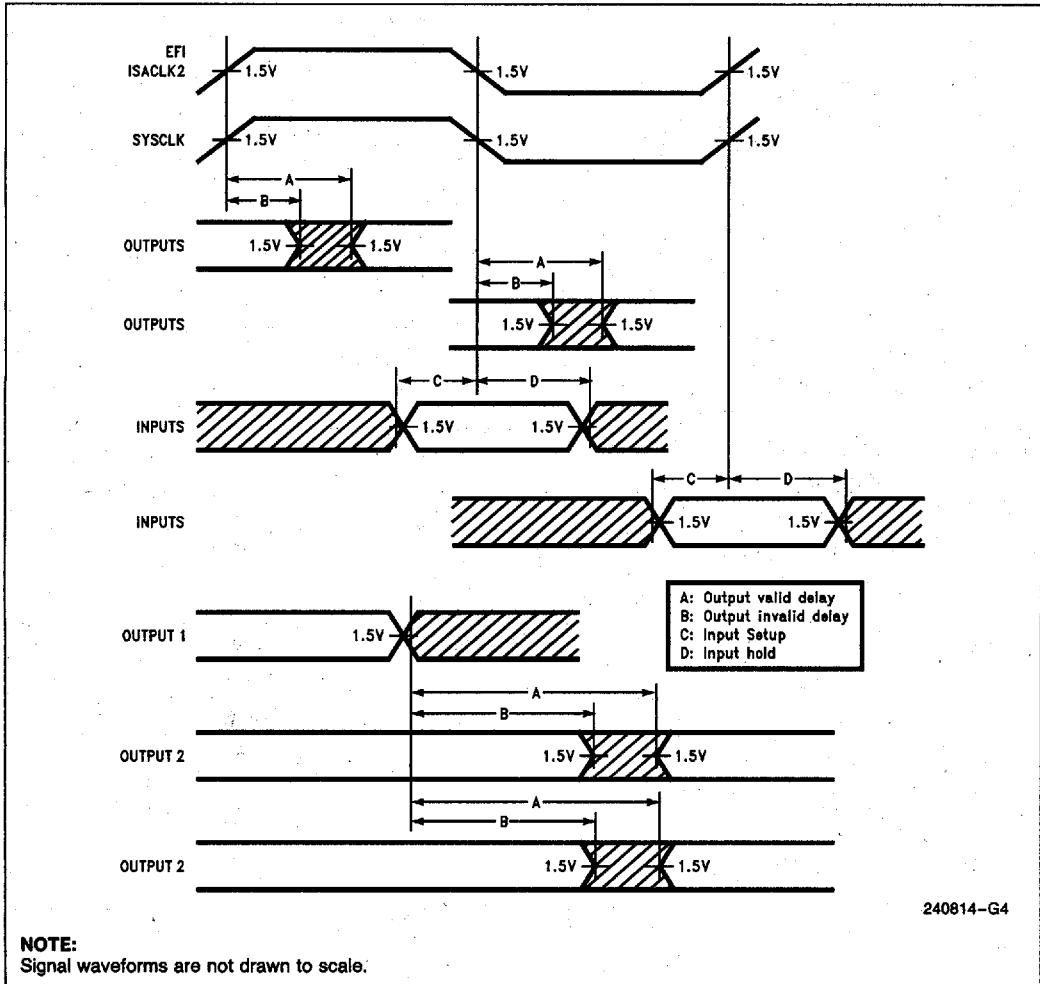
3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications

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A.C. SPECIFICATION DEFINITIONS

The A.C. specifications given in the tables of the following pages consist of output delays, input setup and hold requirements. They may be relative to a clock edge or another signal edge. ALL CPU clock related specifications reference EFI except ISA

bus timings which reference ISACK2. A.C. specifications are defined in Figure 3.4.1. All clock related specifications are tested at the voltage levels shown. Output specifications are derived from tested clock related timings.



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NOTE:
Signal waveforms are not drawn to scale.

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Figure 3.4.1. Drive Levels and Measurement Points for A.C. Specifications



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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)**Table 3.4-1. ISA-Bus Clock Timings**

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 201	ISACK2 Period	62.5		ns		3.5.2	
Ct 202	ISACK2 High Time at 1.65V	28	32.5	ns		3.5.2	
Ct 203	ISACK2 Low Time at 1.65V	28	32.5	ns		3.5.2	
Ct 204	ISACK2 Fall Time from 0.8 V _{CC3.3V} to 0.2 V _{CC3.3V}		7	ns		3.5.2	
Ct 205	ISACK2 Rise Time from 0.2 V _{CC3.3V} to 0.8 V _{CC3.3V}		7	ns		3.5.2	
Ct 206	ISACK2 to SYSCLK delay Falling to Rising Edge	2	50	ns	FR; SR	3.5.2	
Ct 207	ISACK2 to SYSCLK delay Falling to Falling Edge	2	50	ns	FF; SF	3.5.2	
Ct 211	SYSCLK Period	125		ns		3.5.2	
Ct 212	SYSCLK High Time at 1.5V	52		ns		3.5.2	
Ct 213	SYSCLK Low Time at 1.5V	57		ns		3.5.2	
Ct 214	SYSCLK Fall Time from (V _{CC5V-0.8V}) to 0.8V		10	ns		3.5.2	
Ct 215	SYSCLK Rise Time from 0.8V to (V _{CC5V-0.8V})		10	ns		3.5.2	
Ct 272a	A20GATE Setup to EFl (phi 1)	10		ns			
Ct 272b	A20GATE Hold Time	24		ns			

Table 3.4-2. ISA-Bus Timings

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 221	BALE Active Delay from Ts phi 2 Low		68	ns	SR	3.5.12	
Ct 222	BALE Inactive Delay from Tc phi 1 Low	5	68	ns	FF; SF	3.5.12	
Ct 223	LA17-23 Valid Delay from Ti or Tc phi 2 Low		69	ns	S	3.5.12	
Ct 224	LA17-23 Invalid Delay from Tc phi 2 Low	0		ns	F	3.5.12	
Ct 225	SA1-19 Valid Delay from Ts phi 1 Low		93	ns	S	3.5.12	
Ct 226	SA0-19, SBHE#, LA17-23 Valid Setup to phi 1 Low (External Master)	18		ns		3.5.27	
Ct 227	SA1-19 Invalid Delay from Ts or Ti phi 1 Low	0		ns	F	3.5.12	

3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)
Table 3.4-2. ISA-Bus Timings (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 228	SA0, SBHE# Valid Delay from Ts phi 2 Low		71	ns	SF	3.5.12	
Ct 229	SA0, SBHE# Invalid Delay from Ts or Ti phi 2 Low	0	71	ns	FR; SR	3.5.12	
Ct 230	MEMR#, MEMW# Active from Tc phi 1 Low (16-Bit MEMR# / MEMW#)	7	55	ns	FF; SF	3.5.18	
Ct 231	Command Active Setup to phi 1 Low (External Master)	18		ns		3.5.27	
Ct 232	HALT# Valid Delay or Invalid Delay from phi 1 Low	0	53	ns	SF	3.5.24a	
Ct 233	Command Inactive to Float Delay from Ti phi 1 Low (External Master)		66	ns	S	3.5.27	
Ct 234	Command Active Delay from Tc phi 2 Low (IOR# / IOW# 8, 16-Bit, MEMR# / MEMW# 8-Bit)	7	55	ns	FF; SF	3.5.12	
Ct 235	Command Inactive Delay from Teoc phi 1 Low (MEMR# / MEMW#, IOR# / IOW#)	7	65	ns	FR; SR	3.5.12	
Ct 238	MEMCS16# Setup to Tc phi 1 Low	2		ns		3.5.13	
Ct 239	MEMCS16# Hold from Tc phi 1 Low	35		ns		3.5.13	
Ct 240	IOCS16# Setup to Tc phi 2 Low	45		ns		3.5.21	
Ct 241	IOCS16# Hold from Teoc phi 1 Low	21		ns		3.5.21	
Ct 242	ZEROWS# Setup to Tc or Ti phi 1 Low	38		ns		3.5.15	
Ct 244	ZEROWS# Hold from Tc or Ti phi 1 Low	22		ns		3.5.15	
Ct 245	MEMCS16# Active Delay from Valid Address (External Master Cycles)		80	ns	SF	3.5.28b	
Ct 246	SD0-15 Valid Setup to IOR# / MEMR#, INTA# Inactive	63		ns		3.5.13	
Ct 247	SD0-15 Hold from IOR# / MEMR#, INTA# Inactive	0		ns		3.5.12	
Ct 248	SD0-7 Valid Delay from Ts phi 2 Low	38	114	ns	F; S	3.5.12	
Ct 249	SD8-15 Valid Delay from Ts phi 2 Low	38	114	ns	F; S		
Ct 250	SD0-15 Invalid Delay from Teoc phi 2 Low	5		ns		3.5.12	
Ct 251	IOCHRDY Setup to Tc phi 1 Low (8-bit I/O or Mem)	6		ns		3.5.14	
Ct 251a	IOCHRDY Inactive Setup to Tc phi 2 Low (16-Bit I/O or Mem)	5		ns		3.5.20	
Ct 252	IOCHRDY Hold from Tc phi 1 Low (8-Bit or 16-Bit)	26		ns		3.5.14	

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**3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)**

Table 3.4-2. ISA-Bus Timings (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 259	INTA# Active Delay from Tc phi 2 Low		58	ns	SF	3.5.23	
Ct 260	INTA# Inactive Delay from Teoc phi 1 Low		64	ns	SR	3.5.23	
Ct 261	HRQ Setup to Tc or Ti phi 2 Low	15		ns		3.5.24	
Ct 262	HRQ Hold from Th phi 2 Low	24		ns		3.5.24	
Ct 263	HLDA Active Delay from Th phi 1 Low	0	57	ns	FR; SR	3.5.24	
Ct 264	HLDA Inactive Delay from Th phi 1 Low	7	57	ns	FF; SF	3.5.24	
Ct 265	DMA8/16# Setup to Th phi 2 Low	15		ns		3.5.24	
Ct 266	MASTER# Setup to Th phi 2 Low	15		ns		3.5.26	
Ct 267	REFREQ Setup to Ti or Tc phi 2 Low	15		ns		3.5.25	
Ct 268	VGACS# Active Delay from LA[23:17]		58		SF	3.5.10	
Ct 269	VGACS# Inactive Delay from LA[23:17]		58	ns	SR	3.5.10	
Ct 269a	VGACS# Active Delay from Tc phi 2 Low		64	ns	SF	3.5.18	
Ct 269b	VGACS# Inactive Delay from Tc phi 2 Low		64	ns	SR	3.5.18	
Ct 270	ROMCS0#/CMUX14# Active Delay from Ts phi 2 Low		51	ns	SF	3.5.11	
Ct 271	ROMCS0#/CMUX14# Inactive Delay from Ts phi 2 Low	5		ns	FR	3.5.11	
Ct 272	ROMCS0#/CMUX14# Active Delay from Address		67	ns	SF	3.5.9	
Ct 273	ROMCS0#/CMUX14# Inactive Delay from Address		65	ns	SR	3.5.9	
Ct 274	SMRAMCS# Active Delay from Ts phi 2 Low	5	70	ns	FF; SF	3.5.11	
Ct 275	SMRAMCS# Inactive Delay from Ts or Ti phi 2 Low	5	70	ns	FR; SR	3.5.11	
Ct 275a	TURBO Setup	16		ns			



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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-2. ISA-Bus Timings (Continued)

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Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 276	SD15-0 Valid Setup to IOCHRDY Asserted (External Master)	15		ns	FR; F	3.5.28b	
Ct 277	SD15-0 Data Invalid Delay from MEMR# Inactive (External Master)	0		ns	F	3.5.28b	
Ct 278	SD15-0 Data Invalid Delay from IOR# Inactive (External Master)	0		ns	F	3.5.28a	
Ct 279	SD15-0 Data Setup to MEMW# Active (External Master)	-45		ns		3.5.28b	
Ct 280	SD15-0 Data Hold from MEMW# Inactive (External Master)	0		ns		3.5.28b	
Ct 281	SD15-0 Data Setup to IOW# Active (External Master)	3		ns		3.5.28a	
Ct 282	BALE Active Delay from Th phi 1 Low (External Master)		77	ns	SR	3.5.26	
Ct 283	BALE Inactive from Th phi 1 Low (External Master)		77		SF	3.5.26	
Ct 284	LA23-17, SA19-0, SBHE# Float to Invalid Delay from Th phi 2 (External Master)		64	ns	S	3.5.26	
Ct 285	LA23-17, SA19-0, SBHE# Invalid to Float Delay from Th phi 1 (External Master)		73	ns	S	3.5.26	
Ct 286	SA19-17 Delay from LA19-17 (DMA Cycle)	4	46	ns	F; S	3.5.24	
Ct 287	Command Float to Inactive from Th phi 2 Low (External Master)		58	ns	S	3.5.24	
Ct 288	Address Setup to Command Active (External Master)	28		ns		3.5.28a	
Ct 289	SA15-0 Hold after IOR# or IOW# Inactive (External Master)	15				3.5.28a	
Ct 290	IOCS16# Active Delay from Valid Address (External Master)		63	ns	SF	3.5.28a	
Ct 291	SD15-0 Valid Delay from IOR# Active (External Master Read from CPU I/O Ports)		80	ns	S	3.5.28a	
Ct 293	SD15-0 Hold After IOW# Inactive (External Master)	15		ns		3.5.28a	
Ct 294	Byte Swap Delay (External Master)	7	72	ns	F; S	3.5.26	
Ct 295	IOCHRDY Invalid from Command Active (External Master)		44	ns	SF	3.5.28b	
Ct 296	IOCHRDY Active from phi 1 Low (External Master)		85	ns	SR	3.5.28b	
Ct 297	MEMR#, MEMW# Inactive from IOCHRDY	0		ns	SR; FR	3.5.28b	
Ct 298	IOCS16# Inactive from Valid Address (External Master)		96	ns	SR	3.5.28a	
Ct 299	IOCS16#/MEMCS16#/MASTER# Float to High (External Master)		78	ns			

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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

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16 MHz Timings**Table 3.4-3. EFI Clock Timings: 32 MHz CPU @ 16 MHz**

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 101	EFI Period	31.25		ns		3.5.1	
Ct 102a	EFI High Time at 1.65V	12		ns			
Ct 102b	EFI High Time at 0.8 V _{CC3.3V}	7					
Ct 103a	EFI Low Time at 1.65V	12		ns			
Ct 103b	EFI Low Time at 0.2 V _{CC3.3V}	7					
Ct 104	EFI Fall Time from 0.8 V _{CC3.3V} to 0.2 V _{CC3.3V}		5	ns			
Ct 105	EFI Rise Time from 0.2 V _{CC3.3V} to 0.8V _{CC3.3V}		5	ns			

Table 3.4-4. General Timings: 16 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 111	PWRGOOD Minimum Pulse Width	4		EFI			
Ct 111a	PWRGOOD Setup to EFI	2		ns			
Ct 111b	PWRGOOD Hold Time	20		ns			
Ct 112	CPURESET Minimum Pulse Width	4		EFI			
Ct 112a	CPURESET Setup to EFI	2		ns			
Ct 112b	CPURESET Hold Time	20		ns			
Ct 113a	STPCLK# Setup to EFI	10		ns			
Ct 113b	STPCLK# Hold Time	24		ns			
Ct 114a	SUS__STAT# Setup to EFI	20		ns			
Ct 114b	SUS__STAT# Hold Time	15		ns			
Ct 115	ONCE# Minimum Pulse Width	35		ns			
Ct 115a	ONCE# Setup to EFI	20		ns			
Ct 115b	ONCE# Hold Time	15		ns			
Ct 116a	SMI# Setup to EFI	15		ns			
Ct 116b	SMI# Hold Time	24		ns			
Ct 117a	INTR Setup to EFI	15		ns			
Ct 117b	INTR Hold Time	23		ns			
Ct 118a	NMI Setup to EFI	11		ns			
Ct 118b	NMI Hold Time	16		ns			

3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-5. PI-Bus Timings: 16 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 301	Min. Chip Select and Command Setup to PSTART# Active	10		ns	SF, SF	3.5.7	
Ct 302	Min. Chip Select and Command Hold from PSTART# Active	58		ns	FF, SR		
Ct 304	Min. Read Data Setup Time to PCMD# Inactive	48		ns			
Ct 305	Min. Read Data Hold Time from PCMD# Inactive	12		ns			
Ct 307	Maximum Write Data Valid Delay from PSTART# Active		64	ns	SF, S		
Ct 308	Min. Write Data Invalid Delay from PSTART# Inactive	31		ns	FF, F		
Ct 309	Min. Address Setup Time to PSTART# Active	32.5		ns	SF, S		
Ct 310	Min. Address Hold Time from PSTART# Active	62		ns	FF, F		
Ct 311	PSTART# Pulse Width	55		ns			
Ct 312	Min. Delay from PSTART# Active to PCMD# Active	50		ns	SF, SF		
Ct 313	Min. Delay from PRDY# Active to PCMD# Inactive	37.5		ns	FR		
Ct 314	Min. Delay from PCMD# Inactive to PSTART# Active	0		ns	FR, FF		
Ct 315	PRDY# Hold from PCMD# Inactive	0	40	ns			

Table 3.4-6. External Master Timings: SYSClk at 8 MHz (Slave CPU)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 321	PW/R# Valid Delay		55	ns	SF	3.5.8	
Ct 321	PM/IO# Valid Delay		55	ns	SF		
Ct 321	VGACS# Valid Delay		55	ns	SF		
Ct 325	PSTART# Valid Delay		54	ns	SF		
Ct 326	PCMD# Valid Delay		55	ns	SF		
Ct 327a	PRDY# Setup	5		ns			
Ct 327b	PRDY# Hold	25		ns			

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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)**Table 3.4-7. Math Coprocessor Timings: NPXCLK 32 MHz Math Coprocessor @ 16 MHz**

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 421	CA2 Valid Delay (MCP Cyc)	2	36	ns	FR, F; SR, S	3.5.3	
Ct 422	NPXADS# Valid Delay	4	40	ns	FR, FF; SR, SF	3.5.3	
Ct 423	NPXW/R# Valid Delay	4	40	ns	FR, FF; SR, SF	3.5.3	
Ct 424	CD Valid Delay (MCP Cyc)	2	50	ns	FR, F; SR, S	3.5.4	
Ct 425a	NPXRDY# Setup	22		ns		3.5.5	
Ct 425b	NPXRDY# Hold	3		ns		3.5.5	
Ct 426a	BUSY#, PEREQ, ERROR# Setup to NPXCLK phi 1 High	26		ns		3.5.5	
Ct 426b	BUSY#, PEREQ, ERROR# Hold from NPXCLK phi 1 High	5		ns		3.5.5	
Ct 427a	CD Setup (MCP Cycle)	12		ns		3.5.3	
Ct 427b	CD Hold (MCP Cycle)	6		ns		3.5.3	
Ct 441	NPXCLK Period	31.25		ns		3.5.1	
Ct 442a	NPXCLK High Time at 1.65V	11		ns		3.5.1	
Ct 442b	NPXCLK High Time at 0.8 V _{CC3.3V}	6		ns		3.5.1	
Ct 443a	NPXCLK Low Time at 1.65V	11		ns		3.5.1	
Ct 443b	NPXCLK Low Time at 0.2 V _{CC3.3V}	6		ns		3.5.1	
Ct 444	NPXCLK Fall Time from 0.8 V _{CC3.3V} to 0.2 V _{CC3.3V}		6	ns		3.5.1	
Ct 445	NPXCLK Rise Time from 0.2 V _{CC3.3V} to 0.8 V _{CC3.3V}		6	ns		3.5.1	
Ct 446	NPXCLK to NPXRESET Inactive Delay	1	21	ns	FR, FF; SR, SF	3.5.1	



3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-8. DRAM Mode Timings: 16 MHz

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes	
Lt1601	tRAC	Access Time from RAS# Active	80		ns		Figure 3.5.29	F1	
Lt1602		Access Time from RAS# Active	100		ns			F2	
Lt1603		Access Time from RAS# Active	100		ns			P1	
Lt1604	tCAC	Access Time from CAS# Active	35		ns			F1	
Lt1605		Access Time from CAS# Active	35		ns			F2	
Lt1606		Access Time from CAS# Active	55		ns			P1	
Lt1607	tASR	Row Addr Setup to RAS# Active	0		ns	SF, S		F1	CR = Max, CT = Max
Lt1608		Row Addr Setup to RAS# Active	0		ns			F2	
Lt1609		Row Addr Setup to RAS# Active	0		ns			P1	
Lt1610	tRAH	Row Addr Hold from RAS# Active	15		ns	SF, S		F1	CR = Max, CT = Max
Lt1611		Row Addr Hold from RAS# Active	20		ns			P2	
Lt1612		Row Addr Hold from RAS# Active	20		ns			P1	
Lt1613	tASC	Col Addr Setup to CAS# Active	0, 10*		ns	SF, S		F1	CR = Max, CT = Max
Lt1614		Col Addr Setup to CAS# Active	0, 20*		ns			F2	
Lt1615		Col Addr Setup to CAS# Active	0		ns			P1	
Lt1616	tCAH	Col Addr Hold from CAS# Active	20		ns	SF, S		F1	CR = Max, CT = Max
Lt1617		Col Addr Hold from CAS# Active	20		ns		F2		
Lt1618		Col Addr Hold from CAS# Active	25		ns		P1		
Lt1619	tRCD	RAS# to CAS# Delay	35		ns	SF, SF	F1	CR = Max, CT = Max	
Lt1620		RAS# to CAS# Delay	35		ns		F2		
Lt1621		RAS# to CAS# Delay	55		ns		P1		
Lt1622	tCSH	CAS# Hold Time from RAS# Active	80		ns	SF, SR	F1	CR = Max, CT = Max	
Lt1623		CAS# Hold Time from RAS# Active	100		ns		F2		
Lt1624		CAS# Hold Time from RAS# Active	100		ns		P1		
Lt1625	tRSH	RAS# Hold Time from CAS# Active	35		ns	SF, SR	F1	CR = Max, CT = Max	
Lt1626		RAS# Hold Time from CAS# Active	35		ns		F2		
Lt1627		RAS# Hold Time from CAS# Active	55		ns		P1		
Lt1628	tRPC	RAS# Precharge to CAS# Active	0		ns		F1		
Lt1629		RAS# Precharge to CAS# Active	0		ns		F2		
Lt1630		RAS# Precharge to CAS# Active	0		ns		P1		
Lt1631	tCRP	CAS# Precharge to RAS# Active	5		ns		F1		
Lt1632		CAS# Precharge to RAS# Active	10		ns		F2		
Lt1633		CAS# Precharge to RAS# Active	10		ns		P1		

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NOTE:

*Applicable only in page mode.

3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-8. DRAM Mode Timings: 16 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes	
Lt1634		RAS# Active Pulse Width	80		ns		Figure 3.5.29	F1	
Lt1635	tRAS	RAS# Active Pulse Width	100		ns			F2	
Lt1636		RAS# Active Pulse Width	100		ns			P1	
Lt1637		CAS# Active Pulse Width	35		ns			F1	
Lt1638	tCAS	CAS# Active Pulse Width	35		ns			F2	
Lt1639		CAS# Active Pulse Width	55		ns			P1	
Lt1640		RAS# Precharge Pulse Width	70		ns			F1	
Lt1641	tRP	RAS# Precharge Pulse Width	90		ns			F2	
Lt1642		RAS# Precharge Pulse Width	90		ns			P1	
Lt1643		CAS# Precharge Pulse Width	25		ns			F1	
Lt1644	tCP	CAS# Precharge Pulse Width	25		ns			F2	
Lt1645		CAS# Precharge Pulse Width	45		ns			P1	
Lt1646		Read Cmd Setup to CAS# Active	0		ns	SF, SR		F1	CR = Max, CT = Max
Lt1647	tRCS	Read Cmd Setup to CAS# Active	0		ns			F2	
Lt1648		Read Cmd Setup to CAS# Active	0		ns			P1	
Lt1649		Read Cmd Hold from CAS# Inact.	0		ns	SF, SR		F1	CR = Max, CT = Max
Lt1650	tRCH	Read Cmd Hold from CAS# Inact.	0		ns			F2	
Lt1651		Read Cmd Hold from CAS# Inact.	0		ns			P1	
Lt1652		Write Cmd Setup to CAS# Active	0		ns	SF, SF		F1	CR = Max, CT = Max
Lt1653	tWCS	Write Cmd Setup to CAS# Active	0		ns			F2	
Lt1654		Write Cmd Setup to CAS# Active	0		ns				
Lt1655		Write Cmd Hold from CAS# Act.	20		ns	SF, SR		F1	CR = Max, CT = Max
Lt1656	tWCH	Write Cmd Hold from CAS# Act.	20		ns			F2	
Lt1657		Write Cmd Hold from CAS# Act.	20		ns			P1	
Lt1658		Write Data Setup to CAS# Active	0		ns	SF, S		F1	CR = Max, CT = Max
Lt1659	tWDS	Write Data Setup to CAS# Active	0		ns			F2	
Lt1660		Write Data Setup to CAS# Active	0		ns			P1	
Lt1661		Write Data Hold from CAS# Active	20		ns	SF, S		F1	CR = Max, CT = Max
Lt1662	tWDH	Write Data Hold from CAS# Active	20		ns		F2		
Lt1663		Write Data Hold from CAS# Active	20		ns		P1		
Lt1664		Read Parity Valid from CAS# Act.	35		ns	SF, S	F1	CR = Max, CT = Max	
Lt1665	tRPV	Read Parity Valid from CAS# Act.	35		ns		F2		
Lt1666		Read Parity Valid from CAS# Act.	55		ns		P1		

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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-8. DRAM Mode Timings: 16 MHz (Continued)

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Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Lt1667	tWPS	Write Parity Setup to CAS# Active	0		ns	SF, SF	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1668		Write Parity Setup to CAS# Active	0		ns			F2
Lt1669		Write Parity Setup to CAS# Active	0		ns			P1
Lt1670	tWPH	Write Parity Hold from CAS# Act.	20		ns	SF, SR	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1671		Write Parity Hold from CAS# Act.	20		ns			F2
Lt1672		Write Parity Hold from CAS# Act.	20		ns			P1
Lt1673	tCSR	CAS# Setup to RAS# Active (CBR Refresh)	10		ns	SF, SF	Figure 3.5.31	F1
Lt1674		CAS# Setup to RAS# Active (CBR Refresh)	10		ns			F2 CR = Max, CT = Max
Lt1675		CAS# Setup to RAS# Active (CBR Refresh)	10		ns			P1
Lt1676	tCHR	CAS# Hold from RAS# Active (CBR Refresh)	20		ns	FF, FR	Figure 3.5.31	F1
Lt1677		CAS# Hold from RAS# Active (CBR Refresh)	20		ns			F2 CR = Min, CT = Min
Lt1678		CAS# Hold from RAS# Active (CBR Refresh)	20		ns			P1
Lt1679	tWSR	Read Cmd Setup to RAS# Act. (CBR Refresh)	20		ns	SF, SF	Figure 3.5.30	F1
Lt1680		Read Cmd Setup to RAS# Act. (CBR Refresh)	20		ns			F2 CR = Min, CT = Max
Lt1681		Read Cmd Setup to RAS# Act. (CBR Refresh)	20		ns			P1
Lt1682	tWHR	Read Cmd HOLD from RAS# Act. (CBR Refresh)	30		ns	FF, FR	Figure 3.5.30	F1
Lt1683		Read Cmd HOLD from RAS# Act. (CBR Refresh)	30		ns			F2 CR = Min, CT = Min
Lt1684		Read Cmd HOLD from RAS# Act. (CBR Refresh)	30		ns			P1



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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)**Table 3.4-8. DRAM Mode Timings: 16 MHz (Continued)**

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Lt1685	tRASS	RAS# Active Pulse Width (CBR Self Refresh)	100K		ns		Figure 3.5.30	F1
Lt1686		RAS# Active Pulse Width (CBR Self Refresh)	100K		ns			F2
Lt1687		RAS# Active Pulse Width (CBR Self Refresh)	100K		ns			P1
Lt1688	tCHS	CAS# Hold Time from RAS# (CBR Self Refresh)	-50		ns			F1
Lt1689		CAS# Hold Time from RAS# (CBR Self Refresh)	-60		ns			F2
Lt1690		CAS# Hold Time from RAS# (CBR Self Refresh)	-70		ns			P1
Lt1691	tRPS	RAS# Precharge Pulse Width (CBR Self Refresh)	150		ns			F1
Lt1692		RAS# Precharge Pulse Width (CBR Self Refresh)	170		ns			F2
Lt1693		RAS# Precharge Pulse Width (CBR Self Refresh)	200		ns			P1
The Following Pin Timing Parameters Are Independent of DRAM Modes F1, F2, P1								
Lt1694	tPED	PERR# Delay from SYSCLK		38	ns	SR, SF	Figure 3.5.33	CR = Max, CT = Max
Lt1695	tRDS	RAS# Delay from SYSCLK		55	ns	SF	Figure 3.5.32	
Lt1696	tADS	Address Delay from SYSCLK		65	ns	S	Figure 3.5.32	

3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

20 MHz Timings

Table 3.4-9. EFI Clock Timings: 40 MHz CPU @20 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 101	EFI Period	25		ns		3.5.1	
Ct 102a	EFI High Time at 1.65V	10		ns		3.5.1	
Ct 102b	EFI High Time at 0.8V _{CC3.3V}	5		ns		3.5.1	
Ct 103a	EFI Low Time at 1.65V	10		ns		3.5.1	
Ct 104b	EFI Low Time at 0.2V _{CC3.3V}	5		ns		3.5.1	
Ct 104	EFI Fall Time from 0.8V _{CC3.3V} to 0.2V _{CC3.3V}		5	ns		3.5.1	
Ct 105	EFI Rise Time from 0.2V _{CC3.3V} to 0.8V _{CC3.3V}		5	ns		3.5.1	

Table 3.4-10. General Timings: 20 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 111	PWRGOOD Minimum Pulse Width	4		EFI			
Ct 111a	PWRGOOD Setup to EFI	2		ns			
Ct 111b	PWRGOOD Hold Time	20		ns			
Ct 112	CPURESET Minimum Pulse Width	4		EFI			
Ct 112a	CPURESET Setup to EFI	2		ns			
Ct 112b	CPURESET Hold Time	20		ns			
Ct 113a	STPCLK# Setup to EFI	10		ns			
Ct 113b	STPCLK# Hold Time	24		ns			
Ct 114a	SUS_STAT# Setup to EFI	20		ns			
Ct 114b	SUS_STAT# Hold Time	15		ns			
Ct 115	ONCE# Minimum Pulse Width	35		ns			
Ct 115a	ONCE# Setup to EFI	20		ns			
Ct 115b	ONCE# Hold Time	15		ns			
Ct 116a	SMI Setup to EFI	15		ns			
Ct 116b	SMI Hold Time	24		ns			
Ct 117a	INTR Setup to EFI	15		ns			
Ct 117b	INTR Hold Time	23		ns			
Ct 118a	NMI Setup to EFI	11		ns			
Ct 118b	NMI Hold Time	16		ns			

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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)
Table 3.4-11. PI-Bus Timings: 20 MHz

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Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 301	Min. Chip Select and Command Setup to PSTART# Active	10		ns	SF, SF	3.5.7	
Ct 302	Min. Chip Select and Command Hold from PSTART# Active	48		ns	FF, SR	3.5.7	
Ct 304	Min. Read Data Setup Time to PCMD# Inactive	48		ns		3.5.7	
Ct 305	Min. Read Data Hold Time from PCMD# Inactive	12		ns		3.5.7	
Ct 307	Maximum Write Data Valid Delay from PSTART# Active		57	ns	SF, S	3.5.7	
Ct 308	Min. Write Data Invalid Delay from PSTART# Inactive	25		ns	FF, F	3.5.7	
Ct 309	Min. Address Setup Time to PSTART# Active	20		ns	SF, S	3.5.7	
Ct 310	Min. Address Hold Time from PSTART# Active	50		ns	FF, F	3.5.7	
Ct 311	PSTART# Pulse Width	45		ns		3.5.7	
Ct 312	Min. Delay from PSTART# Active to PCMD# Active	40		ns	SF, SF	3.5.7	
Ct 313	Min. Delay from PRDY# Active to PCMD# Inactive	32		ns	FR	3.5.7	
Ct 314	Min. Delay from PCMD# Inactive to PSTART# Active	0		ns	FR, FF	3.5.7	
Ct 315	PRDY# Hold from PCMD# Inactive	0	40	ns		3.5.7	

Table 3.4-12. External Master Timings: SYSCLK at 8 MHz (Slave CPU)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 321	PW/R# Valid Delay		55	ns	SF	3.5.8	
Ct 321	PM/IO# Valid Delay		55	ns	SF	3.5.8	
Ct 321	VGACS# Valid Delay		55	ns	SF	3.5.8	
Ct 325	PSTART# Valid Delay		54	ns	SF	3.5.8	
Ct 326	PCMD# Valid Delay		55	ns	SF	3.5.8	
Ct 327a	PRDY# Setup	5		ns		3.5.8	
Ct 327b	PRDY# Hold	25		ns		3.5.8	



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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-13. Cache Bus Timings: 20 MHz

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Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 401	CA Valid Delay to CD Valid		25	ns		3.5.6	
Ct 402	COE# Pulse Width	45		ns	SF, SR	3.5.6	
Ct 403	CCSH#, CCSL# Active to CD Valid		25	ns		3.5.6	
Ct 404a	COE# Active to CD Valid		12	ns		3.5.6	
Ct 404b	CD Hold from COE# Inactive	1		ns		3.5.6	
Ct 405	CA Valid Setup to CWE# Active	1		ns	FF, F	3.5.6	CR = Min, CT = Max
Ct 406	CWE# Active Width	25		ns	SR, SR	3.5.6	
Ct 407	CD Setup to CWE# Inactive	15		ns	SR, S	3.5.6	CR = Min, CT = Max
Ct 408	CD Hold from CWE# Inactive	0		ns	SR, S	3.5.6	CR = Max, CT = Max
Ct 409	CA Hold to CWE# Inactive	0		ns	FR, F	3.5.6	CR = Max, CT = Min

Table 3.4-14. Math Coprocessor Timings: NPXCLK 40 MHz Math Coprocessor @20 MHz

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 421	CA2 Valid Delay (NPX Cyc)	2	30	ns	FR, F; SR, S	3.5.3	
Ct 422	NPXADS# Valid Delay	4	35	ns	FR, FF; SR, SF	3.5.3	
Ct 423	NPXW/R# Valid Delay	4	35	ns	FR, FF, SR, SF	3.5.3	
Ct 424	CD15-0 Valid Delay (NPX Cyc)	2	50	ns	FR, F; SR, S	3.5.4	
Ct 425a	NPXRDY# Setup	18		ns		3.5.5	
Ct 425b	NPXRDY# Hold	3		ns		3.5.5	
Ct 426a	BUSY#, PEREQ, ERROR# Setup to NPXCLK phi 1 High	20		ns		3.5.5	
Ct 426b	BUSY#, PEREQ, ERROR# Hold from NPXCLK phi 1 High	5		ns		3.5.5	
Ct 427a	CD15-0 Setup (NPX Cycle)	12		ns		3.5.3	
Ct 427b	CD15-0 Hold (NPX Cycle)	6		ns		3.5.3	

**3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)****Table 3.4-14. Math Coprocessor Timings: NPXCLK 40 MHz Math Coprocessor @20 MHz (Continued)**

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Ct 441	NPXCLK Period	25		ns		3.5.1	
Ct 442a	NPXCLK High Time at 1.65V	9		ns		3.5.1	
Ct 442b	NPXCLK High Time at 0.8 V _{CC3.3V}	4		ns		3.5.1	
Ct 443a	NPXCLK Low Time at 1.65V	9		ns		3.5.1	
Ct 443b	NPXCLK Low Time at 0.2 V _{CC3.3V}	4		ns		3.5.1	
Ct 444	NPXCLK Fall Time from 0.8 V _{CC3.3V} to 0.2 V _{CC3.3V}		6	ns		3.5.1	
Ct 445	NPXCLK Rise Time from 0.2 V _{CC3.3V} to 0.8 V _{CC3.3V}		6	ns		3.5.1	
Ct 446	NPXCLK to NPXRESET Inactive Delay	1	17	ns	FR, FF, SR, SF	3.5.1	

Table 3.4-15. DRAM Mode Timings: 20 MHz

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Lt1601	tRAC	Access Time from RAS# Active	60		ns		Figure 3.5.29	F1
Lt1602		Access Time from RAS# Active	80		ns			F2
Lt1603		Access Time from RAS# Active	100		ns			P1
Lt1604	tCAC	Access Time from CAS# Active	20		ns			F1
Lt1605		Access Time from CAS# Active	20		ns			F2
Lt1606		Access Time from CAS# Active	40		ns			P1
Lt1607	tASR	Row Addr Setup to RAS# Active	0		ns	SF, S		F1
Lt1608		Row Addr Setup to RAS# Active	0		ns			F2
Lt1609		Row Addr Setup to RAS# Active	0		ns			P1
Lt1610	tRAH	Row Addr Hold from RAS# Active	12		ns	SF, S		F1
Lt1611		Row Addr Hold from RAS# Active	15		ns			F2
Lt1612		Row Addr Hold from RAS# Active	15		ns			P1
Lt1613	tASC	Col Addr Setup to CAS# Active	0, 10*		ns	SF, S		F1
Lt1614		Col Addr Setup to CAS# Active	0, 18*		ns			F2
Lt1615		Col Addr Setup to CAS# Active	0, 15*		ns			P1
Lt1616	tCAH	Col Addr Hold from CAS# Active	15		ns	SF, S		F1
Lt1617		Col Addr Hold from CAS# Active	15		ns			F2
Lt1618		Col Addr Hold from CAS# Active	20		ns			P1

NOTES:

*Applicable only in page mode.

**For F2 mode, it has been assumed that DRAM will derate its specifications, t_{ASC}, by 2 ns because CPU will only have 47 pF on DRAM's data lines instead of 100 pF.



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3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-15. DRAM Mode Timings: 20 MHz (Continued)

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Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Lt1619	tRCD	RAS# to CAS# Delay	20		ns	SF, SF	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1620		RAS# to CAS# Delay	20		ns			F2
Lt1621		RAS# to CAS# Delay	40		ns			P1
Lt1622	tCSH	CAS# Hold Time from RAS# Active	60		ns	SF, SR	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1623		CAS# Hold Time from RAS# Active	80		ns			F2
Lt1624		CAS# Hold Time from RAS# Active	100		ns			P1
Lt1625	tRSH	RAS# Hold Time from CAS# Active	20		ns	SF, SR	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1626		RAS# Hold Time from CAS# Active	20		ns			F2
Lt1627		RAS# Hold Time from CAS# Active	40		ns			P1
Lt1628	tRPC	RAS# Precharge to CAS# Active	0		ns		Figure 3.5.29	F1
Lt1629		RAS# Precharge to CAS# Active	0		ns			F2
Lt1630		RAS# Precharge to CAS# Active	0		ns			P1
Lt1631	tCRP	CAS# Precharge to RAS# Active	5		ns		Figure 3.5.29	F1
Lt1632		CAS# Precharge to RAS# Active	5		ns			F2
Lt1633		CAS# Precharge to RAS# Active	10		ns			P1
Lt1634	tRAS	RAS# Active Pulse Width	60		ns		Figure 3.5.29	F1
Lt1635		RAS# Active Pulse Width	80		ns			F2
Lt1636		RAS# Active Pulse Width	100		ns			P1
Lt1637	tCAS	CAS# Active Pulse Width	20		ns		Figure 3.5.29	F1
Lt1638		CAS# Active Pulse Width	20		ns			F2
Lt1639		CAS# Active Pulse Width	40		ns			P1
Lt1640	tRP	RAS# Precharge Pulse Width	50		ns		Figure 3.5.29	F1
Lt1641		RAS# Precharge Pulse Width	80		ns			F2
Lt1642		RAS# Precharge Pulse Width	80		ns			P1
Lt1643	tCP	CAS# Precharge Pulse Width	15		ns		Figure 3.5.29	F1
Lt1644		CAS# Precharge Pulse Width	15		ns			F2
Lt1645		CAS# Precharge Pulse Width	30		ns			P1
Lt1646	tRCS	Read Cmd Setup to CAS# Active	0		ns	SF, SR	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1647		Read Cmd Setup to CAS# Active	0		ns			F2
Lt1648		Read Cmd Setup to CAS# Active	0		ns			P1
Lt1649	tRCH	Read Cmd Hold from CAS# Inact.	0		ns	SR, SF	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1650		Read Cmd Hold from CAS# Inact.	0		ns			F2
Lt1651		Read Cmd Hold from CAS# Inact.	0		ns			P1

3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

Table 3.4-15. DRAM Mode Timings: 20 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Lt1652	tWCS	Write Cmd Setup to CAS# Active	0		ns	SF, SF	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1653		Write Cmd Setup to CAS# Active	0		ns			F2
Lt1654		Write Cmd Setup to CAS# Active	0		ns			P1
Lt1655	tWCH	Write Cmd Hold from CAS# Act.	20		ns	SF, SR	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1656		Write Cmd Hold from CAS# Act.	20		ns			F2
Lt1657		Write Cmd Hold from CAS# Act.	20		ns			P1
Lt1658	tWDS	Write Data Setup to CAS# Active	0		ns	SF, S	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1659		Write Data Setup to CAS# Active	0		ns			F2
Lt1660		Write Data Setup to CAS# Active	0		ns			P1
Lt1661	tWDH	Write Data Hold from CAS# Active	20		ns	SR, S	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1662		Write Data Hold from CAS# Active	20		ns			F2
Lt1663		Write Data Hold from CAS# Active	20		ns			P1
Lt1664	tRPV	Read Parity Valid from CAS# Act.	20		ns	SF, S	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1665		Read Parity Valid from CAS# Act.	20		ns			F2
Lt1666		Read Parity Valid from CAS# Act.	40		ns			P1
Lt1667	tWPS	Write Parity Setup to CAS# Active	0		ns	SF, SF	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1668		Write Parity Setup to CAS# Active	0	ns				F2
Lt1669		Write Parity Setup to CAS# Active	0		ns			P1
Lt1670	tWPH	Write Parity Hold from CAS# Act.	20		ns	SF, SR	Figure 3.5.29	F1 CR = Max, CT = Max
Lt1671		Write Parity Hold from CAS# Act.	20		ns			F2
Lt1672		Write Parity Hold from CAS# Act.	20		ns			P1
Lt1673	tCSR	CAS# Setup to RAS# Active (CBR Refresh)	10		ns	SF, SF	Figure 3.5.31	F1
Lt1674		CAS# Setup to RAS# Active (CBR Refresh)	10		ns			F2 CR = Max, CT = Max
Lt1675		CAS# Setup to RAS# Active (CBR Refresh)	10		ns			P1
Lt1676	tCHR	CAS# Hold from RAS# Active (CBR Refresh)	20		ns	FF, FR	Figure 3.5.31	F1
Lt1677		CAS# Hold from RAS# Active (CBR Refresh)	20		ns			F2 CR = Min, CT = Min
Lt1678		CAS# Hold from RAS# Active (CBR Refresh)	20		ns			P1



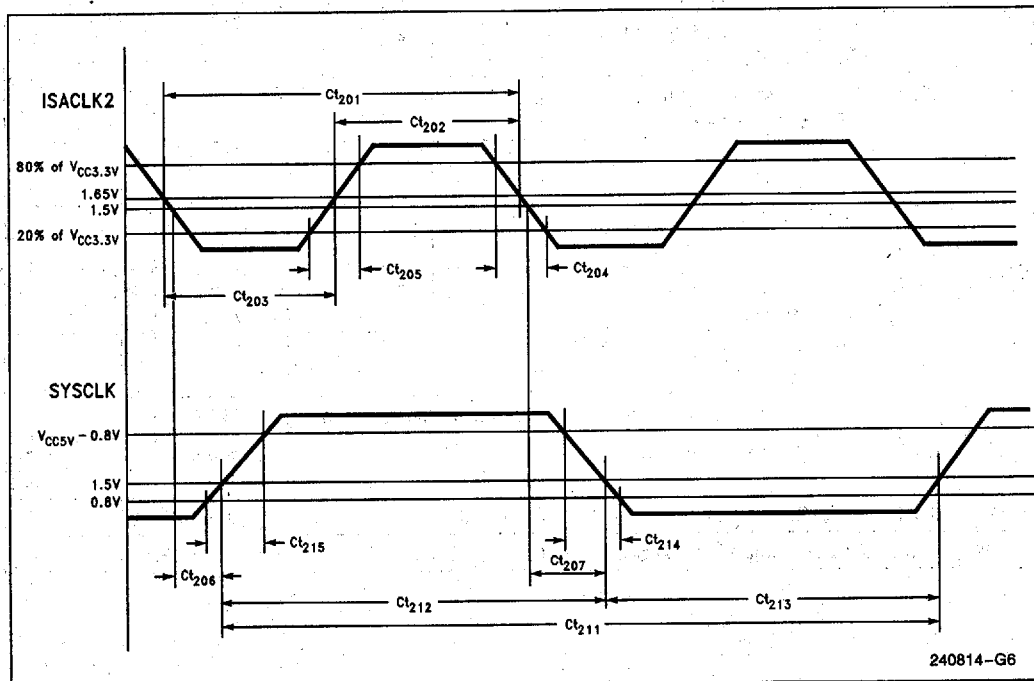
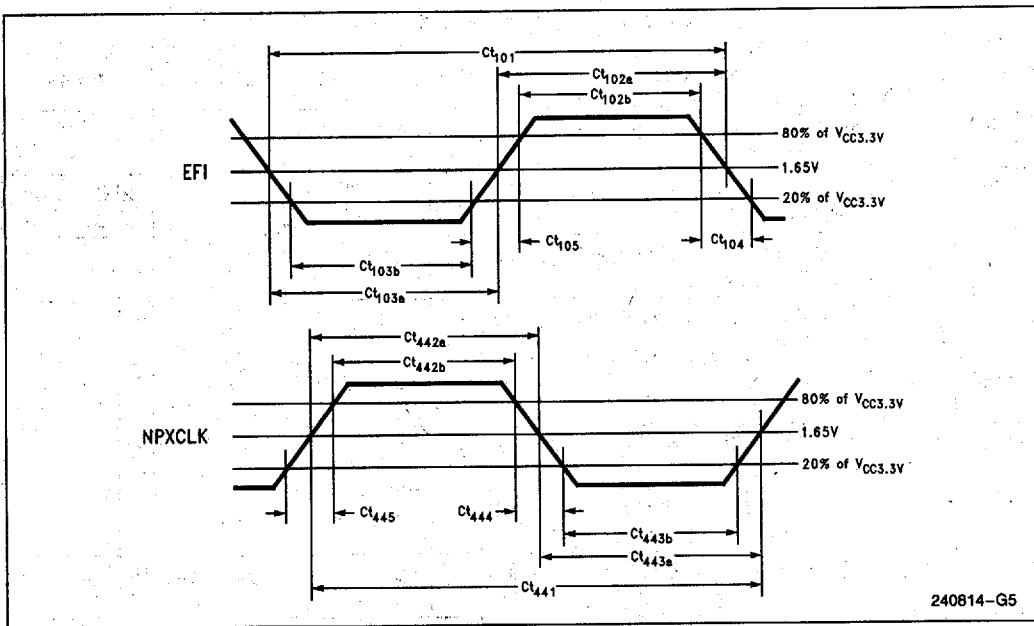
56E D ■ 4826175 0119200 925 ■ ITL1 T-49-17-34

3.4 Intel386™ SL CPU (Low-Voltage) Timing Specifications (Continued)

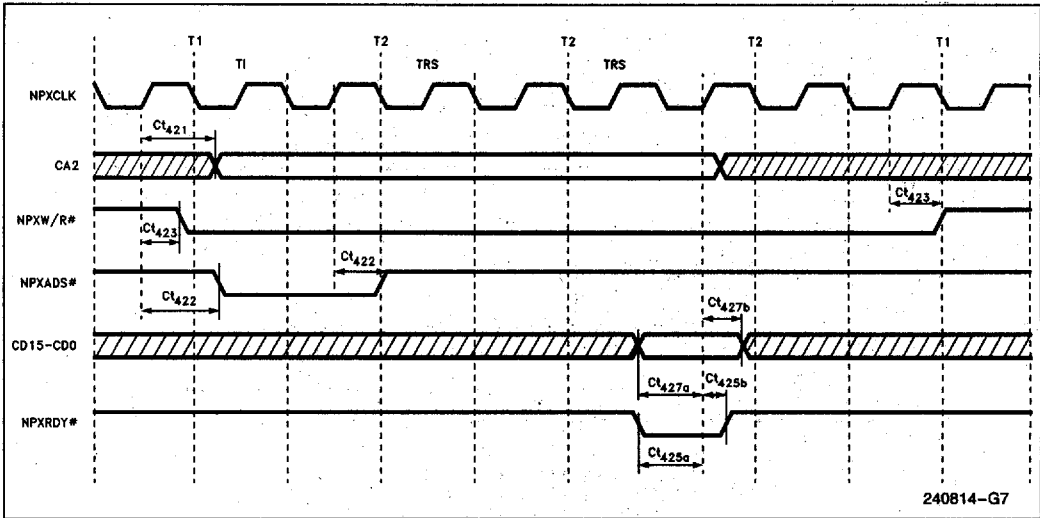
Table 3.4-15. DRAM Mode Timings: 20 MHz (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
Lt1679	tWSR	Read Cmd Setup to RAS# Act. (CBR Refresh)	20		ns		Figure 3.5.30	F1
Lt1680		Read Cmd Setup to RAS# Act. (CBR Refresh)	20		ns	SF, SF		F2 CR = Min, CT = Max
Lt1681		Read Cmd Setup to RAS# Act. (CBR Refresh)	20		ns			P1
Lt1682	tWHR	Read Cmd HOLD from RAS# Act. (CBR Refresh)	30		ns			F1
Lt1683		Read Cmd HOLD from RAS# Act. (CBR Refresh)	30		ns	FF, FR		F2 CR = Min, CT = Min
Lt1684		Read Cmd HOLD from RAS# Act. (CBR Refresh)	30		ns			P1
Lt1685	tRASS	RAS# Active Pulse Width (CBR Self Refresh)	100K		ns			F1
Lt1686		RAS# Active Pulse Width (CBR Self Refresh)	100K		ns			F2
Lt1687		RAS# Active Pulse Width (CBR Self Refresh)	100K		ns			P1
Lt1688	tCHS	CAS# Hold Time from RAS# (CBR Self Refresh)	-50		ns			F1
Lt1689		CAS# Hold Time from RAS# (CBR Self Refresh)	-60		ns		F2	
Lt1690		CAS# Hold Time from RAS# (CBR Self Refresh)	-70		ns		P1	
Lt1691	tRPS	RAS# Precharge Pulse Width (CBR Self Refresh)	150		ns		F1	
Lt1692		RAS# Precharge Pulse Width (CBR Self Refresh)	170		ns		F2	
Lt1693		RAS# Precharge Pulse Width (CBR Self Refresh)	200		ns		P1	
The Following Pin Timing Parameters are Independent of DRAM Modes F1, F2, P1								
Lt1694	tPED	PERR# Delay from SYSCLK		38	ns	SR, SF	Figure 3.5.33	CR = Max, CT = Max
Lt1695	tRDS	RAS# Delay from SYSCLK		55	ns	SF	Figure 3.5.32	
Lt1696	tADS	Address Delay from SYSCLK		65	ns	S	Figure 3.5.32	

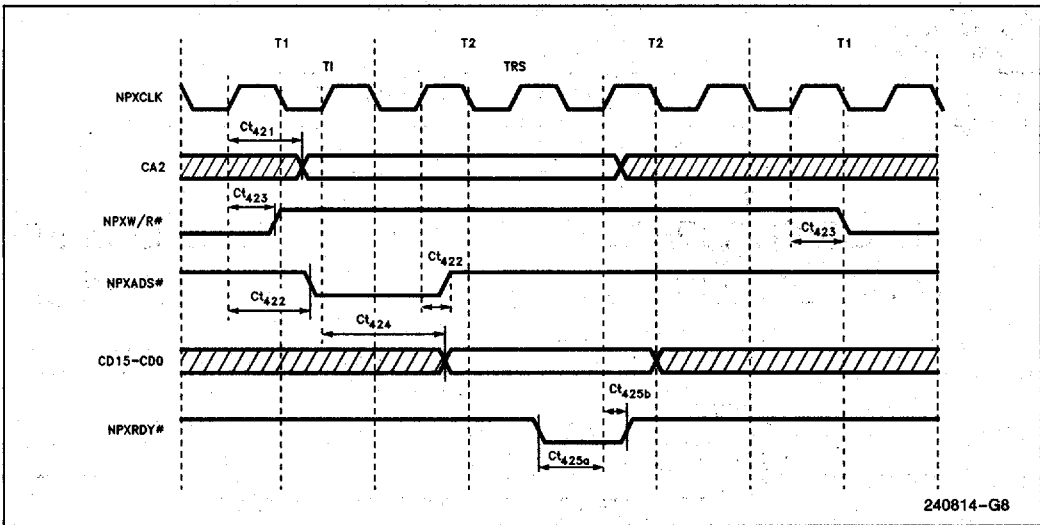
3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams



3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)



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3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

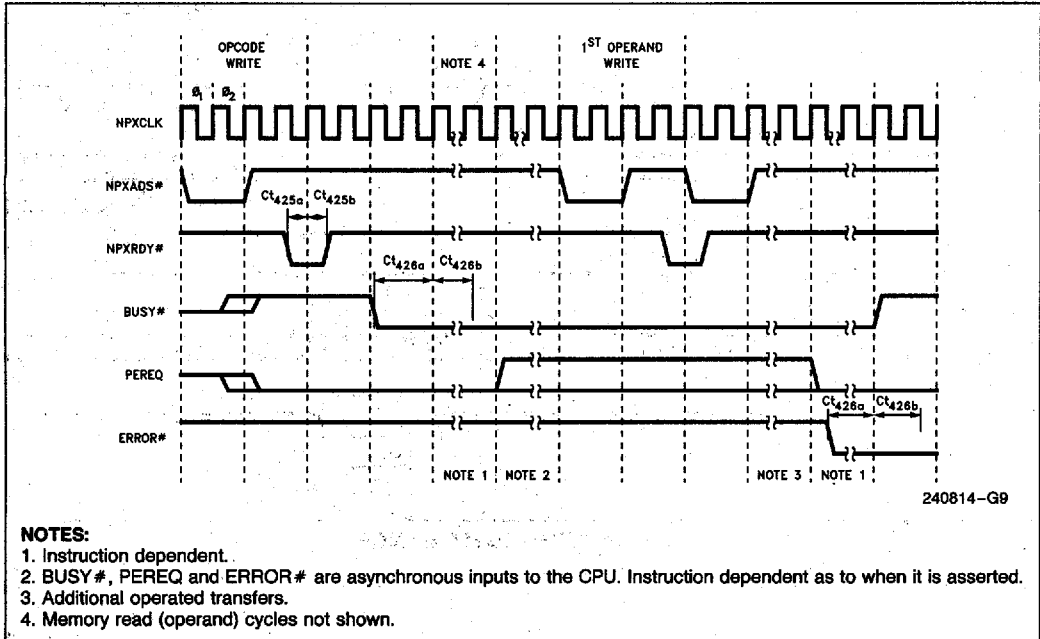


Figure 3.5.5. MCP BUSY#, PEREQ and ERROR# Timings

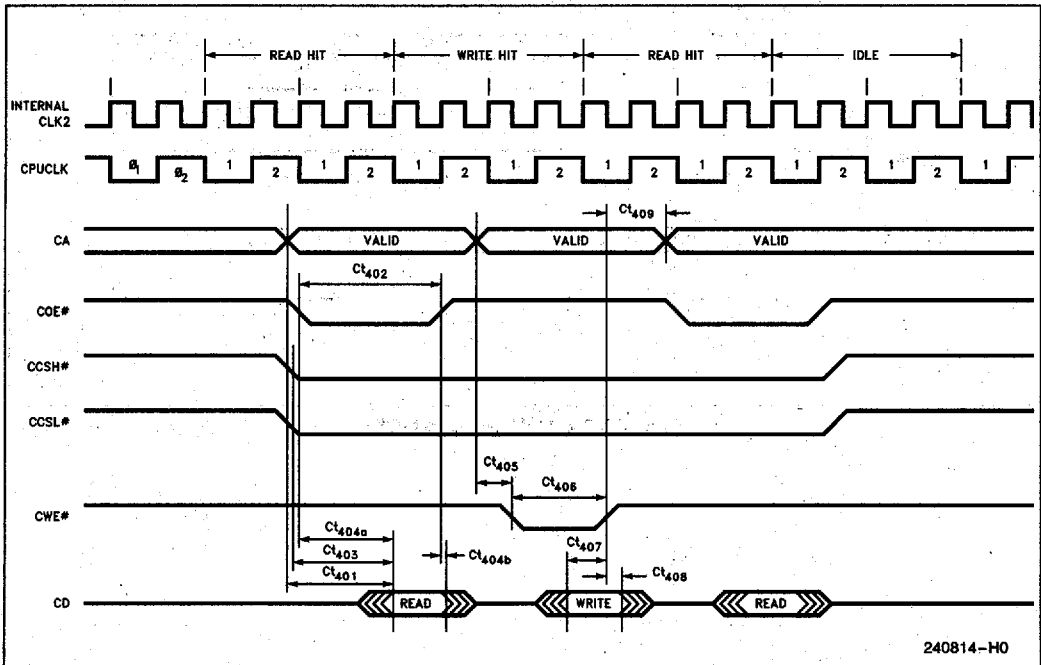
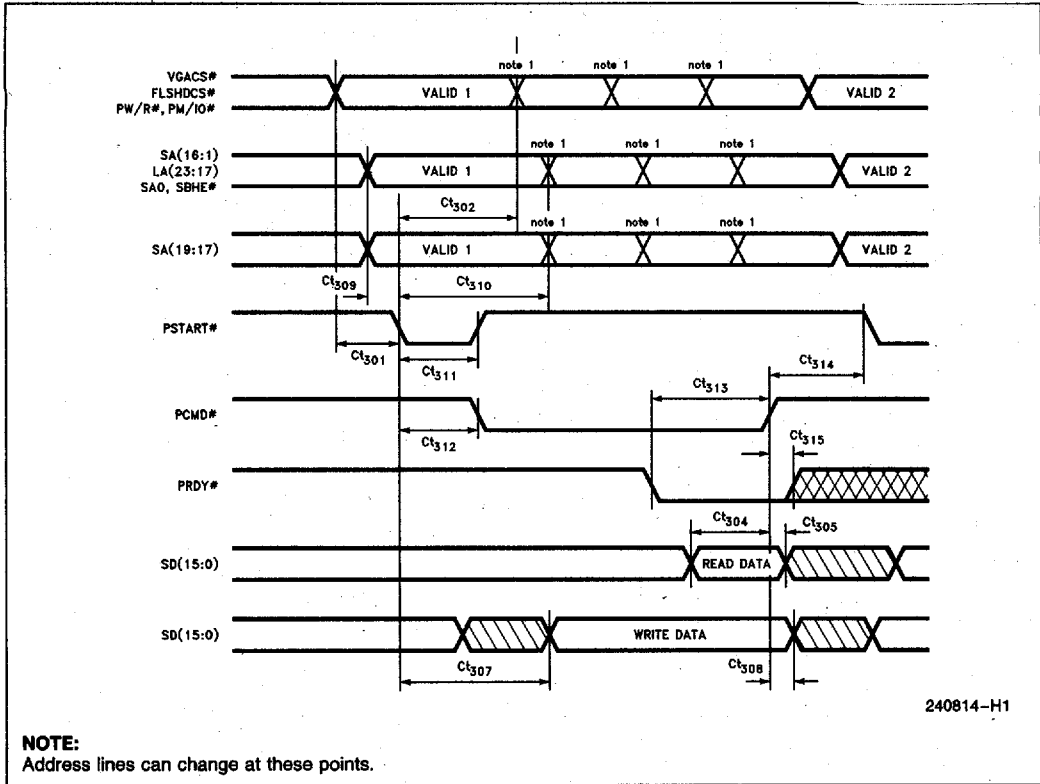


Figure 3.5.6. Cache Read/Write Hit Cycles

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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Figure 3.5.7. PI-Bus Timings

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3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

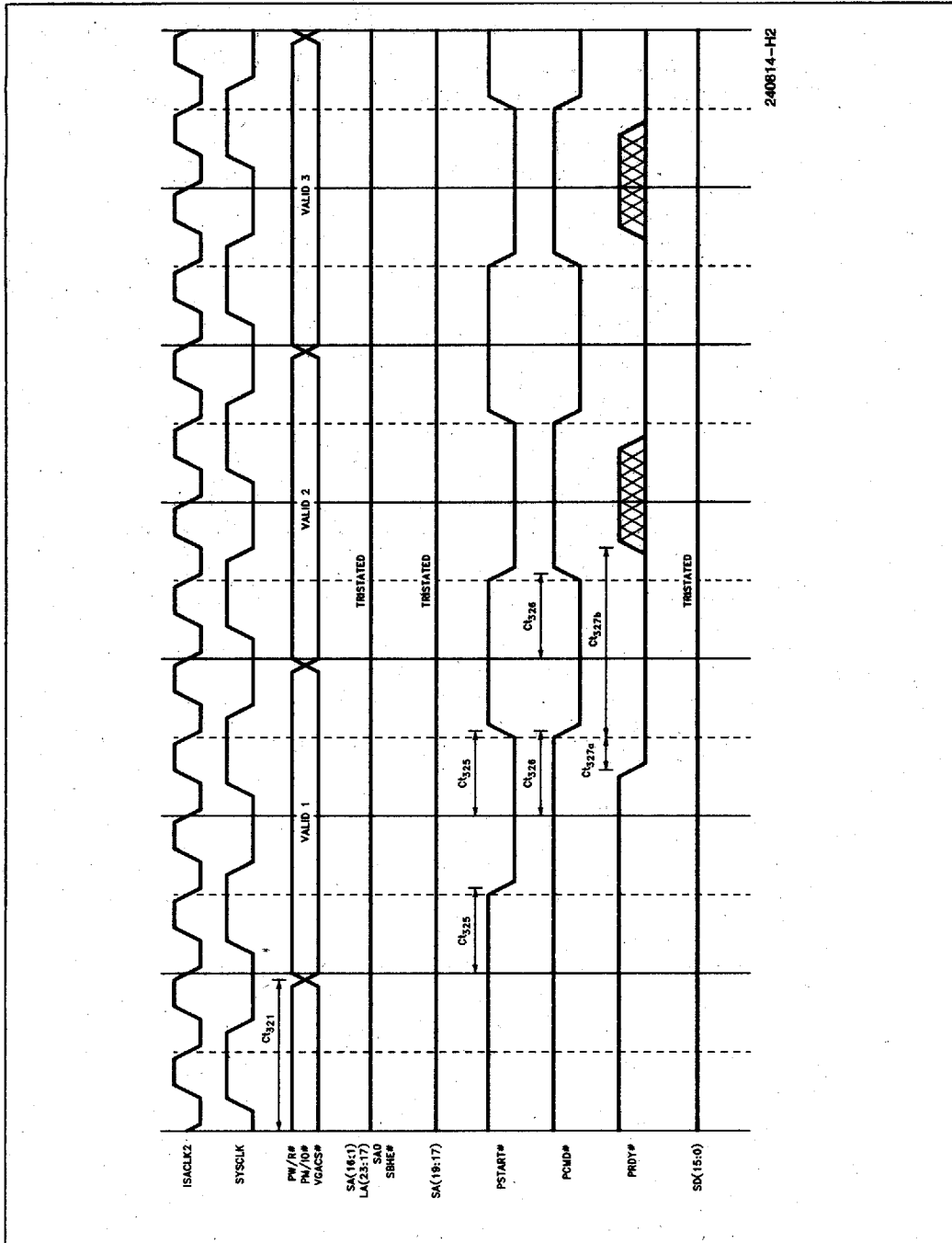


Figure 3.5.8. PI-Bus Slave Controller Generated Timings

56E D ■ 4826175 0119206 343 ■ ITL1

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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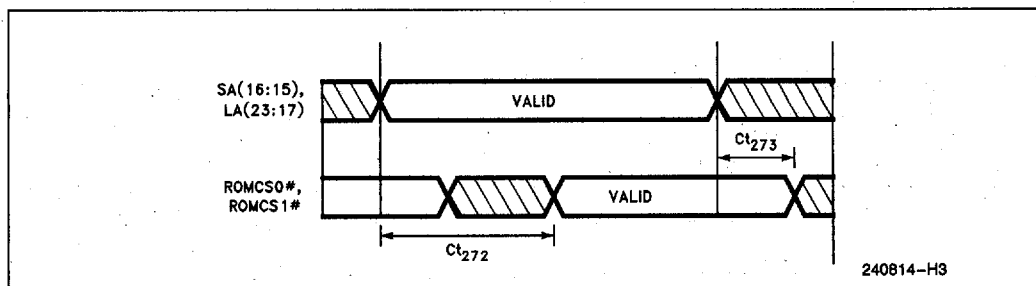


Figure 3.5.9. ISA Bus Slave Controller Generated Timings (ROMCS0#/CS1# with respect to Address)

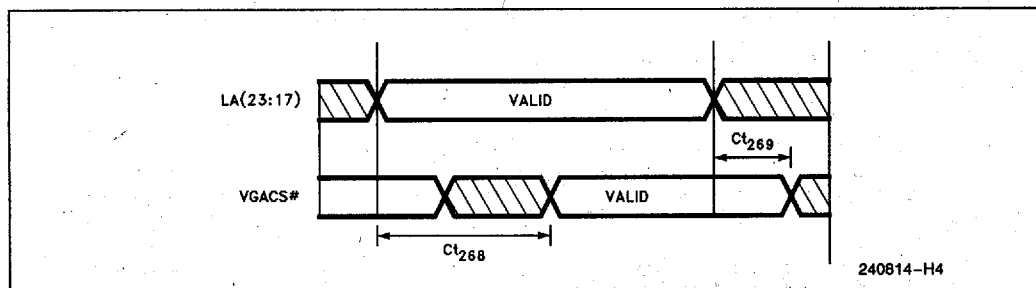


Figure 3.5.10. ISA Bus Master Controller Generated Timings (VGACS# with respect to Address)

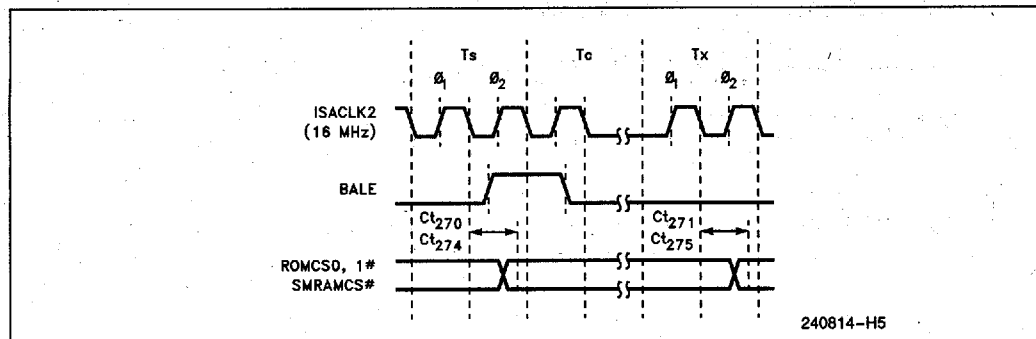


Figure 3.5.11. ROMCS0, ROMCS1, SMRAMCS# Propagation Delays

56E D ■ 4826175 0119207 28T ■ ITL1

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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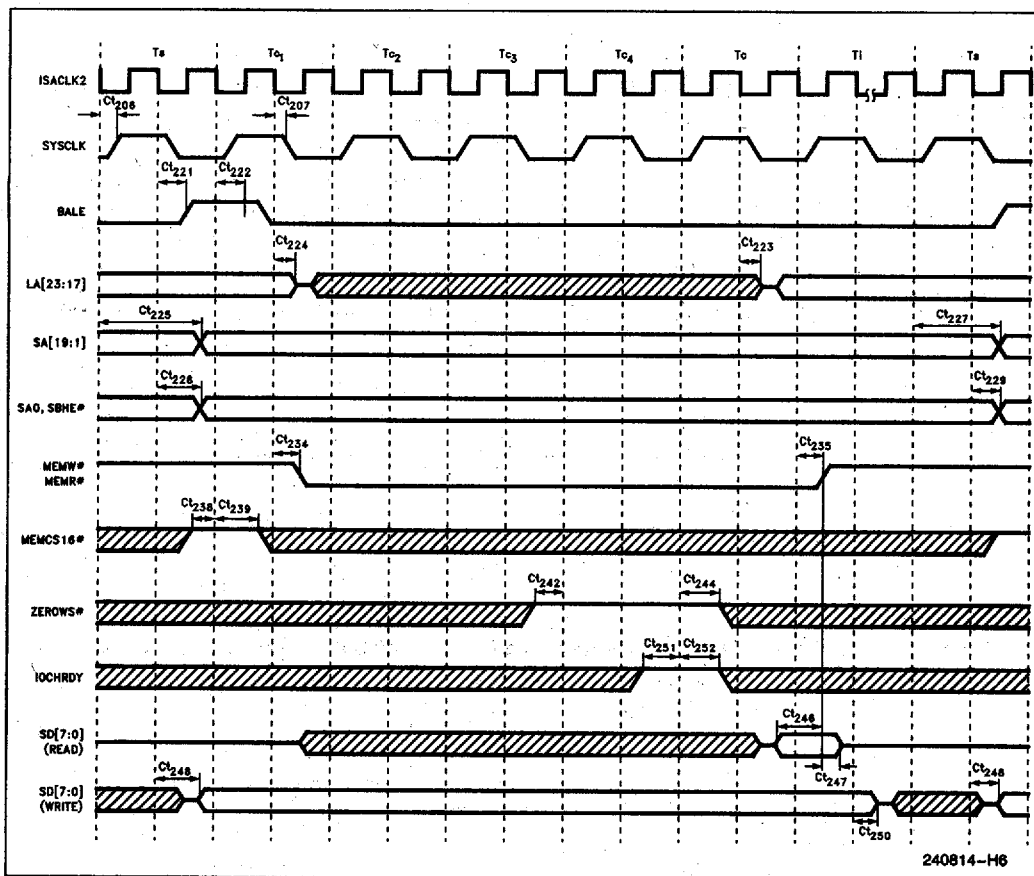


Figure 3.5.12. ISA Bus 8-Bit Memory Read/Write Standard ISA Bus Cycle (6 SYSLKs)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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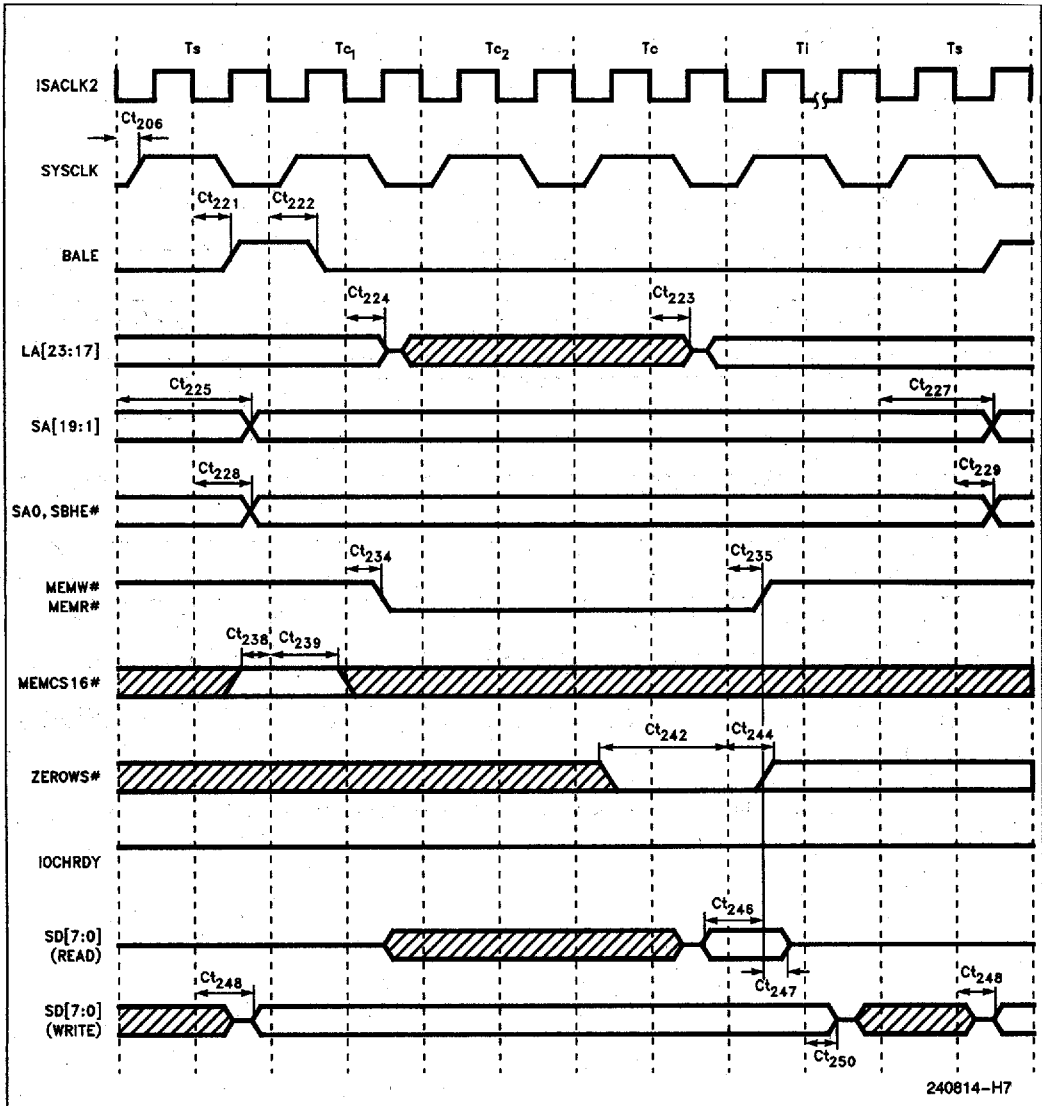


Figure 3.5.13. ISA Bus 8-Bit Memory Read/Write with ZEROWS# Asserted (4 SYSClKs)

2

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

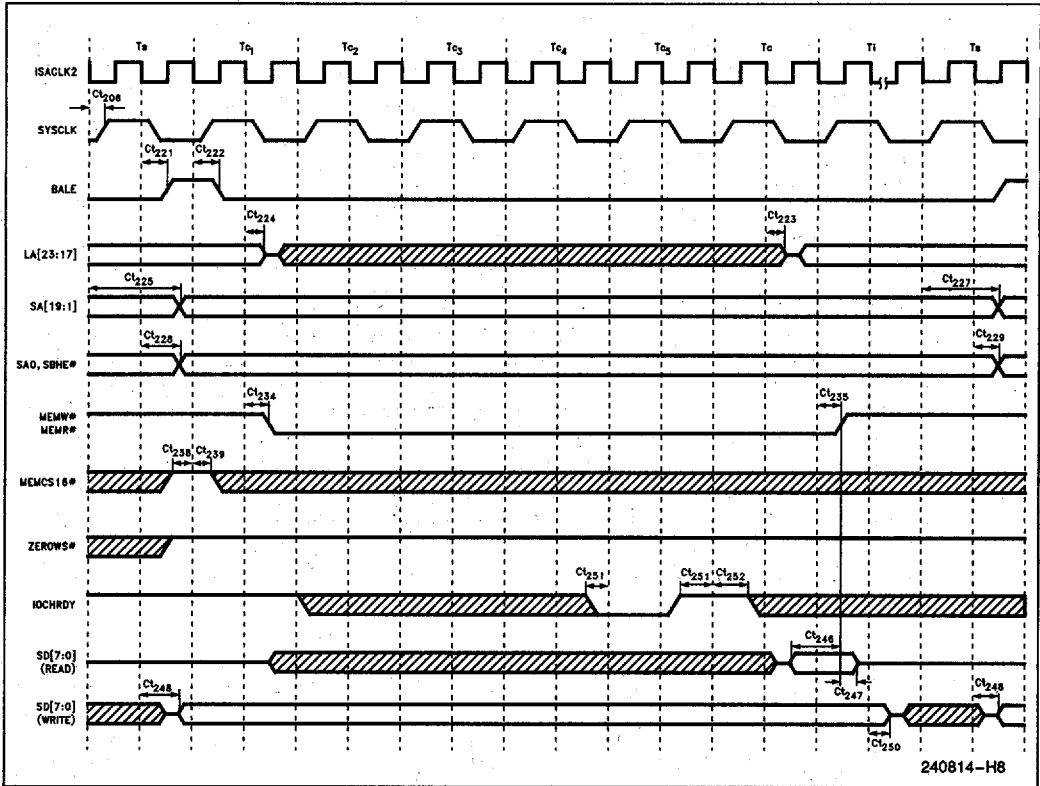


Figure 3.5.14. ISA Bus 8-Bit Memory Read/Write w/IOCHRDY De-Asserted (Added Wait States)

56E D ■ 4826175 0119210 874 ■ ITL1

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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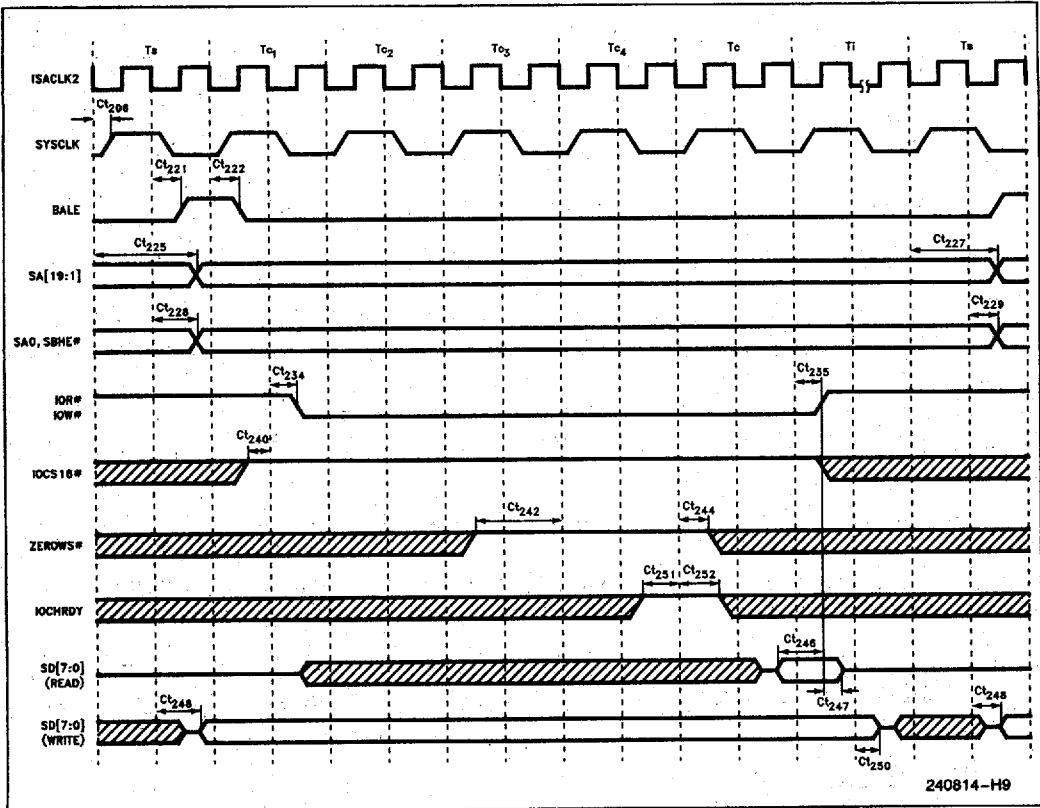


Figure 3.5.15. ISA Bus 8-Bit I/O Read/Write Standard ISA Bus Cycles (6 SYSCLKs)

2

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

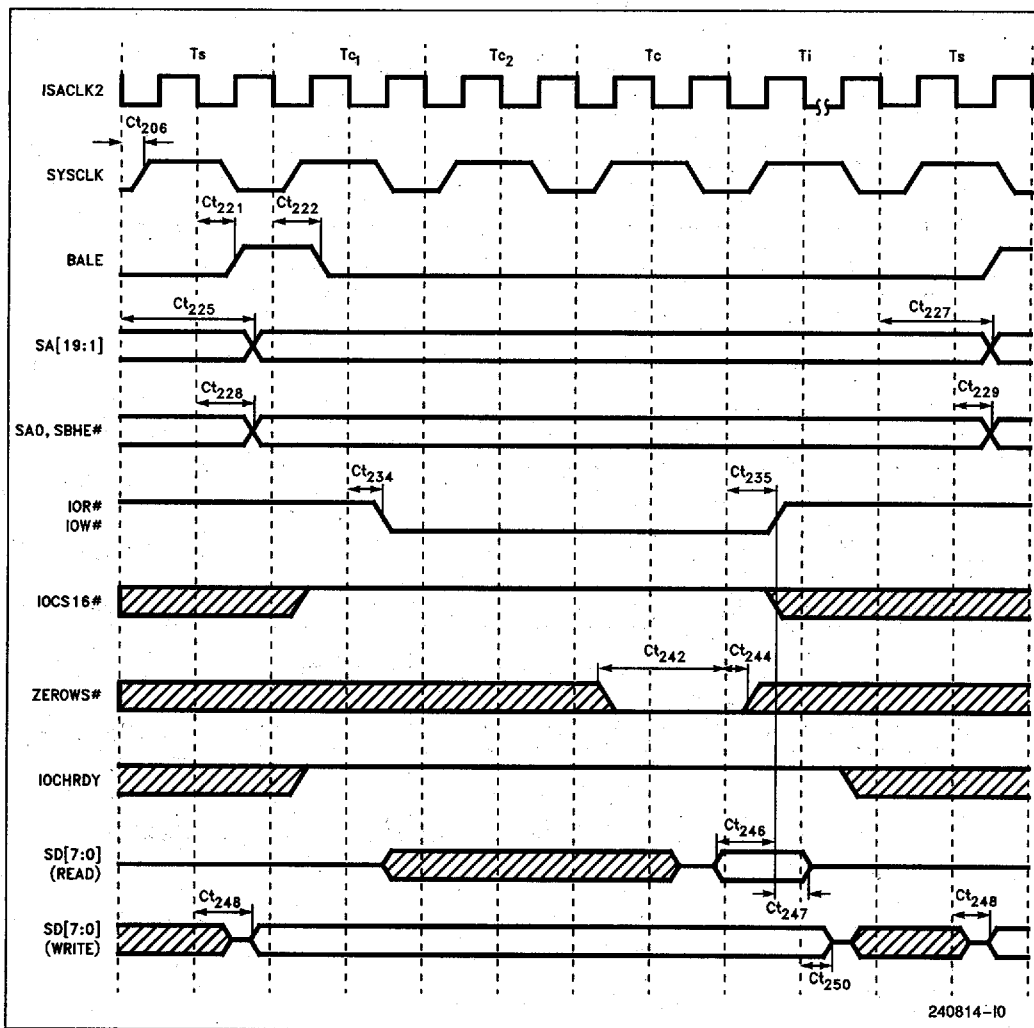


Figure 3.5.16. ISA Bus 8-Bit I/O Read/Write with ZEROWS# Asserted (4 SYSCLKs)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

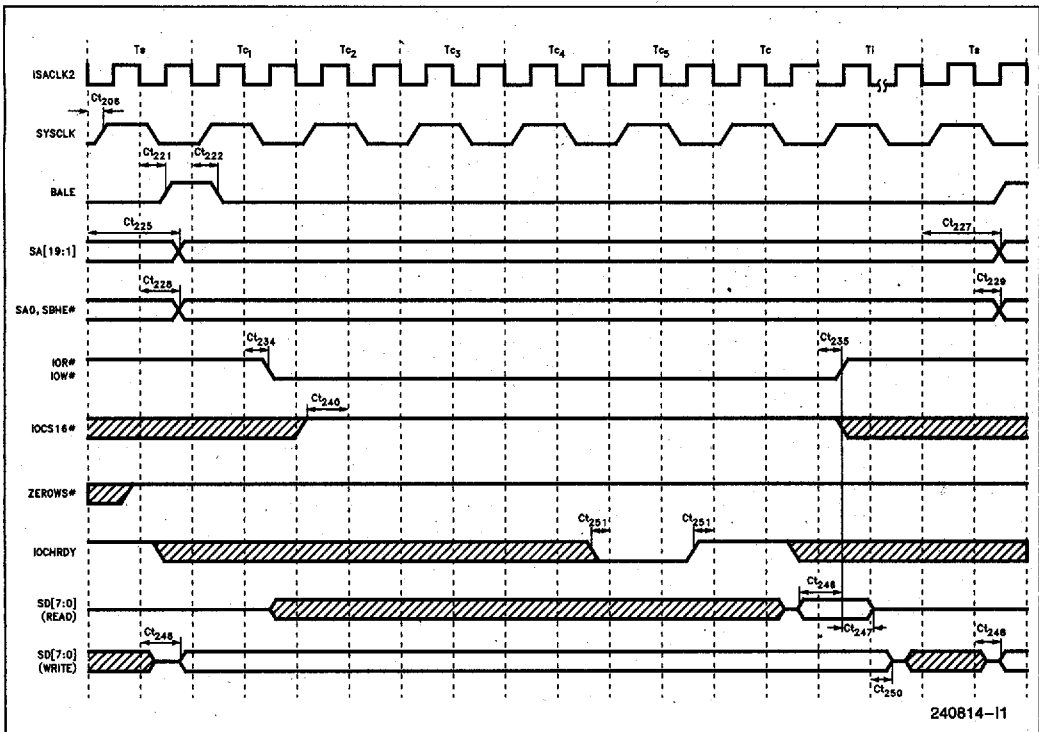
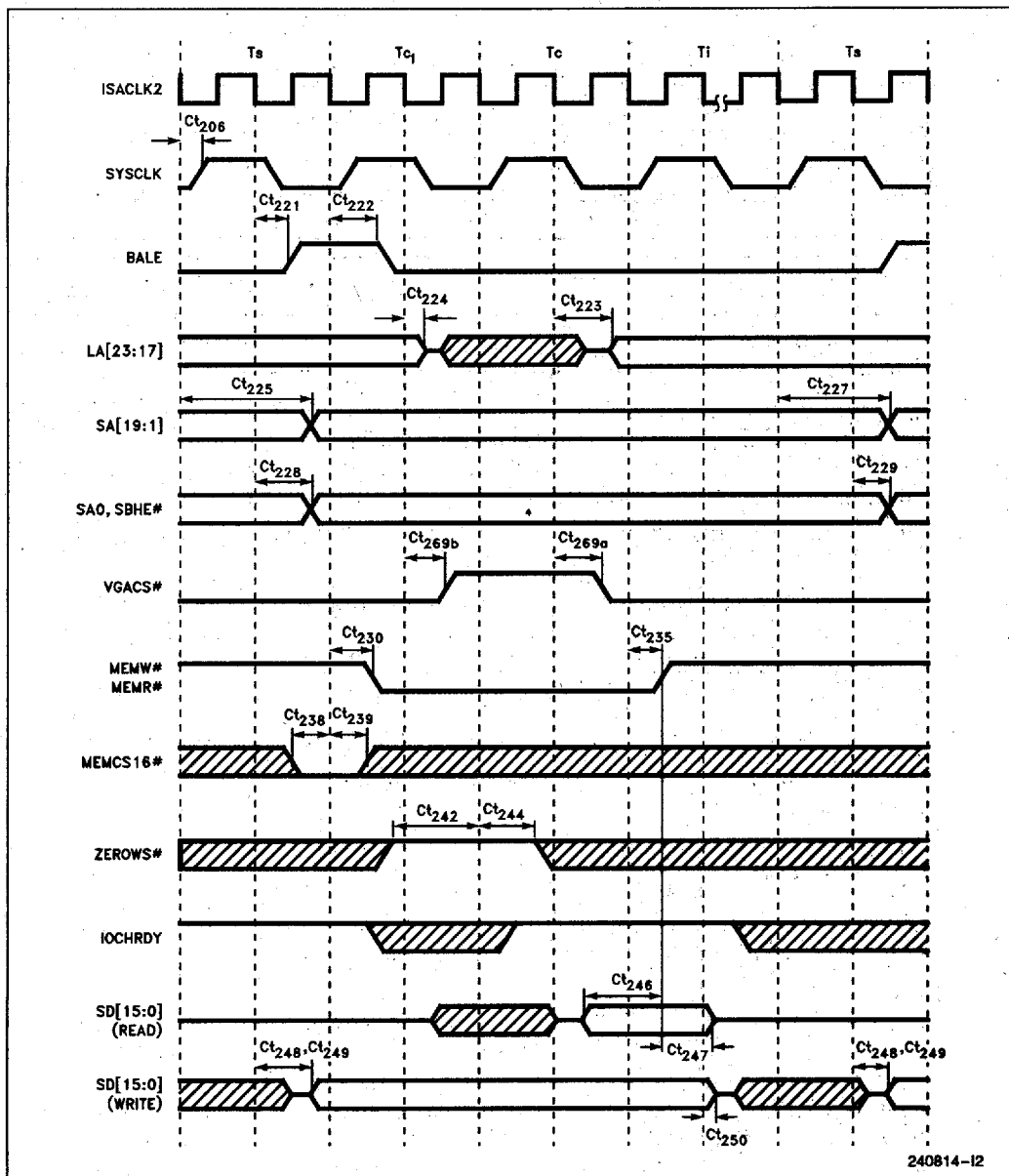


Figure 3.5.17. ISA Bus 8-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)



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Figure 3.5.18. ISA Bus 16-Bit Memory Read/Write Standard ISA Bus Cycles (3 SYSCLKs)

56E D ■ 4826175 0119214 41T ■ ITL1

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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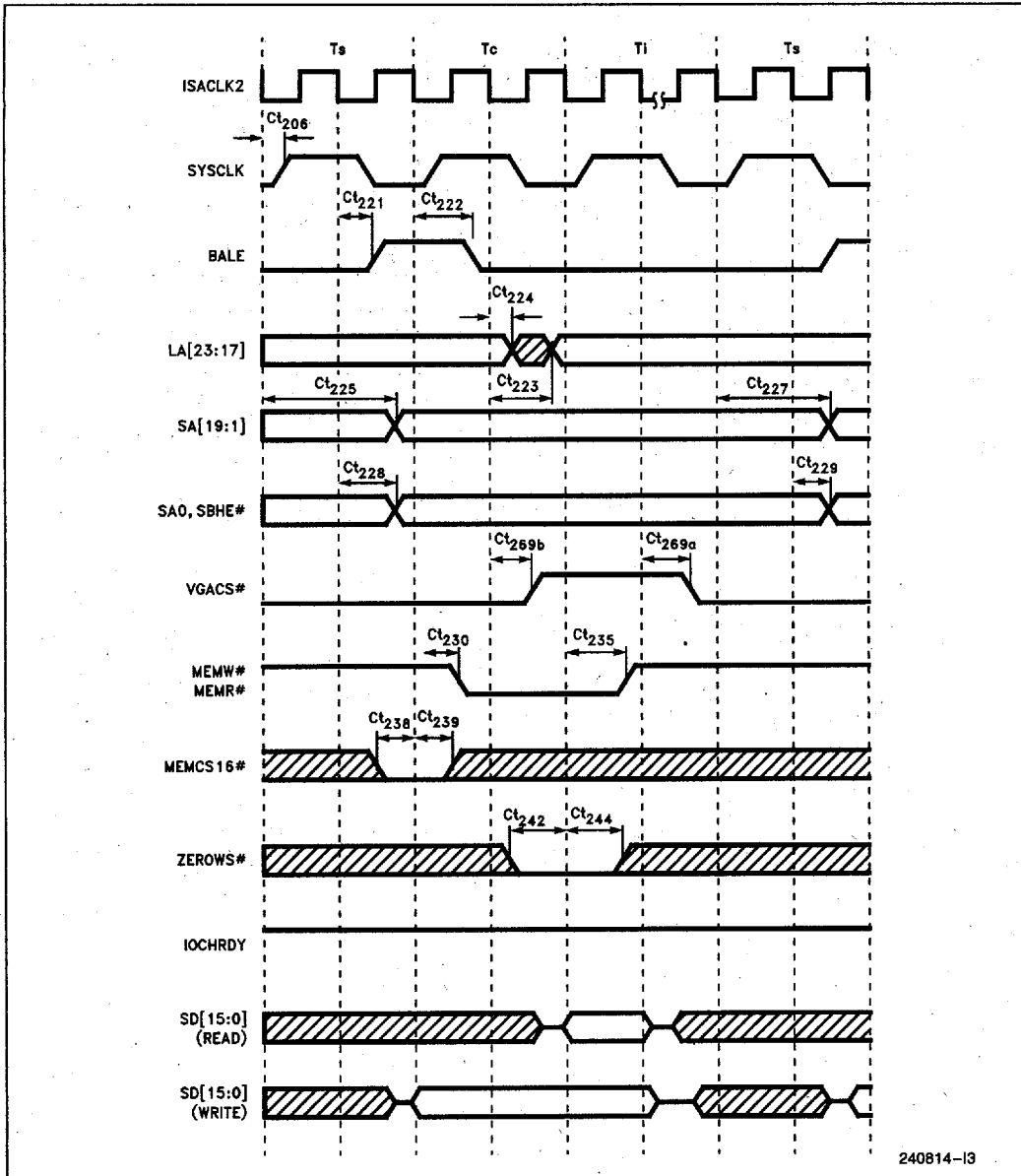
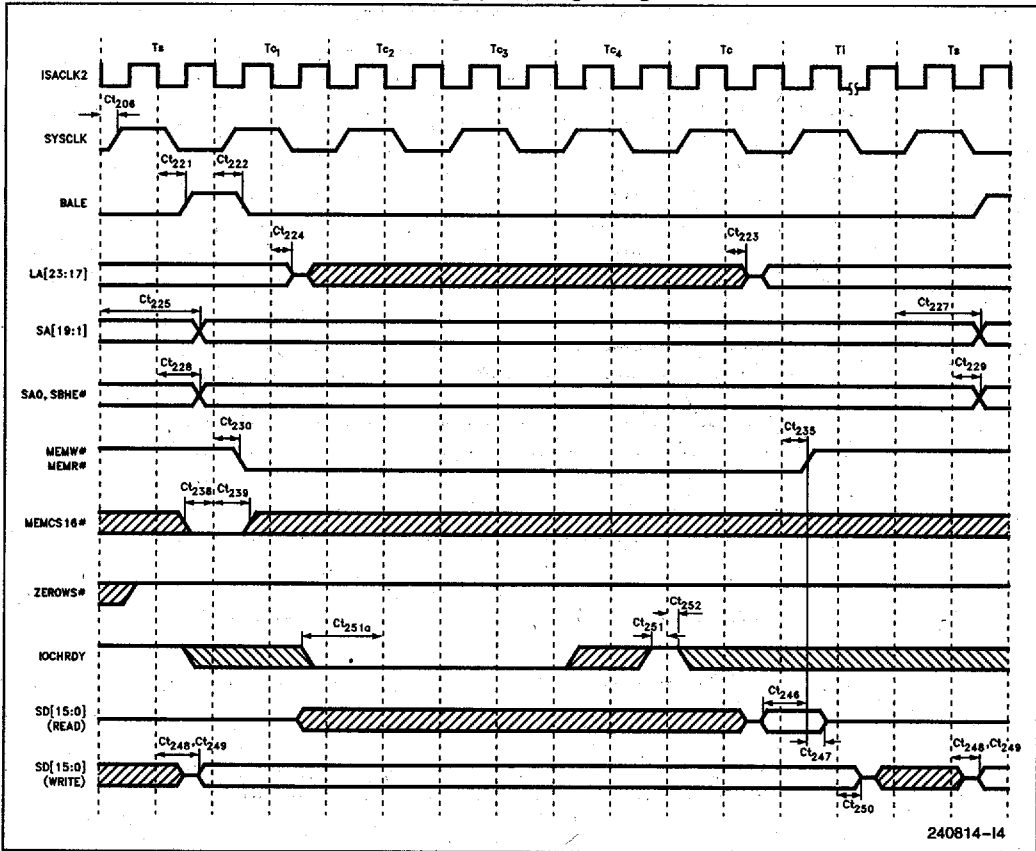


Figure 3.5.19. ISA Bus 16-Bit Memory Read/Write with ZEROWS# Asserted (2 SYSCLKs)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)



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Figure 3.5.20. ISA Bus 16-Bit Memory Read/Write w/IOCHRDY De-Asserted (Added Wait States)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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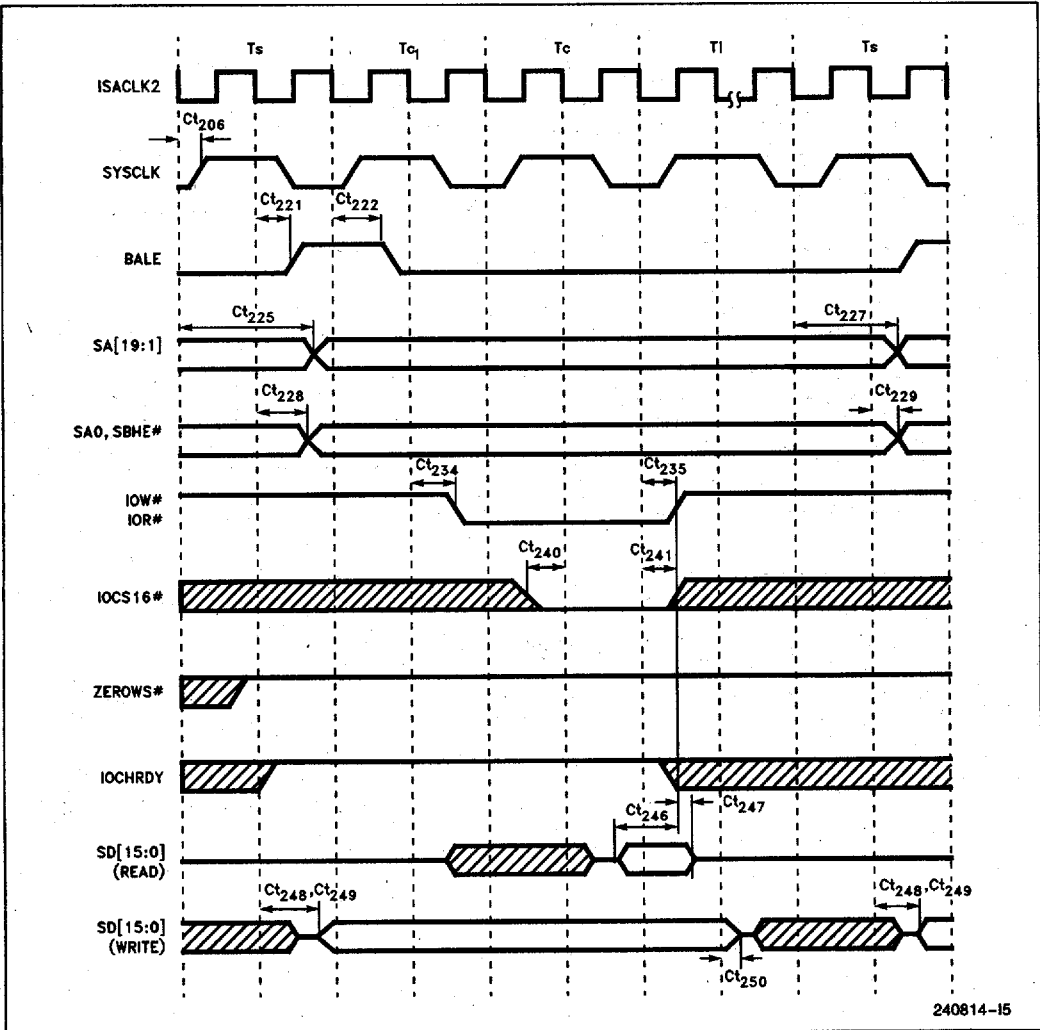


Figure 3.5.21. ISA Bus 16-Bit I/O Read/Write Standard ISA Bus Cycles (3 SYSCLKs)

56E D ■ 4826175 0119217 129 ■ ITL1

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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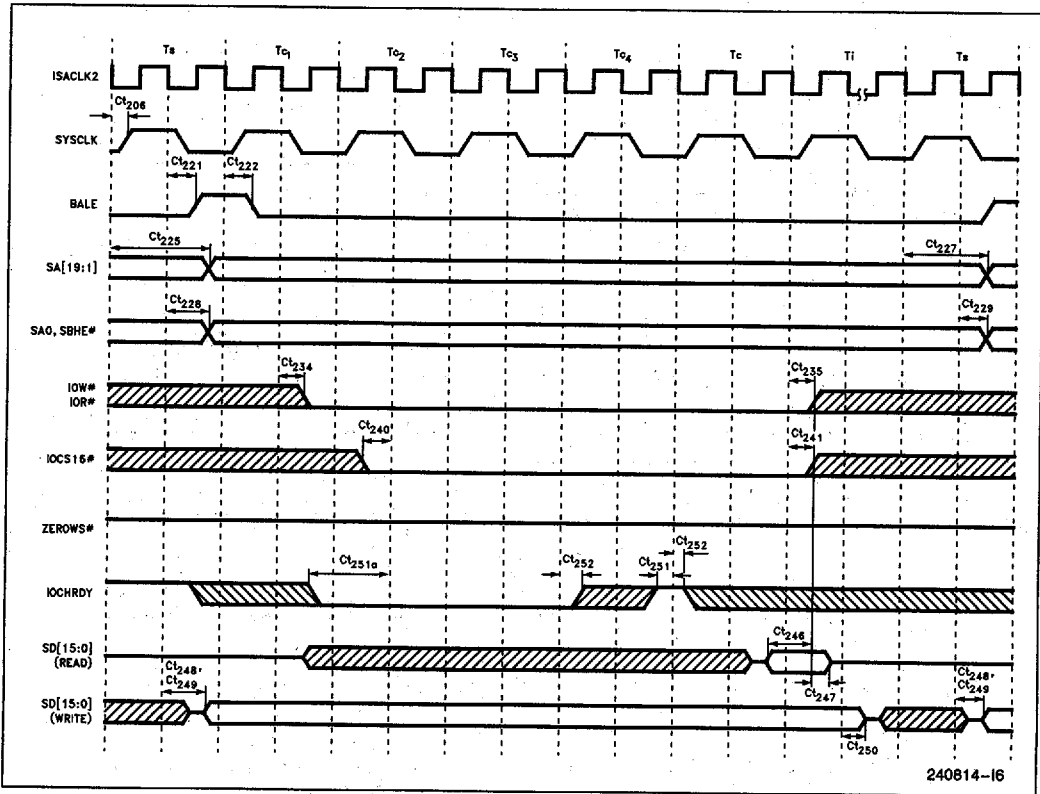


Figure 3.5.22. ISA Bus 16-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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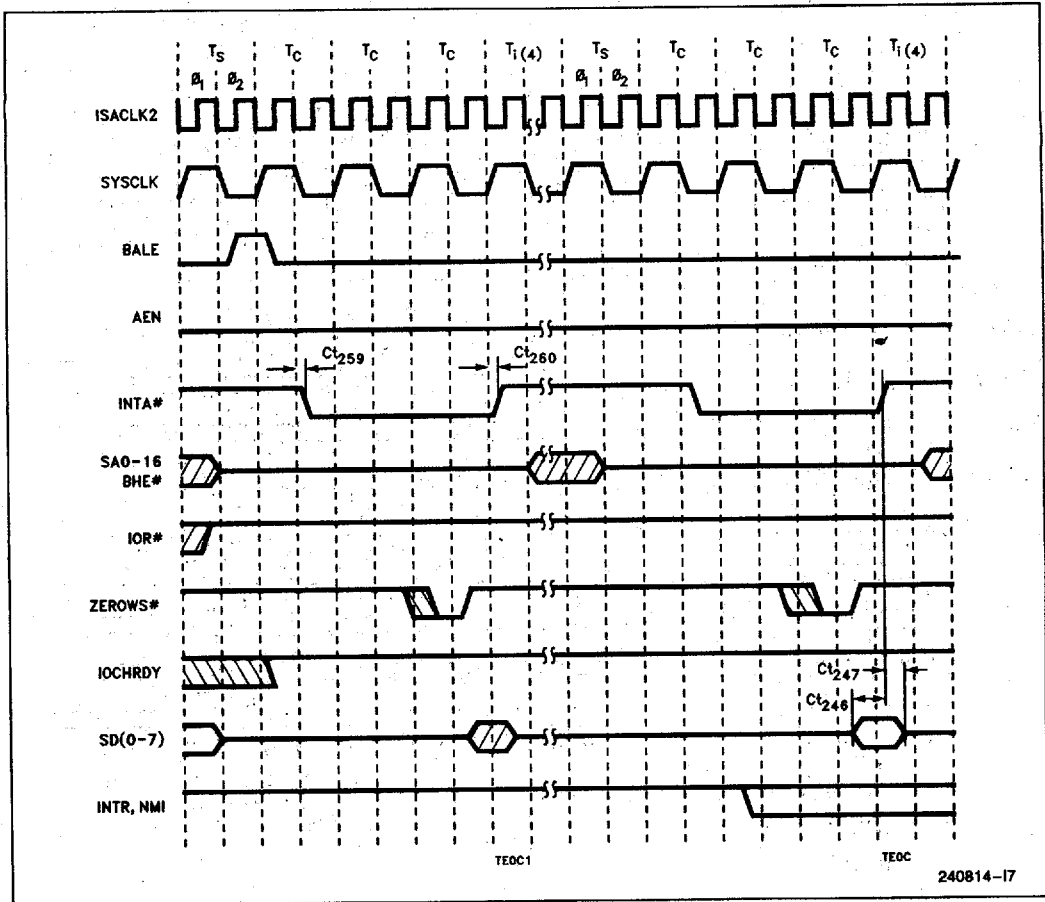


Figure 3.5.23. ISA Bus Interrupt Acknowledge Bus Cycle

240814-17

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

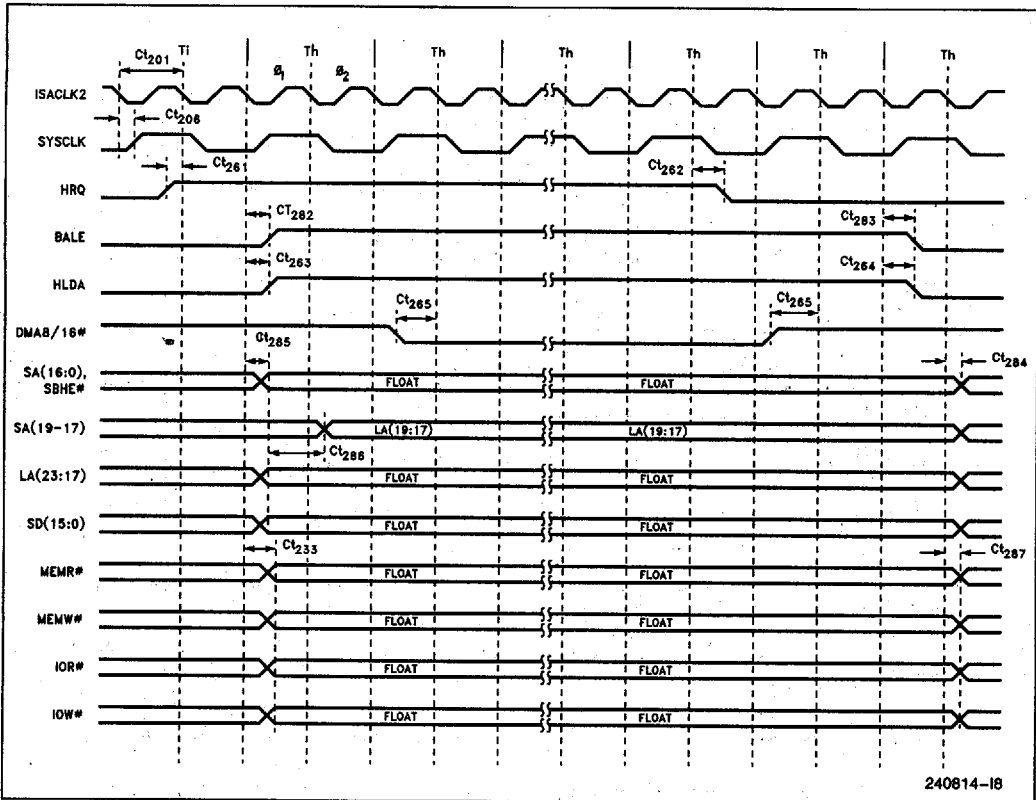


Figure 3.5.24. ISA Bus Controller DMA Cycles

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

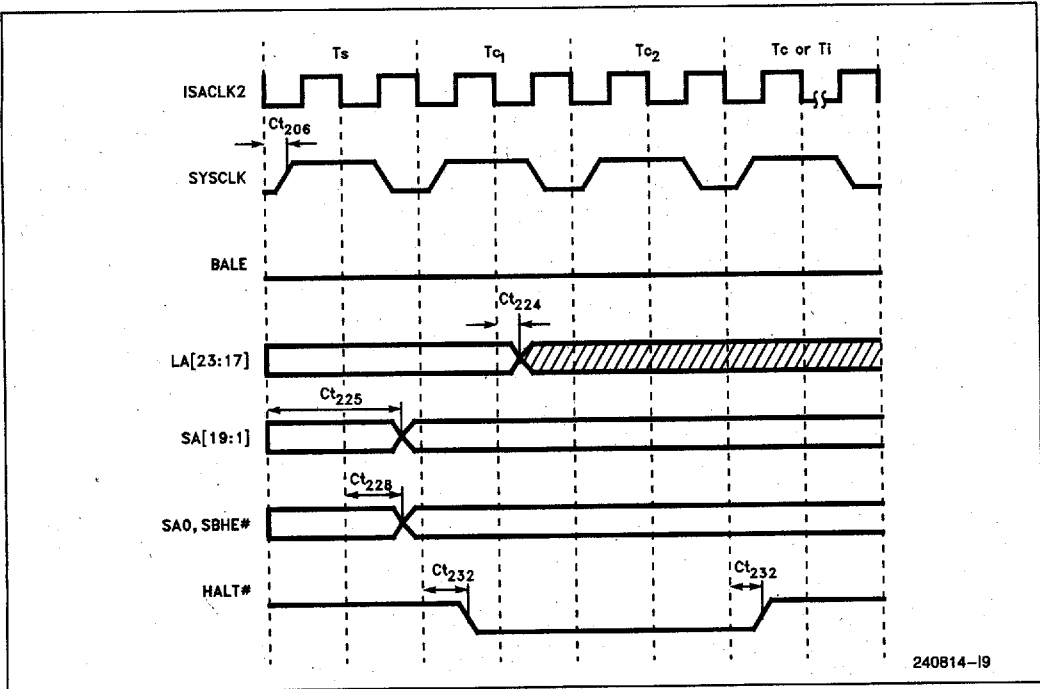


Figure 3.5.24a. ISA Bus HALT Cycles

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

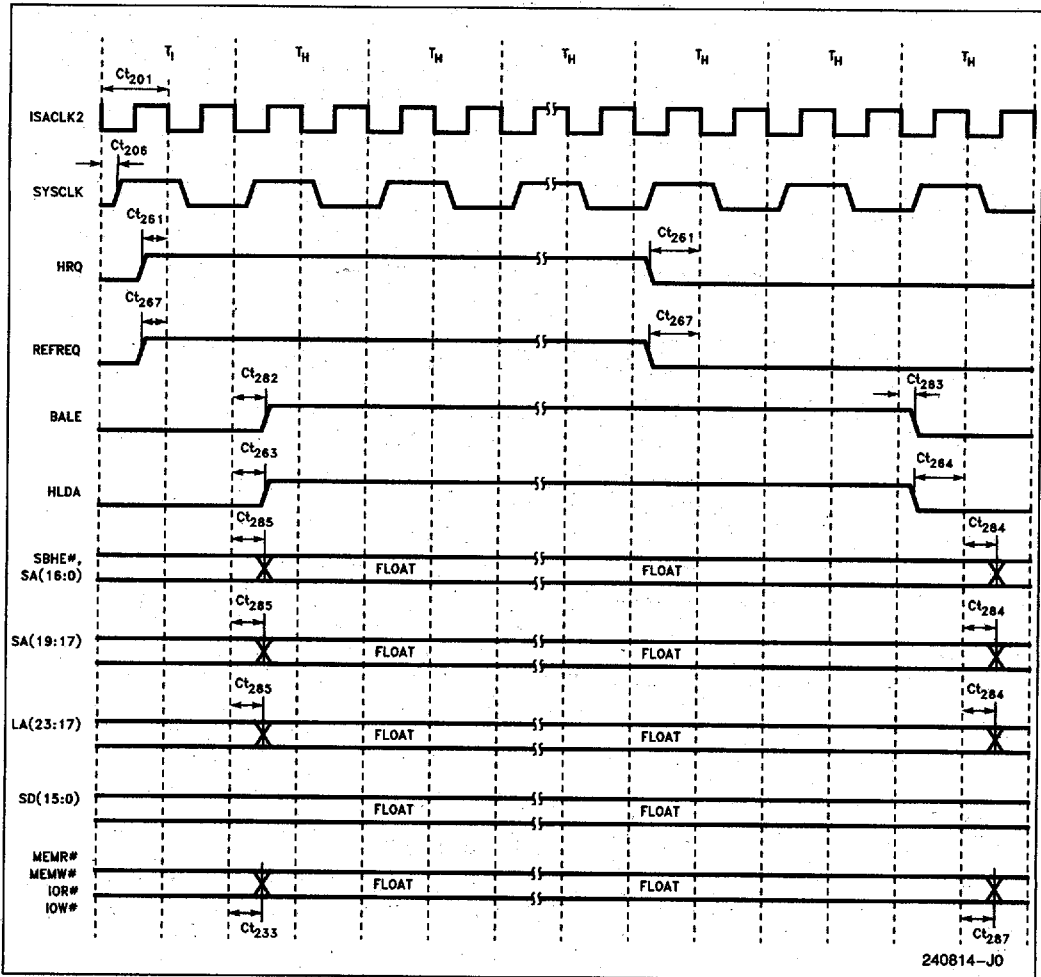


Figure 3.5.25. ISA Bus Controller Refresh Cycle

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

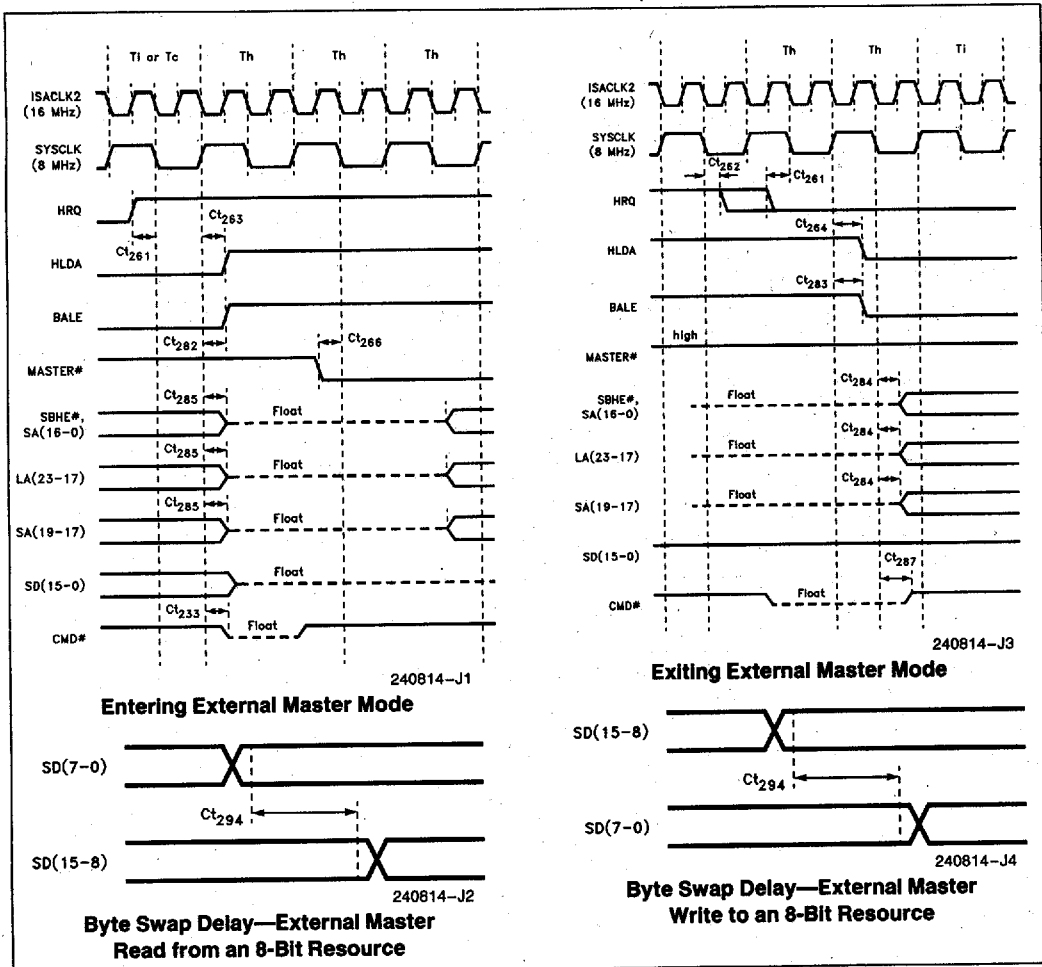


Figure 3.5.26. ISA Bus External Master

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

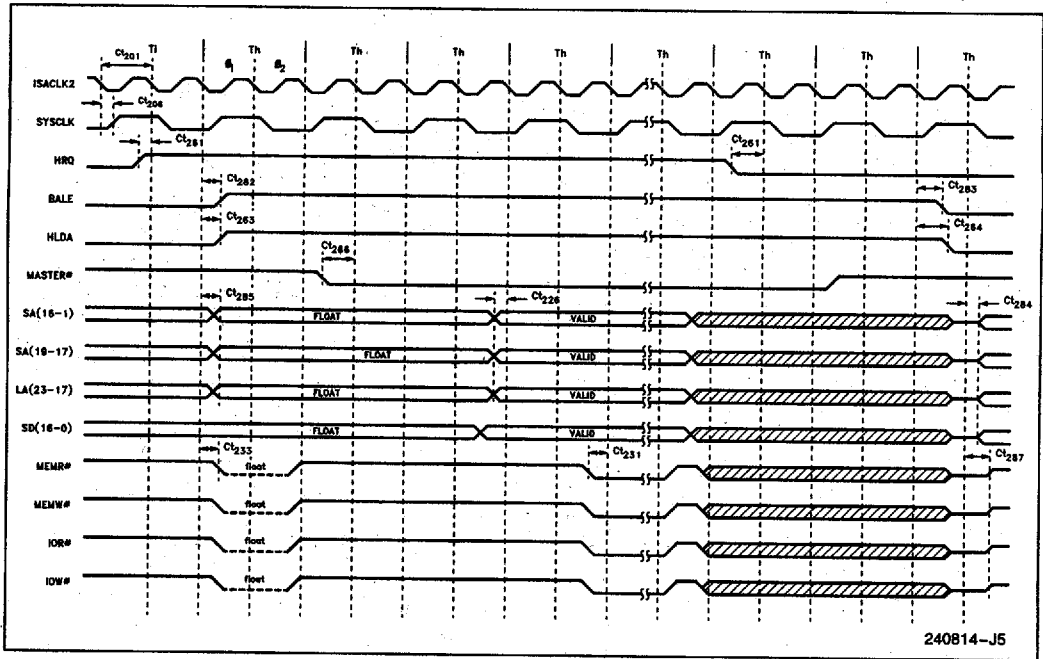
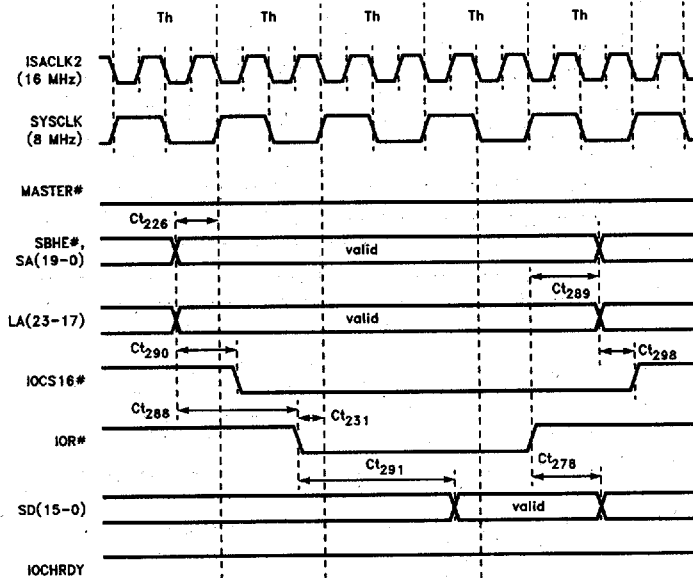


Figure 3.5.27. ISA Bus External Bus Master to Off-Board I/O Ports (No Byte Swapping)

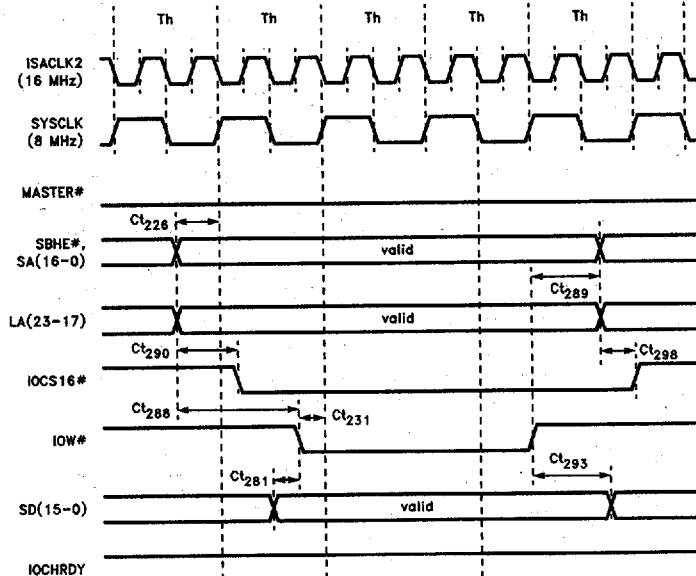
3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

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External Master Read from On-Board I/O Ports

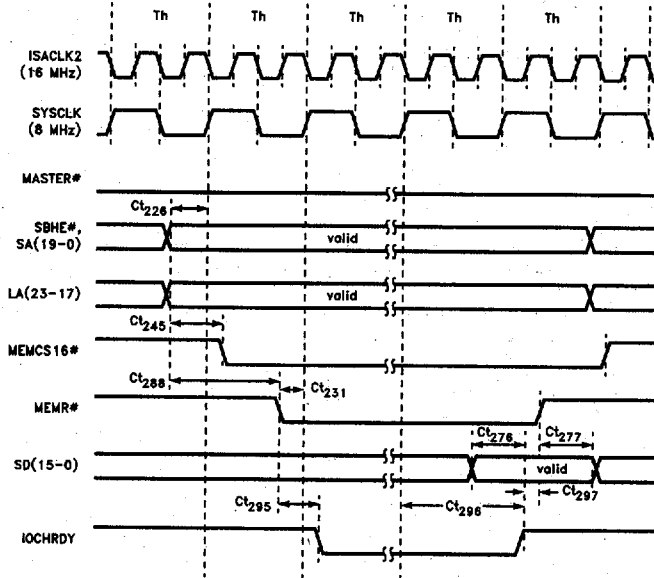


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External Master Write to On-Board I/O Ports

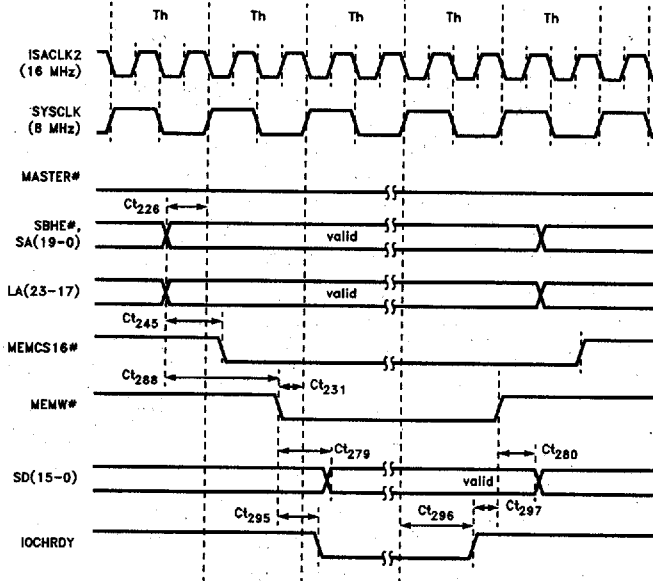
Figure 3.5.28a. ISA Bus External Bus Master to On-Board I/O Ports (Read/Write)

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)



External Master Read from On-Board Memory

240814-J8



External Master Write to On-Board Memory

240814-J9

Figure 3.5.28b. ISA Bus External Bus Master Accesses to On-Board Memory

3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

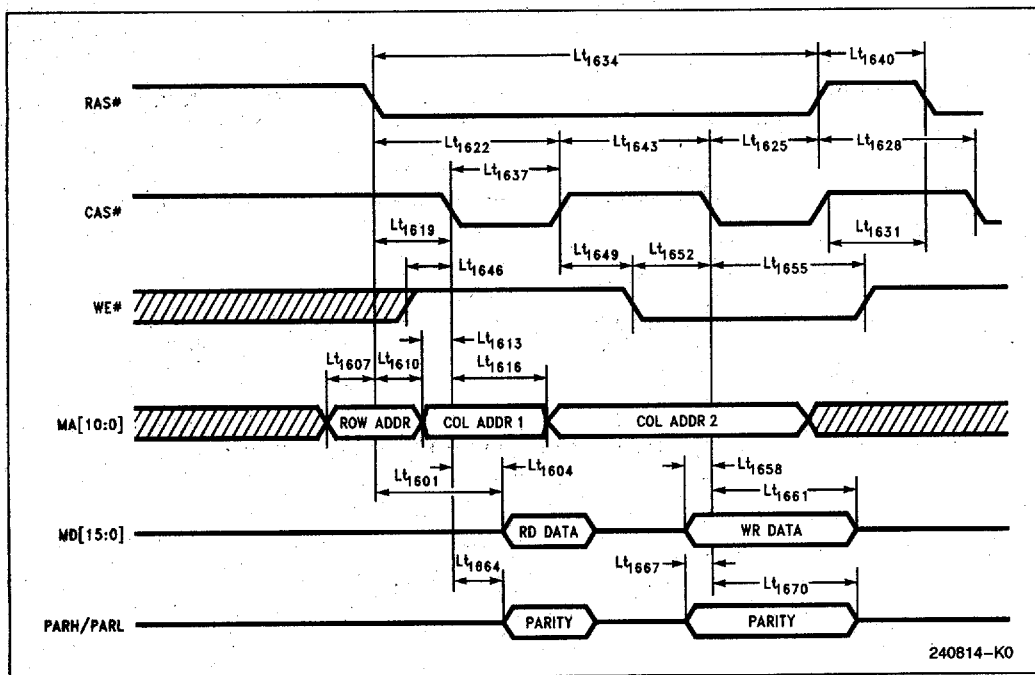


Figure 3.5.29. CPU Memory Controller Timings

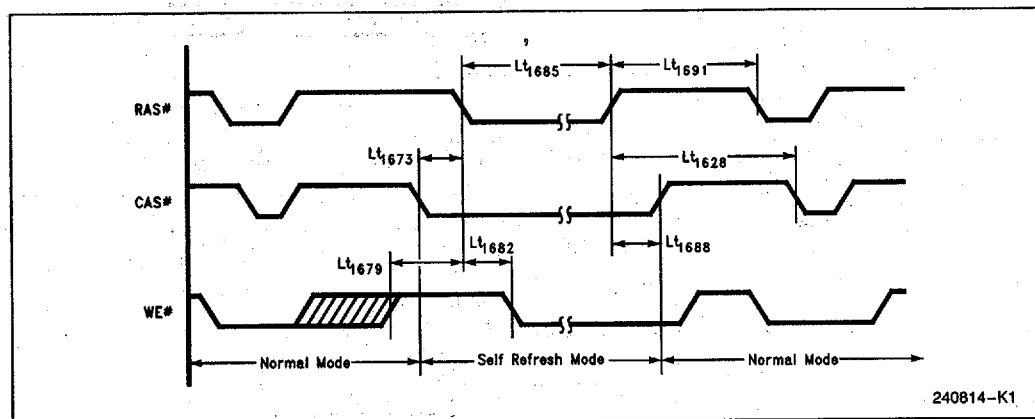


Figure 3.5.30. DRAM Self-Refresh Timings

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3.5 Intel386™ SL CPU (Low-Voltage) Timing Diagrams (Continued)

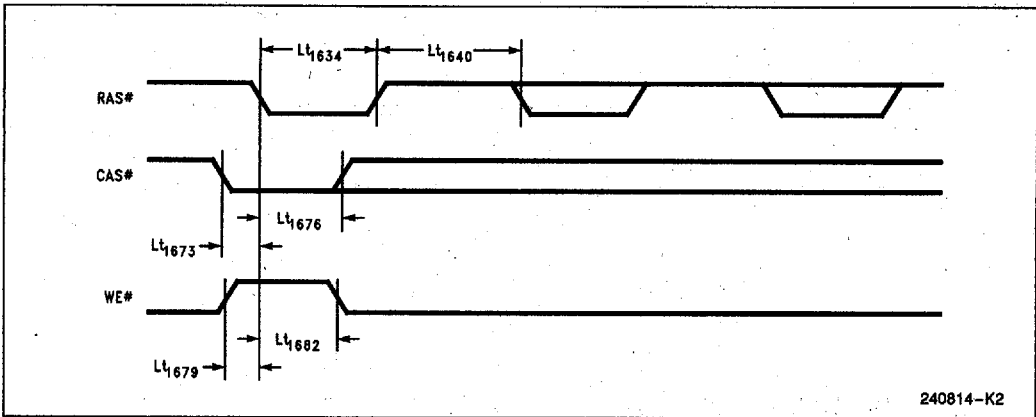


Figure 3.5.31. CAS# before RAS# Refresh Timings

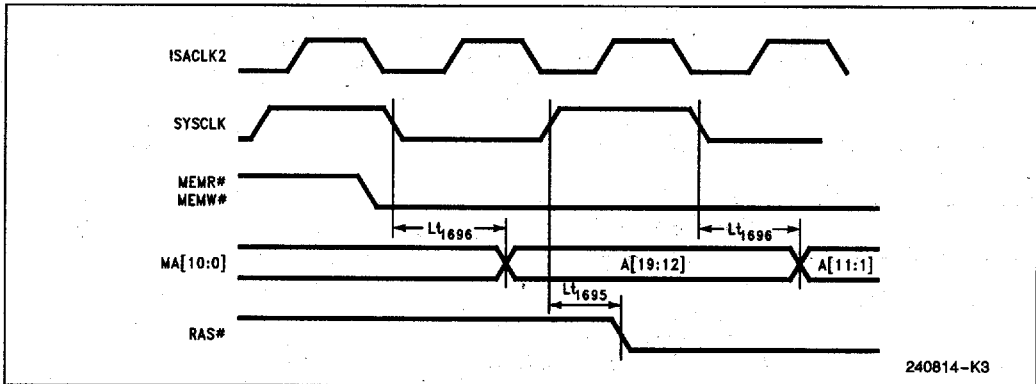


Figure 3.5.32. DMA/Master Timings (Address and RAS# Delay from SYSCLK)

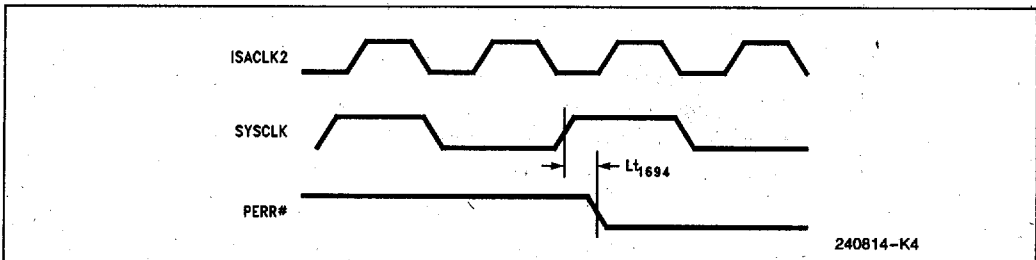


Figure 3.5.33. DMA/Master Timings (PERR# Delay from SYSCLK)



3.6 Power Sequencing Specifications

Since the low-voltage CPU is powered by two different supply voltages, 5.0V and 3.3V, proper sequencing of ramping up and down the voltage signals is necessary to ensure functional reliability of the chip. In Table 3.6-1, power sequencing parameters are

given as guidelines for system designers to follow when designing power supply circuitry. Waveforms that indicate all of the timing specifications are shown in Figures 3.6.1, 3.6.2 and 3.6.3.

3.6.1 A.C. SPECIFICATIONS

Table 3.6-1. Power Sequencing Timing Specifications

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
t3	PWRGOOD Turn on Delay from 3.0V of V _{CC3.3V} AND 4.5V of V _{CC5V} when Both V _{CCs} are Ramping Up	50		ms		3.6.1	
t5	PWRGOOD Inactive Setup Time to 3.0V of V _{CC3.3V} AND 4.5V of V _{CC5V} when Both V _{CCs} are Removed	10		μs		3.6.1	1
t7	PWRGOOD Hold from SUS_STAT# Active	5		ns		3.6.1	
t8	CPURESET Active Pulse and RESETDRV Active Pulse	50		ms		3.6.1	
t9	CPURESET Active Hold from PWRGOOD Active	3		ns		3.6.1	
t10	EFI & ISACK2 Stable from 3.0V of V _{CC3.3V} AND 4.5V of V _{CC5V}		40	ms		3.6.1	
t10a	EFI & ISACK2 Stable Hold from SUS_STAT# Active	46		μs		3.6.2	4

NOTES:

1. If a system initialization via RESETDRV (e.g., IDE HD park) is required during Power Down, 10 ms is recommended for this specification.
4. EFI & ISACK2 must hold stable until CPU enters into Suspend Refresh Mode (either RTC or Self Refresh).



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3.6 Power Sequencing Specifications (Continued)**Table 3.6-1. Power Sequencing Timing Specifications** (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
t11a	V _{CC5V} Ramp to 4.5V from Inactive SUS_STAT#		75	ms		3.6.1	
t11b	V _{CC3.3V} Ramp to 3.0V from Inactive SUS_STAT#		75	ms		3.6.1	
t11c	V _{CC3.3V} Turn ON Delay from Inactive SUS_STAT#	0		μs		3.6.1	
t11d	V _{CC5V} Turn ON Delay from Inactive SUS_STAT#	0		μs		3.6.1	
t11e	V _{CC3.3V} Turn OFF Delay from Active SUS_STAT#	0		μs		3.6.1	
t11f	V _{CC3.3V} Turn OFF Delay from Active SUS_STAT#	0		μs		3.6.1	
t11g	V _{CC3.3V} = 3V Lag from V _{CC5V} = 4.5V	0		ms			
t12	CPU 5V, SLIO 5V Power Ramping Delay from 3.0V to 5V	100		ns		3.6.2	2, 3
t13	CPU 5V, SLIO 5V Power Drooping in Delay from 5V to 3.0V	100		ns		3.6.2	2, 3
t20	CPURESET Active Delay from SUS_STAT# Inactive	125		ms		3.6.2	
t21	CPURESET Pulse Width Resume from 5V or 3.3V Suspend	90		μs		3.6.2	
t22	RESETDRV Delay from CPURESET	30		μs		3.6.2	
t23	EFI & ISACK2 Stable before PWRGOOD Active	10		μs		3.6.1	
t23a	EFI & ISACK2 Stable before CPURESET Active	10		μs		3.6.2	

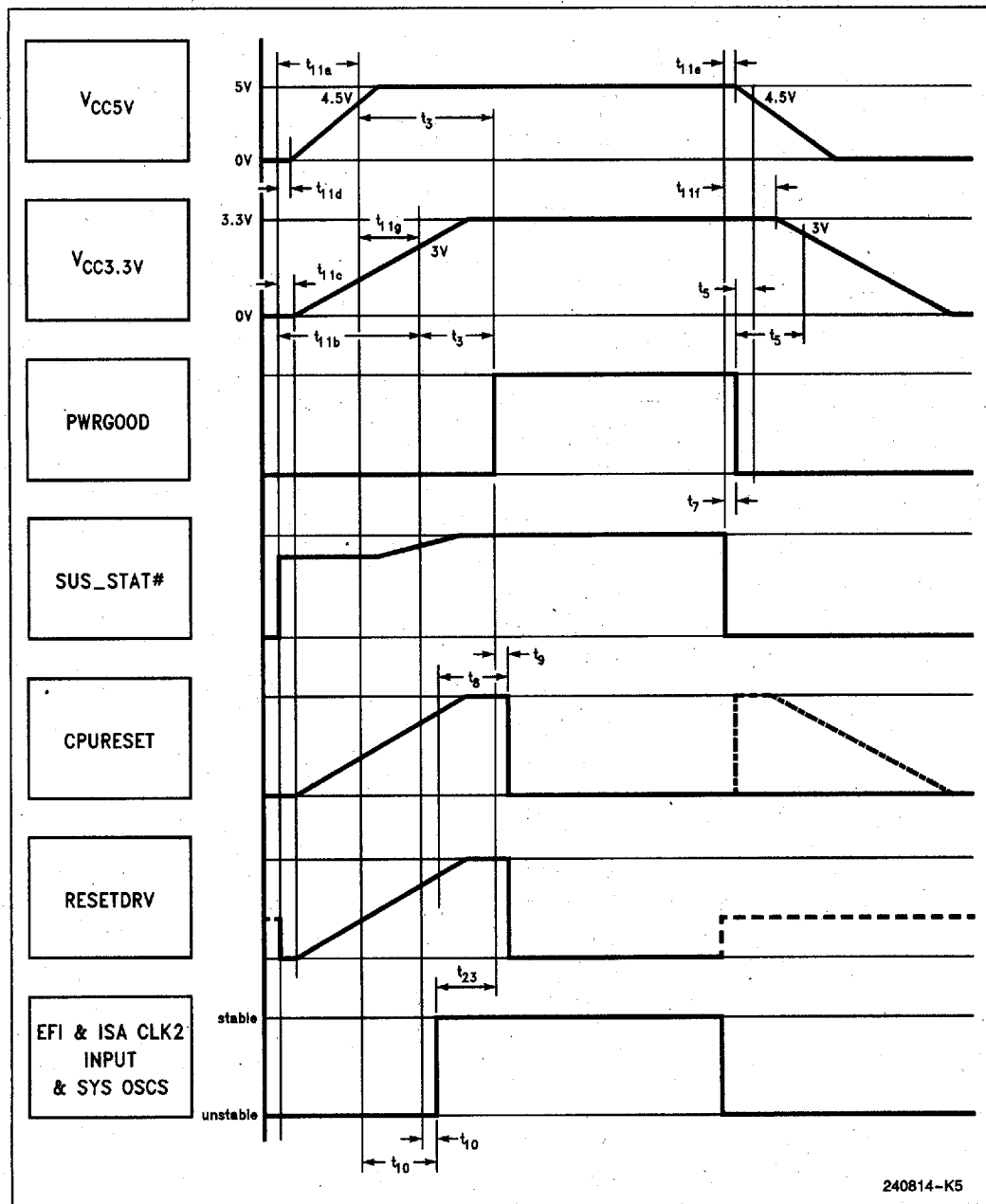
NOTES:

- All 5V signals should not exceed 0.3V above voltage of V_{CC} 5V pins when the system is entering 3.3V suspend (V_{CC5V} pins are drooping down from 5.0V to 3.3V) or when the system is in 3.3V Suspend mode (3.0V < V_{CC5V} pins < 3.6V) or when the system is exiting 3.3V-suspend. (V_{CC5V} pins are ramping up from 3.3V to 5.0V.)
- During 3.3V Suspend, all input signals except CPURESET, REFREQ, PWRGOOD, EFI, ISACK2 and SUS_STAT# are disabled by the CPU and all outputs except DRAM suspend control signals are held high, held low, or tristated.

3.6 Power Sequencing Specifications (Continued)

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3.6.2 TIMING DIAGRAMS

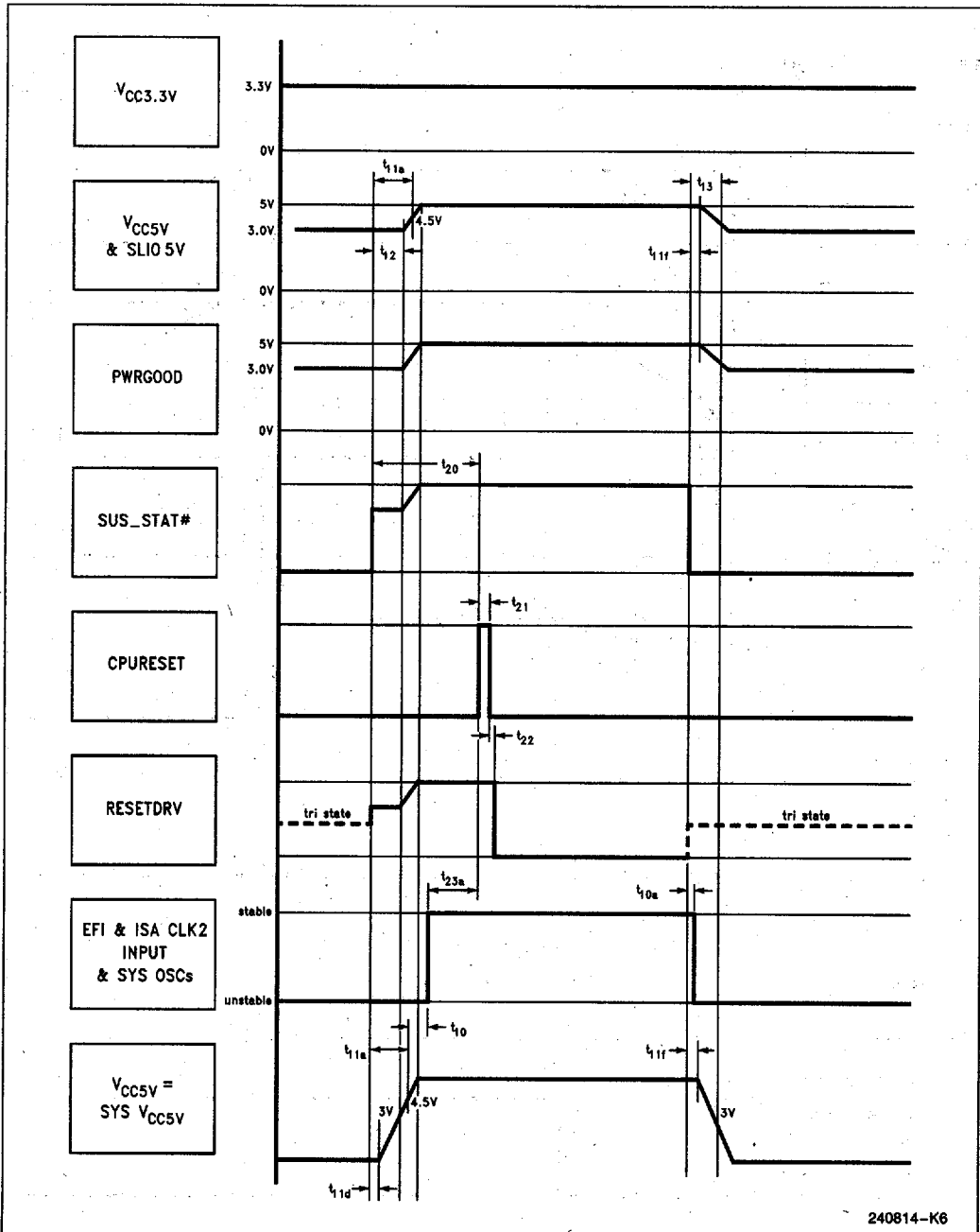


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Figure 3.6.1. Power Up/Down Sequence

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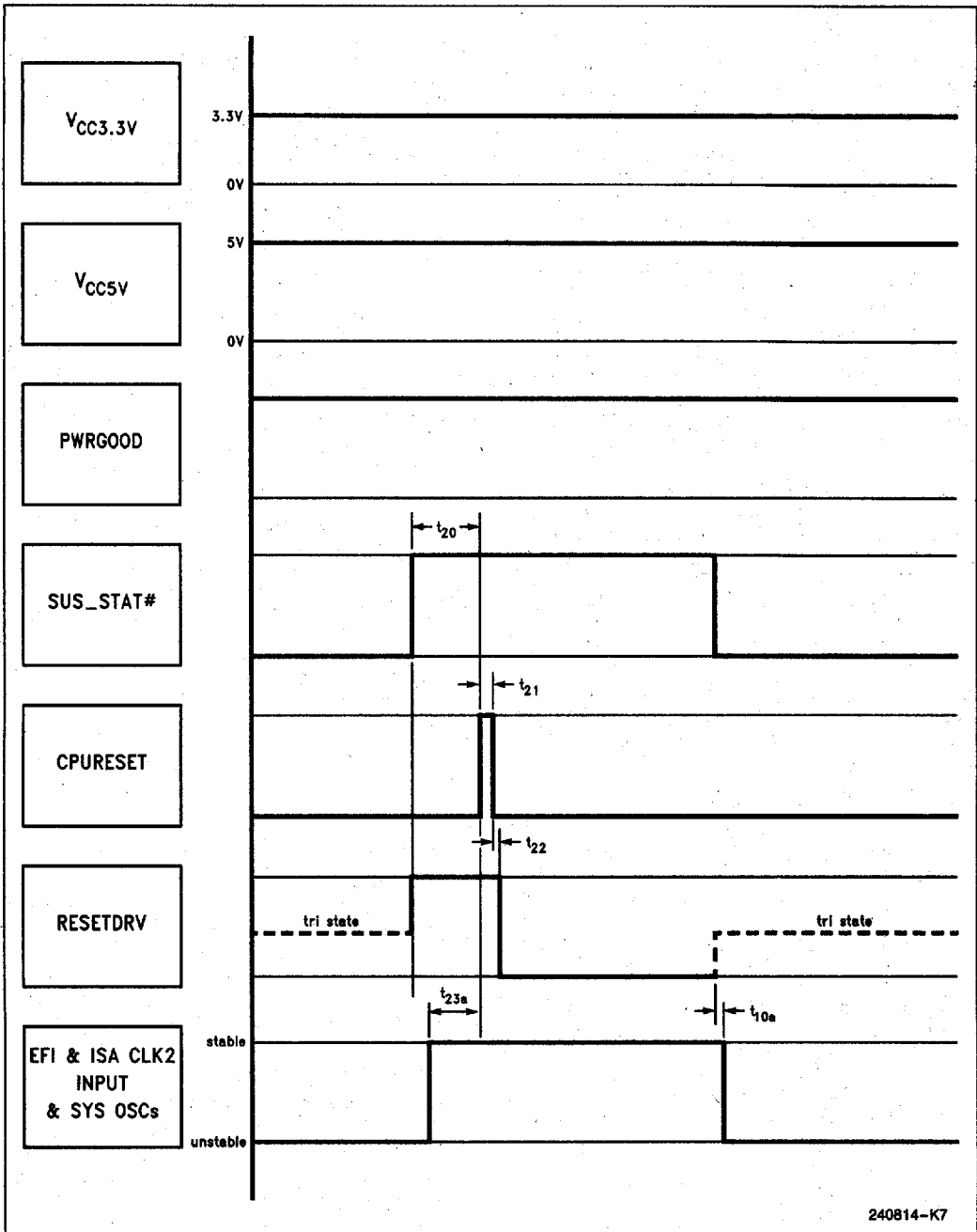
3.6 Power Sequencing Specifications (Continued)



240814-K6

Figure 3.6.2. Suspend/Resume Sequence for 3.3V Suspend/Resume System

3.6 Power Sequencing Specifications (Continued)



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Figure 3.6.3. Suspend/Resume Sequence for 5V Suspend/Resume System

3.7 Capacitive Derating Information

In the A.C. timing tables presented in Section 3.4, all max and min timings are tested at a load of 50 pF. All max timings are specified at the maximum load condition for the pin and all min timings are specified for the minimum load conditions for the pin.

If the load on a pin falls within the range of the min and max capacitance specified, no derating calculations need to be done for synchronous timings. If a lighter or heavier capacitive load is connected to any pin, signal delay will change. To allow the system designer to account for such loading differences in a system, a family of capacitive derating curves are provided in this section.

The derating curves are divided into four groups—Fast rise, fast fall, slow rise and slow fall curves. Each group has one curve for the buffer type associated with the pin corresponding to a signal. Depending upon the parameter for which the timing is being specified, curves of different groups should be used to derate the specification. The group to be used is given in the column "Derating" associated with each specification. The nomenclature used in this column is as follows: FR = Fast Rise, SR = Slow Rise, FF = Fast Fall, SF = Slow Fall. The curve corresponding to the signal in question may be found from the "Derating curve" column of the pin assignment table in Section 3.1.

In the case of output timing specifications, two group notations appear in the "Derating" column. The first of these corresponds to the reference signal and the second corresponds to the target signal.

When a specification is made about a bus or the specification is valid for both rise and fall times, only the type of derating is specified. For instance, F = Fast curve, S = Slow curve. Either the rise or the fall time derating may be used. To make a conservative calculation, use the smaller derating value among rise and fall for fast curves and the larger derating value for the slow curves.

When a specification has both a min and a max time, the derating curves for the min and the max times are separated by a semi-colon.

If loading conditions are not specified in the notes column, the timing parameter is specified for the worst case loading possible.

The rationale in the assignment of derating curves to specifications is as follows.

1. For synchronous (Clock related) specifications, all maximum timings are derated from slow curves. This is the worst case situation.

2. For synchronous (Clock related) specifications, all minimum timings are derated from fast curves. The reasoning here is that fast parts cause the worst case for minimum timings since the signal transition occurs earlier than for slow parts. Since these fast parts have fast buffers, the fast derating curves are used.

3. For output to output timings, the derating curve to be chosen depends on a combination of internal delays and buffer delays in fast and slow parts. From an analysis of the worst case situation, appropriate curves are selected for the system designer.

To use the derating curves, follow the procedure outlined here.

1. From the "Derating" column of A.C. timing table in Section 3.4, find the group of curves that must be used for a particular specification.

2. From the Pin assignment chart in Section 3.1, find the letter corresponding to the signal(s) under consideration from the column "Derating Curve".

3. In this section, find the derating curve of the correct group and letter.

4. Calculate the capacitive loading on the signal(s) under consideration.

5. Find this load point on the capacitive load axis of the derating curve.

6. Project a vertical line to the derating curve from the load point and draw a horizontal line and from the point the vertical line intersects the curve.

7. Estimate the amount of time from the Nominal point to the point where the horizontal line meets the delay axis. This is the derating value for the signal under consideration.

8. If the point where the horizontal meets the delay axis is **above** the nominal value, then

If the signal under consideration is **the reference signal** (in output to output timings) the derating value should be **subtracted** from the timing specification.

If the signal under consideration is **the target signal** (in all timings) the derating value should be **added** to the timing specification.

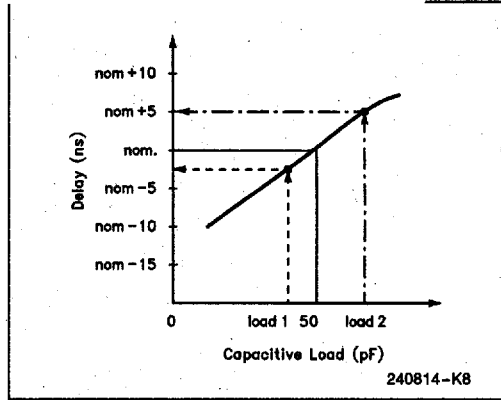
9. If the point where the horizontal meets the delay axis is **below** the nominal value, then

If the signal under consideration is **the reference signal** (in output to output timings) the derating value should be **added** to the timing specification.

If the signal under consideration is **the target signal** (in all timings) the derating value should be **subtracted** from the timing specification.

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In some output to output specifications, the loads are not at the nominal points for the curves specified. The loads at which the specifications are made are indicated in the notes column. The same procedure as above may be used for derating except that a nominal point corresponding to the load specified must first be found on the curve specified.



Using the Capacitive Derating Curves



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**Intel386™ SL CPU Maximum Derating Curves
in FlexibleVoltage Mode—5V Signals**

Rising

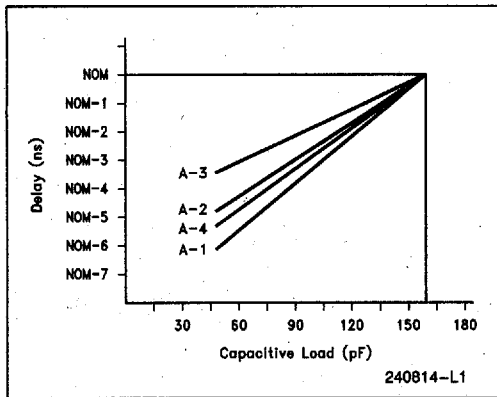


Figure 3.7.1a

Falling

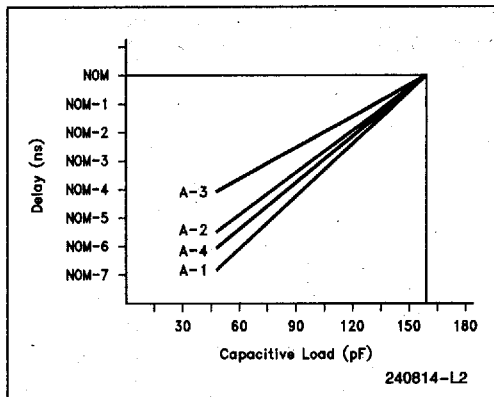


Figure 3.7.1b

Rising

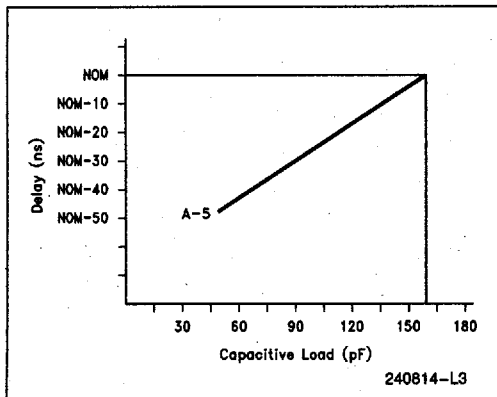


Figure 3.7.2a

Falling

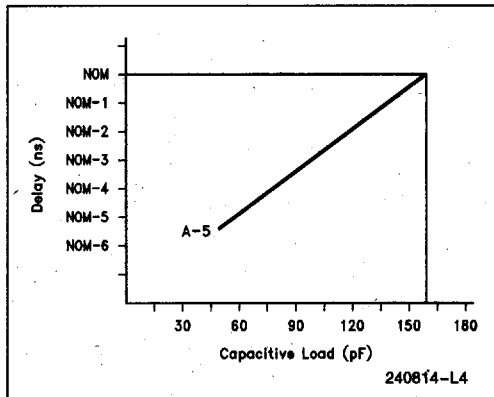


Figure 3.7.2b

**Intel386™ SL CPU Maximum Derating Curves
in Flexible Voltage Mode—5V Signals (Continued)**

Rising

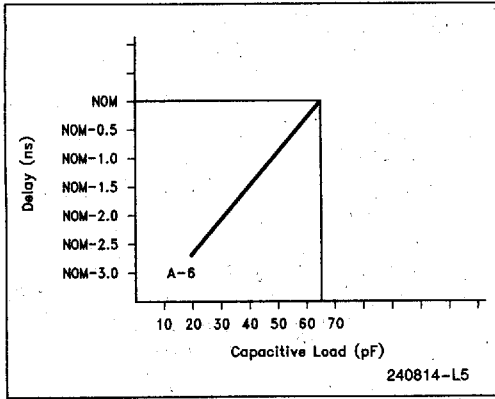


Figure 3.7.3a

Falling

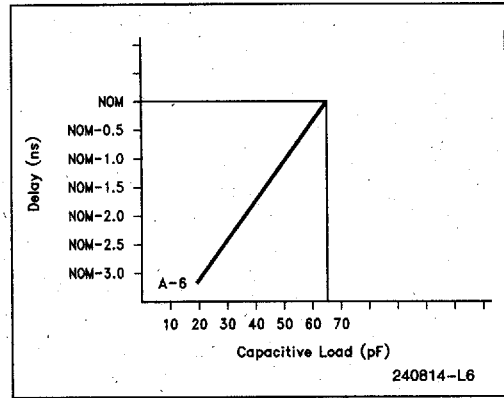


Figure 3.7.3b

Rising

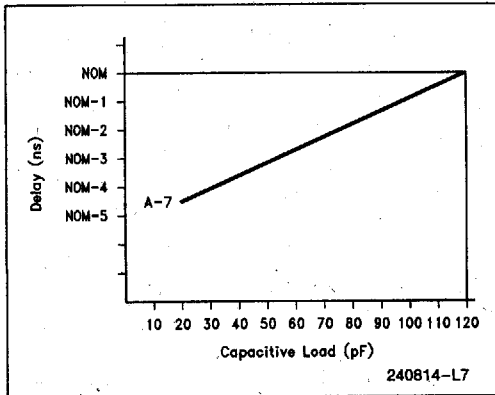


Figure 3.7.4a

Falling

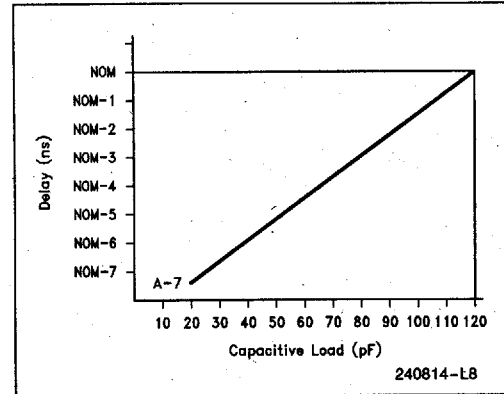


Figure 3.7.4b

2

Intel386™ SL CPU Maximum Derating Curves
in Flexible Voltage Mode—5V Signals (Continued)

Rising

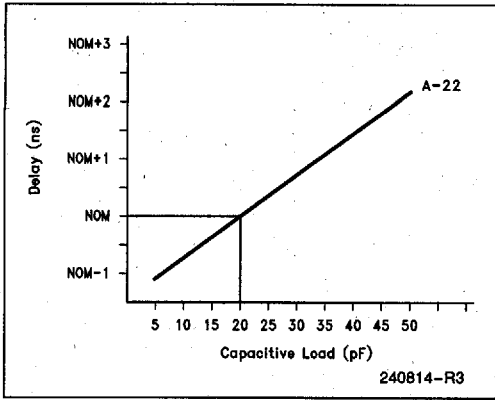


Figure 3.7.5a

Falling

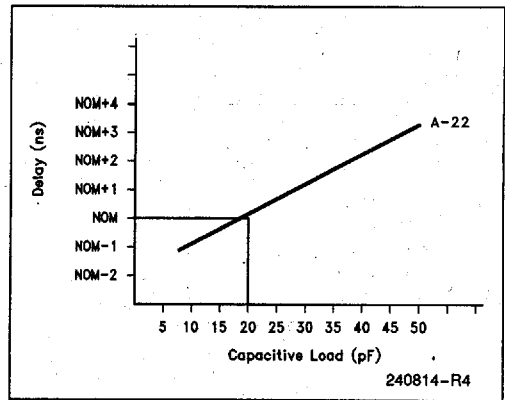


Figure 3.7.5b

**Intel386™ SL CPU Maximum Derating Curves
in Flexible Voltage Mode—3.3V Signals**

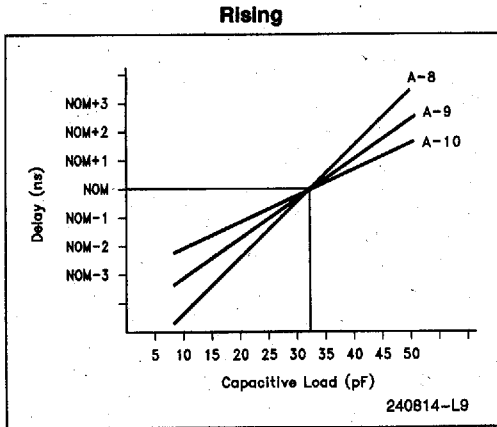


Figure 3.7.6a

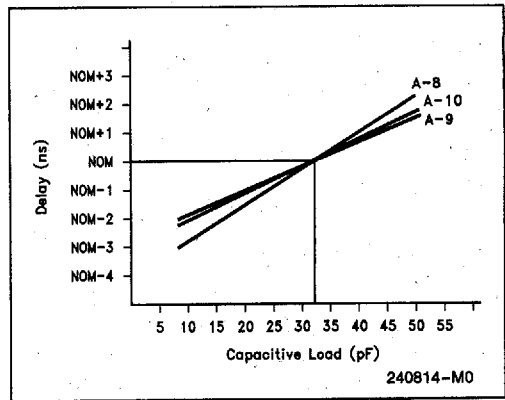


Figure 3.7.6b

2

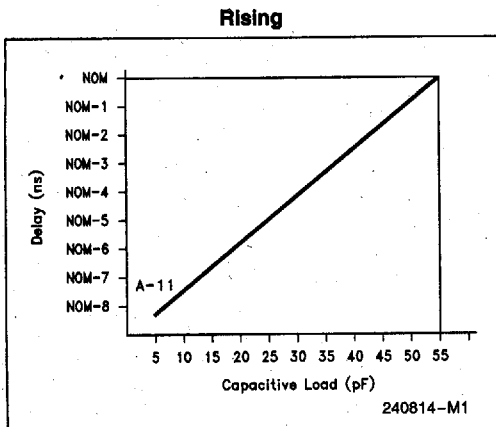


Figure 3.7.7a

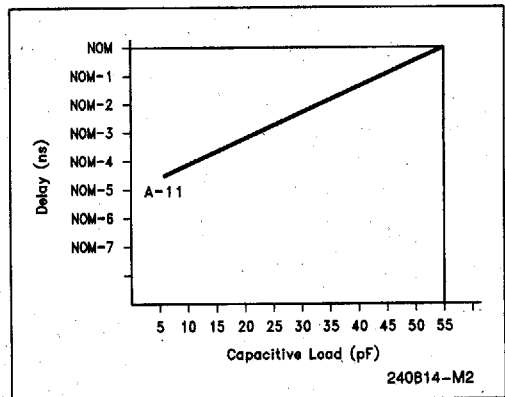


Figure 3.7.7b

**Intel386™ SL CPU Maximum Derating Curves
in FlexibleVoltage Mode—3.3V Signals (Continued)**

Rising

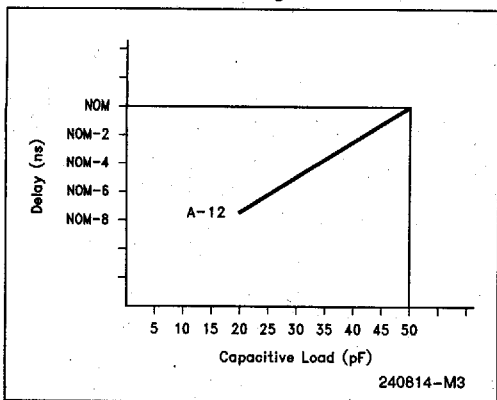


Figure 3.7.8a

Falling

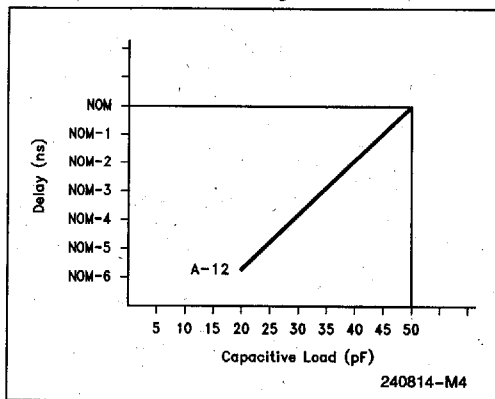


Figure 3.7.8b

Rising

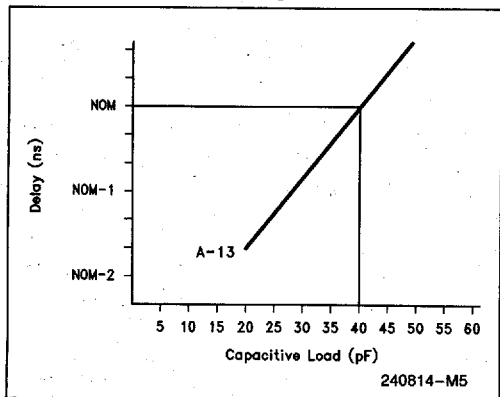


Figure 3.7.9a

Falling

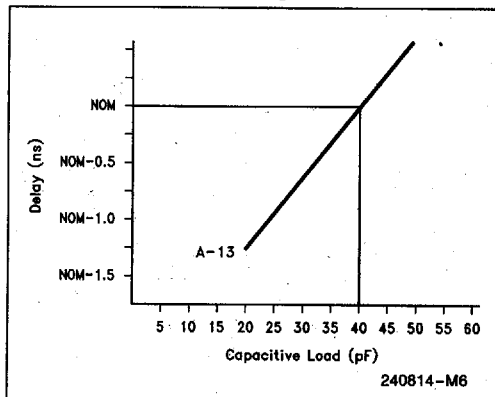


Figure 3.7.9b



Intel386™ SL CPU Maximum Derating Curves
in FlexibleVoltage Mode—3.3V Signals (Continued)

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2

Rising

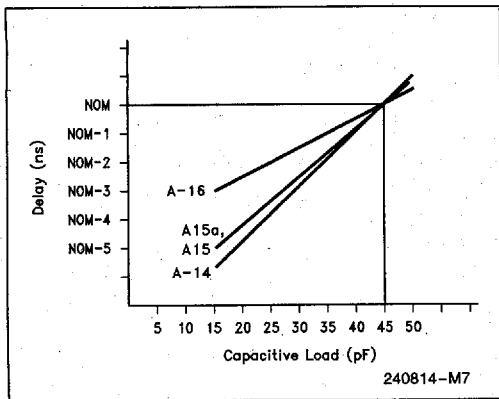


Figure 3.7.10a

Falling

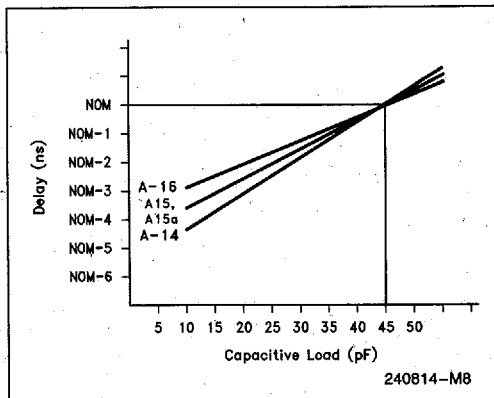


Figure 3.7.10b

Rising

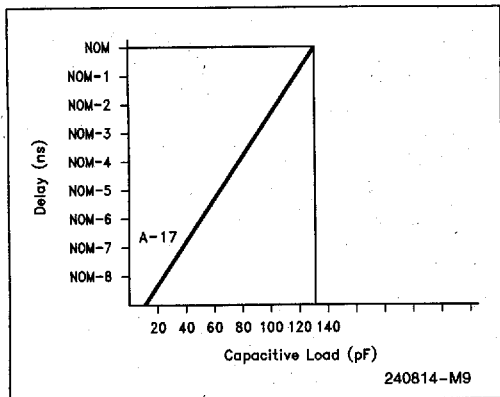


Figure 3.7.11a

Falling

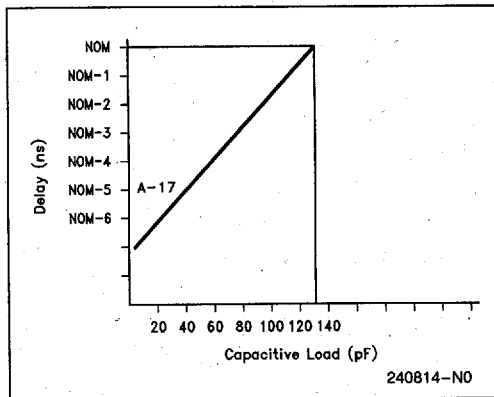


Figure 3.7.11b

**Intel386™ SL CPU Maximum Derating Curves
in FlexibleVoltage Mode—3.3V Signals (Continued)**

Rising

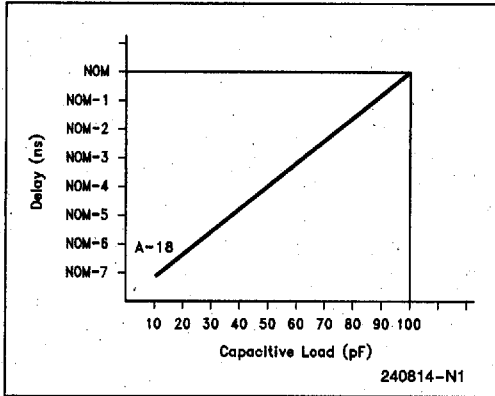


Figure 3.7.12a

Falling

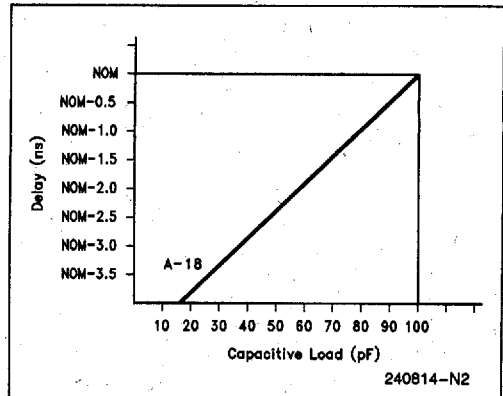


Figure 3.7.12b

Rising

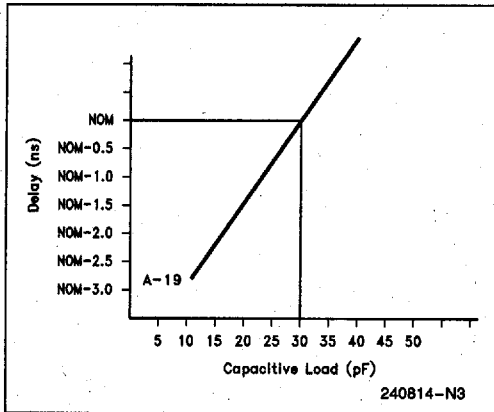


Figure 3.7.13a

Falling

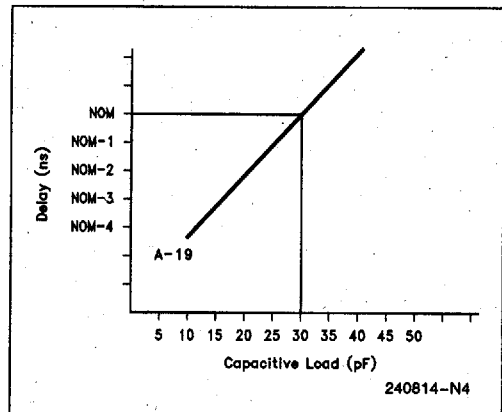


Figure 3.7.13b

**Intel386™ SL CPU Maximum Derating Curves
in FlexibleVoltage Mode—3.3V Signals (Continued)**

Rising

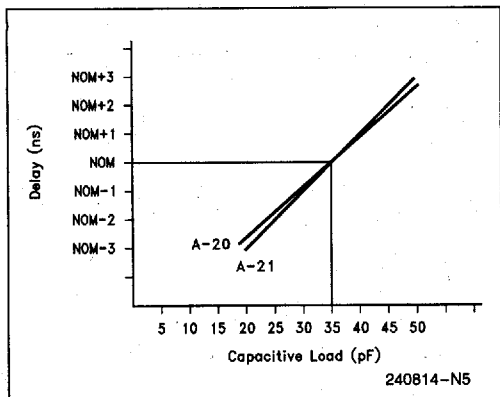


Figure 3.7.14a

Falling

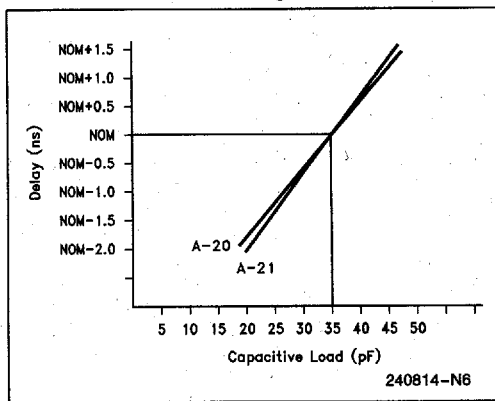


Figure 3.7.14b

56E D ■ 4826175 0119243 210 ■ ITL1 T-49-17-34

Intel386™ SL CPU Minimum Derating Curves
in FlexibleVoltage Mode—5V Signals

Rising

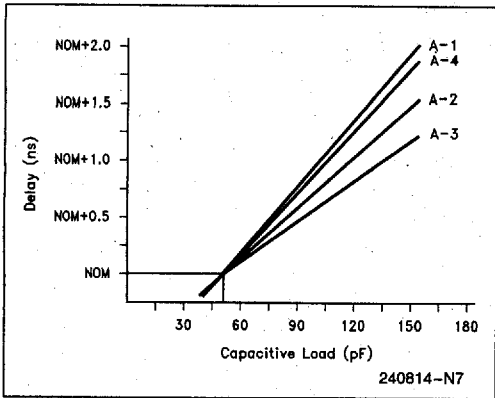


Figure 3.7.15a

Falling

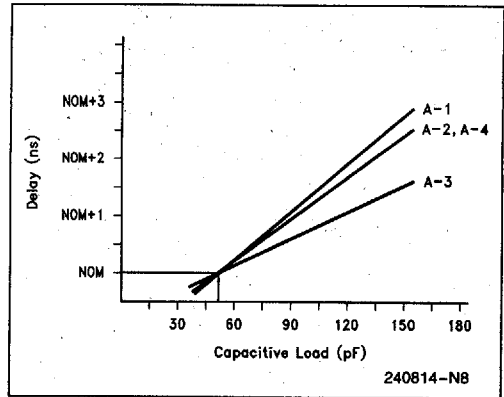


Figure 3.7.15b

Rising

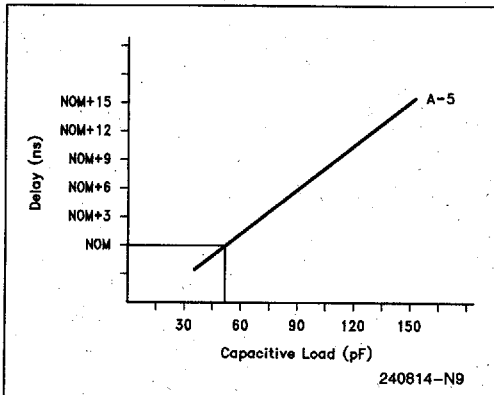


Figure 3.7.16a

Falling

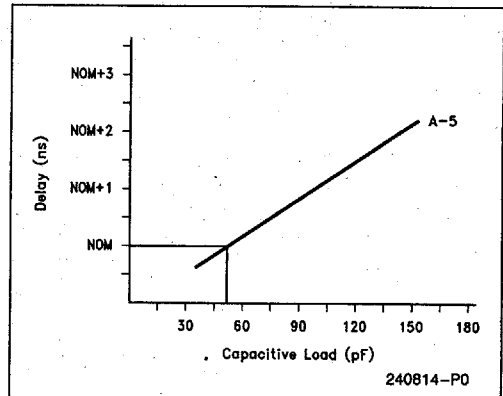


Figure 3.7.16b



56E D ■ 4826175 0119244 157 ■ ITL1

Intel386™ SL CPU Minimum Derating Curves
in FlexibleVoltage Mode—5V Signals (Continued)

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Rising

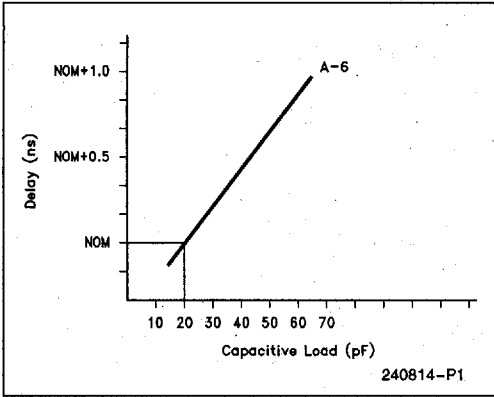


Figure 3.7.17a

Falling

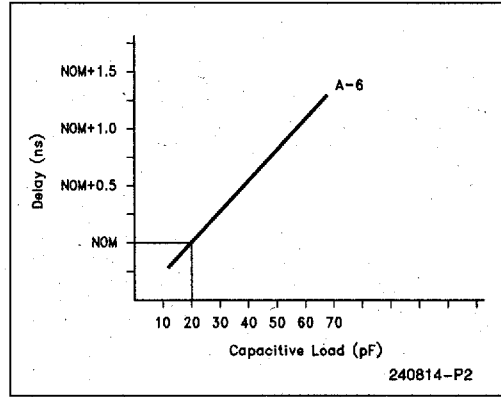


Figure 3.7.17b

Rising

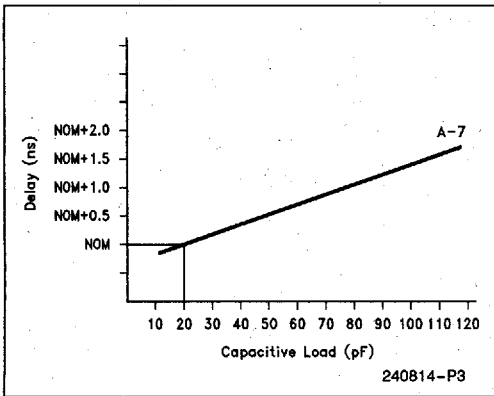


Figure 3.7.18a

Falling

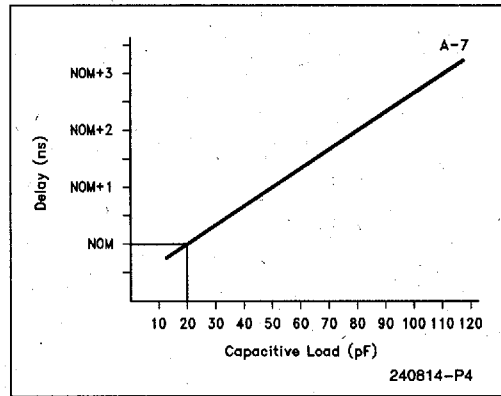


Figure 3.7.18b

Intel386™ SL CPU Minimum Derating Curves in Flexible Voltage Mode—5V Signals (Continued)

Rising

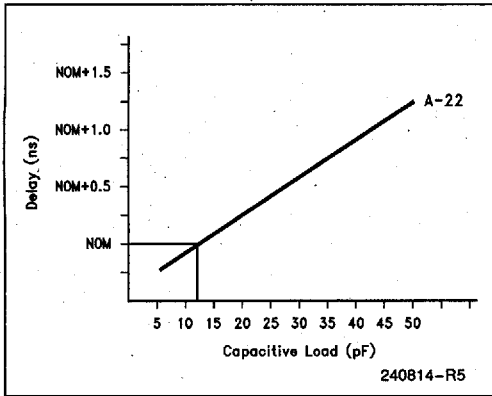


Figure 3.7.19a

Falling

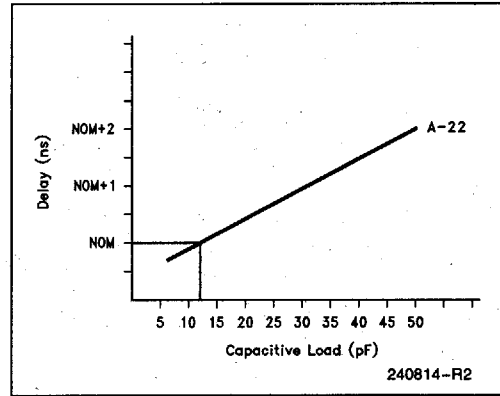


Figure 3.7.19b

Intel386™ SL CPU Minimum Derating Curves
in Flexible Voltage Mode—3.3V Signals

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2

Rising

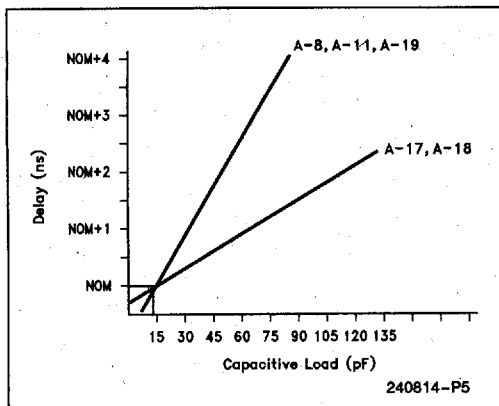


Figure 3.7.20a

Falling

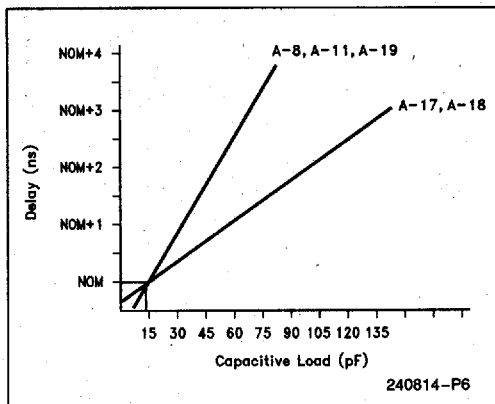


Figure 3.7.20b

Rising

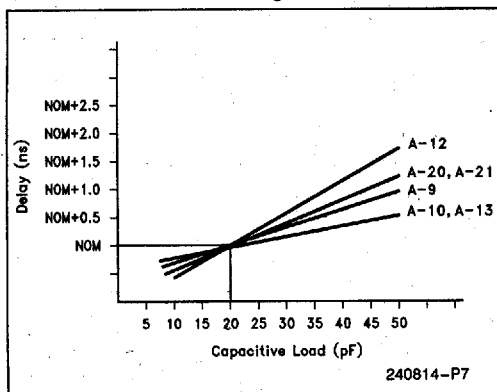


Figure 3.7.21a

Falling

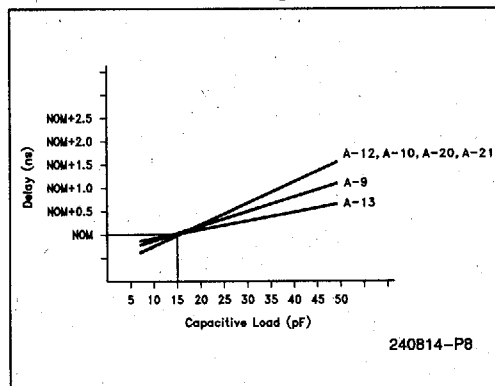


Figure 3.7.21b



56E D ■ 4826175 0119247 966 ■ ITL1

Intel386™ SL CPU Minimum Derating Curves
in Flexible Voltage Mode—3.3V Signals (Continued)

T-49-17-34

Rising

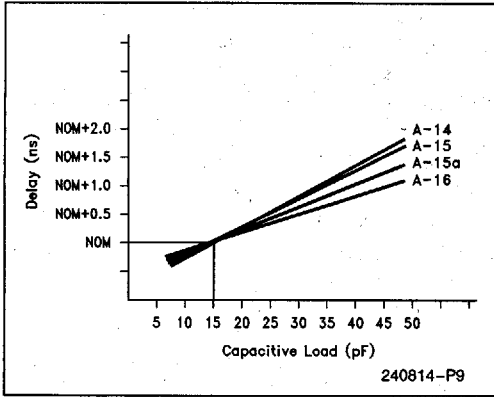


Figure 3.7.22a

Falling

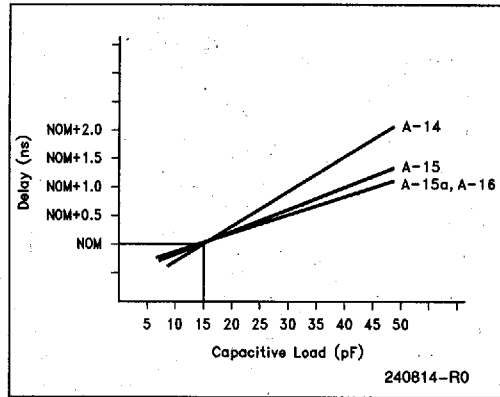


Figure 3.7.22b



56E D ■ 4826175 0119248 8T2 ■ ITL1

4.0 82360SL I/O

4.1 Pin Assignments and Signal Characteristics

Section 4.1 provides information for the 82360SL I/O pin assignment with respect to the signal

mnemonics. In addition to the package pin out diagrams, two tables are provided for easy location of signals. The table lists the 82360SL package device pinouts in the 196 lead JEDEC Plastic Quad Flat Package (PQFP). The table also includes additional information for the signals and associated pin numbers. A brief explanation of each column of the table is given in Table 4.1-1.

Table 4.1-1. Description of the Columns of Tables 4.1-2

PQFP	This column lists the pin numbers of the Intel386 SL CPU and the 82360SL in a Plastic Quad Flat Package.
Signal Name	This column lists the signal name associated with the package pins.
Type	Indicates whether the pin is an Input (I), an Output (O) or an Input-Output (IO).
Term	Specifies the internal terminator on the pin. This could be an internal pull-up or pull-down resistor value or a hold circuit. Pull-up (PU) or Pull-down (PD) is indicated in the Term column.(2)
Drive	Specifies the drive current I_{OL} (Current Output Logic Low) and I_{OH} (Current Output Logic High) in milli-Amperes (mA) for output (O), and bi-directional (IO), pins.
Load	This column lists the maximum specified capacitive load which the buffer can directly drive in pico-Farads (pF) for each signal. This is specified for output and input-output pins only.
Susp.	This column specifies the state of the pin during a suspend operation. Input signals have the representation Tri. This indicates that the input is internally isolated and that the internal termination on the pin is tri-stated or disabled. The additional output buffer abbreviations are explained below. Tri - Tristated Actv - Active (Active input signals must be held at valid logic levels) 0 - held low 1 - held high Hold - held at last state
ONCE	This column specifies the state of the pin when the ONCE# (On Circuit Emulator) pin is asserted, allowing in-circuit testing while the device is still populated on the logic board. Tri - Floats Actv - Active 0 - held low 1 - held high Hold - held at last state
Derating Curve	This column specifies which derating curve(1) is used for each output buffer associated with the pin.

NOTE:

- For more information on derating curves and how to use them, see Section 4.6 (Capacitive Derating Information).
- Typical resistor values are given as guidelines only. Not tested.

2

56E D 4826175 0119249 739 ITL1

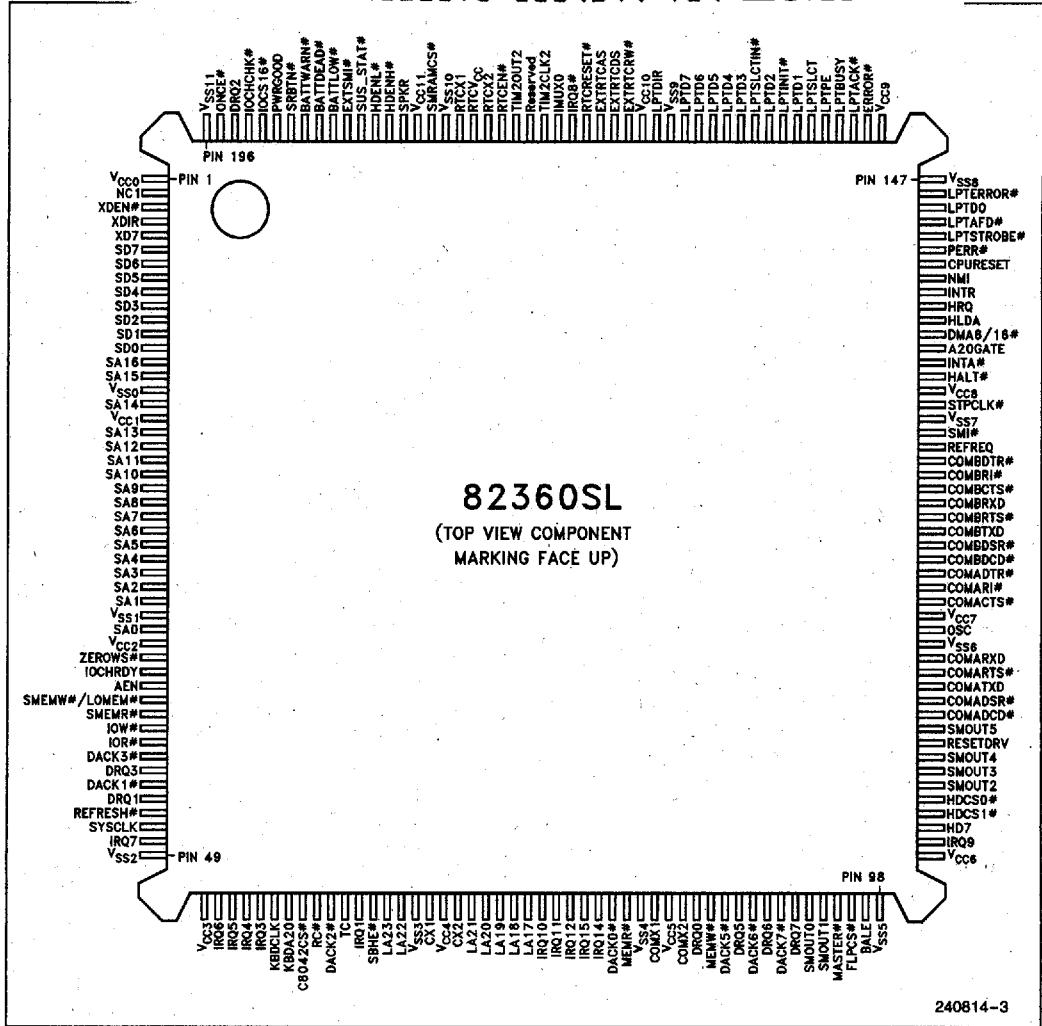


Figure 4.1.1. Pin Assignments for the 82360SL in a 196-Lead Plastic Quad Flat Package



56E D ■ 4826175 0119250 450 ■ ITL1 T-49-17-34

Table 4.1-2. 82360SL Pin Characteristics

Signal Name	PQFP Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	ONCE	Derating Curve
A20GATE	B135	O		12, 2	20, 50	Tri	Tri	B-7
AEN	B37	O		24, 4	50, 240	Tri	Tri	B-4
BALE	B97	I				Tri	Tri	
BATTDEAD#	B188	I				Actv	Tri	
BATTLOW#	B187	I				Actv	Tri	
BATTWARN#	B189	I	60K PU			Tri	Tri	
C8042CS#	B57	O		12, 2	20, 50	Tri	Tri	B-7
COMACTS#	B117	I	60K PU			Tri	Tri	
COMADCD#	B109	I	60K PU			Tri	Tri	
COMADSR#	B110	I	60K PU			Tri	Tri	
COMADTR#	B119	O		12, 2	20, 50	Tri	Tri	B-7
COMARI#	B118	I	60K PU			Actv ⁽¹⁾	Tri	
COMARTS#	B112	O		12, 2	20, 50	Tri	Tri	B-7
COMARXD	B113	I	20K PD			Tri	Tri	
COMATXD	B111	O		12, 2	20, 50	Tri	Tri	B-7
COMBCTS#	B125	I	60K PU			Tri	Tri	
COMBDCCD#	B120	I	60K PU			Tri	Tri	
COMBDSR#	B121	I	60K PU			Tri	Tri	
COMBDTR#	B127	O		12, 2	20, 50	Tri	Tri	B-7
COMBRI#	B126	I	60K PU			Actv ⁽¹⁾	Tri	
COMBRTS#	B123	O		12, 2	20, 50	Tri	Tri	B-7
COMBRXD	B124	I	20K PD			Tri	Tri	
COMBTXD	B122	O		12, 2	20, 50	Tri	Tri	B-7
COMX1	B82	I				Tri	Tri	
COMX2	B84	O				1	1	B-7
CPURESET	B141	O		12, 2	20, 50	Actv	Tri	B-7
CX1	B66	I				Tri	Tri	
CX2	B68	O				1	1	B-7
DACK0#	B79	O		12, 2	20, 50	Tri	Tri	B-7
DACK1#	B44	O		12, 2	20, 50	Tri	Tri	B-7
DACK2#	B59	O		12, 2	20, 50	Tri	Tri	B-7
DACK3#	B42	O		12, 2	20, 50	Tri	Tri	B-7
DACK5#	B87	O		12, 2	20, 50	Tri	Tri	B-7
DACK6#	B89	O		12, 2	20, 50	Tri	Tri	B-7
DACK7#	B91	O		12, 2	20, 50	Tri	Tri	B-7

NOTE:

1. These pins can be programmed to remain isolated during suspend.



56E D ■ 4826175 0119251 397 ■ ITL1 T-49-17-34

Table 4.1-2. 82360SL Pin Characteristics (Continued)

Signal Name	PQFP Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	ONCE	Derating Curve
DMA8/16#	B136	O		12, 2	20, 50	Tri	Tri	B-7
DRQ0	B85	I	20K PD			Tri	Tri	
DRQ1	B45	I	20K PD			Tri	Tri	
DRQ2	B194	I	20K PD			Tri	Tri	
DRQ3	B43	I	20K PD			Tri	Tri	
DRQ5	B88	I	20K PD			Tri	Tri	
DRQ6	B90	I	20K PD			Tri	Tri	
DRQ7	B92	I	20K PD			Tri	Tri	
ERROR#	B149	I	60K PU			Tri	Tri	
EXTRTCRW#	B166	O	60K PU	12, 2	20, 50	1	Tri	B-7
EXTRTCAS	B168	O	20K PD	12, 2	20, 50	0	Tri	B-7
EXTRTCDS	B167	O	60K PU	12, 2	20, 50	1	Tri	B-7
EXTSMI#	B186	I	60K PU			Tri	Tri	
FLPCS#	B96	O		12, 2	20, 50	Tri	Tri	B-7
HALT#	B133	I	60K PU			Tri	Tri	
HD7	B101	IO	60K PU	24, 4	20, 100	Tri	Tri	B-3
HDCS0#	B103	O		12, 2	20, 50	Tri	Tri	B-7
HDCS1#	B102	O		12, 2	20, 50	Tri	Tri	B-7
HDENH#	B183	O		12, 2	20, 50	Tri	Tri	B-7
HDENL#	B184	O		12, 2	20, 50	Tri	Tri	B-7
HLDA	B137	I	20K PD			Tri	Tri	
HRQ	B138	O		12, 2	20, 50	Tri	Tri	B-7
IMUX0	B171	I	20K PD			Tri	Tri	
INTA#	B134	I	60K PU			Tri	Tri	
INTR	B139	O		12, 2	20, 50	Tri	Tri	B-7
IOCHCK#	B193	I	4.7K PU			Tri	Tri	
IOCHRDY	B36	IO OD		24, 4	20, 240	Tri	Tri	B-8
IOCS16#	B192	I				Tri		
IOR#	B41	IO		24, 4	50, 240	Tri	Tri	B-2
IOW#	B40	IO		24, 4	50, 240	Tri	Tri	B-2
IRQ1	B61	I	10K PU			Tri	Tri	
IRQ3	B54	I	10K PU			Tri	Tri	
IRQ4	B53	I	10K PU			Tri	Tri	
IRQ5	B52	I	10K PU			Tri	Tri	
IRQ6	B51	I	10K PU			Tri	Tri	
IRQ7	B48	I	10K PU			Tri	Tri	

intel.

Intel386™ SL SuperSet

ADVANCE INFORMATION

56E D ■ 4826175 0119252 223 ■ ITL1

Table 4.1-2. 82360SL Pin Characteristics (Continued)

Signal Name	PQFP Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	ONCE	Derating Curve
IRQ8#	B170	I	20K PD			Actv	Tri	
IRQ9	B100	I	10K PU			Tri	Tri	
IRQ10	B74	I	10K PU			Tri	Tri	
IRQ11	B75	I	10K PU			Tri	Tri	
IRQ12	B76	I	10K PU			Tri	Tri	
IRQ14	B78	I	10K PU			Tri	Tri	
IRQ15	B77	I	10K PU			Tri	Tri	
KBDA20	B56	I	60K PU			Tri	Tri	
KBDCLK	B55	O		12, 2	20, 50	Tri	Tri	B-7
LA17	B73	IO		24, 4	50, 240	Tri	Tri	B-1
LA18	B72	IO		24, 4	50, 240	Tri	Tri	B-1
LA19	B71	IO		24, 4	50, 240	Tri	Tri	B-1
LA20	B70	IO		24, 4	50, 240	Tri	Tri	B-1
LA21	B69	IO		24, 4	50, 240	Tri	Tri	B-1
LA22	B64	IO		24, 4	50, 240	Tri	Tri	B-1
LA23	B63	IO		24, 4	50, 240	Tri	Tri	B-1
LPTACK#	B150	I	60K PU			Tri	Tri	
LPTAFD#	B144	O OD(1)	4.7K PU	12	20, 100	Tri	Tri	B-6
LPTBUSY	B151	I	20K PU			Tri	Tri	
LPTD0	B145	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD1	B154	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD2	B156	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD3	B158	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD4	B159	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD5	B160	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD6	B161	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTD7	B162	IO	20K PD	8, 2	20, 100	Tri	Tri	B-5
LPTDIR	B164	O OD(1)	4.7K PU	12	20, 100	Tri	Tri	B-6
LPTERROR#	B146	I	60K PU			Tri	Tri	
LPTINIT#	B155	O OD(1)	4.7K PU	12	20, 100	Tri	Tri	B-6
LPTPE	B152	I	20K PD			Tri	Tri	
LPTSLCT	B153	I	20K PD			Tri	Tri	
LPTSLCTIN#	B157	O OD(1)	4.7K PU	12	20, 100	Tri	Tri	B-6
LPTSTROBE#	B143	O OD(1)	4.7K PU	12	20, 100	Tri	Tri	B-6

NOTE:

1. These outputs become CMOS drivers when bit 7 of the FPP_CNTRL register is set.



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Table 4.1-2. 82360SL Pin Characteristics (Continued)

Signal Name	PQFP Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	ONCE	Derating Curve
MASTER#	B95	I				Tri	Tri	
MEMR#	B80	IO		24, 4	20, 240	Tri	Tri	B-2
MEMW#	B86	IO		24, 4	20, 240	Tri	Tri	B-2
NC	B2							
NMI	B140	O		12, 2	20, 50	Tri	Tri	B-7
ONCE#	B195	I	60K PU			Tri	Actv	
OSC	B115	O		24	50, 240	Tri	Tri	B-4
PERR#	B142	I	60K PU			Tri	Tri	
PWRGOOD	B191	I				Actv	Tri	
RC#	B58	I	60K PU			Tri	Tri	
REFREQ	B128	O		12, 2	20, 50	Actv	Tri	B-7
REFRESH#	B46	IO OD	1.2K PU	8	50, 240	Tri	Tri	B-4
RESETDRV	B107	O		24	50, 240	Tri	Tri	B-4
RTCEN#	B175	I				Actv	Tri	
RTCRESET#	B169	I				Actv	Tri	
RTCVCC	B177							
RTCX1	B178	I				Actv	Tri	
RTCX2	B176	O				Actv	1	B-7
Reserved	B173							
SA0	B33	IO		24, 4	50, 240	Tri	Tri	B-1
SA1	B31	IO		24, 4	50, 240	Tri	Tri	B-1
SA2	B30	IO		24, 4	50, 240	Tri	Tri	B-1
SA3	B29	IO		24, 4	50, 240	Tri	Tri	B-1
SA4	B28	IO		24, 4	50, 240	Tri	Tri	B-1
SA5	B27	IO		24, 4	50, 240	Tri	Tri	B-1
SA6	B26	IO		24, 4	50, 240	Tri	Tri	B-1
SA7	B25	IO		24, 4	50, 240	Tri	Tri	B-1
SA8	B24	IO		24, 4	50, 240	Tri	Tri	B-1
SA9	B23	IO		24, 4	50, 240	Tri	Tri	B-1
SA10	B22	IO		24, 4	50, 240	Tri	Tri	B-1
SA11	B21	IO		24, 4	50, 240	Tri	Tri	B-1
SA12	B20	IO		24, 4	50, 240	Tri	Tri	B-1
SA13	B19	IO		24, 4	50, 240	Tri	Tri	B-1



Table 4.1-2. 82360SL Pin Characteristics (Continued)

Signal Name	PQFP Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	ONCE	Derating Curve
SA14	B17	IO		24, 4	50, 240	Tri	Tri	B-1
SA15	B15	IO		24, 4	50, 240	Tri	Tri	B-1
SA16	B14	IO		24, 4	50, 240	Tri	Tri	B-1
SBHE#	B62	O		24, 4	50, 240	Tri	Tri	B-4
SD0	B13	IO		24, 4	50, 240	Tri	Tri	B-2
SD1	B12	IO		24, 4	50, 240	Tri	Tri	B-2
SD2	B11	IO		24, 4	50, 240	Tri	Tri	B-2
SD3	B10	IO		24, 4	50, 240	Tri	Tri	B-2
SD4	B9	IO		24, 4	50, 240	Tri	Tri	B-2
SD5	B8	IO		24, 4	50, 240	Tri	Tri	B-2
SD6	B7	IO		24, 4	50, 240	Tri	Tri	B-2
SD7	B6	IO		24, 4	50, 240	Tri	Tri	B-2
SMEMR#/LOMEM#	B39	O	60K PU	24, 4	50, 240	Tri	Tri	B-4
SMEMW#	B38	O	60K PU	24, 4	50, 240	Tri	Tri	B-4
SMI#	B129	O		12, 2	20, 50	Tri	Tri	B-7
SMOUT0	B93	O		12, 2	20, 50	Tri	Tri	B-7
SMOUT1	B94	O		12, 2	20, 50	Tri	Tri	B-7
SMOUT2	B104	O		12, 2	20, 50	Tri	Tri	B-7
SMOUT3	B105	O		12, 2	20, 50	Tri	Tri	B-7
SMOUT4	B106	O		12, 2	20, 50	Tri	Tri	B-7
SMOUT5	B108	O		12, 2	20, 50	Tri	Tri	B-7
SMRAMCS#	B180	I	60K PU			Tri	Tri	
SPKR	B182	O		12, 2	20, 50	Tri	Tri	B-7
SRBTN#	B190	I				Actv	Tri	
STPCLK#	B131	O		12, 2	20, 50	Tri	Tri	B-7
SUS_STAT#	B185	O		12, 2	20, 50	Actv	Tri	B-7
SYSCLK	B47	I				Tri	Tri	
TC	B60	O		24, 4	50, 240	Tri	Tri	B-4
TIM2CLK2	B172	I	20K PD			Tri	Tri	
TIM2OUT2	B174	O		12, 2	20, 50	Tri	Tri	B-7
XD7	B5	IO	60K PU	24, 4	20, 100	Tri	Tri	B-3
XDEN#	B3	O		12, 2	20, 50	Tri	Tri	B-7
XDIR	B4	O		12, 2	20, 50	Tri	Tri	B-7
ZEROWS#	B35	O OD		24, 4	50, 240	Tri	Tri	B-4

Power Pins

V_{CC} : B001, B018, B034, B050, B067, B083, B099, B116, B132, B148, B165, B181
V_{SS} : B016, B032, B049, B065, B081, B098, B114, B130, B147, B163, B179, B196



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4.2 Signal Descriptions

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82360SL ISA Peripheral I/O

The following table provides a brief description of the signals of the 82360SL I/O. Signal names which end with the character “#” indicate that the corresponding signal is low true when active.

Symbol	Name and Function
A20GATE	A20 Gate (direct to CPU): This active HIGH output signal allows the Intel386™ SL CPU to pass A20 on the system address bus. When this signal is LOW, A20 is masked to allow emulation of an 8086.
AEN	Address Enabled (ISA-bus signal): This active HIGH output indicates a DMA access or refresh. The 82360SL drives this signal high to signify a valid DMA address. It is used by bus slaves to decode I/O ports. All ports must be decoded for AEN low. There are no DMA cycles to addressed I/O ports.
BALE	Buffered Address Latch Enable (ISA-bus signal): This active HIGH input to the 82360SL is driven by the Intel386™ SL CPU during standard ISA bus cycles. During ISA bus memory and I/O cycles BALE is used to indicate valid addresses at the start of a bus cycle. SA[19:0] are valid on the falling edge and LA[23:17] are valid while BALE is high. BALE is also driven high by the Intel386™ SL CPU and remains high during DMA, REFRESH and Master cycles.
BATTDEAD#	BATTERY DEAD: This signal acts as a reset to the state machines connected to RTCVCC. This signal must be connected to an RC combination which will allow it to meet the AC specification It 250.
BATTLOW#	BATTERY LOW: This active LOW input indicates that the battery power is low. BATTLOW# is typically driven by a D.C. to D.C. power converter associated with the battery power supply. A thermal power monitor indicates that the main battery power is dropping below the adequate charge level to sustain operation. If this signal is asserted LOW a SMI request will be generated. The feature is enabled via S/W control. The signal will also prevent a resume operation if asserted LOW.
BATTWARN#	BATTERY WARNING: This active LOW input indicates the battery has minimal charge left (eg. one half an hour of full power use remaining). It is used to generate a battery low warning tone.
CS042CS#	Keyboard controller Chip Select: This active LOW output is driven when there is an I/O read or write to the Keyboard Controller Ports 60 or 64 hex.
COM(A,B)CTS#	Clear To Send: This active LOW input indicates to the Serial Port Controller for COMA or COMB that a serial device is clear to accept data. This signal is typically used for a modem control function. A change in the state of this signal generates a modem status interrupt. The modem or data set asserts this signal when it is ready to accept data for transmission.
COM(A,B)DCD#	Data Carrier Detect: This active LOW input indicates that the Serial Port Controller COMA or COMB has detected a data carrier from the data set of a serial device. Typically this signal is from a modem.
COM(A,B)DSR#	Data Set Ready: This active LOW input signal is used by the modem or data set to indicate that the modem or data set is ready to establish the communication link and transfer data with the Serial Port Controller.
COM(A,B)DTR#	Data Terminal Ready: This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to communicate.
COM(A,B)RXD	Serial data Receive: This input signal is used to receive serial data. Each character can consist of from five to eight bits of data with one start bit and one, one and a half or two stop bits. The least significant bit is received first.



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82360SL ISA Peripheral I/O Signal Descriptions (Continued)

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Symbol	Name and Function
COM(A,B)RI #	Ring Indicator: This active LOW input signal is used for a modem control function. A change in the state (either from high to low or from low to high) of this signal generates a modem status interrupt. The modem or data set asserts this signal to indicate that it has detected a telephone ring. This will cause the 82360SL to wake the Intel386™ SL CPU from a suspended state if modem ring is enabled as a wake-up event.
COM(A,B)RTS #	Request To Send: This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to send data.
COM(A,B)TXD	Serial data transmission: This output signal is used to transmit data serially between the Serial Port Controller and serial device. Each character can consist of five to eight bits of data with one start bit and either one, one and a half, or two stop bits. The least significant bit is transmitted first. The control of the format of a character is defined under S/W control via the Line Control Register. Please consult the Intel386™ SL Microprocessor SuperSet Programmer's Reference Manual for additional information. Information regarding the functional timing specifications of transmitted and received serial data may be found in sections 6 and 7 (A.C. timing specifications and timing diagrams).
COMX1,COMX2	Crystal oscillator input and output pins: The crystal attached to these signals should be tuned to 1.8432 Mhz. The on-chip oscillator uses an external crystal and tank circuit to generate an internal clock. This clock is used to generate the various baud rates for the serial ports. Optionally an external oscillator may be connected to the COMX1 input.
CPURESET	CPU RESET: This active HIGH output is connected directly to the Intel386™ SL CPU to provide a reset of the Intel386™ CPU core. CPURESET always occurs during a PWRGOOD reset. CPURESET may also be generated by RC# from a keyboard controller, Fast Reset from I/O Port 92 or other programmable Reset, or a resume from suspend.
CX1,CX2	Crystal oscillator input and output pins: The crystal should be tuned to 14.31818 Mhz. It is used for the ISA bus signal OSC signal and is internally divided by 12 to clock the timer counters. The oscillator input may be directly driven from an external source.
DACK[7:5], [3:0] #	DMA ACKnowledge channel n (ISA bus signal): The 82360SL DMA controller drives the respective DMA acknowledge signal low after a device has requested DMA service. The corresponding output signal indicates that the DMA channel transfer may begin.
DMA8/16 #	DMA 8-bit or 16-bit cycle: This output signal is directly connected to the Intel386™ SL CPU. When the signal is HIGH it indicates that the current DMA cycle is 8-bit. When this signal is low it indicates that the DMA cycle is using a 16-bit channel.
DRQ[7:5], [3:0]	DMA ReQuest channel n (ISA bus signal): These input signals are used to request DMA service from devices residing on the ISA bus. An ISA bus device drives this signal to request service from the appropriate DMA channel by asserting this signal high.
ERROR #	MCP ERROR: This signal is an active LOW input to the 82360SL. The math coprocessor error signal generates a IRQ13 through the 82360SL.
EXTSMI #	EXTERNAL System Management Interrupt request: This active low input will generate a SMI request if the function is enabled.
EXTRTCAS	EXTERNAL RTC Address Strobe: This output signal is active HIGH when there is a write access to the RTC I/O address port and when an external RTC is selected.
EXTRTCDS	EXTERNAL RTC read Data Strobe: This output signal is active LOW when there is a read access to an external RTC I/O data port and when an external RTC is selected.
EXTRTCRW #	EXTERNAL RTC (Real Time Clock) Read/Write: This output signal is active LOW when there is a write access to an external RTC I/O data port and when an external RTC is selected.

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82360SL ISA Peripheral I/O Signal Descriptions (Continued)

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Symbol	Name and Function
FLPCS#	FLoPpy Chip Select: This LOW true output signal is the chip select for the floppy disk controller I/O ports 03F0-03F5 and 3F7 hex.
HALT#	HALT: This LOW true input signal is driven by the Intel386 SL CPU and indicates when the CPU has executed a HLT instruction (address=2) or is in a shutdown condition (address=0).
HD7	HD-bus Data bit HD7: The bi-directional System Data Bit 7 is controlled separately for the Integrated Drive Electronics (I.D.E.) hard disk drive and floppy disk drive. This is provided to accommodate the I/O address 3F7 hex which is split between the floppy disk drive controller and I.D.E. hard disk. Data transfer between storage peripherals connected to the I.D.E. Hard Disk and Floppy Disk and the 82360SL are on separate busses. Data bit 7 has to be separated from data bits [6:0]. The 82360SL controls and buffers data bit 7 separately.
HDCS[1:0]#	Hard Disk Chip Select: These LOW true output signals are the I.D.E. hard disk drive chip selects decoded from the I/O address ports 01F0-01F7h (HDCS0#) and 03F6-03F7h (HDCS1#).
HDEN(H,L)#	Hard Disk buffer ENable: These LOW true output signals control the I.D.E. hard disk data buffers, high and low bytes.
HLDA	HoLD Acknowledge (direct to CPU): This HIGH true input signal indicates that the Intel386 SL CPU has released the ISA bus for refresh, DMA or master cycles.
HRQ	Hold ReQuest (direct to CPU): This active HIGH output signal indicates a request to the Intel386 SL CPU to release the ISA bus when the 82360SL requests the bus for ISA bus style refresh, DMA or master mode cycles.
IMUX0	This pin is multiplexed. It can be used as Timer 2 gate 2 input or an external audio input.
INTA#	INTerrupt Acknowledge (direct to CPU): This active LOW input to the 82360SL indicates that the Intel386 SL CPU has recognized an interrupt and will initiate an interrupt acknowledge bus cycle. The INTA bus cycle is comprised of two eight-bit I/O cycles in which the interrupt vector transferred on the second eight-bit I/O write of the INTA cycle.
INTR	INTerrupt Request (direct to CPU): This active HIGH output requests a standard maskable interrupt to the Intel386 SL CPU.
IOCHCK#	IO CHannel Check (ISA bus signal): This maskable active LOW input is driven by a device on the ISA bus typically used to indicate a parity error on the ISA bus. This signal is one of the possible sources which may generate an NMI. NMI generation via IO Channel Check may be enabled or disabled using PORT 61 (IOCKEN). NMI may be masked using the ISA bus compatible NMI control port at I/O 70 hex bit 7.
IOCHRDY	I/O CHannel ReaDY (ISA bus signal): This active HIGH I/O signal is used by the 82360SL DMA controller to extend ISA bus cycles. IOCHRDY is also used to extend bus cycles for I/O device trapping. Additional wait states extend the bus cycle, allowing for start up during Resume mode. The ISA bus is a normally ready bus, an external device can extend a DMA cycle or ISA bus cycle by deasserting this signal (driven low). This signal is normally high on the ISA bus.
IOCS16#	16-bit I/O Chip Select (ISA bus signal): This active LOW input signal to the 82360SL is used to indicate a 16-bit I/O bus cycle. The I.D.E. hard disk high byte buffer enable is generated when IOCS16# is driven low during an I.D.E. 16-bit I/O access. IOCS16# is also an input to the Intel386 SL CPU driven by devices residing on the ISA bus to indicate a 16-bit I/O bus cycle.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

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Symbol	Name and Function
IOR#	I/O Read (ISA bus signal): This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O read. This signal is an output from the 82360SL during DMA bus cycles for I/O to memory transfers.
IOW#	I/O Write (ISA bus signal): This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O write. This signal is an output from the 82360SL during DMA bus cycles for memory to I/O transfers.
IRQ[15, 14, 12-9, 7-3, 1]	Interrupt ReQuest n (ISA bus signal): These active HIGH input signals are used to request interrupt service. The interrupt request lines are driven by devices on the ISA bus which have a corresponding interrupt service routine associated with the interrupt vector and interrupt request.
IRQ8#	Interrupt ReQuest 8: This active LOW signal is used by the external Real Time Clock to request interrupt service.
KBDA20	KeyBoarD A20 gate: This active HIGH input is "ORed" with internal bits to produce A20GATE which goes to the Intel386 SL CPU. The bit is connected to port 2, bit 1 of an 8042 in a standard ISA bus compatible system.
KBDCLK	KeyBoarD CLock: This output signal is used to drive the clock input to the keyboard controller. It is derived from the 8 MHz SYSCLK and can be divided by 1, 2, 4 or stopped.
LA[23:17]	Local Address bus (ISA bus signal): These are input signals to the 82360SL during memory transfers (decoding for X-bus buffer controls) and output signals during DMA accesses and refresh. The latching address lines allow access to physical memory on the ISA bus to 16 megabytes.
LPTACK#	Line PrinTer ACKnowledge: Active LOW input signal which is part of the parallel port data handshake. The line printer asserts this signal to show that data transfer was complete and that it is ready for the next transfer. If the interrupt enable bit is set in the LPT control register, this signal can be used to generate an interrupt.
LPTAFD#	Line Printer Auto line FeED: This signal is an active LOW output from 82360SL to a printer. When asserted, it instructs the printing device to insert a line feed at the end of every line. In the Fast parallel port mode, this signal is used as a data strobe. It can be used to latch data during write cycles and to enable buffers during read cycles.
LPTBUSY	Line PrinTer BUSY: This signal is an active HIGH input to 82360SL. The printer asserts this signal when it is not ready to accept further data from 82360SL. In the Fast parallel port mode this signal is active LOW.
LPTD[7:0]	Line printer Data bus: These signals are the 8-bit bi-directional data bus for the parallel port. In PC/AT mode these signals are output only. The 82360SL also supports a bidirectional mode for the PS/2 style parallel port.
LPTDIR	Line PrinTer DIRection: This active HIGH output signal is only valid in bidirectional mode for data transfer using the parallel port. This signal is LOW in ISA compatible and Fast parallel port modes. In the PS/2 expanded mode, this signal is LOW for writes and HIGH for reads.
LPTERROR#	Line PrinTer ERROR: This active LOW input signal is driven by a peripheral device to flag an error condition.
LPTINIT#	Line PrinTer InITialize: This active LOW output from 82360SL instructs the peripheral to initialize itself.
LPTPE	Line PrinTer Paper End: This active HIGH input to 82360SL signals that the printer has run out of paper when asserted.
LPTSLCT	Line PrinTer SeLeCTed: This active HIGH input signal is asserted by the printer to confirm that it has been selected.



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82360SL ISA Peripheral I/O Signal Descriptions (Continued)

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Symbol	Name and Function
LPTSLCTIN#	Line PrinTer SeLeCT IN: This active LOW output signal is asserted to select the printer interfaced to the parallel port. In the Fast parallel port mode, this signal is used as an address strobe. It indicates that an access is being made to the port X7Bh.
LPTSTROBE#	Line PrinTer STROBE: This active LOW output signal is used to strobe data into the peripheral device. The parallel port controls are read and written through I/O registers. In the Fast parallel port mode, this signal is used to indicate a write cycle.
MASTER#	ISA bus MASTER (ISA bus signal): This active LOW input signal is used by the 82360 SL to determine when to go into an external master refresh arbitration mode. In this mode, the master controls the REFRESH signal but the 82360SL generates the address, the REFREQ# signal, the AEN and command signals.
MEMR#	MEMory cycle Read (ISA bus signal): This bi-directional active LOW signal indicates a read cycle anywhere in the 16 Mbyte memory address space. During memory read cycles to memory on the ISA bus, this signal is an input into the 82360SL. MEMR# is driven by the 82360SL during DMA cycles.
MEMW#	MEMory cycle Write (ISA bus signal): This bi-directional active LOW signal indicates a write cycle anywhere in the 16 Mbyte memory address space. During memory write cycles to memory on the ISA bus, this signal is an input. MEMW# is an output from the 82360SL during DMA cycles.
N/C	No Connection: These signals must not be connected to any voltage. The No Connection signals must be left floating in order to guarantee proper operation of the 82360SL and compatibility with future Intel processors.
NMI	Non Maskable Interrupt (direct to CPU): This active HIGH output is directly connected to the Intel386 SL CPU. The 82360SL asserts NMI to request the Intel386 SL CPU to service a high priority non-maskable interrupt. The low to high transition of this signal is recognized by the Intel386 SL CPU.
ONCE#	ON-board Circuit Emulation: This active LOW input pin floats the appropriate outputs of the 82360SL as indicated in Section 2 pin assignments. This allows the system to be tested with external logic while the 82360SL is still physically populated on the motherboard. Note that the ONCE# pin on the 82360SL I/O should not be connected to the ONCE# pin on the Intel386 SL CPU.
OSC	OSCillator (ISA bus signal): This is the 14.31818 MHz output signal with a 50% duty cycle and is asynchronous to SYSCLK.
PERR#	Parity ERROR (direct from CPU): This active LOW input signal is connected to the output of the Intel386 SL CPU. When the Intel386 SL CPU detects a parity error from the local DRAM subsystem it drives this signal to the 82360SL. The system memory parity error will generate a NMI via the 82360SL when NMI is enabled via I/O port 70h bit 7 and PERR# is enabled via port 61h.
PWRGOOD	Power GOOD: This active HIGH input is typically supplied by the power supply. When Power good is activated high this indicates that the supply voltage is stable. Power Good low is also used to generate System Reset, RESETDRV, and CPURESET.
RC#	Reset CPU: This active low input is typically driven by the keyboard controller. RC# is "ORed" with internal bits to produce a programmable pulse width CPURESET signal. It is connected to port 2, bit 0 of an 8042 in a standard ISA bus compatible system.
REFREQ	REFresh REQUEST (direct to CPU): This active HIGH output signal is directly connected to the Intel386 SL CPU. When Refresh Request is asserted it indicates that the Intel386 SL CPU should refresh the local DRAM subsystem.
REFRESH#	System REFRESH (ISA bus signal): This active LOW input signal indicates a refresh cycle. It is driven for the duration of the cycle. It is an input during master generated refresh bus cycles.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

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Symbol	Name and Function
RESETDRV	RESET DRIVe (ISA bus signal): This active HIGH output is the main system cold reset, generated from the power supply "power good" signal and by system resume.
RTCEN#	RTC ENable: This active LOW input signal should be strapped to GND or RTCVCC depending on whether an internal or external RTC is used in the system. The 82360SL on-chip real time clock and CMOS RAM are enabled by this signal when LOW.
RTCRESET#	Internal RTC RESET input: This active LOW input signal is used to reset the internal RTC status and flag registers, (typically when the RTC battery has been changed).
RTCVCC	This is a separate power supply input for the internal RTC. It should be connected to a 3V battery when the system is fully off and 5V during active operation.
RTCX1,RTCX2	RTC Crystal oscillator input and output pins: The crystal should be tuned to 32.768 Khz. It is used for the RTC and system power management state machines. The oscillator may be driven directly from the input signal.
SA[16:0]	System Address bus (ISA bus signal): The bi-directional system address bus is an input for decoding internal I/O registers and an output during DMA and refresh cycles.
SBHE#	System Byte High Enable (ISA bus signal): The active LOW output signal indicates when there is valid data on the upper data byte of the system data bus.
SD[7:0]	System Data bus (ISA bus signal): This is the bidirectional system data bus. The 82360SL directly drives the ISA bus system data bits [7:0] without external transceivers or buffers. 8-bit data is transferred to and from the 82360SL with these signals.
SMEMR# / LOMEM#	System MEMORY Read (ISA bus signal): This multiplexed signal has two functions. When configured as SMEMR#, this signal is driven by the 82360SL to signify a memory read cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles. When configured as LOMEM#, this signal indicates that the lower 1 Mbyte is being addressed.
SMEMW#	System MEMORY Write (ISA bus signal): This signal is driven by the 82360SL to signify memory write cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles.
SMI#	System Management Interrupt (direct to CPU): This active LOW output is directly connected to the Intel386 SL CPU. When the falling edge of SMI# is detected by the Intel386 SL CPU it generates the highest priority interrupt when enabled. The typical use of SMI# is for power management.
SMOUT[5:0]	System Management OUTput control: These six outputs can be connected to control the power circuits for various devices in the system. These output pins are directly controlled by the SMOUT_CNTRL register.
SMRAMCS#	System Management RAM Chip Select: This active LOW input is driven by the Intel386 SL CPU whenever the Intel386 SL CPU is accessing the System Management SM-RAM. It is active even when SM-RAM is part of the Intel386 SL CPU system memory RAM. The 82360SL uses the SMRAMCS# to determine when the SMI code is being executed on the ISA bus, and enables the X-bus control signals.
SPKR	SPEaKeR output: This is the output of the 8254 megacell, timer/counter # 1, channel 2, or directly driven through IMUX0, or from the 8254 megacell, timer/counter # 2, channel 1 depending on the programming. This output signal is typically connected to an external speaker. There is additional circuitry to ensure that the signal is low when not being used.
SRBTN#	Suspend/Resume BuTtoN: This active LOW input generates a SMI requesting a system suspend or resume. Activation of this input can be used as a wake up event for the STPCLK# signal.

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82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
STPCLK#	SToP CLoCK: This active LOW output signal stops the clock to the Intel386 CPU core of the Intel386 SL Microprocessor. Stop clock is directly connected to the Intel386 SL CPU from the 82360SL. The 82360SL activates this signal upon detection of a halt bus cycle or when an I/O read to the stop clock register in the 82360SL occurs.
SYSCLK	SYStem CLoCK (ISA bus signal): This signal is an output from the Intel386 SL CPU and an input to the 82360SL. The SYSCLK signal is used to clock the ISA bus state machines and is also used to derive the internal DMA clock signal and to generate the KBDCLK output in the 82360SL. The SYSCLK is the 8 MHz typical clock which is one half of the frequency of ISACK2.
SUS_STAT#	SUSpend STATus: The 82360SL power management controls this active low output signal to switch the power off to all non-critical devices during a suspend.
TC	Terminal Count (ISA bus signal): This active HIGH output signal is used to indicate the termination of a DMA transfer.
TIM2CLK2	TIMER 2 CLK: This is the input clock for timer/counter #2, channel 2 when it is programmed to be used in the General Purpose (GP) mode.
TIM2OUT2	TIMER 2 OUTPUT: This signal is the frequency output from timer/counter #2 and can be used as a general purpose timer/counter output when programmed for GP mode.
V _{CC}	System Power: Provides the +5V nominal D.C. supply inputs for the 82360SL.
V _{SS}	System Ground: Provides the 0V connection from which all inputs and outputs are referenced.
XD7	X-bus Data bit XD7: I/O port 3F7h is split between the floppy and hard disk and the storage peripherals which transfer data reside on separate busses. Data bit XD7 is separated from bits XD[6:0]. The 82360SL separately controls and buffers bit XD7 to isolate data bit 7 from the floppy disk and I.D.E. hard disk.
XDEN#	X-bus Data ENable: This active LOW output signal is used to control the X-bus data transceiver. It is only activated by the 82360SL on valid accesses to X-bus peripherals.
XDIR	X-bus data DIRection: This active HIGH output signal controls the direction of the X-bus and HD-bus data transceivers. XDIR is high for read cycles.
ZEROWS#	ZERO Wait State (ISA-bus signal): This active LOW output signal is driven by the 82360SL when it can accept a zero wait state write cycle.

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4.3 82360SL D.C. SpecificationsFunctional operating range: $V_{CC} = 5.0V \pm 10\%$, $T_{CASE} = 0^{\circ}C$ to $90^{\circ}C$.

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Table 4.3-1. 82360SL D.C. Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3		0.8	V	(Note 15)
				0.8	V	(Note 11)
				0.8	V	(Note 12)
				0.8	V	(Note 13)
V_{IH}	Input High Voltage	2.0 2.0 4.0 1.5		$V_{CC} + 0.3$	V	(Note 16)
					V	(Note 11)
					V	(Note 12)
					V	(Note 13)
I_{LI}	Input Leakage Current			± 15	μA	(Note 1)
I_{LO}	Output Leakage Current			± 15	μA	
C_{IN}	Input Capacitance			15	pF	(Note 14)
C_{OUT}	Output or I/O Capacitance					(Note 14)
I_{CCS1}	Suspend with Slow Refresh		200	40	μA	(Note 8)
I_{CCS2}	Suspend without Slow Refresh		150	350	μA	(Note 8)
I_{CC}	Power Supply Current		50	10	mA	(Note 9)
D.C. Specifications for Standard ISA Bus Signals						
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 24$ mA (Note 3)
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -4.0$ mA (Note 3)
D.C. Specifications for Parallel Port						
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 8$ mA (Note 2)
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -2$ mA (Note 2)
D.C. Specifications for Open Drain Outputs						
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 24$ mA (Note 4) $I_{OL} = 12$ mA (Note 5) $I_{OL} = 8$ mA (Note 10)
D.C. Specifications for All Other Outputs						
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 12$ mA (Note 6)
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -2$ mA (Note 6)
D.C. Specifications for Power-Down Mode						
RTCVCC	RTC Supply Voltage	2.5	5		V	(Note 17)
I_{RTCVCC}	RTC Supply Current		20	75	μA	RTCVCC = 5V RTCVCC = 2.5V (Note 7)
			10	35	μA	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4$ mA
				0.5	V	$I_{OL} = 8$ mA
V_{OH}	Output High Voltage	2.0			V	$I_{OH} = -2$ mA

NOTES:

- No pullup or pulldown.
- For outputs—LPTD7:0
- For outputs—OSC, AEN, SA16:0, LA23:17, MEMR#, MEMW#, IOR#, IOW#, SMEMW#, SMEMR#, SBHE#, TC, SD7:0, XD7, HD7, RESETDRV.
- ZEROWS#, IOCHRDY.
- LPTSTROBE#, LPTAFD, LPTINIT#, LPTSLCTIN#, LPTDIR.
- For all other outputs of the module.
- Measured at $V_{CC} = 0V$, $V_{BATT} = 2.5V$, 32 kHz RTC clock with input rise time and fall time, $t_r = t_f < 50$ ns.
- RTC clock at 32 kHz; Timer Clock, Serial clock and SYSCLK internally disabled; $V_{CC} = 5.5V$ and RTCVCC = 5.5V, $C_L = 50$ pF with outputs unloaded.

NOTES (Continued):

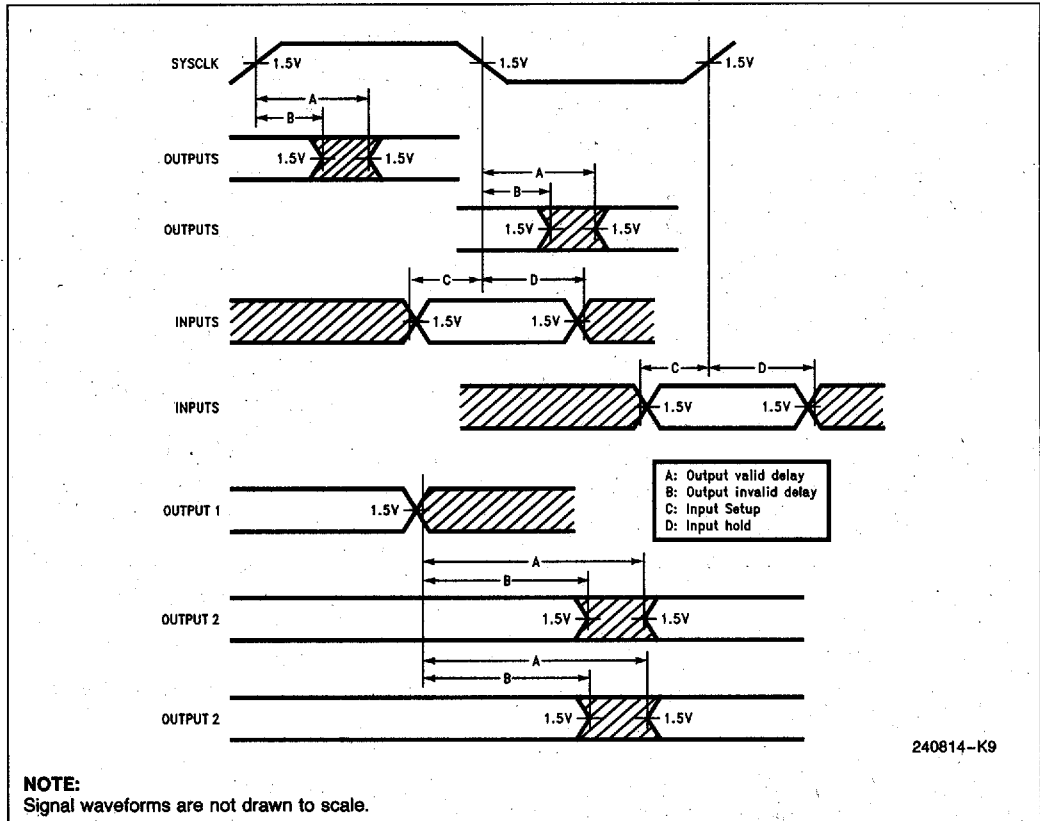
- 9. I_{CC} tests at maximum frequency with no resistive loads on the outputs.
- 10. REFRESH#
- 11. For RTC oscillator at 3V V_{CC}.
- 12. For all oscillators.
- 13. For all input buffers at 3V V_{CC}.
- 14. Characterized by design.
- 15. Min for system design reference only.
- 16. Max for system design reference only.
- 17. RTCVCC must be less than or equal to V_{CC} during normal operation.

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4.4 Timing Specifications

A.C. SPECIFICATION DEFINITIONS

The A.C. specifications given in the tables of the following pages consist of output delays, input setup and hold requirements. They may be relative to a clock edge or another signal edge. ALL timings reference SYSCLK. A.C. specifications are defined in Figure 4.4.1. All clock related specifications are tested at the voltage levels shown with a fully capacitive load. Output specifications are derived from tested clock related timings.



NOTE:
Signal waveforms are not drawn to scale.

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Figure 4.4.1. Drive Levels and Measurement Points for A.C. Specifications



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4.4 Timing Specifications

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Table 4.4-1. 82360SL I/O Timing Specifications⁽¹⁾

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
It1	SYSCLK Period	125		ns		4.5-1	
It2	SYSCLK Low Time @V _{IL} = 1.5V	55		ns		4.5-1	
It3	SYSCLK High Time @V _{IH} = 1.5V	50		ns		4.5-1	
It4	SYSCLK Rise Time and Fall time		10	ns		4.5-2	
It5a	RESETDRV from SYSCLK		125		S		
It6a	A20GATE Active (HIGH) Delay from KBDA20 Active (HIGH)		30	ns	SR	4.5-1	
It6b	A20GATE Active (HIGH) Delay from SYSCLK		45	ns	SR	4.5-1	
It7	SYSCLK to KBDCLK Delay		30	ns		4.5-1	(Note 3)
It8a	RC# /PERR# /IOCHCK# Pulse Width	250				4.5-2	
It8b	RC# /PERR# /IOCHCK# Setup to SYSCLK Falling Edge	12				4.5-1	(Note 3)
It9a	Programmable CPURESET Active (HIGH) from SYSCLK	5		ns	FR, SR	4.5-1	
It10a	NMI Active (HIGH) from SYSCLK		125		SR	4.5-1	(Note 3)
It10b	NMI Inactive from IOW# Active (LOW)				FF	4.5-1	
It11	RTCRESSET# Pulse Width			μs		4.5-1	
It14	BALE hold from SYSCLK	2				4.5-3	
It15	IOR# /IOW# /INTA# Input Active (LOW) Delay from SYSCLK Low			ns		4.5-1	
It15a	IOR# /IOW# /MEMW# Output Active (LOW) Delay from SYSCLK		30	ns	SF	4.5-8	
It16	IOR# /IOW# /INTA# /MEMW# /MEMR# Input Inactive from SYSCLK		35	ns		4.5-3	
It16a	IOR# /IOW# Output Inactive from SYSCLK		120	ns	SR	4.5-8	
It17	ZEROWS# Output Active from SYSCLK		65	ns	SF	4.5-4	
It18	ZEROWS# Output Inactive from SYSCLK	0		ns	SR	4.5-4	
It19	BALE Setup to SYSCLK (DMA enable)	18		ns		4.5-7	
It20	IOCHRDY Input Active Setup to SYSCLK	15		ns		4.5-7	
It20a	IOCHRDY Input Inactive Setup to SYSCLK	15		ns		4.5-7	
It21	DMA8/16# Active Delay from SYSCLK		65	ns	SF	4.5-7	
It22	DMA8/16# Inactive Delay from SYSCLK (4 MHz DMACLK)		65	ns	SR	4.5-7	
It22a	DMA8/16# Inactive Delay from SYSCLK Low (8 MHz DMACLK)		65	ns	SR	4.5-23	
It23	AEN Active from HLDA Active		35	ns	SR	4.5-7	

NOTE:

1. The A.C. specifications given in Table 4.4-1 are made with the assumption that the input signals IOR#, IOW#, BALE, SYSCLK and SA[16:0] do not vary independently (i.e., they all have either max delays or min delays and one signal cannot have a max delay while another has a min delay). This condition is guaranteed when these signals are driven by the Intel386™ SL CPU. If used in a system where this condition does not hold true, Intel does not guarantee the timings of the output signals of the 82360 SL I/O.

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4.4 Timing Specifications (Continued)

Table 4.4-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
t24	AEN Inactive Delay from HLDA Inactive		35	ns	SF	4.5-7	
t25	SA15:0, SBHE# Valid Delay from SYSCLK	10	120	ns	F, S	4.5-7	
t26	SA16 (Only if DMA8/16# = 0) SA15:0, SBHE# Valid Output Hold from SYSCLK	6		ns		4.5-10	
t28a	SA16 (Only if DMA 8/16# = 1), LA17:23 Valid Output Hold from IOR#/IOW#/MEMR#/MEMW# Output	10		ns		4.5-24	
t26f	SA18:0, LA17:23, SBHE# Float Delay from SYSCLK		90	ns	S	4.5-10	
t27	DACKx# Active Delay from SYSCLK (4 MHz DMACLK)		75	ns	SF	4.5-7	
t27a	DACKx# Active Delay from SYSCLK Low (8 MHz DMACLK)				SF	4.5-8	
t28	DACKx# Inactive Delay from SYSCLK (4 MHz DMACLK)		75	ns	SR	4.5-7	
t28a	DACKx# Inactive Delay from SYSCLK Low (8 MHz DMACLK)		75	ns	SR	4.5-8	
t29	IOR#/IOW#/MEMW# Float-to-Drive-Inactive from SYSCLK		6	ns		4.5-23	
t30	IOR#/IOW#/MEMW# Float Delay from SYSCLK		75	ns		4.5-23	
t30a	SMRAMCS# Setup to MEMR#/MEMW# Active			ns	FF	4.5-11	
t31	MEMR#/MEMW# Input Active Delay from SYSCLK		70	ns		4.5-11	
t31a	MEMR#/MEMW# Output Active Delay from SYSCLK		70	ns	SF	4.5-8	
t32a	MEMR#/MEMW# Output Inactive Delay from SYSCLK		75	ns	SR	4.5-7	
t33	T/C Active Delay from SYSCLK		85	ns	SR	4.5-7	
t34	T/C Inactive Delay from SYSCLK		85	ns	SF	4.5-7	
t35	TIM2CLK2 Period	125		ns		4.5-2	
t36	TIM2CLK2 Low Time	55		ns		4.5-2	
t37	TIM2CLK2 High Time	55		ns		4.5-2	
t38	TIM2CLK2 Rise Time		25	ns		4.5-2	
t39	TIM2CLK2 Fall Time		25	ns		4.5-2	
t40	TIM2GAT2 High Pulse Width	45		ns		4.5-22	
t41	TIM2GAT2 Low Pulse Width	45		ns		4.5-22	
t42	TIM2GAT2 Setup to TIM2CLK2	45		ns		4.5-22	

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4.4 Timing Specifications (Continued)

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Table 4.4-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
It43	TIM2GAT2 Hold from TIM2CLK2	45		ns		4.5-22	
It44	TIM2OUT2 from TIM2CLK2 High to Low		110	ns	SR	4.5-22	
It45	TIM2OUT2 from TIM2GAT2 High to Low		110	ns	SR	4.5-22	
It46	SPKR Active Delay from TIM2GAT2 (When EXTAUD is Set)		120	ns	SR	4.5-22	
It50	REFRESH# Active to MEMR# Output Active	150		ns	FF	4.5-10	
It52	Address Valid to MEMR# Active	40		ns	S, SF	4.5-10	
It53	MEMR# Output Inactive from IOCHRDY Input Low to High (During a Master Refresh)	125		ns	FR *	4.5-10	
It55	IOCHRDY Pulse Width		750	ns		4.5-10	
It56	MEMR# Output Pulse Width for Refresh	2		SYSCLK		4.5-10	
It59	FLPCS#/C8042CS# Active Setup to Command Active	10		ns	FF	4.5-13	
It59a	HDCS0#/HDCS1# Active Setup to Command Active	45		ns	FF	4.5-13	
It60	FLPCS#/C8042CS#/HDCS0#/HDCS1# Output Hold from Command Inactive	10		ns	FR	4.5-13	
It60a	SMRAMCS# Hold from MEMR#/MEMW#			ns		4.5-11	
It69	DRQx Setup to SYSCLK High to Low	0		ns		4.5-5	
It78	EXTSMI# Input Pulse Width	1		SYSCLK		4.5-26	
It79	EXTRTCAS Pulse Width			SYSCLK		4.5-14	
It80	IOCS16# Setup to Command	10		ns		4.5-18	
It81	IOCS16# Hold from Command			ns		4.5-18	
It82	STPCLK# Delay from SYSCLK		100	ns	SF	4.5-25	
It82a	STPCLK# Output Pulse Width	2		SYSCLK		4.5-25	
It83	SMI# from SYSCLK		100	ns	SF	4.5-25	
It84	SMOUTx from SYSCLK		110	ns	S	4.5-25	
It85	SUS_STAT# from SYSCLK		100	ns	SF	4.5-25	(Note 3)
It86	IOCHRDY Output High to Low from Command		24	ns	SF	4.5-23	
It94	Delay from IOW# to Modem Output (RTS#, DTR#)		200	ns	SF	4.5-20	
It109	KBDCLK Period (8 MHz)	125		ns		4.5-2	
	KBDCLK Period (4 MHz)	250		ns		4.5-2	
	KBDCLK Period (2 MHz)	500		ns		4.5-2	
It110	KBDCLK High Time (8 MHz)	40		ns		4.5-2	
	KBDCLK High Time (4 MHz)	95		ns		4.5-2	
	KBDCLK High Time (2 MHz)	200		ns		4.5-2	

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4.4 Timing Specifications (Continued)

Table 4.4-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
It111	KBDCLK Low Time (8 MHz)	40		ns		4.5-2	
	KBDCLK Low Time (4 MHz)	95		ns		4.5-2	
	KBDCLK Low Time (2 MHz)	200		ns		4.5-2	
It117	HRQ Inactive to HLDA Inactive	185		ns	FF	4.5-5	
It118	HLDA Inactive to HRQ Active (Back to Back Hold Acknowledge Cycles)	0		ns	FR		(Note 3)
It120	IRQ1, 6, 10: 12, 14, 15, ERROR#, IRQ8# Inactive Pulse Width	100		ns		4.5-21	
It121	INTR Output Delay from IRQ1, 6, 10: 12, 14, 15, ERROR#, IRQ8#		100	ns	SR	4.5-21	
It122	Data Output Valid from INTA# Active		100	ns	S	4.5-21	
It123	Data Output Hold from INTA# Inactive	0		ns	F	4.5-21	
It123f	Data Float from INTA# Inactive		35			4.5-21	
It124a	SD7 Read Data Output Hold from MEMR# Inactive			ns		4.5-11	
It124f	SD7 Float from MEMR# Inactive			ns		4.5-11	
It125	Write Data Input Setup to MEMW# Active	4		ns		4.5-12	
It125a	XD7 Output Valid from MEMW# Active			ns	S	4.5-12	
It126	Write Data Input Hold from MEMW#	15		ns		4.5-12	
It126a	XD7 Output Hold from MEMW# Inactive	5		ns	F	4.5-12	
It126f	XD7 Float from MEMW# Inactive		45	ns		4.5-12	
It129	SMEMR# /SMEMW# Active from MEMR# / MEMW#		30	ns	SF	4.5-11	
It129a	SMEMR# /SMEMW# Inactive from MEMR# / MEMW# Inactive	3	30	ns	FR, SR	4.5-11	
It130	LOMEM# Output Active Setup to MEMR# / MEMW# Output Active	3		ns	FF	4.5-11	
It130a	LOMEM# Output Inactive Setup to MEMR# / MEMW# Input Active	5		ns	FR	4.5-11	
It140	LPTSTROBE# /LPTSLECTIN# /LPTAFD# Output Delay from Command		45	ns	SF	4.5-27	(Note 1)
It141	LPTD Output from LPTSTROBE# /LPTSLECTIN# / LPTAFD# Active		15	ns	SF, S	4.5-27	(Note 1)
It142	LPTD Output Hold from LPTSLECTIN# /LPTAFD# Inactive	50		ns	SR, S	4.5-27	(Note 1)
It143	LPTD Input Setup to LPTSLECTIN# /LPTAFD# Inactive during Read	210		ns		4.5-27	(Note 1)
It144	LPTD Input hold from LPTSLECTIN# /LPTAFD# Inactive during Read	0		ns		4.5-27	(Note 1)
It145	IOCHRDY Output Low from LPTBUSY Low		40	ns	SF	4.5-27	(Note 1)
It200	BALE Active from SYSCLK Low	2	35	ns		4.5-3	
It201	Write Data Input Setup to IOW# Active	40		ns		4.5-3	

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4.4 Timing Specifications (Continued)

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Table 4.4-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
It202	Write Data Input Hold from IOW# Inactive	25		ns		4.5-3	
It203	Read Data Output Setup to IOR# Inactive	62		ns	F	4.5-3	
It204	Read Data Output Hold from IOR# Inactive	0		ns	F	4.5-3	
It204f	Data Bus Float from IOR# /MEMR#		35	ns		4.5-3	
It205	BALE Active Pulse Width	50		ns		4.5-3	
It206	SA Address Input Valid Setup to BALE Inactive	40		ns		4.5-3	
It208a	LA Address Input Valid Setup to BALE Active	40		ns		4.5-11	
It208b	LA Address Input Valid Hold from BALE Inactive	55		ns	*	4.5-11	
It209	IOW# to EXTRTCAS		130	ns	SR	4.5-15	
It210	XD7 Output Valid from IOW# Active		60			4.5-14	
It211	XD7 Output Hold from IOW# Inactive	5				4.5-14	
It211f	XD7 Output Float from IOW# Inactive		45	ns		4.5-14	
It212	EXTRTCRW# /EXTRTCDS Active from Command Active			ns	SF; SR	4.5-16	
It213	EXTRTCRW# / EXTRTCDS Hold from Command Inactive		35	ns	SR; SF	4.5-16	
It214	XDEN# Output Delay from IOR# /IOW#, MEMR# /MEMW# Inputs	10			FF, SF	4.5-11	
It214a	XDEN# Output Delay from IOR# /IOW# Output	5	75	ns	FF, FF SF, SF	4.5-24	
It215a	XDEN# Output Active from XDIR Output Inactive			ns	FR, FF	4.5-11	
It215b	XDIR Output Inactive from XDEN Output Inactive			ns	FR, FF	4.5-11	
It216a	SD7 Read Data Output Delay from XD7 Input		35	ns	S	4.5-11	
It216b	SD7 Read Data Output Delay from HD7 Input		50	ns	S	4.5-18	
It217	SD7 Read Data Output Hold from IOR# Inactive	0		ns	F	4.5-13	
It217f	SD7 Float from IOR# Inactive		35	ns		4.5-13	
It218	Address Input Hold from Command Inactive	40		ns		4.5-3	
It219	HDENL# /HDENH# Output Active Delay from Command		35	ns	SF	4.5-18	
It219a	HDENL# /HDENH# Output Inactive Delay from Command Inactive	5		ns	FR	4.5-18	
It220	HD7 Output Valid from IOW# Active		45	ns	S	4.5-19	
It221	HD7 Output Hold from IOW# Inactive	10		ns	F	4.5-19	
It221f	HD7 Output Float from IOW# Inactive		35	ns		4.5-19	

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4.4 Timing Specifications (Continued)

Table 4.4-1. 82360SL I/O Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Derating	Figure	Notes
It223	HALT# Input Valid from SYSCLK Low		20			4.5-1	
It224	XD7/HD7 Input Setup to IOR#/MEMR#	60		ns		4.5-13	
It225	XD7/HD7 Input Hold from IOR#/MEMR#	0		ns		4.5-13	
It230	XD7 Output Valid from EXTRTCRW# Active		35	ns	S	4.5-17	
It231	XD7 Output Hold from EXTRTCRW# Inactive	0		ns	F	4.5-17	
It231f	XD7 Output Float from EXTRTCRW#		35	ns		4.5-17	
It250	BATTDEAD# Inactive from Stable RTCVCC	2		ms		4.5-26	(Note 2)
It251	EXTSMI# active to SMI# Active (for Minimum Programmed Count)	1	2.1	ms		4.5-28	(Note 2)
It252	SMI# Active from SRBTN#/BATT Low# Active (for Minimum Programmed Count)	128	256	ms		4.5-26	(Note 2)
It253	Advanced Power Management (APM) SMI# Active from IOW# Active	2	3	SYSCLK	FF, SF	7.4.56	(Note 2)
It254	COMARI#/COMBRI#/SRBTN# Pulse Width	1		RTCLK		4.5-26	(Note 2)
It305	SA16, LA23:17 Valid Delay from SYSCLK	10	65	ns	F, S	4.5-7	
It311	HRQ Output Active from SYSCLK		45	ns	SR	4.5-6	
It312	HLDA Setup to SYSCLK	18		ns		4.5-6	
It314	HRQ Inactive from SYSCLK	5		ns	FF	4.5-6	
It317	REFREQ Active from SYSCLK		45	ns	SR	4.5-6	
It319	REFREQ Inactive from SYSCLK			ns	SF	4.5-6	
It320	Normal REFREQ to Slow REFREQ (when Going to Suspend)	0	2	RTCLK		4.5-24	
It321	Slow REFREQ Active Delay to STANDBY	2	2	RTCLK		4.5-24	
It322	MASTER# Active to REFREQ# Input Active Delay	25		ns		4.5-9	
It324	REFRESH# Output Inactive from HLDA		35	ns	SF	4.5-6	
It325	REFRESH# Output Inactive from SYSCLK	5		ns	FR	4.5-6	
It326	REFRESH# Input Active to REFREQ Active		30	ns	SR	4.5-9	
It327	REFRESH# Input Inactive to REFREQ Inactive	0		ns	FF	4.5-9	
It328	REFRESH# Pulse Width	4	5	SYSCLK		4.5-6	
It329	REFREQ Pulse Width during Master# Cycle	4	5	SYSCLK		4.5-9	
It330	DACKx# to MASTER# Delay	0		ns	SF, SF	4.5-9	
It331	AEN Delay from MASTER#	0	49	ns	FR, FF, SR, SF	4.5-9	
It332	Alternate Master Drives Address and Data		125	ns		4.5-9	
It333	MASTER# Delay from DRQx Inactive		100	ns	SF	4.5-9	
It334	Alternate Master Tri-States Bus Signal	0		ns		4.5-9	

NOTES:

1. Fast parallel port specifications are applicable for I/O accesses to ports 37B-37F and 27B-27F.
2. These specifications are for power management.
3. These specifications are for test purposes only.

4.5 82360SL Timing Diagrams

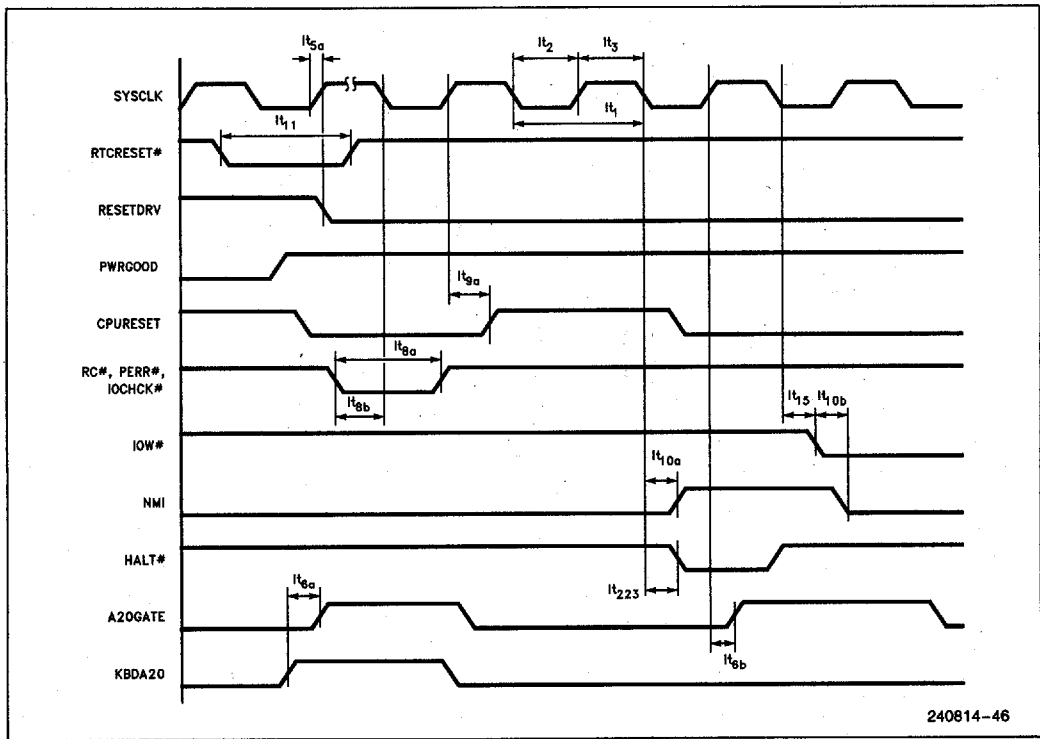


Figure 4.5.1. CPURESET, NMI, A20GATE and RC# Timings

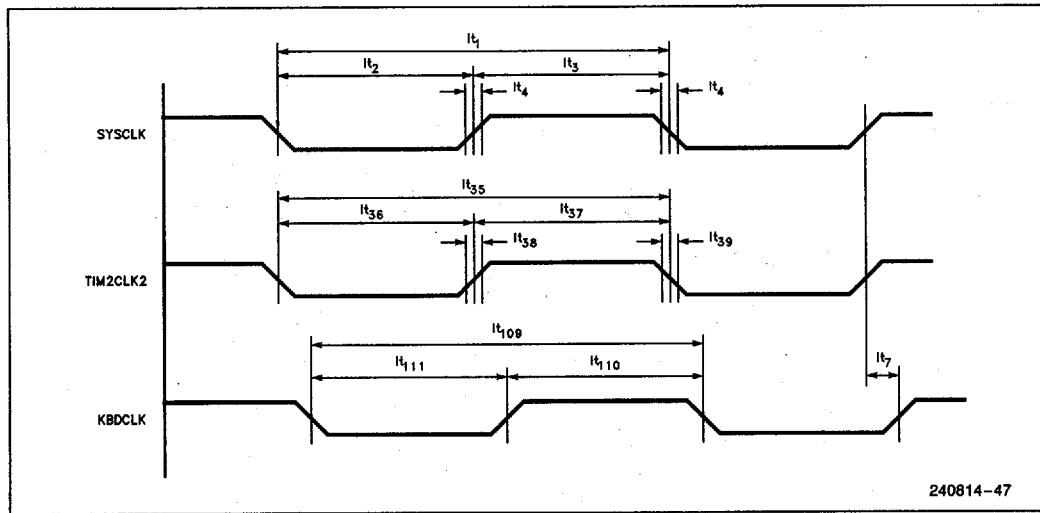


Figure 4.5.2. Clock Timings

2



4.5 82360SL Timing Diagrams (Continued)

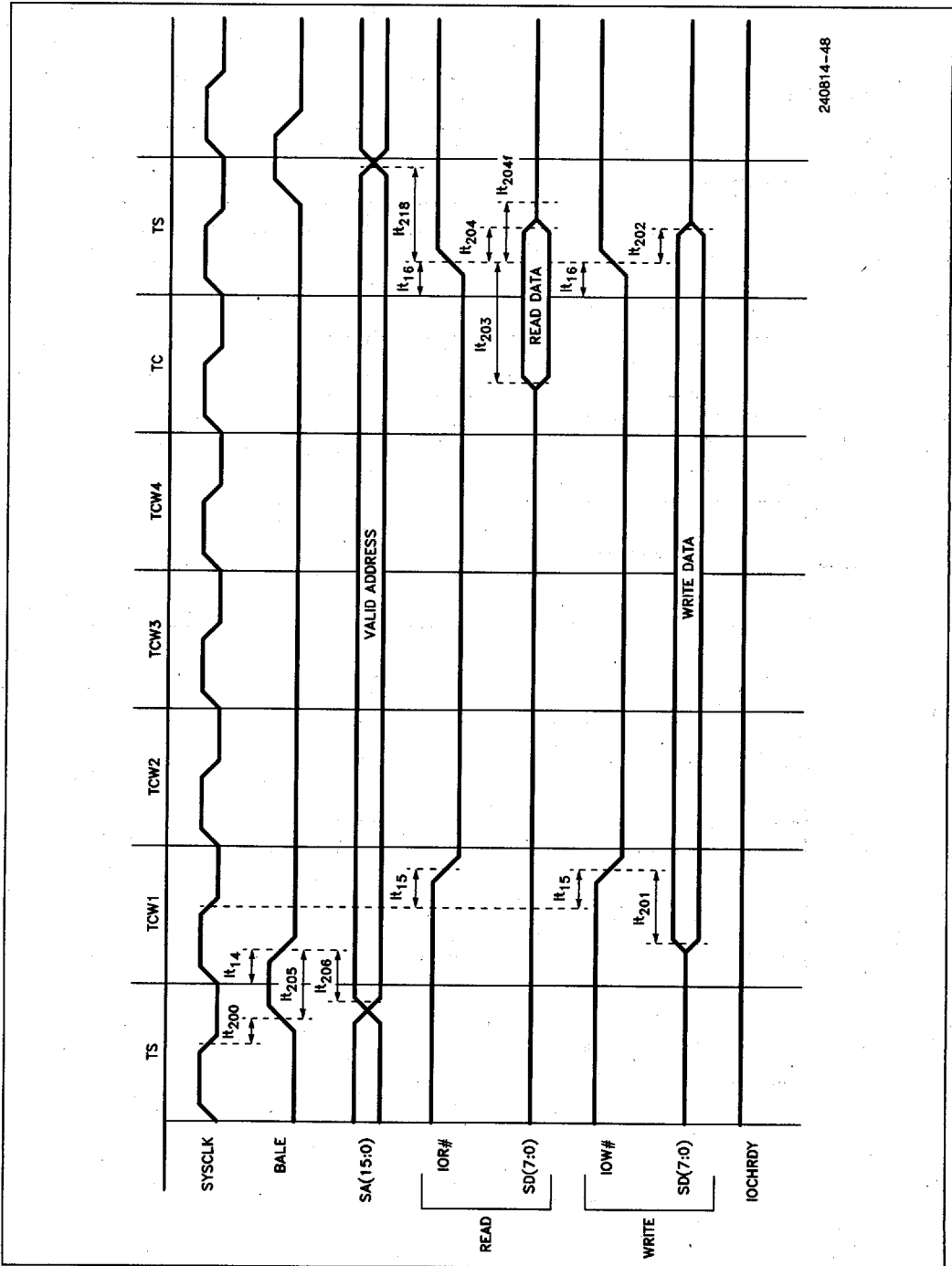
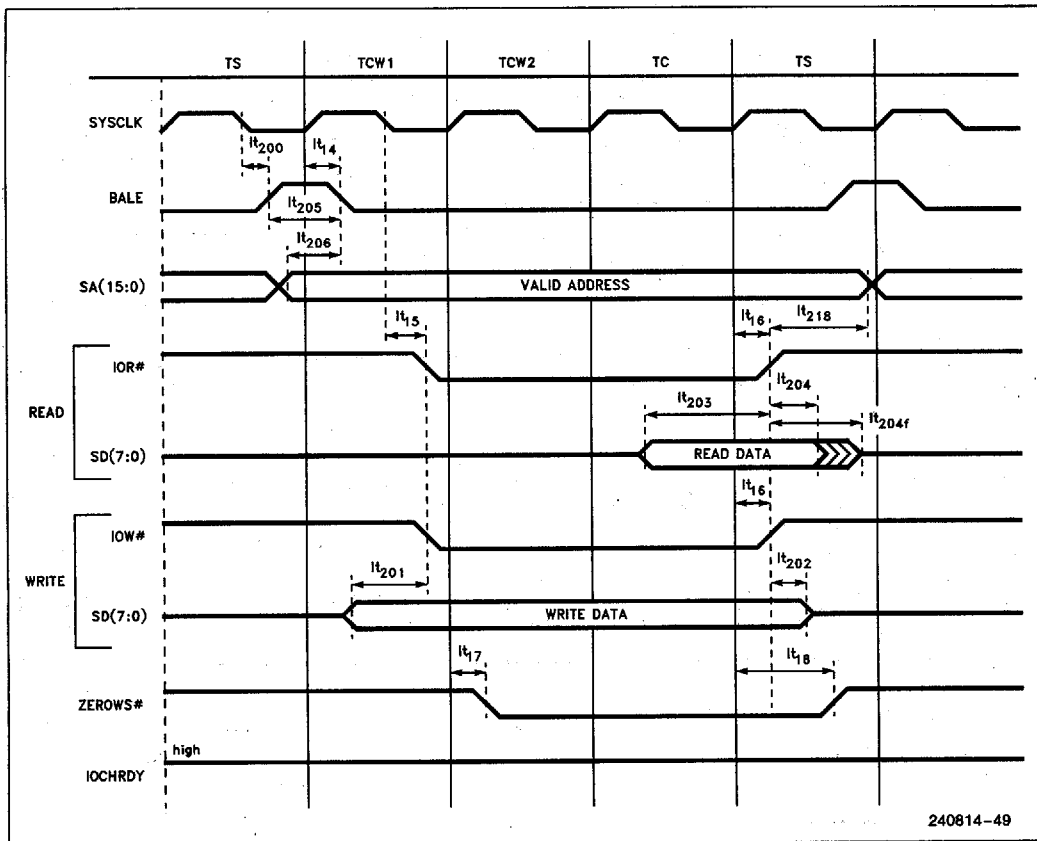


Figure 4.5.3. ISA Bus 8-Bit I/O Read/Write Default Bus Cycle (6 SYSCLKs)

INTEL CORP (UP/PRPHLS)

4.5 82360SL Timing Diagrams (Continued)

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240814-49

Figure 4.5.4. ISA Bus 8-Bit I/O Read/Write Compressed Bus Cycle

2

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34

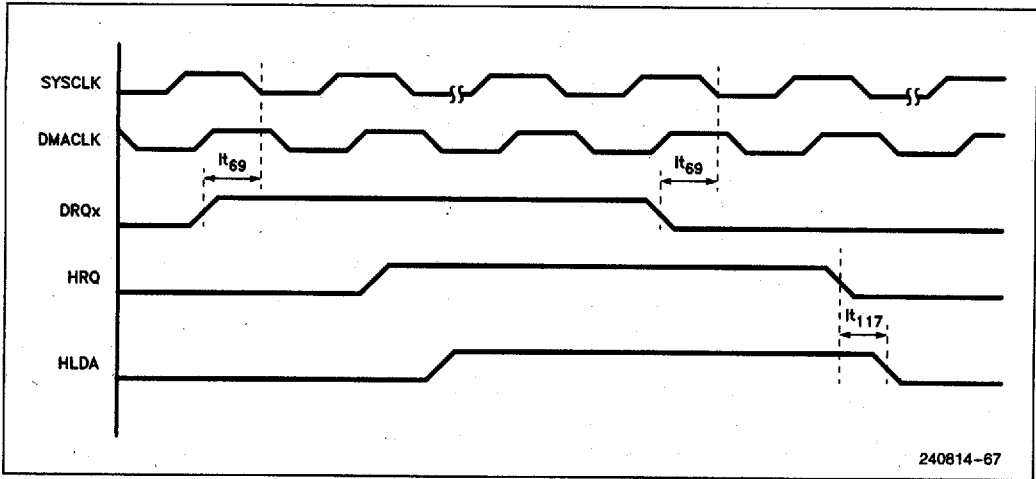


Figure 4.5.5. DMA Controller Timings

240814-67

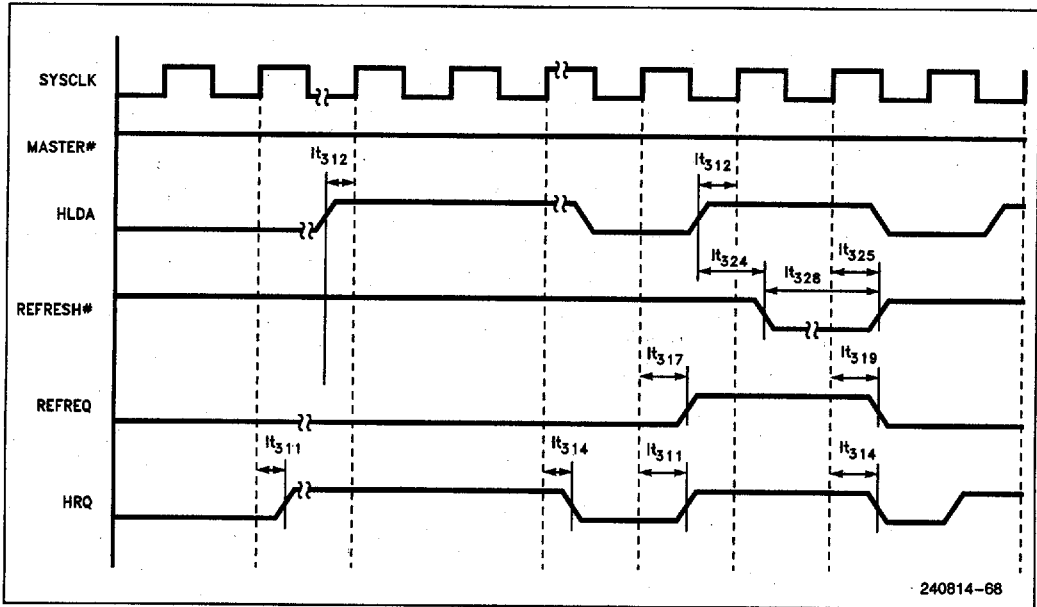
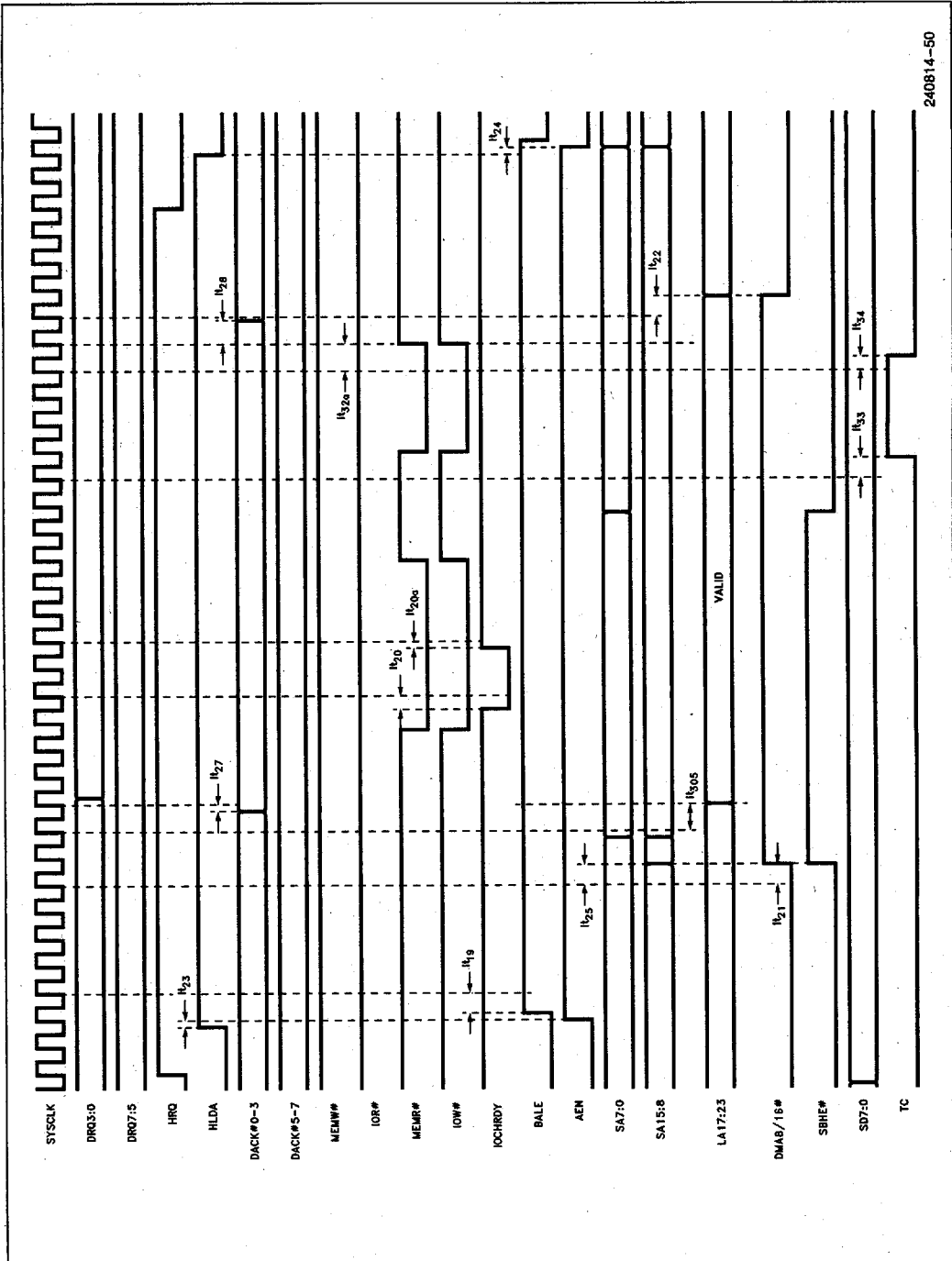


Figure 4.5.6. Refresh Arbitration Timings

240814-68

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34

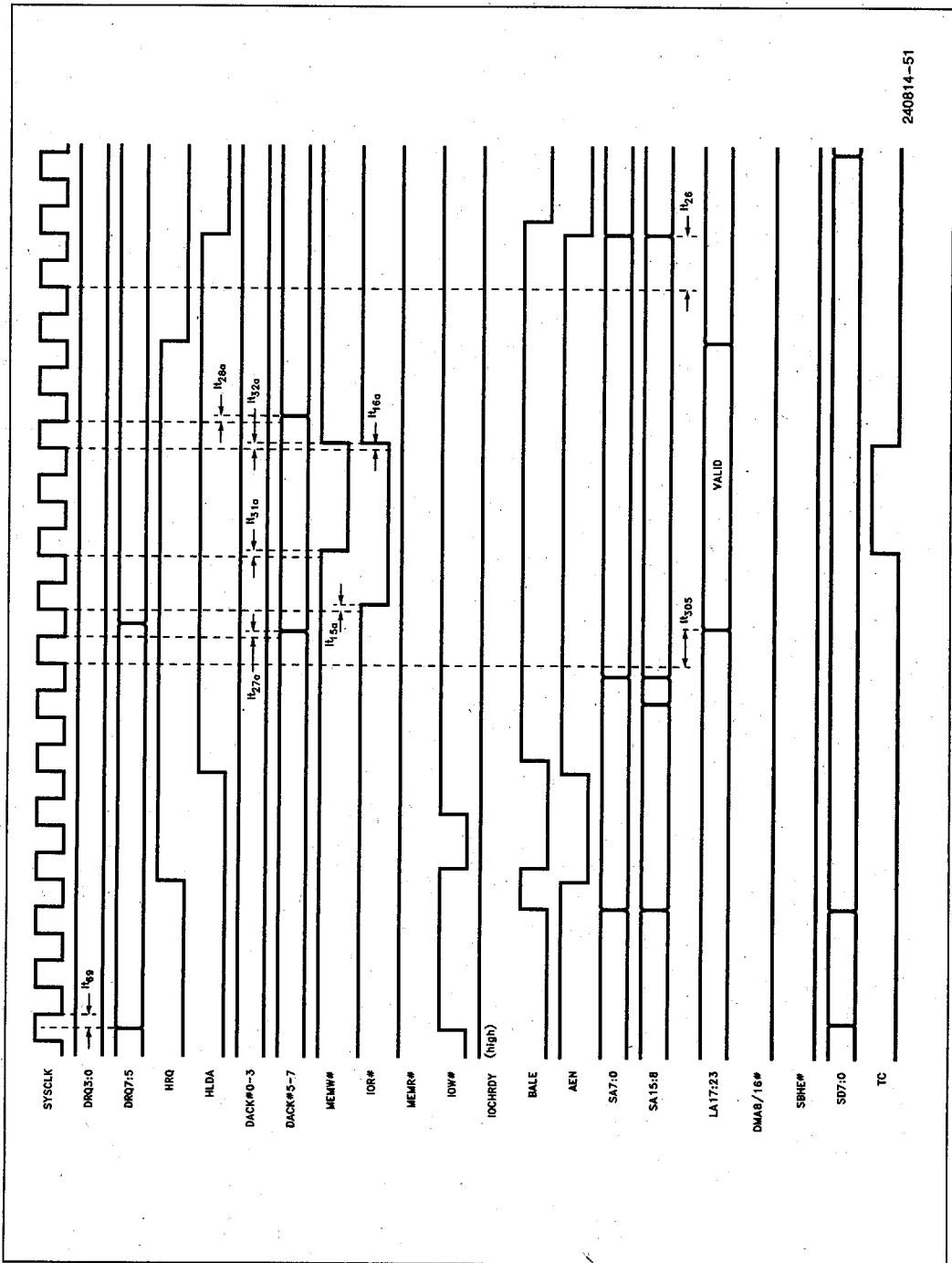


240814-50

Figure 4.5.7. DMA Memory Read Timings (4 MHz)

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34



240814-51

Figure 4.5.8. DMA Memory Write Timings (8 MHz)

56E D ■ 4826175 0119276 767 ■ ITL1 T-49-17-34

4.5 82360SL Timing Diagrams (Continued)

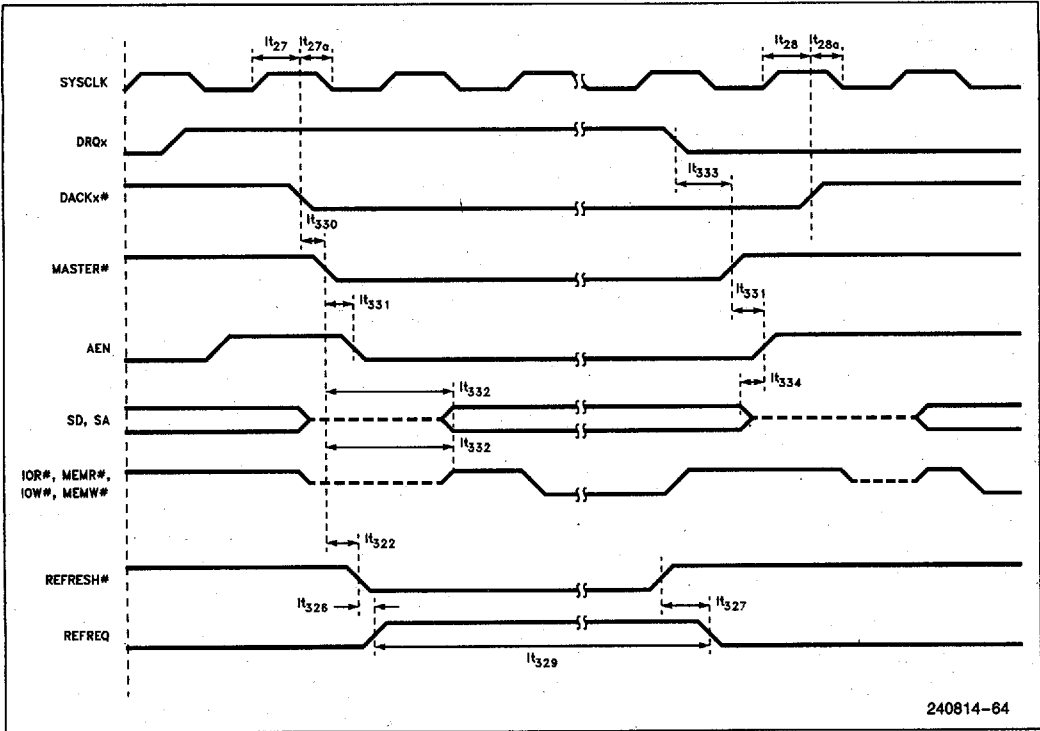


Figure 4.5.9. Bus Master Refresh Cycle Timings

2

240814-64

4.5 82360SL Timing Diagrams (Continued)

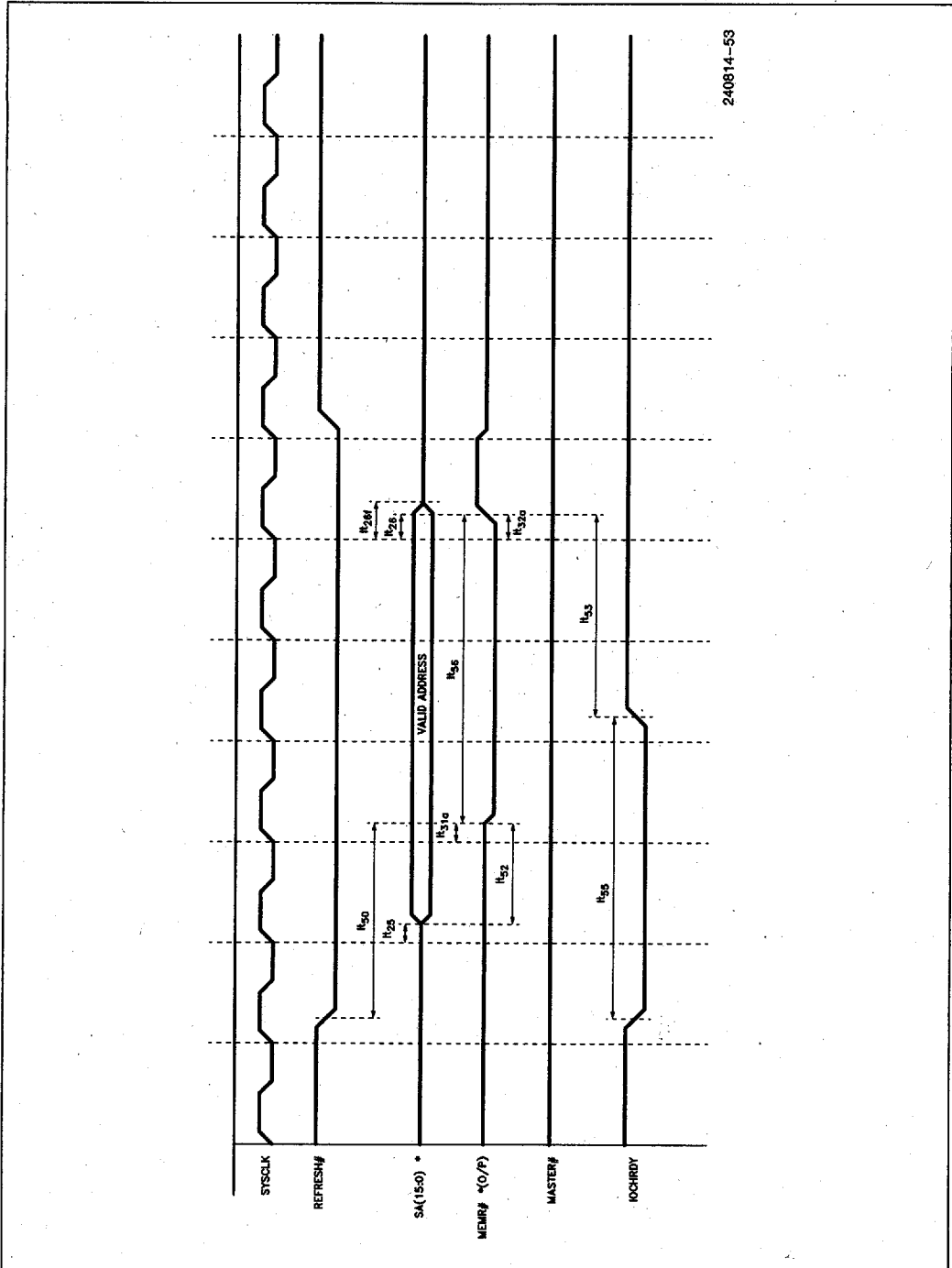
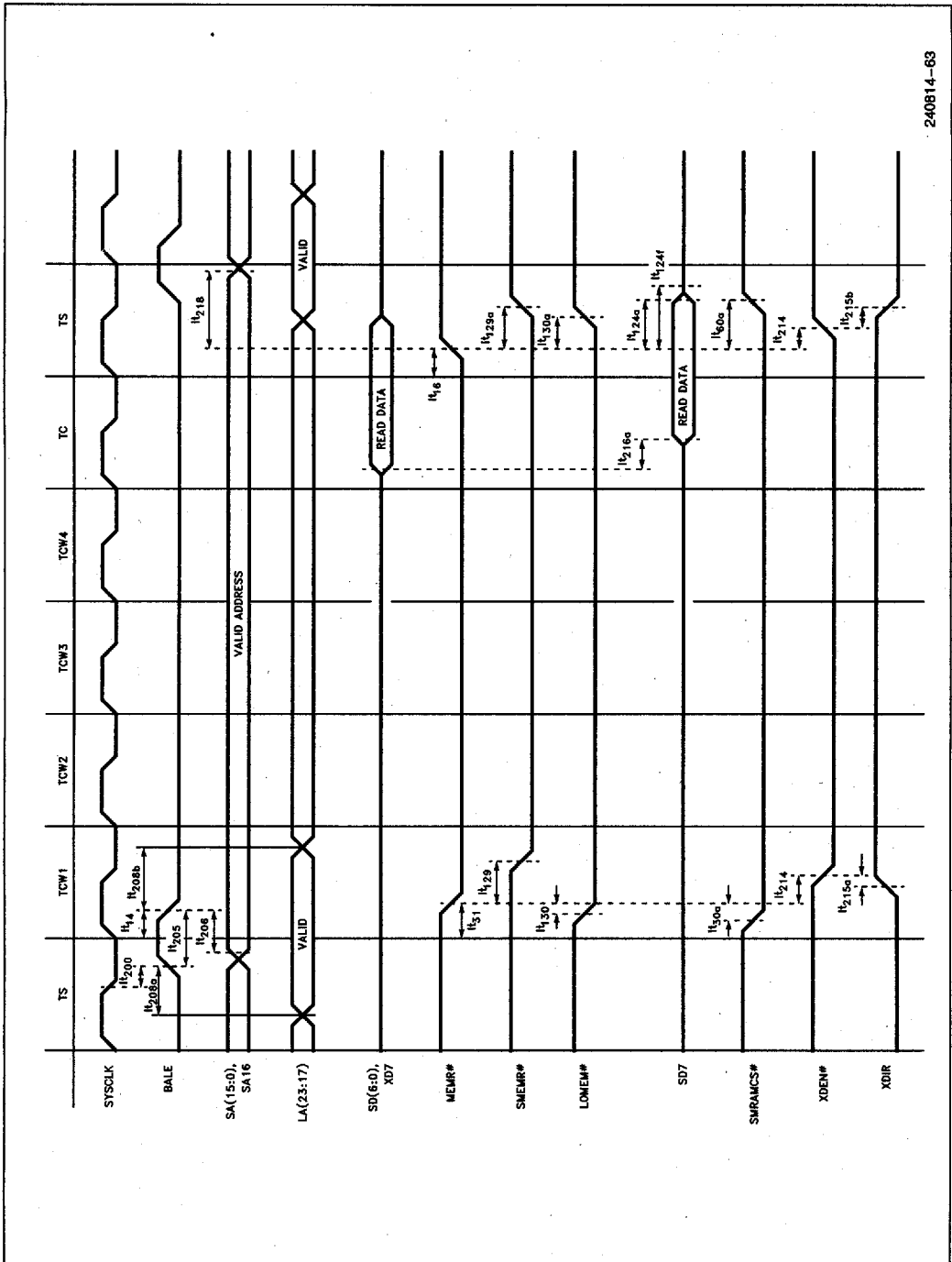


Figure 4.5.10. ISA Bus Master Refresh Cycle with IOCHRDY Timings

4.5 82360SL Timing Diagrams (Continued)

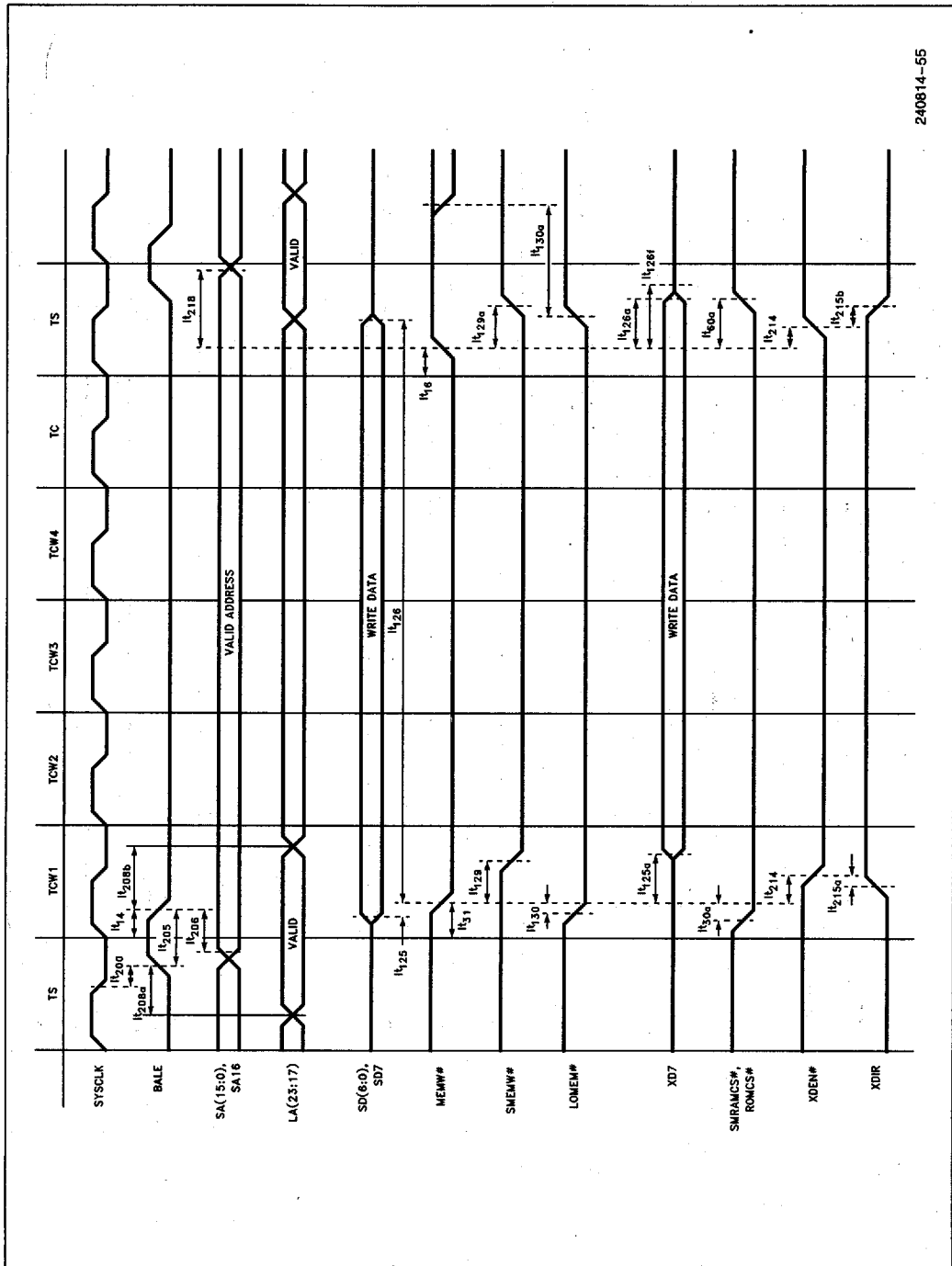


240814-63

2

Figure 4.5.11. X-Bus Control Signals—Memory Read Timings

4.5 82360SL Timing Diagrams (Continued)



240814-55

Figure 4.5.12. X-Bus Control Signals—Memory Write Timings

4.5 82360SL Timing Diagrams (Continued)

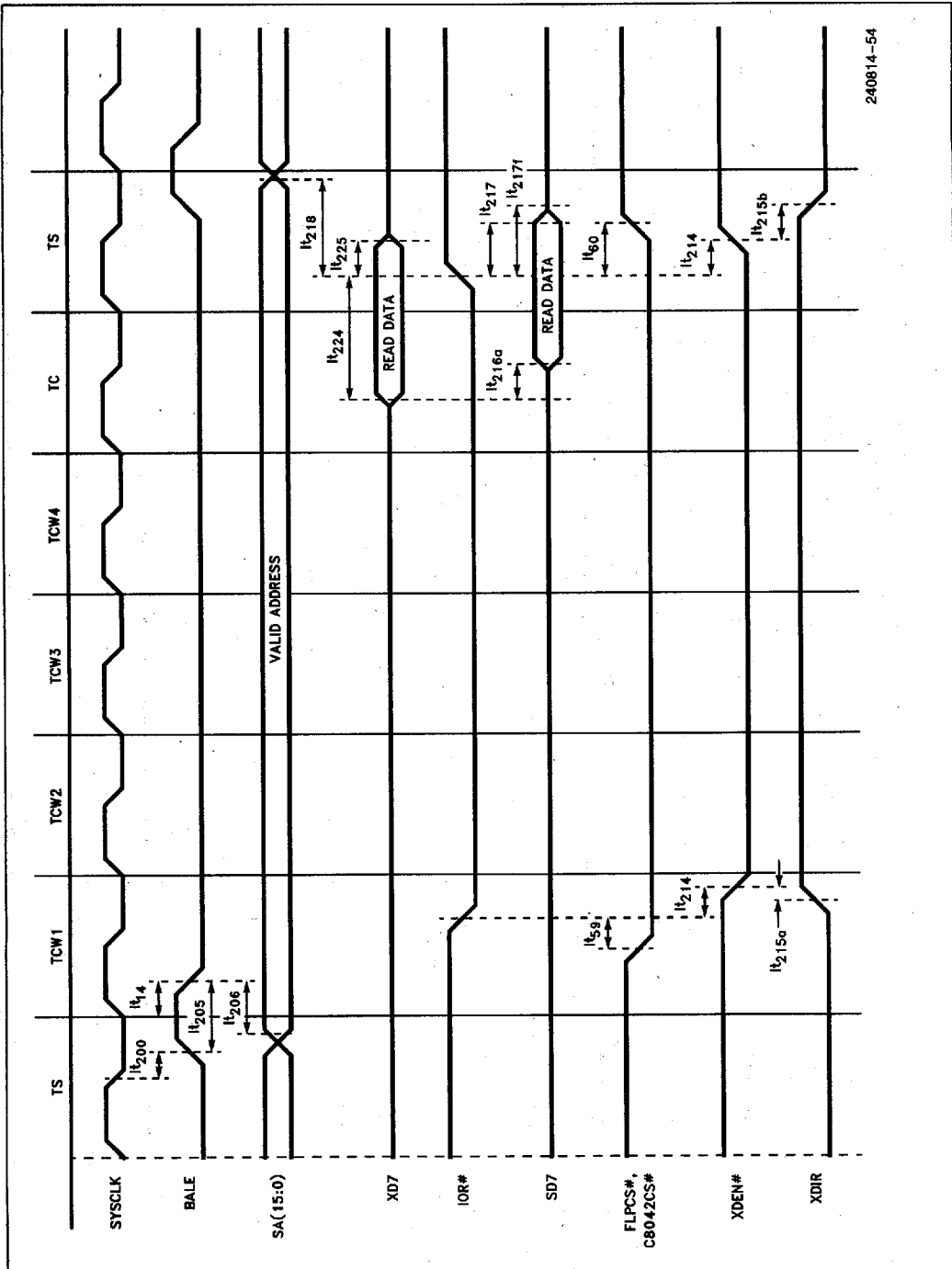


Figure 4.5.13. X-Bus Control Signals—I/O Read Timings

4.5 82360SL Timing Diagrams (Continued)

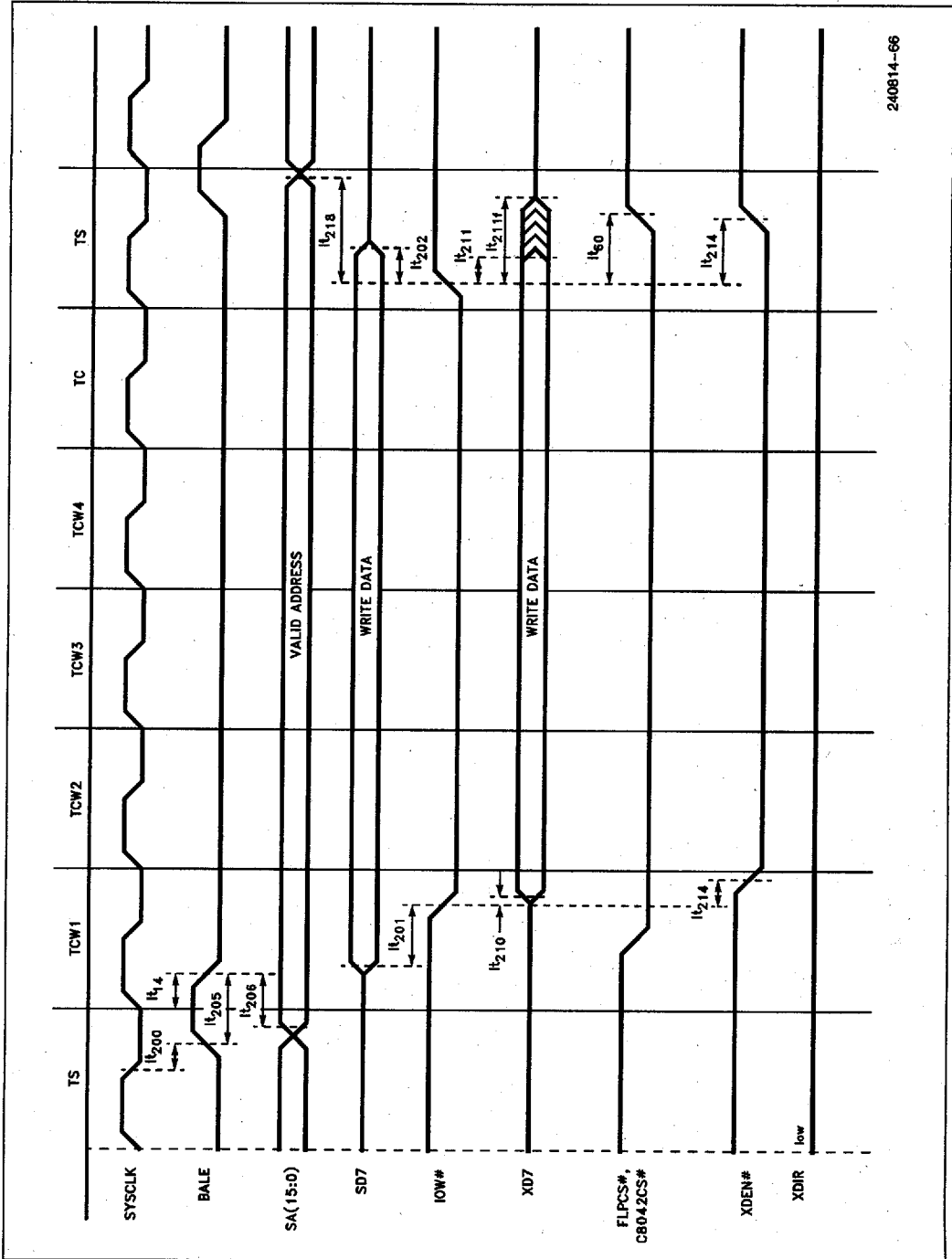


Figure 4.5.14. X-Bus Control Signals—I/O Write Timings

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34

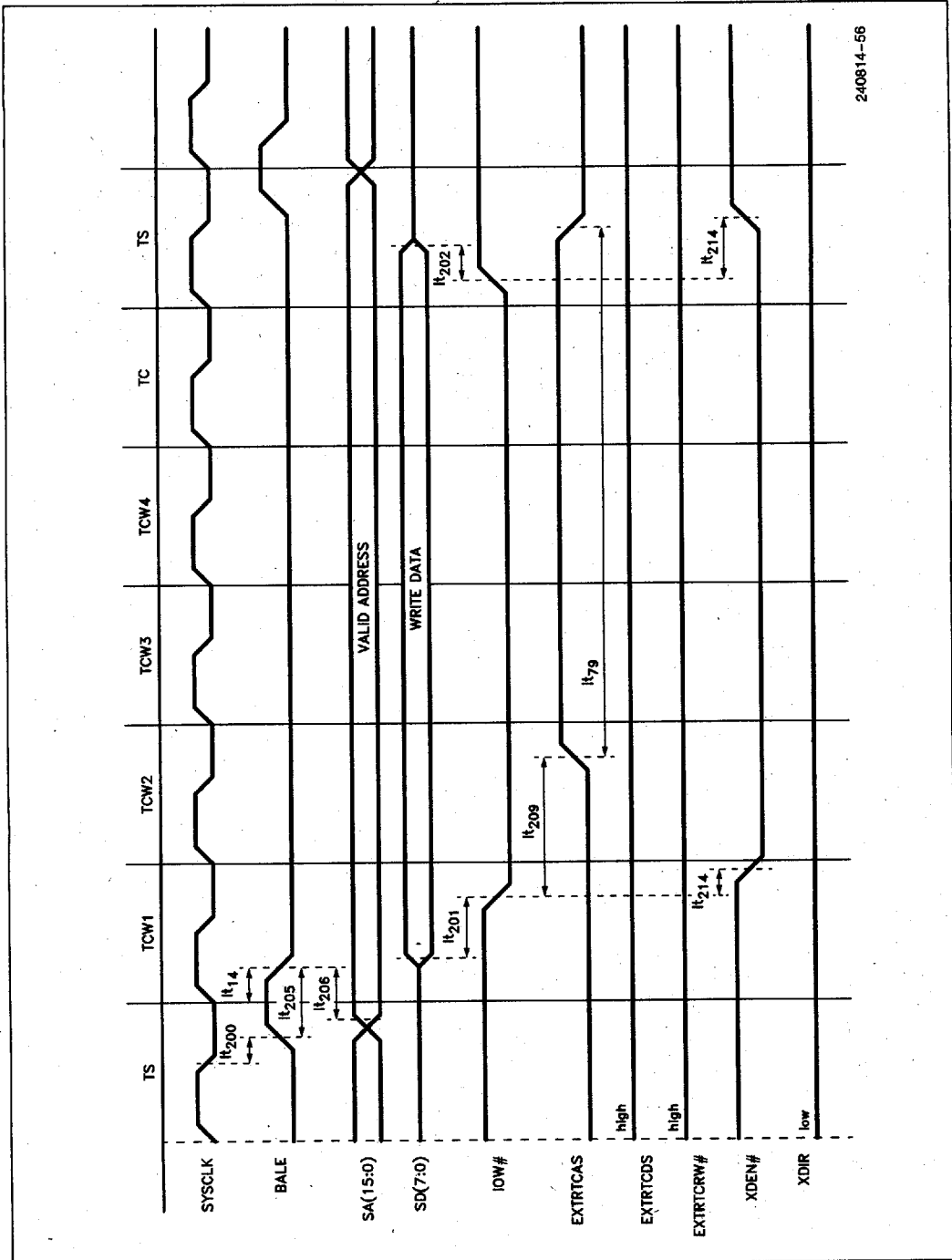


Figure 4.5.15. I/O Port 70 Hex Write—External RTC Timings

4.5 82360SL Timing Diagrams (Continued)

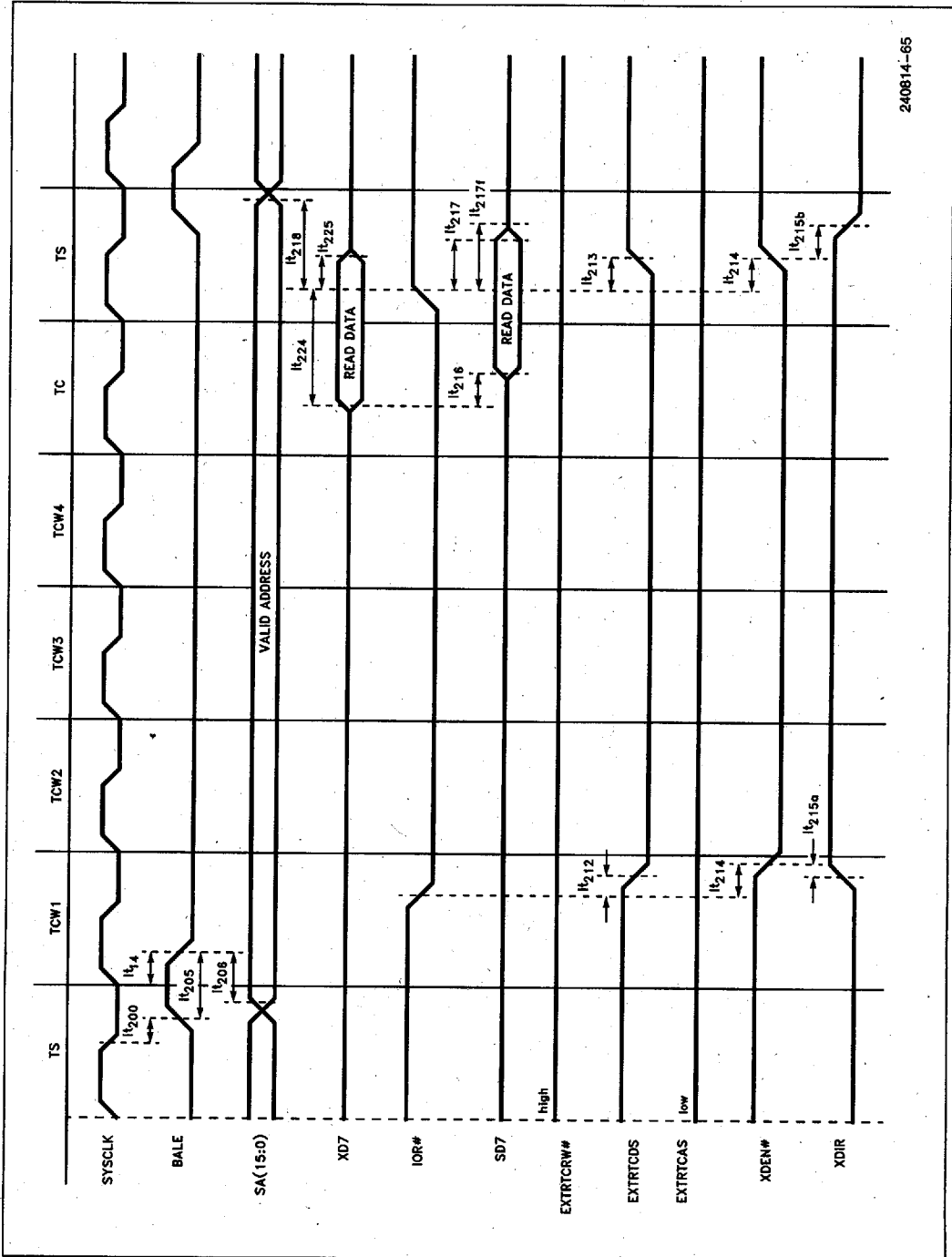


Figure 4.5.16. I/O Port 71 Hex Read—External RTC Timings

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34

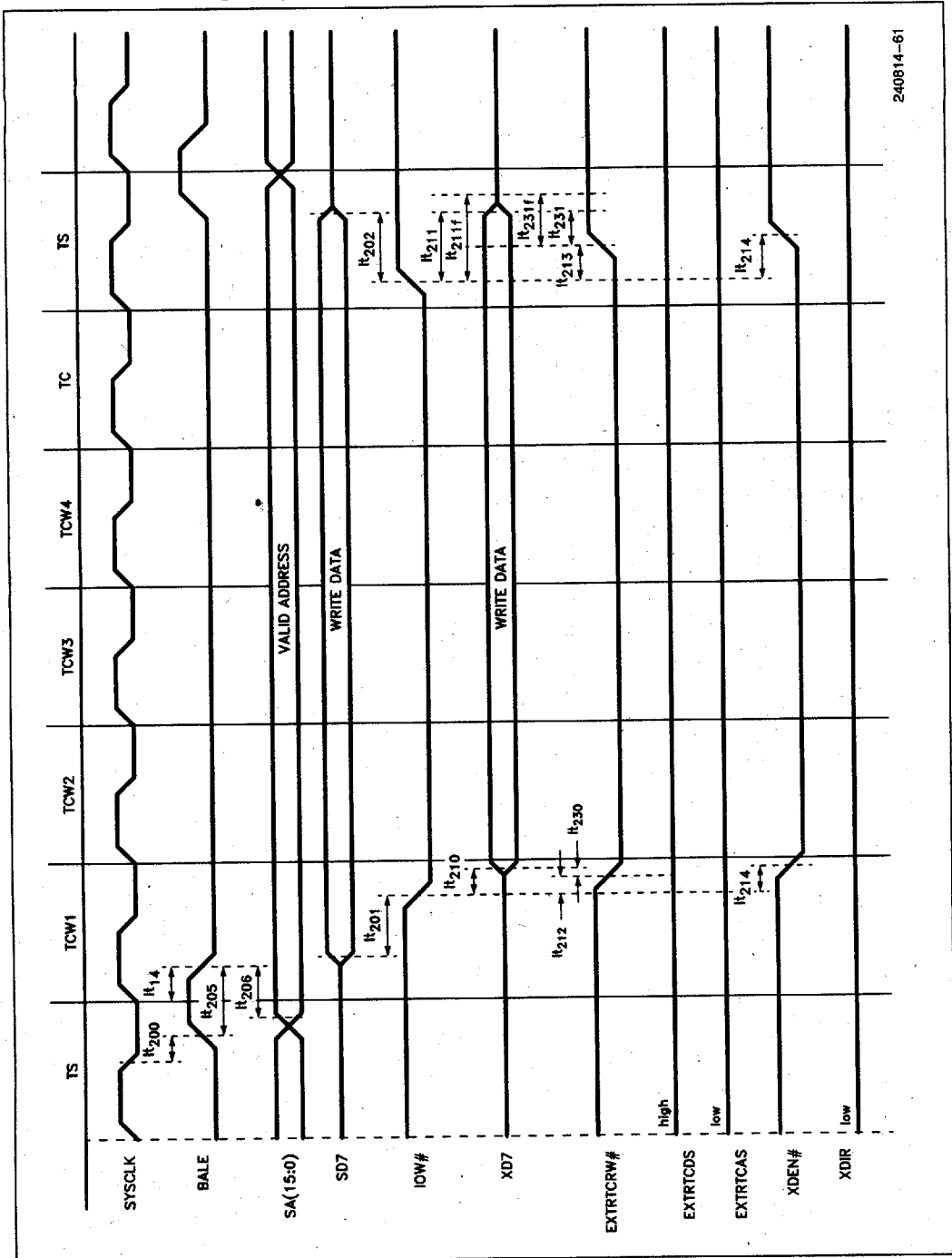
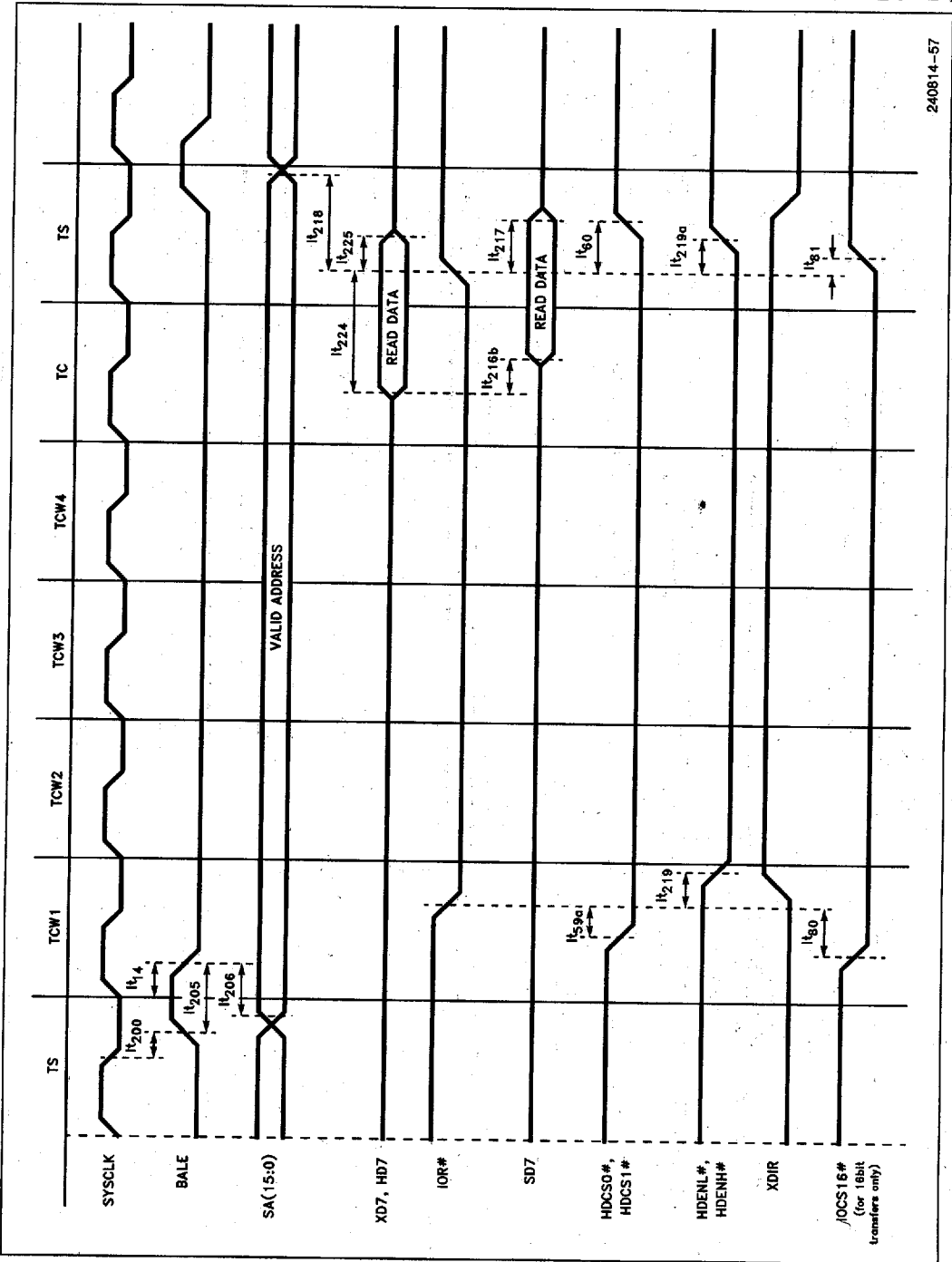


Figure 4.5.17. I/O Port 71 Hex Write—External RTC Timings

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34

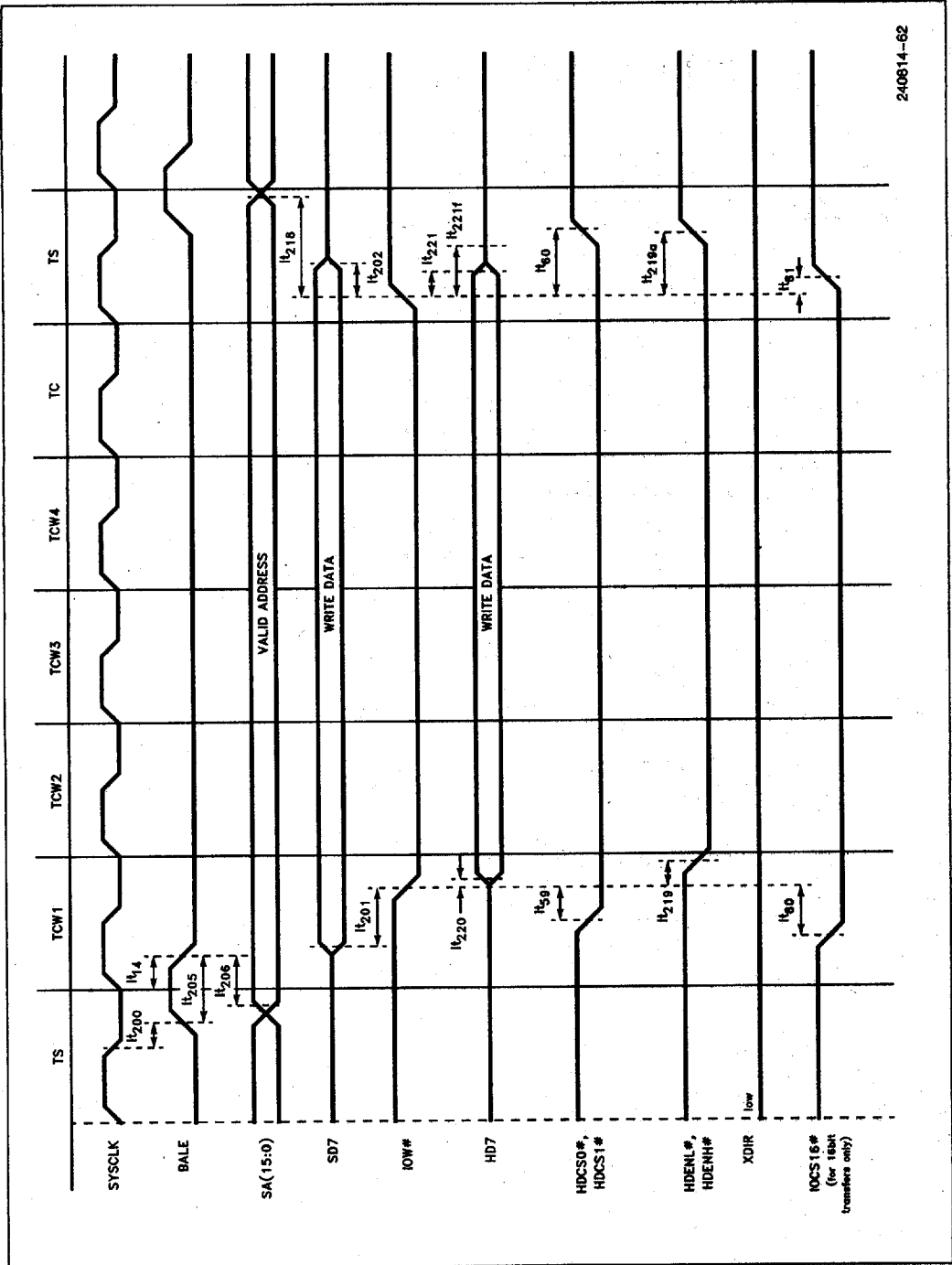


240814-57

Figure 4.5.18. I.D.E. Hard Disk Control Signals—I/O Read Timings

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34



240814-62

Figure 4.5.19. I.D.E. Hard Disk Control Signals—I/O Write Timings

4.5 82360SL Timing Diagrams (Continued)

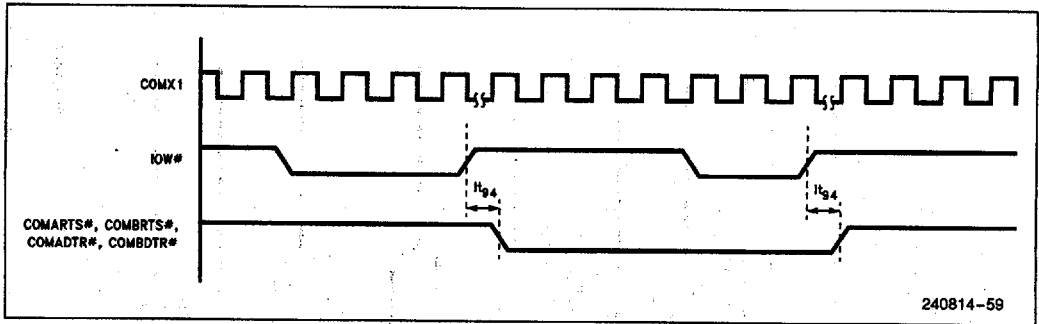
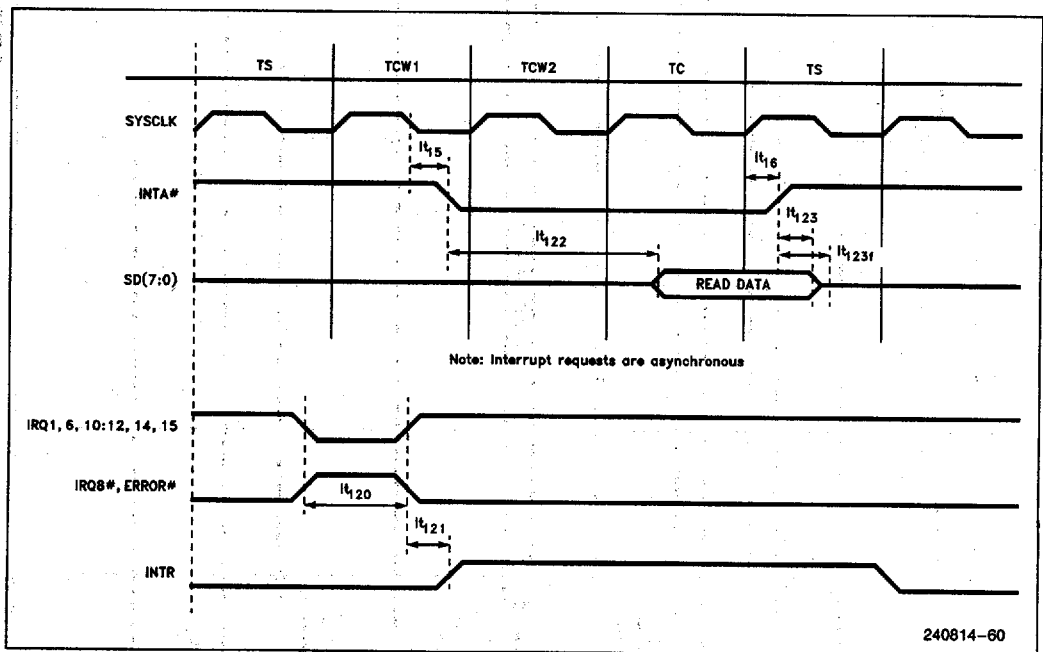


Figure 4.5.20. Serial Port Controller—Modem Control Signal Timings



Note: Interrupt requests are asynchronous

Figure 4.5.21. Interrupt Controller Timings

4.5 82360SL Timing Diagrams (Continued)

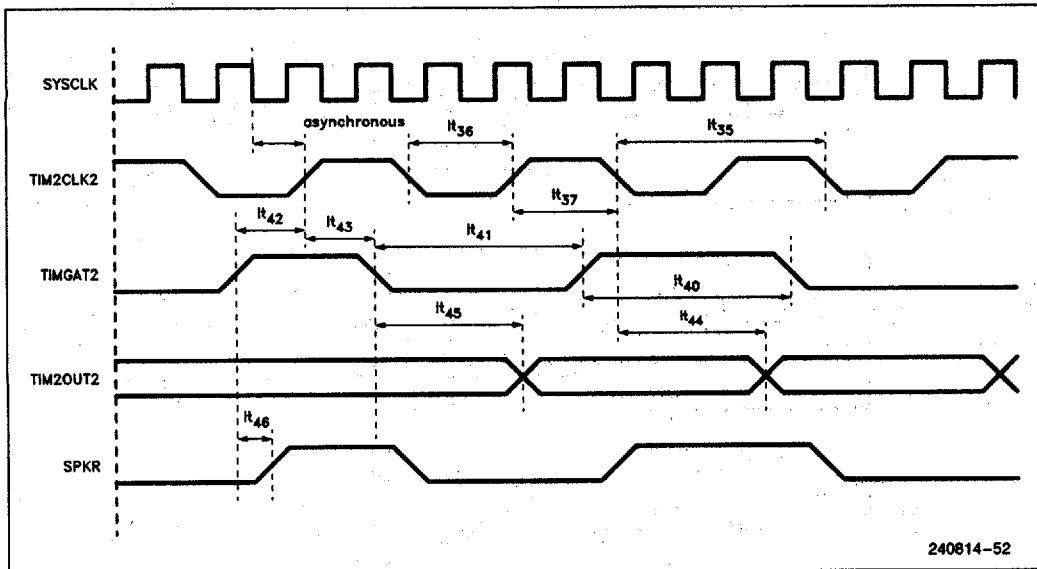


Figure 4.5.22. Programmable Interval Timer/Counter Timings

56E D ■ 4826175 0119289 315 ■ ITL1

T-49-17-34

4.5 82360SL Timing Diagrams (Continued)

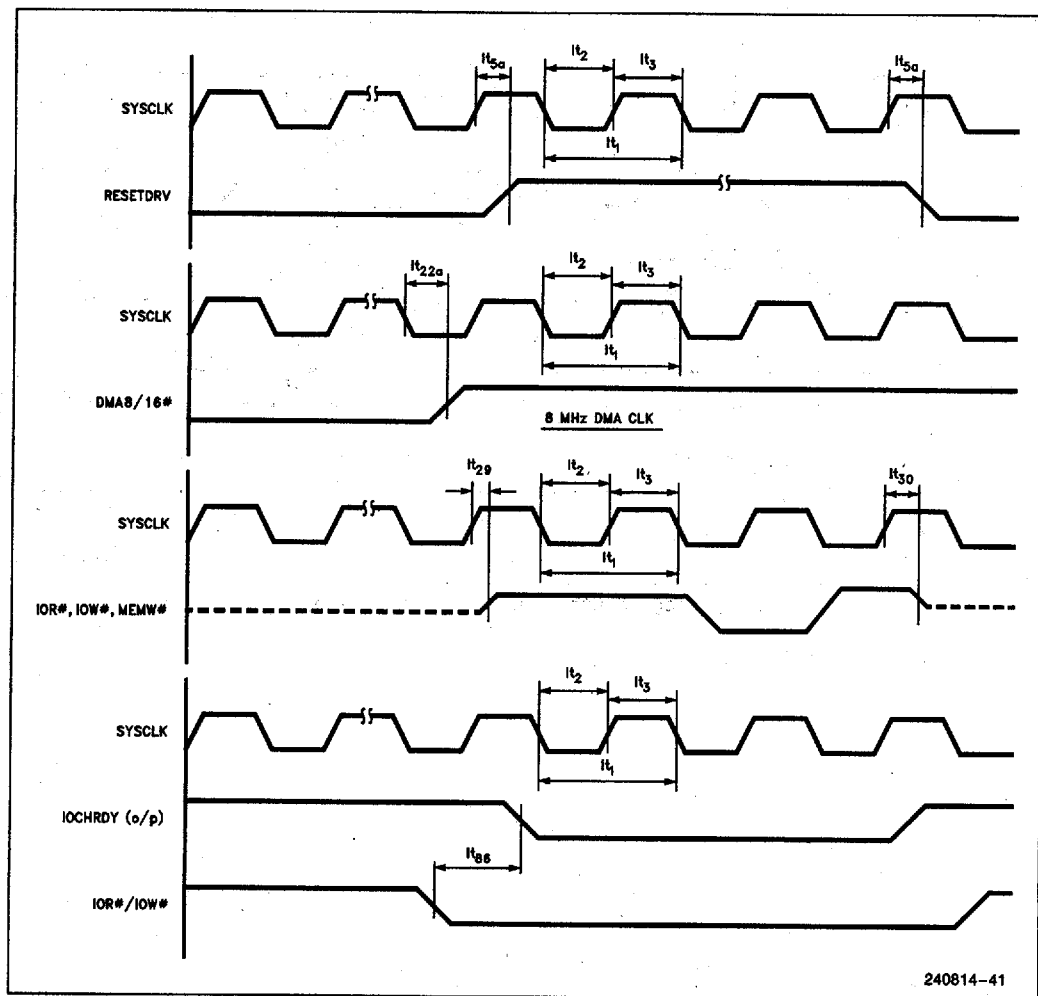


Figure 4.5.23. RESETDRV, DMA8/16#, Command Signals and IOCHRDY with Respect to SYSCLK

4.5 82360SL Timing Diagrams (Continued)

T-49-17-34

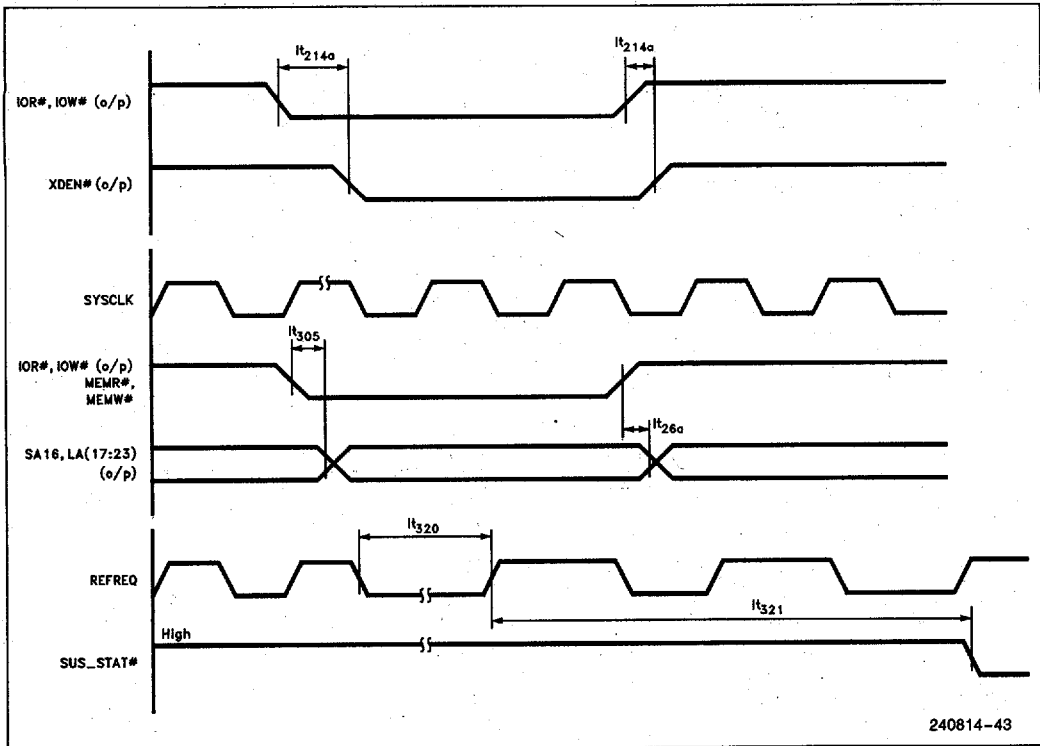


Figure 4.5.24. SUS.STAT#, REFREQ, XDEN# and Command to Address Timings

2

56E D ■ 4826175 0119291 T73 ■ ITL1 T-49-17-34

4.5 82360SL Timing Diagrams (Continued)

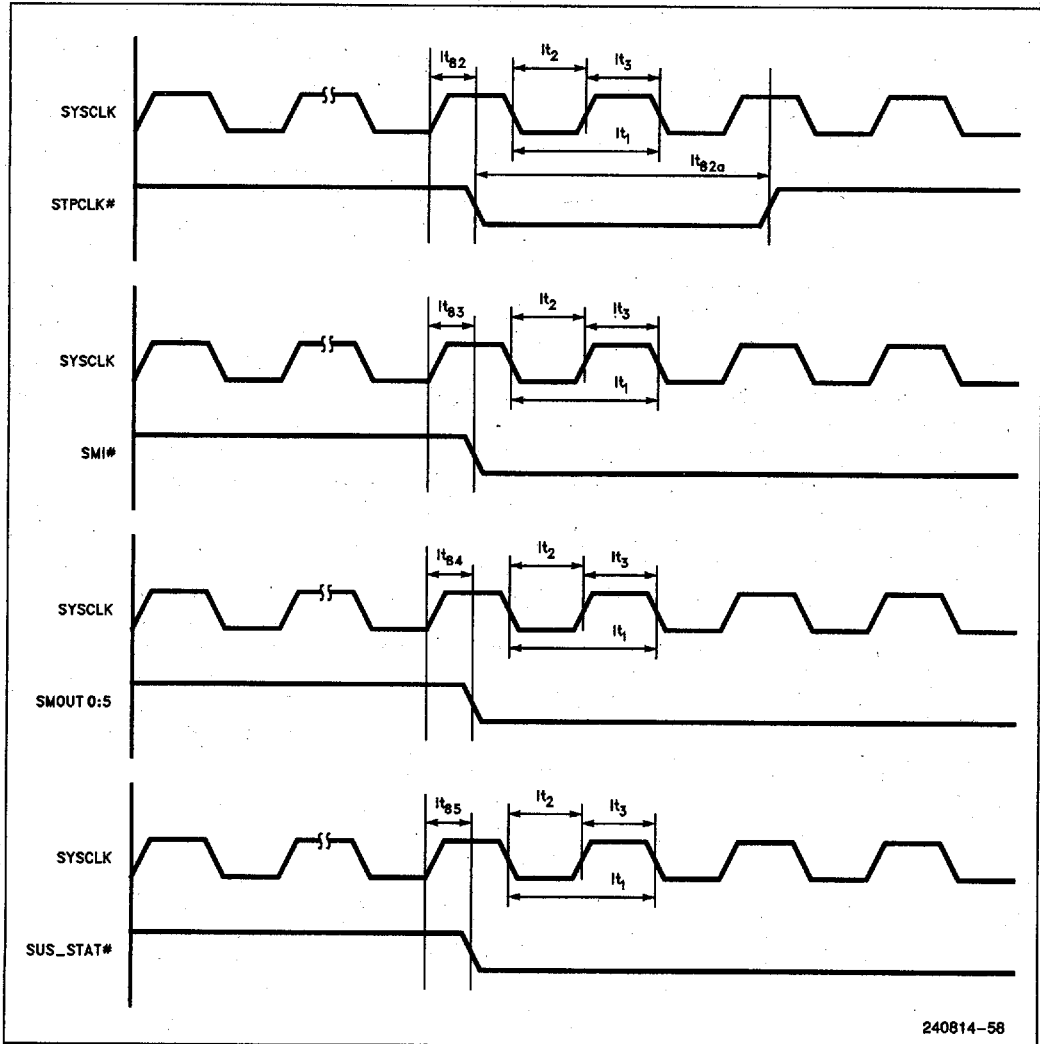


Figure 4.5.25. System Power Management Control Signal Timings

4.5 82360SL Timing Diagrams (Continued)

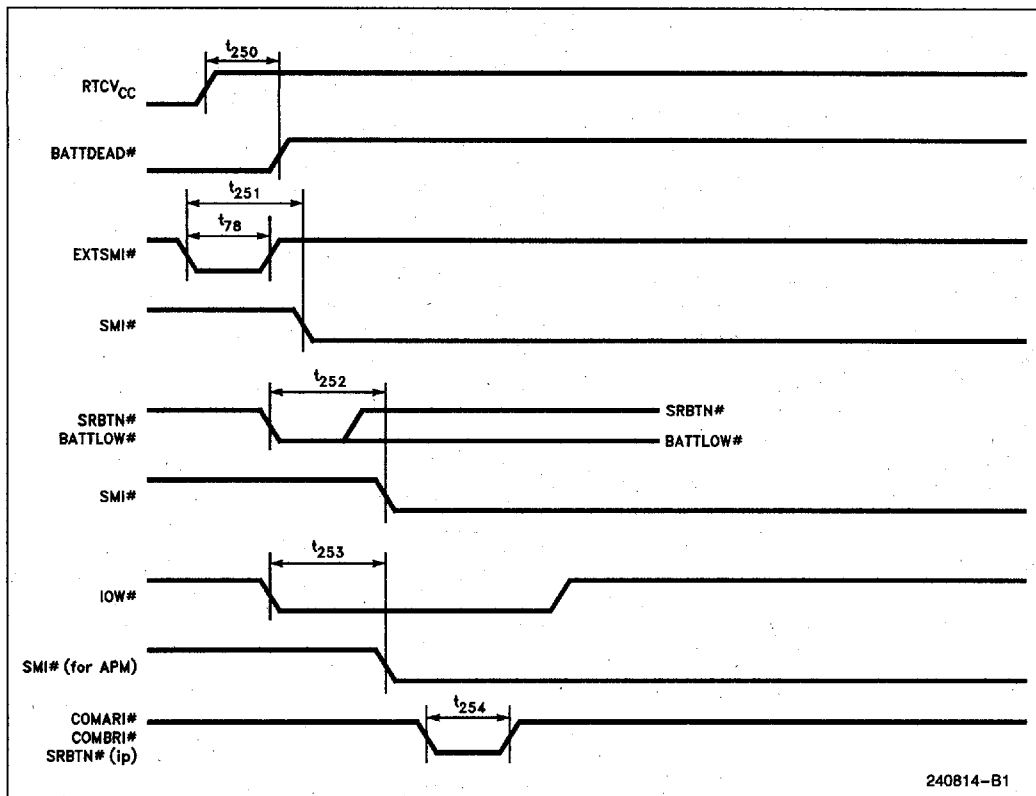
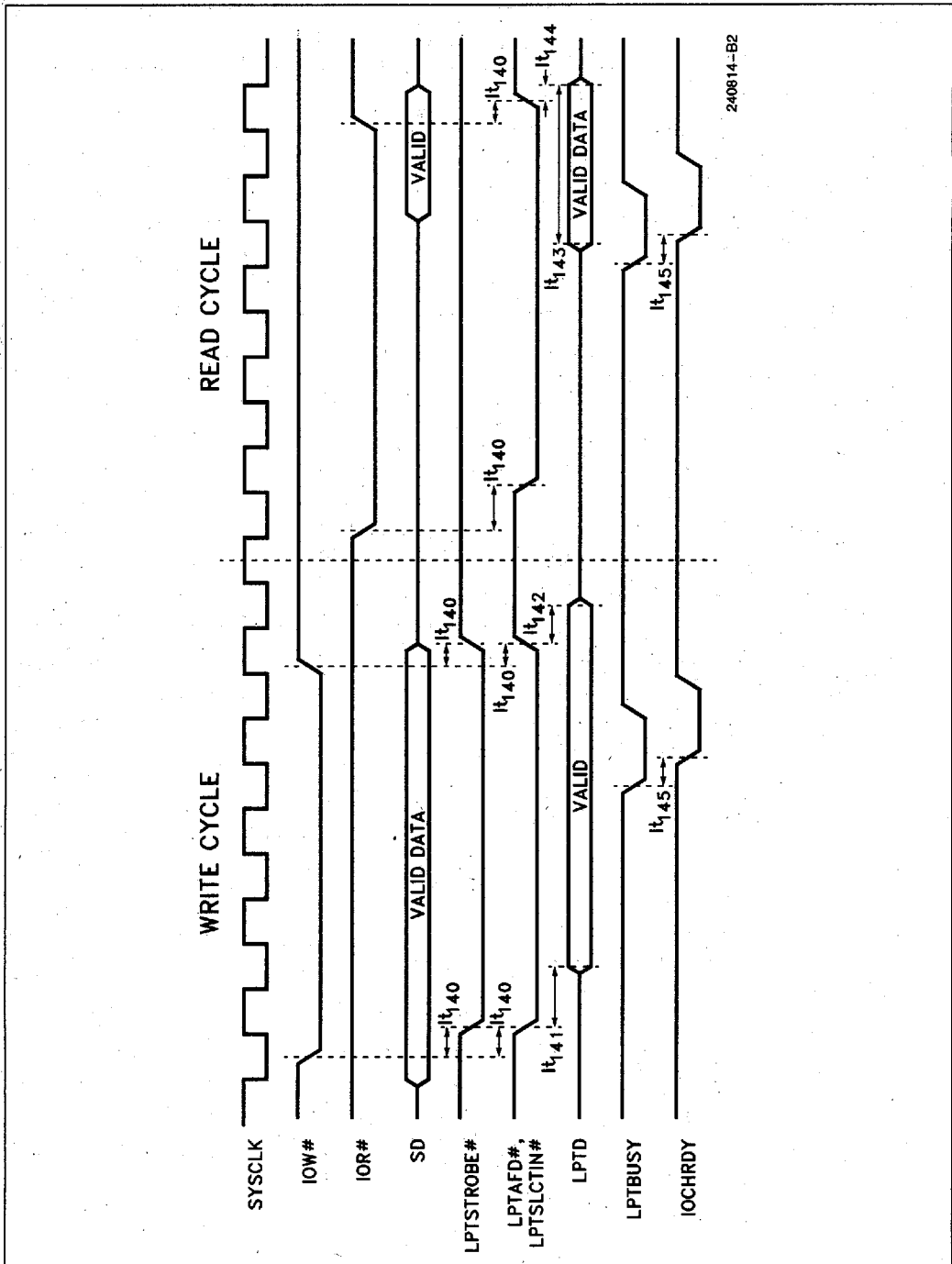


Figure 4.5.26. Power Management Timings

2

4.5 82360SL Timing Diagrams (Continued)



240814-B2

Figure 4.5.27. Fast Parallel Port Timing

4.6 Capacitive Derating Information

In the A.C. timing table presented in Section 4.4, all max and min timings are tested at a load of 50 pF. All max timings are specified at the maximum load condition for the pin and all min timings are specified for the minimum load conditions for the pin.

If the load on a pin falls within the range of the min and max capacitance specified, no derating calculations need to be done for synchronous timings. If a lighter or heavier capacitive load is connected to any pin, signal delay will change. To allow the system designer to account for such loading differences in a system, a family of capacitive derating curves are provided in this section.

The derating curves are divided into four groups—Fast rise, fast fall, slow rise and slow fall curves. Each group has one curve for the buffer type associated with the pin corresponding to a signal. Depending upon the parameter for which the timing is being specified, curves of different groups should be used to derate the specification. The group to be used is given in the column "Derating" associated with each specification. The nomenclature used in this column is as follows: FR = Fast Rise, SR = Slow Rise, FF = Fast Fall, SF = Slow Fall. The curve corresponding to the signal in question may be found from the "Derating curve" column of the pin assignment table in Section 4.1.

In the case of output timing specifications, two group notations appear in the "Derating" column. The first of these corresponds to the reference signal and the second corresponds to the target signal.

When a specification is made about a bus or the specification is valid for both rise and fall times, only the type of derating is specified. For instance, F = Fast curve, S = Slow curve. Either the rise or the fall time derating may be used. To make a conservation calculation, use the smaller derating value among rise and fall for fast curves and the larger derating value for the slow curves.

When a specification has both a min and a max time, the derating curves for the min and the max times are separated by a semi-colon.

If loading conditions are not specified in the notes column, the timing parameter is specified for the worst case loading possible.

The rationale in the assignment of derating curves to specifications is as follows.

1. For synchronous (Clock related) specifications, all maximum timings are derated from slow curves. This is the worst case situation.

2. For synchronous (Clock related) specifications, all minimum timings are derated from fast curves. The reasoning here is that fast parts cause the worst case for minimum timings since the signal transition occurs earlier than for slow parts. Since these fast parts have fast buffers, the fast derating curves are used.

3. For output to output timings, the derating curve to be chosen depends on a combination of internal delays and buffer delays in fast and slow parts. From an analysis of the worst case situation, appropriate curves are selected for the system designer.

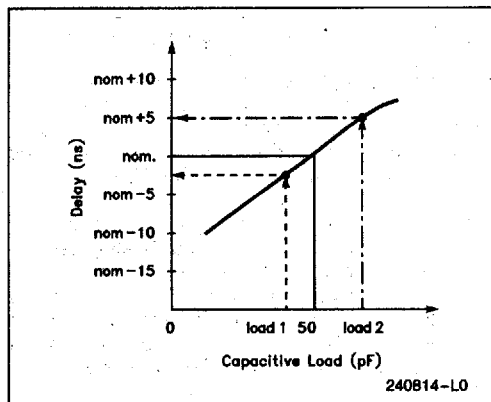
To use the derating curves, follow the procedure outlined here.

1. From the "Derating" column of A.C. timing table in Section 4.4, find the group of curves that must be used for a particular specification.
2. From the Pin assignment chart in Section 4.1, find the letter corresponding to the signal(s) under consideration from the column "Derating Curve".
3. In this section, find the derating curve of the correct group and letter.
4. Calculate the capacitive loading on the signal(s) under consideration.
5. Find this load point on the capacitive load axis of the derating curve.
6. Project a vertical line to the derating curve from the load point and draw a horizontal line and from the point the vertical line intersects the curve.
7. Estimate the amount of time from the Nominal point to the point where the horizontal line meets the delay axis. This is the derating value for the signal under consideration.
8. If the point where the horizontal meets the delay axis is **above** the nominal value, then
 - If the signal under consideration is the **reference signal** (in output to output timings) the derating value should be **subtracted** from the timing specification.
 - If the signal under consideration is the **target signal** (in all timings) the derating value should be **added** to the timing specification.
9. If the point where the horizontal meets the delay axis is **below** the nominal value, then
 - If the signal under consideration is the **reference signal** (in output to output timings) the derating value should be **added** to the timing specification.
 - If the signal under consideration is the **target signal** (in all timings) the derating value should be **subtracted** from the timing specification.

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In some output to output specifications, the loads are not at the nominal points for the curves specified. The loads at which the specifications are made are indicated in the notes column. The same procedure as above may be used for derating except that a nominal point corresponding to the load specified must first be found on the curve specified.



Using the Capacitive Derating Curves

82360SL I/O Maximum Timing Derating Curves

FALLING

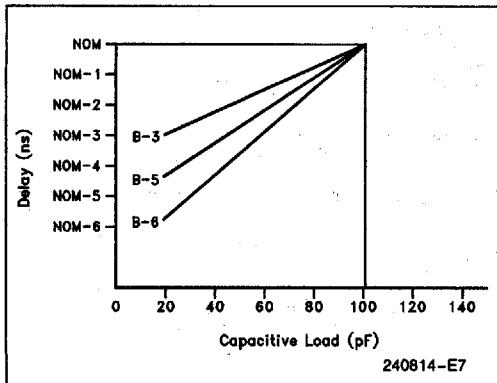


Figure 4.6.1a

RISING

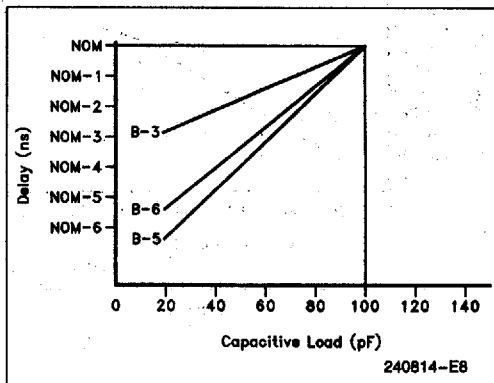


Figure 4.6.1b

2

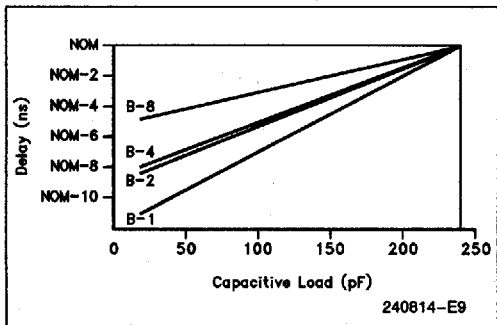


Figure 4.6.2a

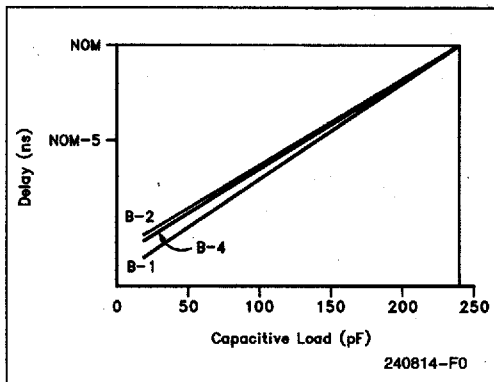


Figure 4.6.2b

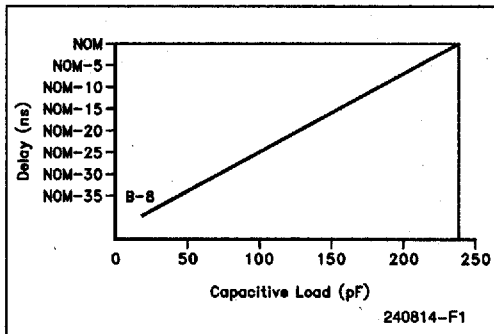


Figure 4.6.2c



56E D ■ 4826175 0119297 491 ■ ITL1

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82360SL I/O Maximum Timing Derating Curves (Continued)

FALLING

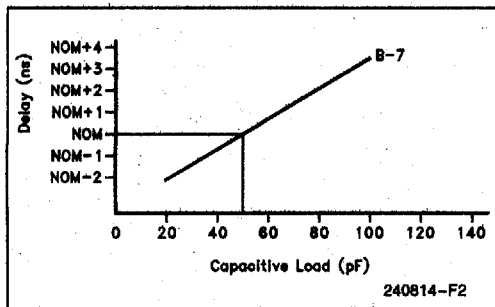


Figure 4.6.3a

RISING

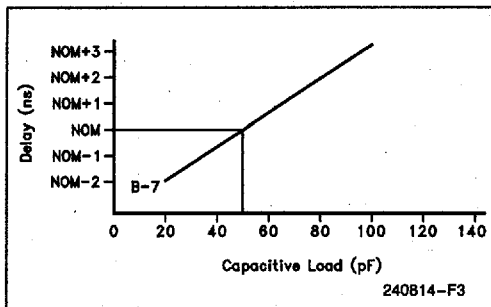


Figure 4.6.3b

56E D ■ 4826175 0119298 328 ■ ITL1

82360SL I/O Minimum Timing Derating Curves (Continued)

T-49-17-34

FALLING

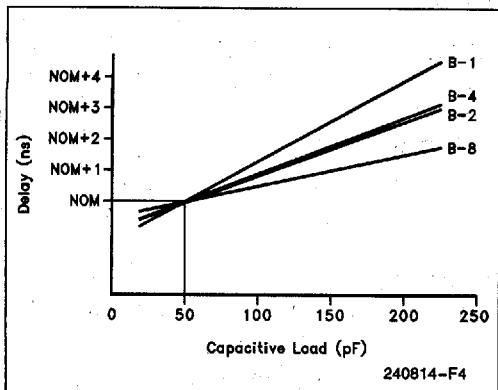


Figure 4.6.4a

RISING

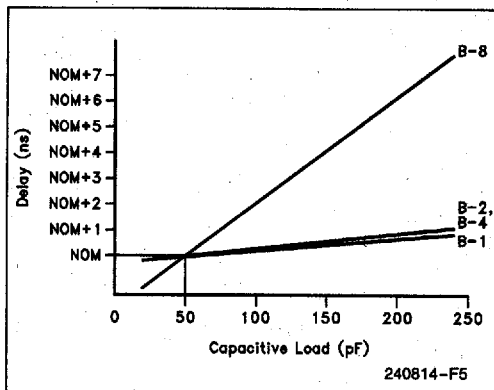


Figure 4.6.4b

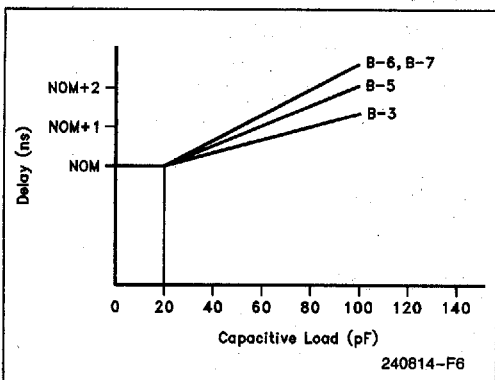


Figure 4.6.5a

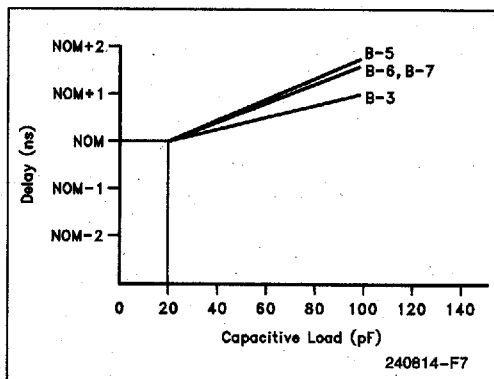


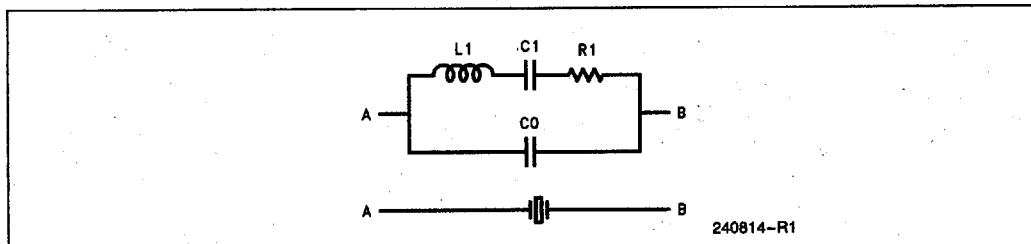
Figure 4.6.5b

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4.7 Crystal and Oscillator Specifications

The three on-chip oscillators are designed for parallel resonant AT cut crystals at 14.31818 MHz, 1.8432 MHz and 32.768 KHz frequencies. Typical crystal parameters are shown below.

Crystal Equivalent Circuit



Pins	CX1, 2	COMX1, 2	RTCX1, 2
Frequency	14.31818 MHz	1.8432 MHz	32.768 KHz
R1	12Ω	100Ω	50 KΩ
C1	0.028 pF	0.012 pF	0.003 pF
L1	4.4 mH	0.65H	8245.5H
C0	7 pF	4 pF	1.7 pF
Q	35K	70K	30K
CL	15 pF-30 pF	15 pF-40 pF	10 pF-20 pF

Q = Quality Factor

CL = Load Capacitance

If external oscillators are used the following timing specs should be observed.

	tr (max)	tf (max)	thi (min)	tlo (min)
CX1	10 ns	10 ns	20 ns	20 ns
COMX1	20 ns	20 ns	200 ns	200 ns
RTCX1	20 ns	20 ns	1200 ns	1200 ns

NOTES:

tr, tf measured from 0.8V to 4V for oscillators at 5V V_{CC}.

tr, tf measured from 0.8V to 2V for oscillators at 3V V_{CC}.

thi measured from 4V to 4V for oscillators at 5V V_{CC}.

thi measured from 2V to 2V for oscillators at 3V V_{CC}.

tlo measured from 0.8V to 0.8V for oscillators at 3/5V V_{CC}.

The above data are system specs and are not tested by Intel.

5.0 PACKAGE AND THERMAL SPECIFICATIONS

The case temperature for CPU is specified in Table 5-2. 82360SL I/O operates at a case temperature range from 0°C to 90°C. The case temperature should be measured in the operating environment to determine whether the SL SuperSet is within the specified operating temperature range. The case temperature should be measured at the center of the top surface of the package. When the SuperSet has a voltage applied the operating temperature range is applicable rather than the storage temperature.

The following definitions and assumptions are used to determine the recommended maximum case temperature for the SuperSet:

T_A = Ambient temperature in °C

T_C = Case Temperature in °C

θ_{JC} = Package thermal resistance between junction and case

θ_{JA} = Package thermal resistance between junction and ambient

T_J = Junction temperature in °C

P = Power consumption in watts

The ambient temperature can be evaluated by using the values of thermal resistance between junction and case, θ_{JC} and the thermal resistance between junction and ambient, θ_{JA} in the following equations:

$$T_J = T_C + P \cdot \theta_{JC}$$

$$T_A = T_J - P \cdot \theta_{JA}$$

$$T_C = T_A + P \cdot [\theta_{JA} - \theta_{JC}]$$

Values for θ_{JA} and θ_{JC} are given in Table 5-1 for the Intel386 SL CPU and 82360SL:

Table 5-1. Thermal Resistance

Package	θ_{JC} (°C/W)	θ_{JA} (°C/W) vs Air Flow- ft/min (m/sec)			
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
196PQFP	6	23	19	16	13.5
227L LGA(1)	5	15	12	10.5	9.5

NOTE:

1. These values reflect use of a typical LGA socket.

ABSOLUTE MAXIMUM RATING

Table 5-2. provides environmental stress rating for the packaged CPU and I/O. Functional operation at the storage maximum and minimum ratings is not guaranteed.

Extended exposures to maximum ratings may affect device reliability. Further, precautions should be taken to avoid high static voltages and electric fields to prevent static electric discharge.

Other system components such as memory subsystem (DRAM), storage peripherals (hard disk/floppy disk), I/O and display subsystem may reduce the absolute maximum storage temperature conditions due to inherent physical characteristics of the other components.

Table 5-2. Absolute Maximum Ratings

Case Temperature under Bias	0°C to +90°C(1)	Standard 5V CPU and I/O
	0°C to 80°C(1)	Low-Voltage CPU
Storage Temperature	-65°C to +150°C	
V_{CC5V} = 5.0V ± 10%		
Voltage on Any 5V Interface Pin with Respect to Ground	-0.5V to V _{CC} + 0.5V	
Supply Voltage with Respect to V _{SS}	-0.5V to 6.5V	
V_{CC3.3V} = 3.3V ± 0.3		
Voltage on Any 3.3V Interface Pin with Respect to Ground	-0.5V to 4.6V	
Supply Voltage with Respect to V _{SS}	-0.5V to 4.6V	

NOTE:

1. Case temperature under Bias maximum rating also includes the case where CPU and 82360 SL I/O are in suspend or standby mode. In standby mode and in specific cases in suspend mode, power is applied to the CPU and I/O for operation of the Real-Time Clock and DRAM refresh.



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6.0 DAMPING RESISTOR REQUIREMENTS

The SL SuperSet has powerful output buffers capable of directly driving large loads. These buffers are designed for fast signal transition times and hence have low output impedance. Due to a mismatch between the output impedance of the buffers and the characteristic impedance of the load (trace capacitance and the total number of devices) voltage overshoot and ringing can occur at signal transitions. By matching the output impedance with the characteristic input impedance and avoiding long trace lengths,

the system designer can minimize the transmission line reflections and ringing.

The ringing at signal transitions of address and data lines cause long unstable periods. Ringing on control signals can cause false latching. To minimize the ringing effect series damping resistors may have to be connected. For the resistor values on specific signals (e.g., MA, MD and NPXCLK), consult the Intel386 SL Microprocessor SuperSet System Design Guide (Intel Order # 240816).

7.0 MECHANICAL DETAILS OF LGA AND PQFP PACKAGES

design the parts in. For more detailed information on packages and package types, please refer to "Surface Mount Technology Guide" (Order #240585)

This section contains mechanical details of the two types of packages used in the SL SuperSet to help

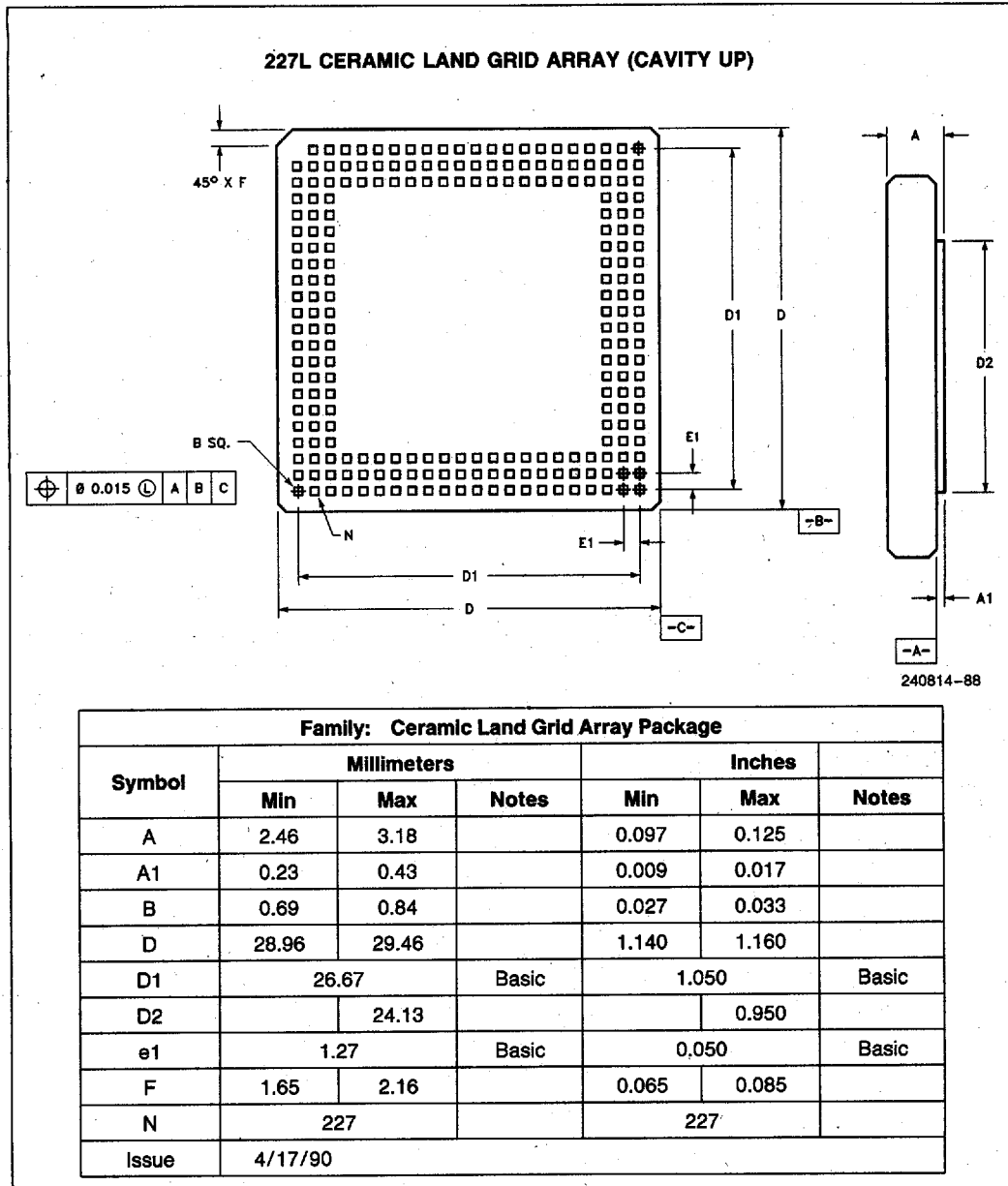


Figure 7.1a. Principal Dimensions of the Intel386™ SL CPU in a 227-Lead LGA Package

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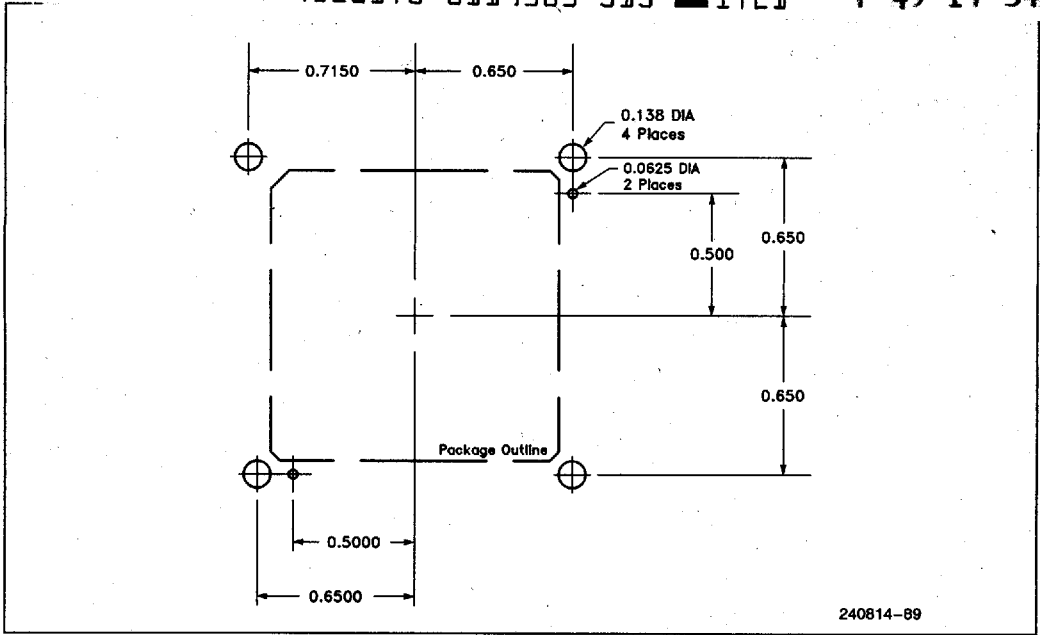


Figure 7.1b. Recommended LGA Socket Footprint

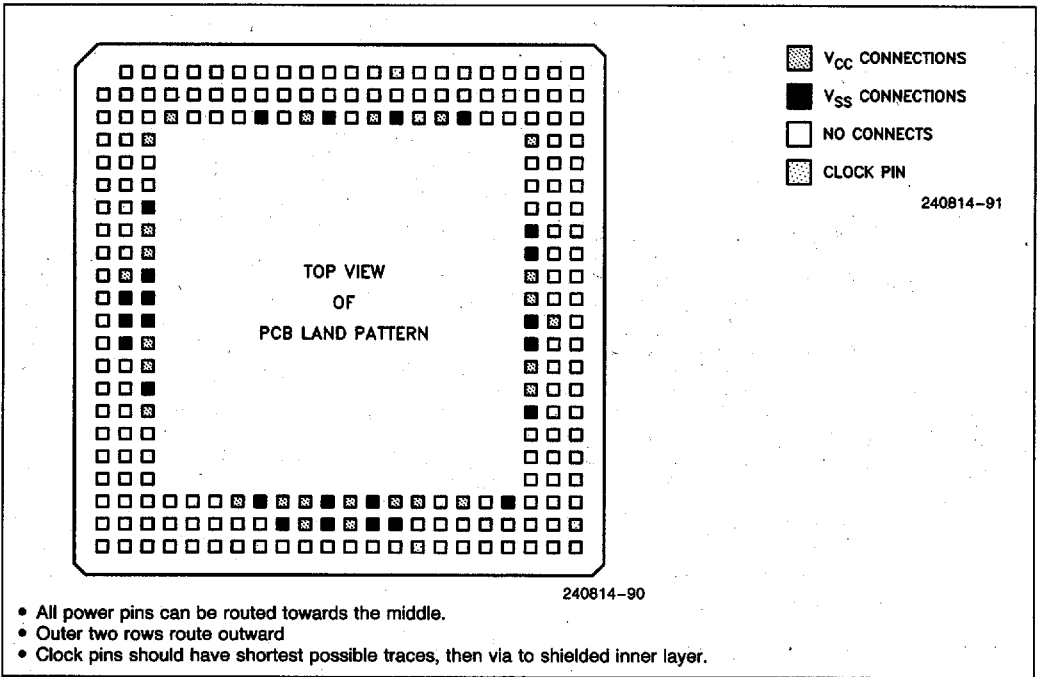


Figure 7.1c. Recommended Signal Routing for LGA Package

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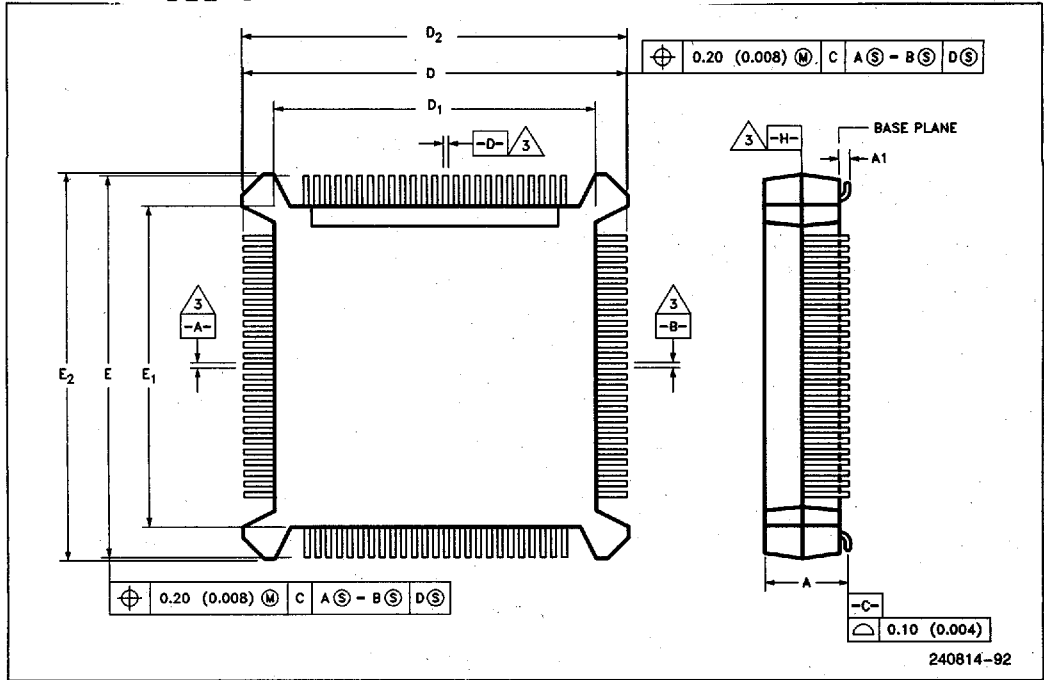


Figure 7.2a. Principle Dimensions of the 82360SL I/O in the 196-Lead PQFP Package

Family: 196-Lead Plastic Quad Flat Package (PQFP) 0.025 Inch (0.635mm) Pitch

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A = Package Height: Distance from seating plane to highest point of the body	4.06	4.32	0.160	0.180
A1 = Standoff: Distance from Seating Plane to Base Plane	0.51	0.76	0.020	0.040
D/E = Overall Package Dimension: Lead Tip to Lead Tip	37.47	37.72	1.470	1.490
D1/E1 = Plastic Body Dimension	34.21	34.37	1.347	1.353
D2/E2 = Bumper Distance	38.02	38.18	1.497	1.503
D3/E3 = Lead Dimension	30.48 Ref		1.200 Ref	
D4/E4 = Foot Radius Location	36.14	36.49	1.423	1.437
L1 = Foot Length	0.51	0.76	0.020	0.030

NOTES:

- All PQFP case outlines are being presented as standards to the JEDEC.
- Typical board footprint area for the 196-lead PQFP is 1.500 inches x 1.5000 inches.
- All dimensions and tolerance conform to ANSI Y14.5M-1982.
- Datum Plane -H- located at the molding parting line and coincident with the bottom of the lead where the lead exits the plastic body.
- Datums A-B and -D- to be determined where the center lead exits the plastic body at datum plane -H-.
- Controlling dimension in inches.
- Dimensions D1, D2, E1, and E2 are measured at the molding parting line and do not include mold protrusions.
- Pin 1 identifier is located within one of the two zones indicated.
- Measured at datum plane -H-.
- Measured at seating plane datum -C-.

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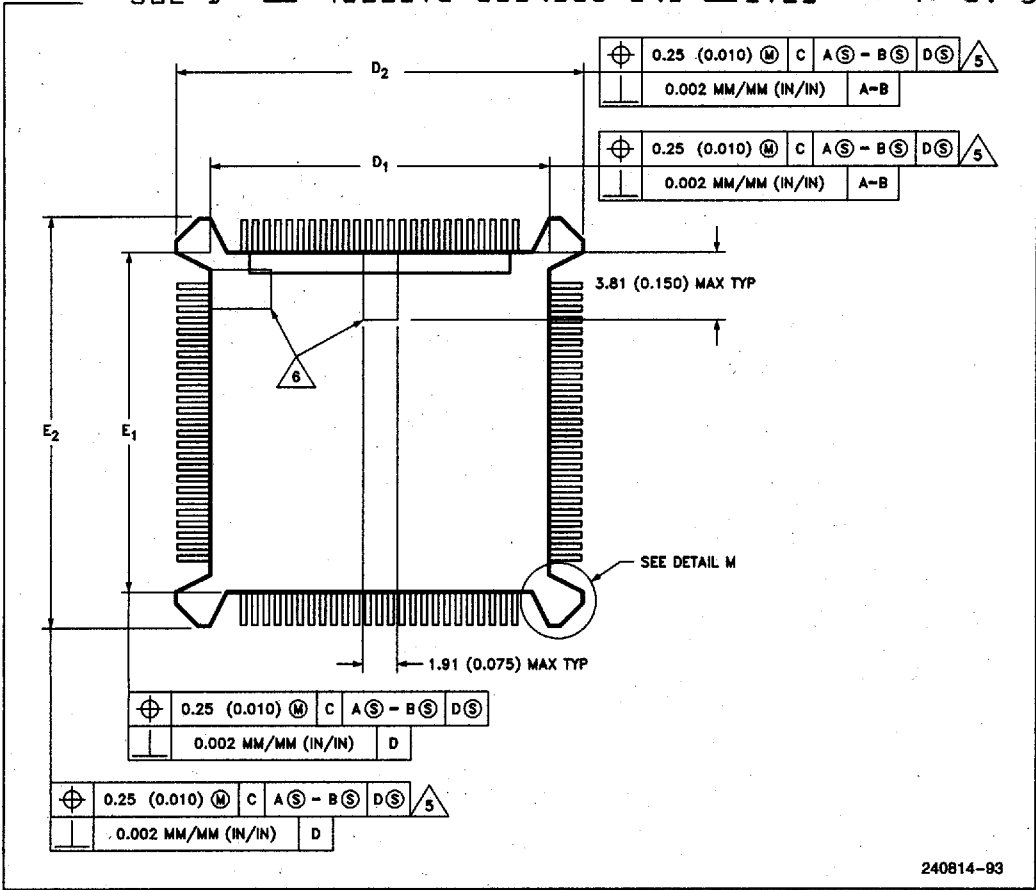


Figure 7.2b. Detailed Dimensions of the 82360SL I/O in the 196-Lead PQFP—Molded Details

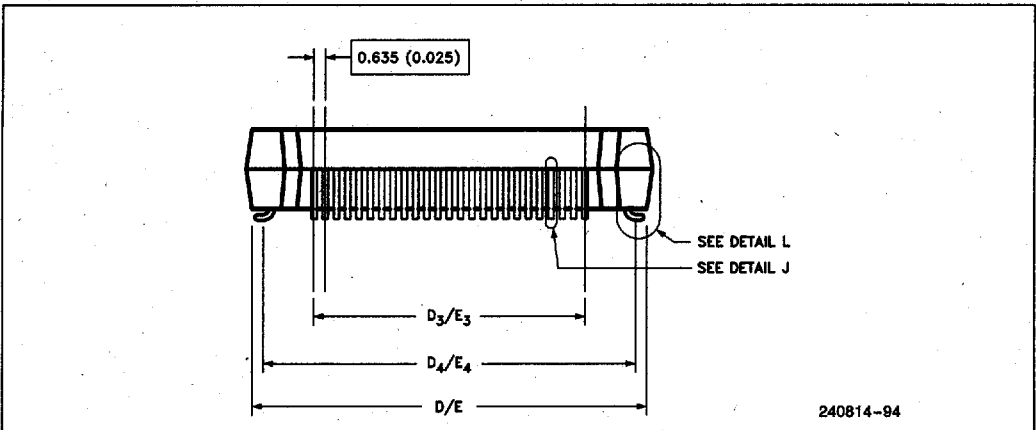
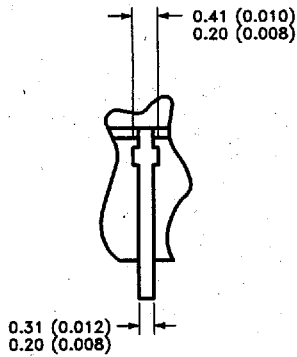


Figure 7.2c. Detailed Dimensions of the 82360SL I/O in the 196-Lead—Terminal Details

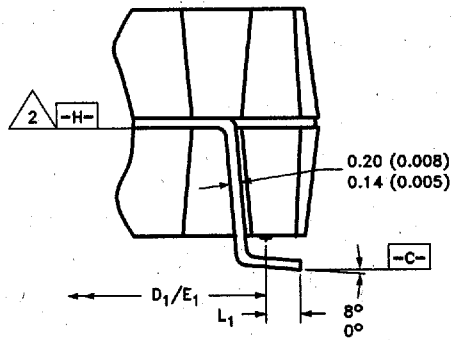
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\oplus	0.13 (0.005)	M	C	A(S) - B(S)	D(S)	7
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\oplus	0.20 (0.008)	M	C	A(S) - B(S)	D(S)	8
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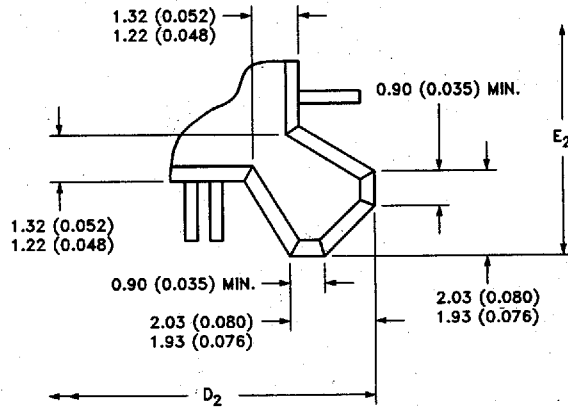
DETAIL J



DETAIL L

240814-95

Figure 7.2d. 196-Lead PQFP Mechanical Package Detail—Typical Lead



DETAIL M

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Figure 7.2e. 196-Lead PQFP Mechanical Package Detail—Protective Bumper

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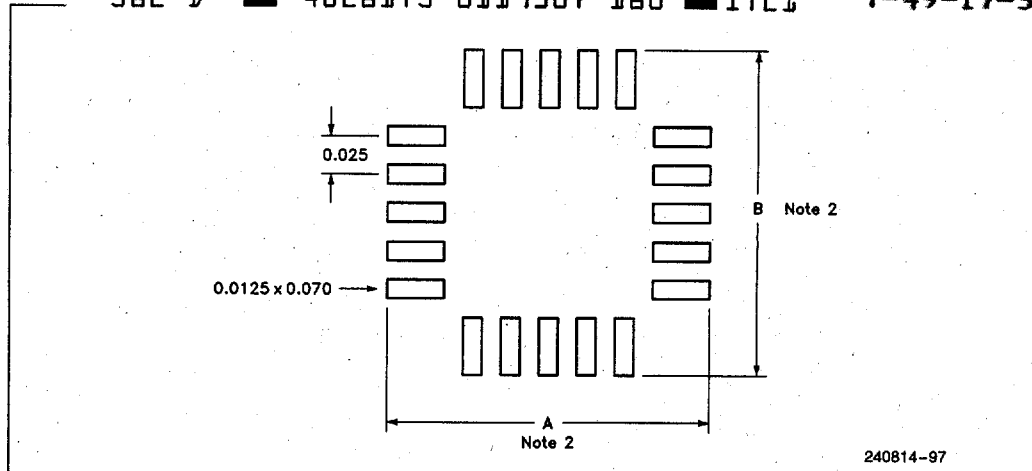


Figure 7.2f. Recommended PQFP Footprint

8.0 REVISION HISTORY

The First Release of the Advanced Information Intel386 SL Microprocessor Superset B Step Data book reflects information believed to be accurate as of July 1991.

This revision has included the specifications for the Intel386 SL CPU both in standard 5V mode and FlexibleVoltage Mode.

Following specification changes are made for the CPU in standard 5V mode:

1. C_{t225} max value is changed from "38 ns" to "44 ns".
2. The I_{OH} of IOCHRDY, IOCS16# and MEMCS16# is changed from "-2 mA" to "-1.6 mA" for $V_{OH} = 2.4V$.
3. The derating corners for C_{t409} in both 20 MHz and 25 MHz are changed from "SR, S" to "FR, F".

Following specifications are added to the CPU in standard 5V mode:

1. A.C. timing specifications at 16 MHz.
2. A.C. timing specifications for DRAM controller in F1 mode at 25 MHz.

Following specification changes are made for the CPU in Flexible Voltage mode:

1. C_{t227} min value is changed from "25 ns" to "0 ns".

Following specifications are added to the I/O:

1. Crystal and oscillator specifications.

Please Consult your Local Intel Field Sales Office for the most current design-in information.