SP8782A & B

1GHz 16/17, 32/33 Multi-Modulus Divider

March 2006

Features

- Advanced Resynchronisation techniques to negate loop delay effects
- CMOS compatible output capability
- Multi-Modulus division
- Available as DESC SMD 5962-9208901MPA

Ordering Information

SP8782/B/MP	8 Pin SOP/SOIC	Tubes
SP8782/A/DG	8 Pin CERDIP	Tubes
SP8782/B/MPTC	8 Pin SOP/SOIC	Tape & Reel
SP8782/B/MP2Q	8 Pin SOP/SOIC**	Tape & Reel

**Pb Free Tin/Silver/Copper

Description

The SP8782 is a multi-modulus divider which divides by 16/17 when the Ratio Select input is low and by 32/33 when theRatio Select input is high. When high, the modulus Control input selects the lower division ratio (16 or 32) and the higher ratio (17 or 33) when it is low.

The device uses resynchronisation techniques to reduce the effects of propagation delays in frequency synthesis.

The SP8782A (ceramic DIL package) is characterised over the full military temperature range of -55 C to +125 C, the SP8782B (miniature plastic DIL package) over the industrial range of -40 C to+85 C.

Absolute Maximum Ratings

Supply Voltage	6V
Clock input level	2.5V p-p
Junction temperature	+175 C
Storage temperature range:	
SP8782A	-55 C to +150 C
SP8782B	-55 C to +125 C

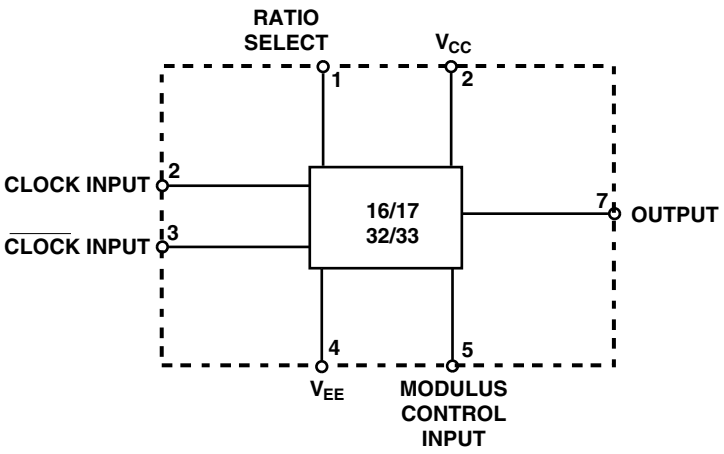


Figure 1 Functional Diagram

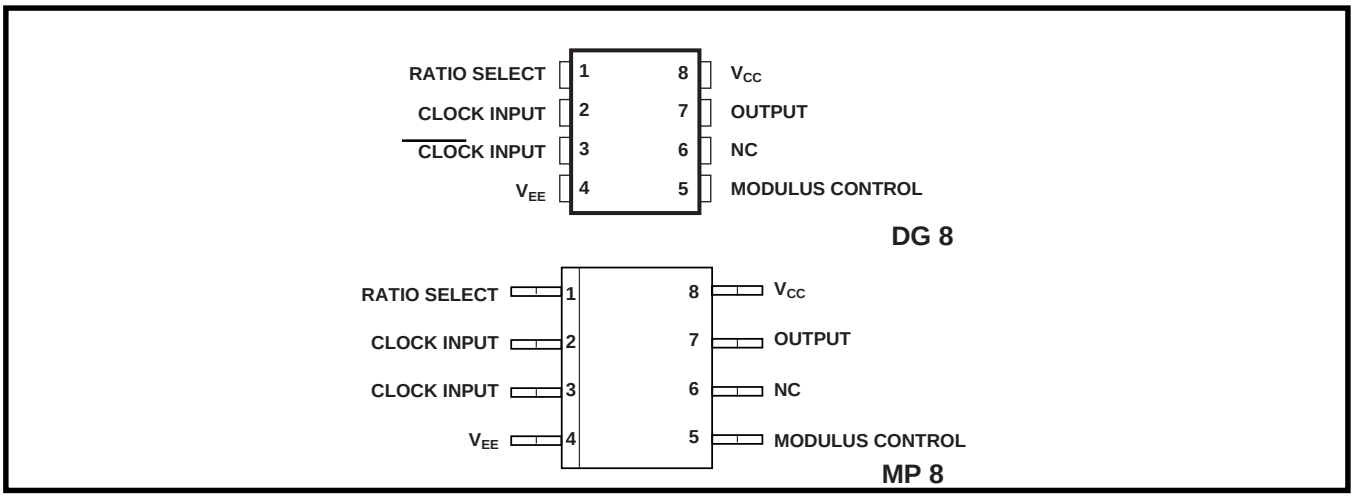


Figure 2 Typical Pin Connections

Electrical Characteristics

Unless otherwise stated, the Electrical Characteristics are guaranteed over the specified supply, frequency and temperature range.

Supply Voltage, V_{CC} = +4V to +5.5V, V_{EE} = 0V

Temperature T_{amb}= -55°C to +125°C, (SP8782A), -40°C to +85° C (SP8782B)

Characteristic	Pin	Value		Units	Conditions
		Min	Max		
Maximum frequency (sinewave input)	2, 3	1		GHz	Input = 200-1200mVp-p
Minimum frequency	2, 3		50	MHz	Input = 400-1200mVp-p
Min Slew rate for low frequency operation	2, 3		100	V/µs	
Power Supply current, I_{CC}	8		60	mA	Output unloaded, V_{CC}=5.5V
Output low voltage	7	0	1.7	V	
Output high voltage	7	V_{CC}-1.4	V_{CC}	V	
Modulus control input high voltage	5	$0.7V_{CC}$	V_{CC}	V	At driver end of 3kΩ resistor
Modulus control input low voltage	5	0	$0.3V_{CC}$	V	At driver end of 3kΩ resistor
Modulus control input high current	5	0.6	1.2	mA	Via 3kΩ resistor to V_{CC}
Modulus control input low current	5	-0.6	-1.2	mA	Via 3kΩ resistor to V_{CC}
Ratio select input high voltage	1	$0.6V_{CC}$	V_{CC}	V	
Ratio selected input low voltage	1	0	$0.4V_{CC}$	V	
Ratio select input current	1	-10	10	µA	
Clock to output propagation Delay	2,3,7		3	ns	
Set-up time, t_s	5,7	3		ns	See note 1 and Fig. 3a
Release time,t_r	5,7	3		ns	See note 2 and Fig. 3b

Notes: 1. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of the modulus control input and the next L→H output transition to ensure that the ÷ 16 (32) mode is obtained.

2. The release time t_r is defined as the minimum time that can elapse between H→L transition of the modulus control input and the next L→H output transition to ensure that the ÷ 17 (33) mode is obtained.

Modulus control input	Ratio select input	
	0	1
0	÷17	÷33
1	÷16	÷32

Table 1 Truth table for control inputs

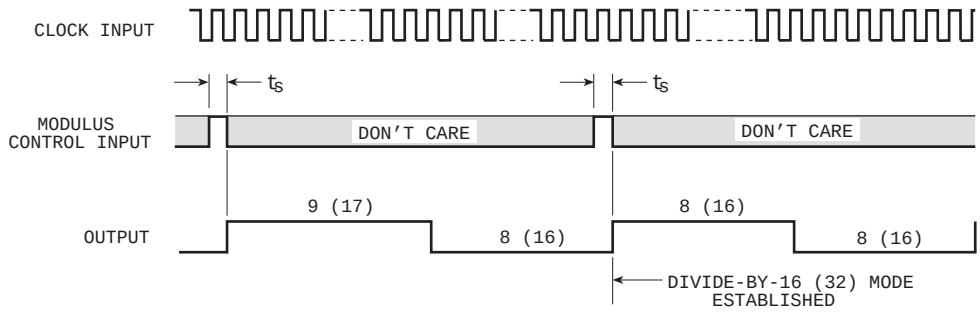


Figure 3a Setting divide - by - 16 (32 mode)

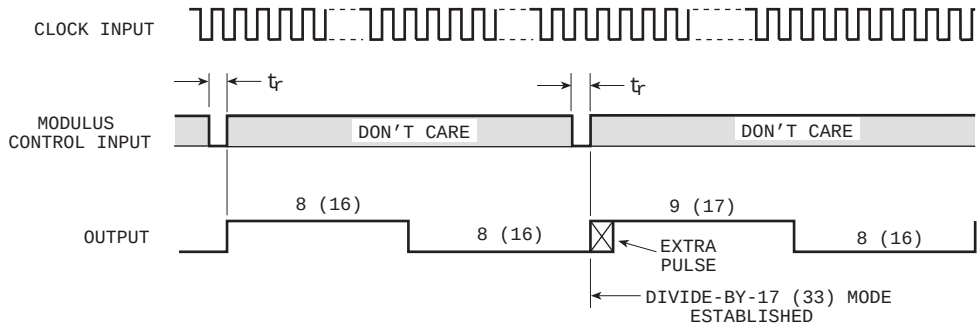
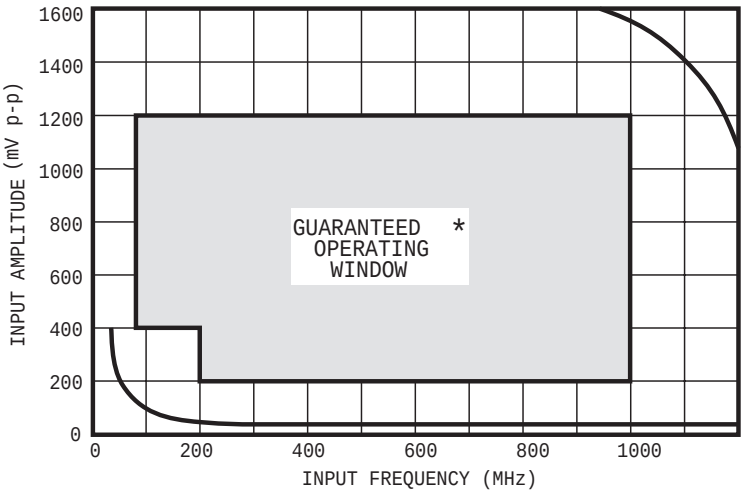


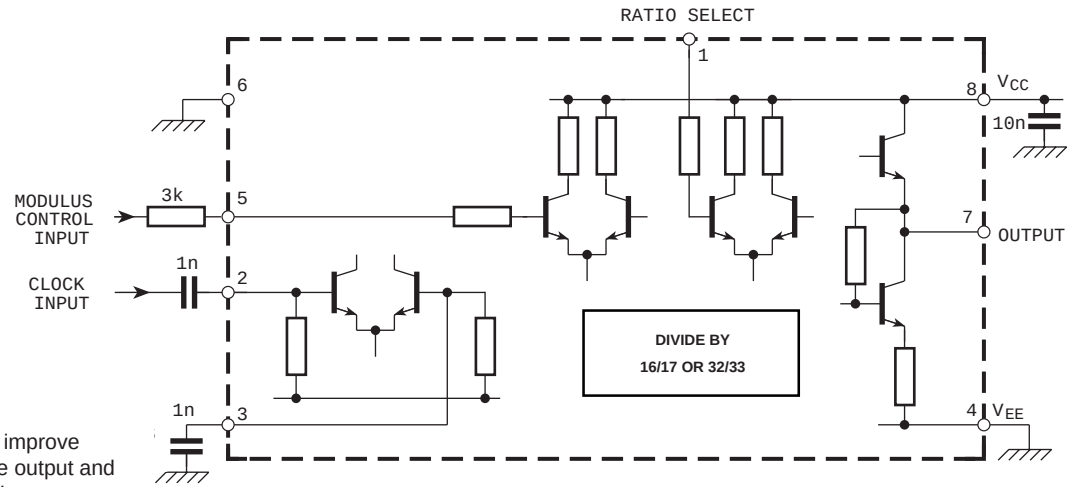
Figure 3b Setting divide - by - 17 (33 mode)

Figure 3 Timing diagrams



*** Tested as specified in table of Electrical Characteristics**

Figure 4 Typical input characteristics



NOTES

1. Pin 6 is grounded to improve isolation between the output and the modulus control input
2. The 3kΩ resistor on pin 5 reduces the amplitude of the modulus control signal to minimise radiation

Figure 5 Typical application showing interfacing

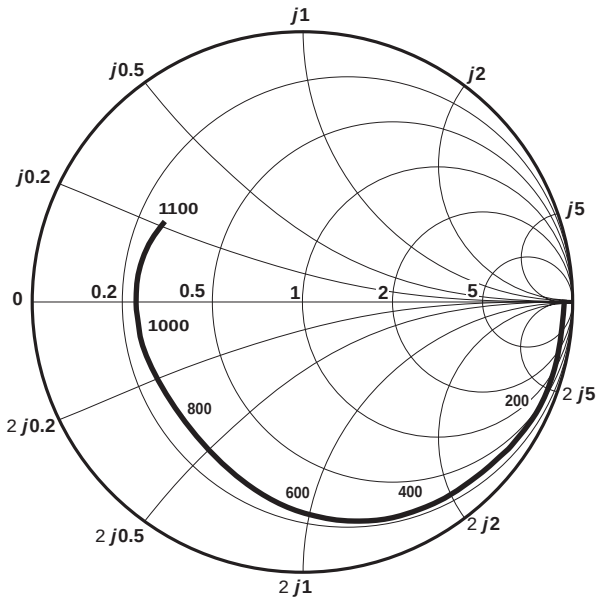
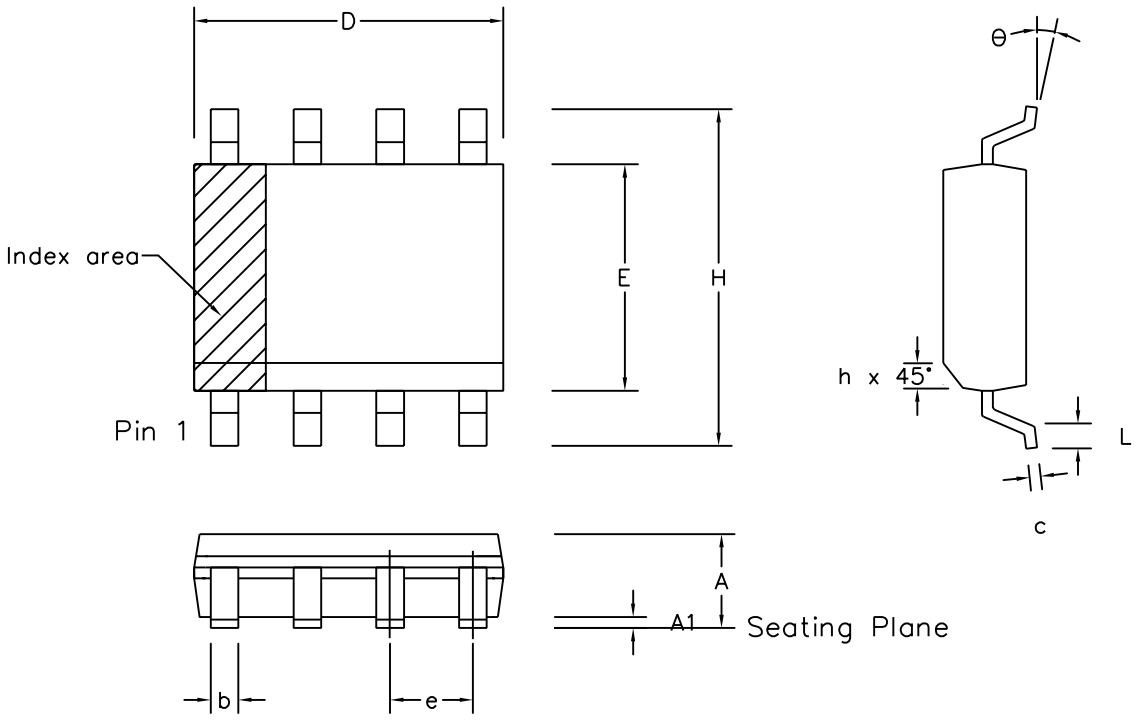


Figure 6 Typical input impedance. Test conditions: supply voltage =5V, ambient temperature =25°C, frequencies in MHz, impedances normalised to 50Ω



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

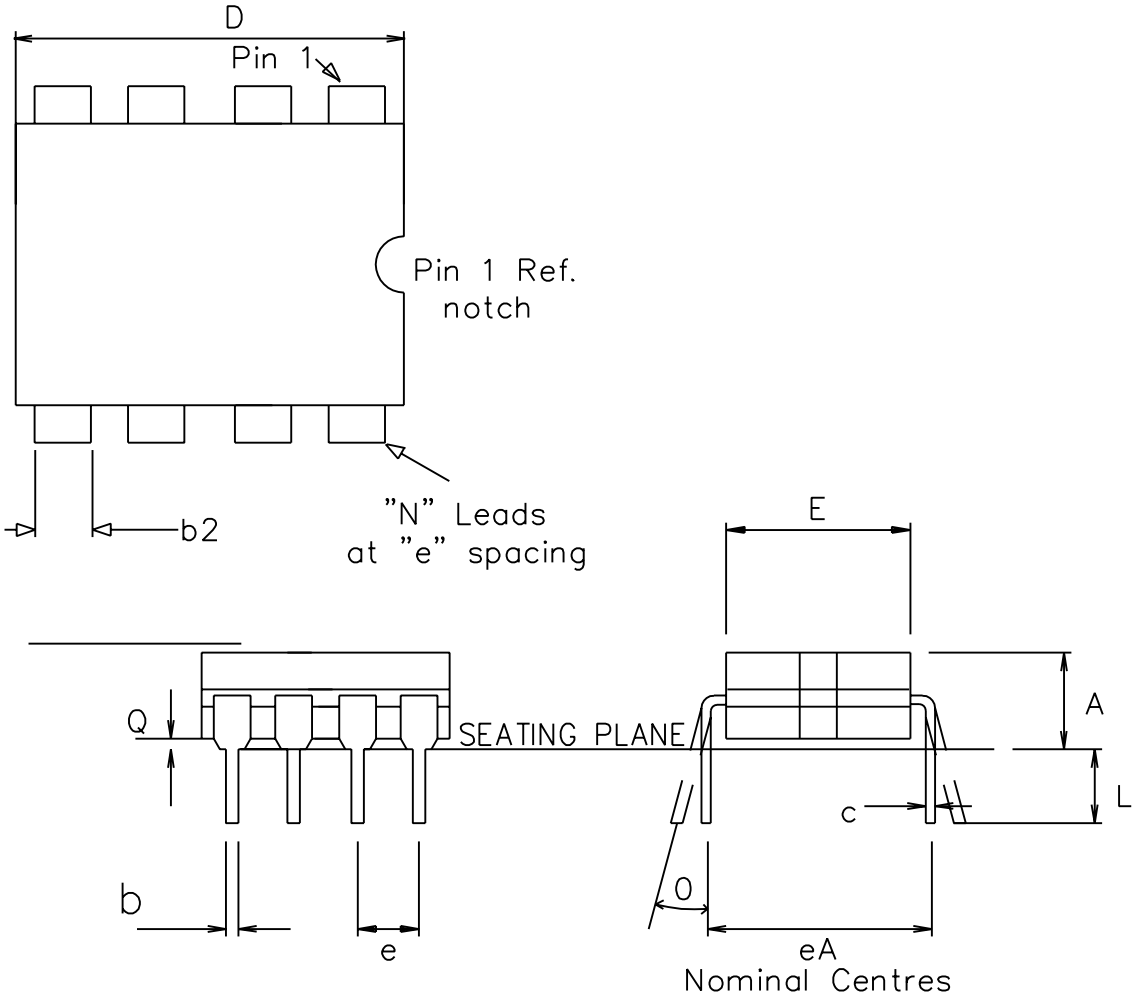
Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

GPD00010



Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
L	3.18		4.06		0.125		0.160
A			5.08				0.200
Q	0.51				0.020		
E	5.59		7.87		0.220		0.310
eA		7.62				0.300	
c	0.20		0.36		0.008		0.014
D			10.29				0.405
e	2.54 BSC.				0.100 BSC.		
b2	1.14		1.65		0.045		0.065
b	0.36		0.58		0.014		0.023
0			15°				15°
	Pin features						
N	8						
ND	4						
NE	0						
NOTE	RECTANGULAR						

This drawing supersedes 418/ED/39501/001 (Swindon)

ISSUE	1	2		
ACN	201728	212450		
DATE	20Nov96	26Mar02		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

DG / C

Package Code DH

Package Outline for 8 lead DIL (Glass Seal Ceramic)

GPD00270

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