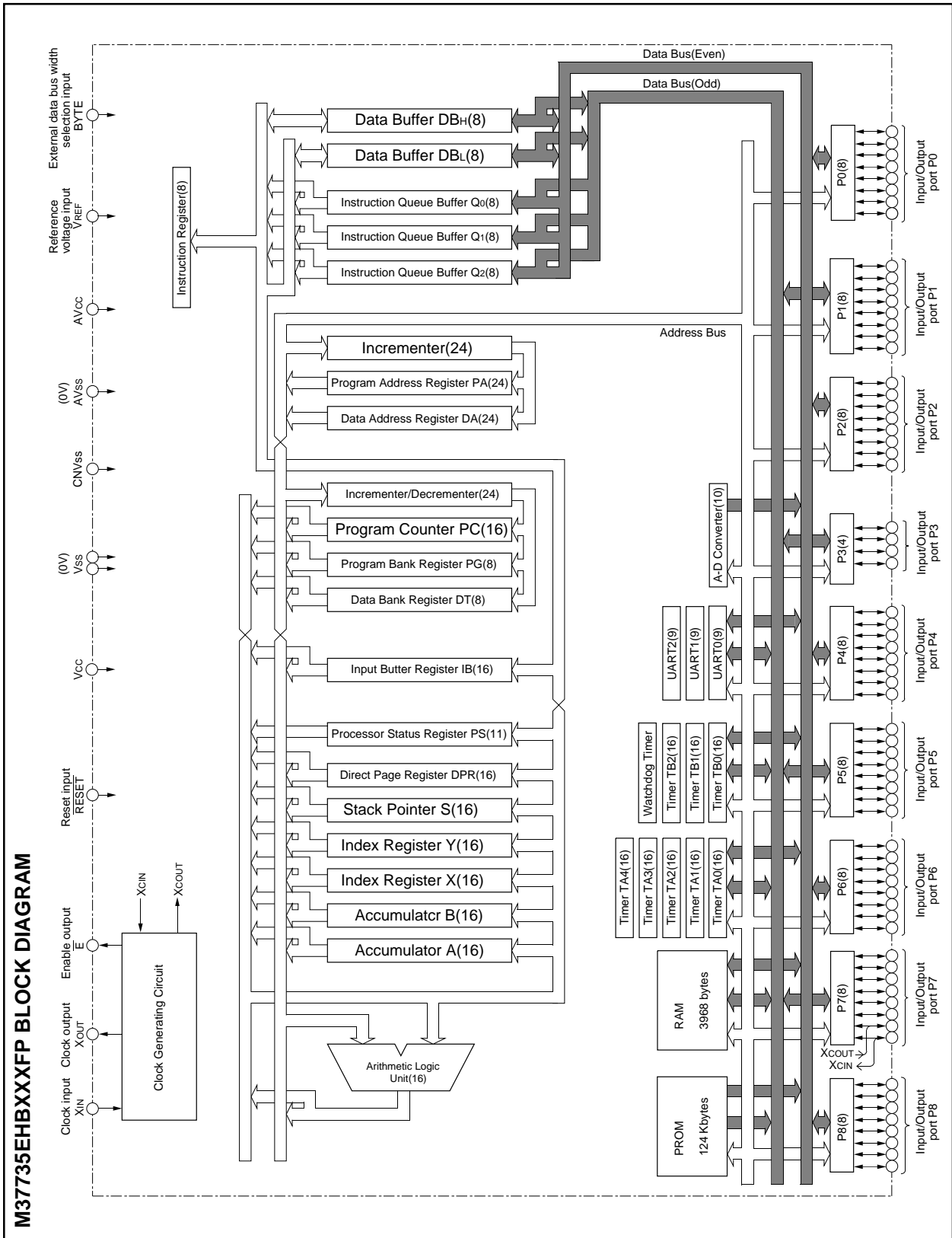




**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**M37735EBXXXXFP**  
**M37735EBBFS**

PROM VERSION OF M37735MHBXXXXFP



**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**FUNCTIONS OF M37735EHBXXXFP**

| Parameter                    |                         | Functions  |
|------------------------------|-------------------------|--|
| Number of basic instructions |                         | 103  |
| Instruction execution time   |                         | 160 ns (the fastest instruction at external clock 25 MHz frequency)                              |
| Memory size                  | PROM                    | 124 Kbytes   |
|                              | RAM                     | 3968 bytes   |
| Input/Output ports           | P0 – P2, P4 – P8        | 8-bit X 8  |
|                              | P3                      | 4-bit X 1  |
| Multi-function timers        | TA0, TA1, TA2, TA3, TA4 | 16-bit X 5   |
|                              | TB0, TB1, TB2           | 16-bit X 3   |
| Serial I/O                   |                         | (UART or clock synchronous serial I/O) X 3   |
| A-D converter                |                         | 10-bit X 1 (8 channels)  |
| Watchdog timer               |                         | 12-bit X 1   |
| Interrupts                   |                         | 3 external types, 16 internal types<br>Each interrupt can be set to the priority level (0 – 7.)  |
| Clock generating circuit     |                         | 2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator) |
| Supply voltage               |                         | 5 V ± 10%  |
| Power dissipation            |                         | 47.5 mW (at external clock 25 MHz frequency)   |
| Input/Output characteristic  | Input/Output voltage    | 5 V  |
|                              | Output current          | 5 mA   |
| Memory expansion             |                         | Maximum 1 Mbytes   |
| Operating temperature range  |                         | –20 to 85 °C   |
| Device structure             |                         | CMOS high-performance silicon gate process   |
| Package                      | M37735EHBXXXFP          | 80-pin plastic molded QFP (80P6N-A)  |
|                              | M37735EHBFS             | 80-pin ceramic LCC (with a window) (80D0)  |

**PIN DESCRIPTION**

| Pin                       | Name                                    | Input/Output | Functions  |
|---------------------------|---|--------------|--|
| Vcc, Vss                  | Power source                            |              | Apply 5 V ± 10% to Vcc and 0 V to Vss.   |
| CNVss                     | CNVss input                             | Input        | This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.   |
| $\overline{\text{RESET}}$ | Reset input                             | Input        | When "L" level is applied to this pin, the microcomputer enters the reset state.   |
| XIN                       | Clock input                             | Input        | These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.   |
| XOUT                      | Clock output                            | Output       |  |
| $\overline{\text{E}}$     | Enable output                           | Output       | This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the memory expansion mode or the microprocessor mode, this pin functions as the RDE signal output pin.  |
| BYTE                      | External data bus width selection input | Input        | In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.   |
| AVcc, AVss                | Analog power source input               |              | Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.  |
| VREF                      | Reference voltage input                 | Input        | This is reference voltage input pin for the A-D converter.   |
| P00 – P07                 | I/O port P0                             | I/O          | In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset.<br>In the memory expansion mode or the microprocessor mode, these pins output $\overline{\text{CS}}_0 - \overline{\text{CS}}_4$ , $\overline{\text{RSM}}\overline{\text{P}}$ signals, and address (A16, A17).                                     |
| P10 – P17                 | I/O port P1                             | I/O          | In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.  |
| P20 – P27                 | I/O port P2                             | I/O          | In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address (A0 – A7) is output.   |
| P30 – P33                 | I/O port P3                             | I/O          | In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, $\overline{\text{WEL}}$ , $\overline{\text{WEH}}$ , $\overline{\text{ALE}}$ , and $\overline{\text{HLDA}}$ signals are output.   |
| P40 – P47                 | I/O port P4                             | I/O          | In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41, and P42 become $\overline{\text{HOLD}}$ and $\overline{\text{RDY}}$ input pins, and a clock $\phi_1$ output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 can be selected as an I/O port.                                  |
| P50 – P57                 | I/O port P5                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ( $\overline{\text{KI}}_0 - \overline{\text{KI}}_3$ ).  |
| P60 – P67                 | I/O port P6                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ( $\overline{\text{INT}}_0 - \overline{\text{INT}}_2$ ) and input pins for timers B0 to B2. P67 also functions as a sub-clock $\phi_{\text{SUB}}$ output pin.  |
| P70 – P77                 | I/O port P7                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. P72 to P75 also function as I/O pins for UART2. Additionally, P76 and P77 have the function as the output pin (XcOUT) and the input pin (XcIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the XcOUT and XcIN pins, connect a resonator or an oscillator between the both. |
| P80 – P87                 | I/O port P8                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.   |

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**PIN DESCRIPTION (EPROM MODE)**

| Pin        | Name                     | Input/Output | Functions  |
|------------|--------------------------|--------------|--|
| VCC, VSS   | Power supply             |              | Supply 5V±10% to VCC and 0V to VSS.  |
| CNVSS      | VPP input                | Input        | Connect to VPP when programming or verifying.  |
| BYTE       | VPP input                | Input        | Connect to VPP when programming or verifying.  |
| RESET      | Reset input              | Input        | Connect to VSS.  |
| XIN        | Clock input              | Input        | Connect a ceramic resonator between XIN and XOUT.  |
| XOUT       | Clock output             | Output       |  |
| $\bar{E}$  | Enable output            | Output       | Keep open.   |
| AVCC, AVSS | Analog supply input      |              | Connect AVCC to VCC and AVSS to VSS.   |
| VREF       | Reference voltage input  | Input        | Connect to VSS.  |
| P00 – P07  | Address input (A0 – A7)  | Input        | Port P0 functions as the lower 8 bits address input (A0 – A7).   |
| P10 – P17  | Address input (A8 – A15) | Input        | Port P1 functions as the higher 8 bits address input (A8 – A15).   |
| P20 – P27  | Data I/O (D0 – D7)       | I/O          | Port P2 functions as the 8 bits data bus(D0 – D7).   |
| P30        | Address input (A16)      | Input        | P30 functions as the most significant bit address input (A16).   |
| P31 – P33  | Input port P3            | Input        | Connect to VSS.  |
| P40 – P47  | Input port P4            | Input        | Connect to VSS.  |
| P50 – P57  | Control signal input     | Input        | P50, P51 and P52 function as PGM, OE and CE input pins respectively. Connect P53, P54, P55 and P56 to VCC. Connect P57 to VSS. |
| P60 – P67  | Input port P6            | Input        | Connect to VSS.  |
| P70 – P77  | Input port P7            | Input        | Connect to VSS.  |
| P80 – P87  | Input port P8            | Input        | Connect to VSS.  |

**BASIC FUNCTION BLOCKS**

The M37735EBXXXXFP has the same functions as the M37735MHBXXXXFP except for the following:

- (1) The built-in ROM is PROM.
- (2) The status of bit 3 of the oscillation circuit control register 1 (address 6F16) at a reset is different.
- (3) The usage condition of bit 3 of the oscillation circuit control register 1 is different.
- (4) Part of the processor mode selection method is different.

Accordingly, refer to the basic function blocks description in the M37735MHBXXXXFP except for Figure 1 (bit configuration of oscillation circuit control register 1), Figure 3 (microcomputer internal status during reset), and Table 1 (microprocessor mode selection method).

In the M37735EBXXXXFP, bit 3 of the oscillation circuit control register 1 must be "0". (Refer to Figure 1.) Bit 3 is "1" at a reset. Accordingly,

write "0" to bit 3 in the single-chip mode after reset.

Figure 2 shows how to write data in oscillation circuit control register 1.

In the M37735EBXXXXFP, the microprocessor mode cannot be selected by connecting the CNVss pin to Vcc. Connect the CNVss pin to Vss and start the microcomputer's operating from the single-chip mode.

Table 1. Relationship between CNVss pin input level and processor modes

| CNVss | Mode  | Description  |
|-------|---|--|
| Vss   | <ul style="list-style-type: none"> <li>· Single-chip</li> <li>· Memory expansion</li> <li>· Microprocessor</li> </ul> | Single-chip mode upon starting after reset. Each mode can be selected by changing the processor mode bits by software. |

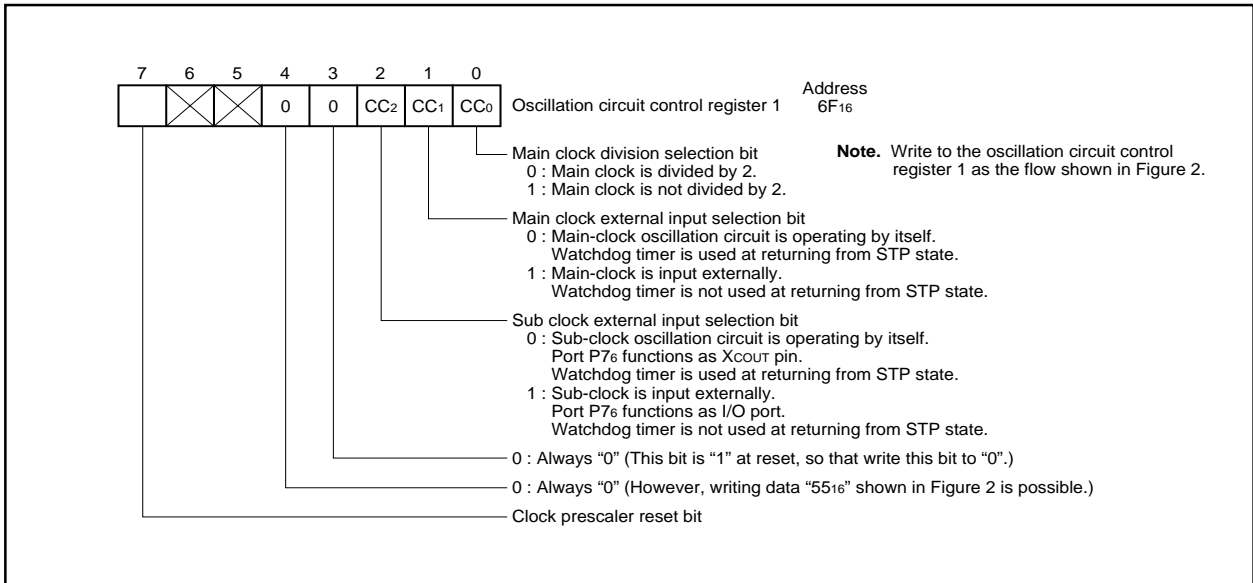


Fig. 1 Bit configuration of oscillation circuit control register 1 (corresponding to Figure 63 in data sheet "M37735MHBXXXXFP")

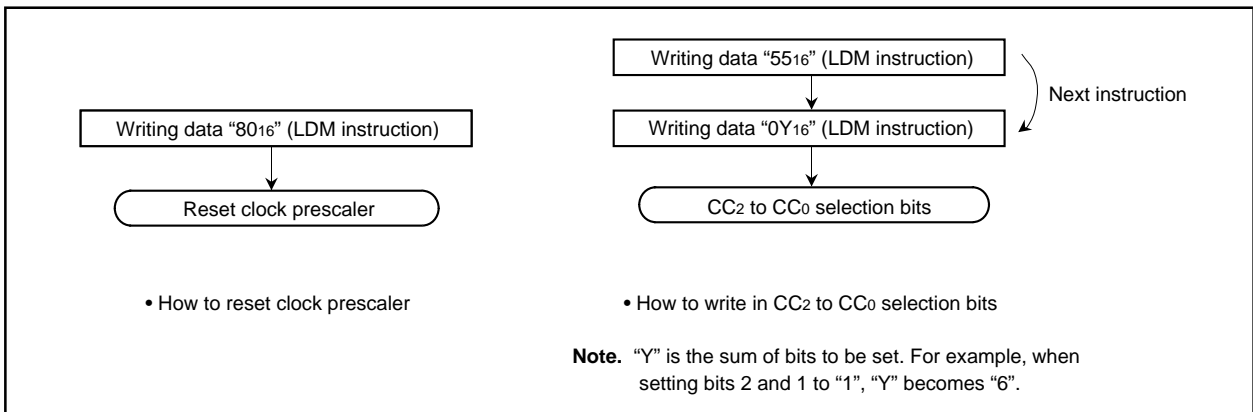


Fig. 2 How to write data in oscillation circuit control register 1 (identical with Figure 64 in data sheet "M37735MHBXXXXFP")

**PRELIMINARY**  
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|  | Address                |                   | Address  |                        |                               |
|--|------------------------|-------------------|--|------------------------|-------------------------------|
| Port P0 direction register                 | (04 <sub>16</sub> )... | 00 <sub>16</sub>  | Watchdog timer frequency selection flag                | (61 <sub>16</sub> )... | XXXXXXXXXX0                   |
| Port P1 direction register                 | (05 <sub>16</sub> )... | 00 <sub>16</sub>  | Memory allocation control register                     | (63 <sub>16</sub> )... | XXXXXXXX00000                 |
| Port P2 direction register                 | (08 <sub>16</sub> )... | 00 <sub>16</sub>  | UART2 transmit/receive mode register                   | (64 <sub>16</sub> )... | X0000000                      |
| Port P3 direction register                 | (09 <sub>16</sub> )... | XXXXX000          | UART2 transmit/receive control register 0              | (68 <sub>16</sub> )... | XXXXX1000                     |
| Port P4 direction register                 | (0C <sub>16</sub> )... | 00 <sub>16</sub>  | UART2 transmit/receive control register 1              | (69 <sub>16</sub> )... | 00000010                      |
| Port P5 direction register                 | (0D <sub>16</sub> )... | 00 <sub>16</sub>  | Oscillation circuit control register 0                 | (6C <sub>16</sub> )... | X00000X1                      |
| Port P6 direction register                 | (10 <sub>16</sub> )... | 00 <sub>16</sub>  | Port function control register                         | (6D <sub>16</sub> )... | 00 <sub>16</sub>              |
| Port P7 direction register                 | (11 <sub>16</sub> )... | 00 <sub>16</sub>  | Serial transmit control register                       | (6E <sub>16</sub> )... | XXXX00XXXX                    |
| Port P8 direction register                 | (14 <sub>16</sub> )... | 00 <sub>16</sub>  | Oscillation circuit control register 1                 | (6F <sub>16</sub> )... | 0XXXX01000                    |
| A-D control register 0                     | (1E <sub>16</sub> )... | 00000???          | A-D/UART2 trans./rece. interrupt control register      | (70 <sub>16</sub> )... | XXXXX0000                     |
| A-D control register 1                     | (1F <sub>16</sub> )... | XXXX00011         | UART 0 transmission interrupt control register         | (71 <sub>16</sub> )... | XXXXX0000                     |
| UART 0 transmit/receive mode register      | (30 <sub>16</sub> )... | 00 <sub>16</sub>  | UART 0 receive interrupt control register              | (72 <sub>16</sub> )... | XXXXX0000                     |
| UART 1 transmit/receive mode register      | (38 <sub>16</sub> )... | 00 <sub>16</sub>  | UART 1 transmission interrupt control register         | (73 <sub>16</sub> )... | XXXXX0000                     |
| UART 0 transmit/receive control register 0 | (34 <sub>16</sub> )... | 00001000          | UART 1 receive interrupt control register              | (74 <sub>16</sub> )... | XXXXX0000                     |
| UART 1 transmit/receive control register 0 | (3C <sub>16</sub> )... | 00001000          | Timer A0 interrupt control register                    | (75 <sub>16</sub> )... | XXXXX0000                     |
| UART 0 transmit/receive control register 1 | (35 <sub>16</sub> )... | 00000010          | Timer A1 interrupt control register                    | (76 <sub>16</sub> )... | XXXXX0000                     |
| UART 1 transmit/receive control register 1 | (3D <sub>16</sub> )... | 00000010          | Timer A2 interrupt control register                    | (77 <sub>16</sub> )... | XXXXX0000                     |
| Count start flag                           | (40 <sub>16</sub> )... | 00 <sub>16</sub>  | Timer A3 interrupt control register                    | (78 <sub>16</sub> )... | XXXXX0000                     |
| One-shot start flag                        | (42 <sub>16</sub> )... | XXXX0000          | Timer A4 interrupt control register                    | (79 <sub>16</sub> )... | XXXXX0000                     |
| Up-down flag                               | (44 <sub>16</sub> )... | 00 <sub>16</sub>  | Timer B0 interrupt control register                    | (7A <sub>16</sub> )... | XXXXX0000                     |
| Timer A0 mode register                     | (56 <sub>16</sub> )... | 00 <sub>16</sub>  | Timer B1 interrupt control register                    | (7B <sub>16</sub> )... | XXXXX0000                     |
| Timer A1 mode register                     | (57 <sub>16</sub> )... | 00 <sub>16</sub>  | Timer B2 interrupt control register                    | (7C <sub>16</sub> )... | XXXXX0000                     |
| Timer A2 mode register                     | (58 <sub>16</sub> )... | 00 <sub>16</sub>  | INT <sub>0</sub> interrupt control register            | (7D <sub>16</sub> )... | XXXX000000                    |
| Timer A3 mode register                     | (59 <sub>16</sub> )... | 00 <sub>16</sub>  | INT <sub>1</sub> interrupt control register            | (7E <sub>16</sub> )... | XXXX000000                    |
| Timer A4 mode register                     | (5A <sub>16</sub> )... | 00 <sub>16</sub>  | INT <sub>2</sub> /Key input interrupt control register | (7F <sub>16</sub> )... | XXXX000000                    |
| Timer B0 mode register                     | (5B <sub>16</sub> )... | 00100000          | Processor status register (PS)                         |                        | 000??0001??                   |
| Timer B1 mode register                     | (5C <sub>16</sub> )... | 001XXXX000        | Program bank register (PG)                             |                        | 00 <sub>16</sub>              |
| Timer B2 mode register                     | (5D <sub>16</sub> )... | 001XXXX000        | Program counter (PC <sub>H</sub> )                     |                        | Content of FFFF <sub>16</sub> |
| Processor mode register 0                  | (5E <sub>16</sub> )... | 00 <sub>16</sub>  | Program counter (PC <sub>L</sub> )                     |                        | Content of FFFE <sub>16</sub> |
| Processor mode register 1                  | (5F <sub>16</sub> )... | XXXXXXXXX0        | Direct page register (DPR)                             |                        | 0000 <sub>16</sub>            |
| Watchdog timer register                    | (60 <sub>16</sub> )... | FFF <sub>16</sub> | Data bank register (DT)                                |                        | 00 <sub>16</sub>              |

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 3 Microcomputer internal status during reset

**PRELIMINARY**  
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**EPROM MODE**

The M37735EHBXXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 2 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, P30, P50, P51, P52, CNVss, and BYTE are used for the EPROM (equivalent to the

M5M27C101K).

When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 01000<sub>16</sub> – 1FFFF<sub>16</sub>.

Connect the clock which is either ceramic resonator or external clock to XIN pin and XOUT pin.

Table 2 Pin function in EPROM mode

|               | M37735EHBXXXFP    | M5M27C101K |
|---------------|-------------------|------------|
| VCC           | VCC               | VCC        |
| VPP           | CNVss, BYTE       | VPP        |
| VSS           | VSS               | VSS        |
| Address input | Ports P0, P1, P30 | A0 – A16   |
| Data I/O      | Port P2           | D0 – D7    |
| CE            | P52               | CE         |
| OE            | P51               | OE         |
| PGM           | P50               | PGM        |



**PRELIMINARY**  
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**M37735EHBXXXFP**  
**M37735EHBFS**

PROM VERSION OF M37735MHBXXXFP

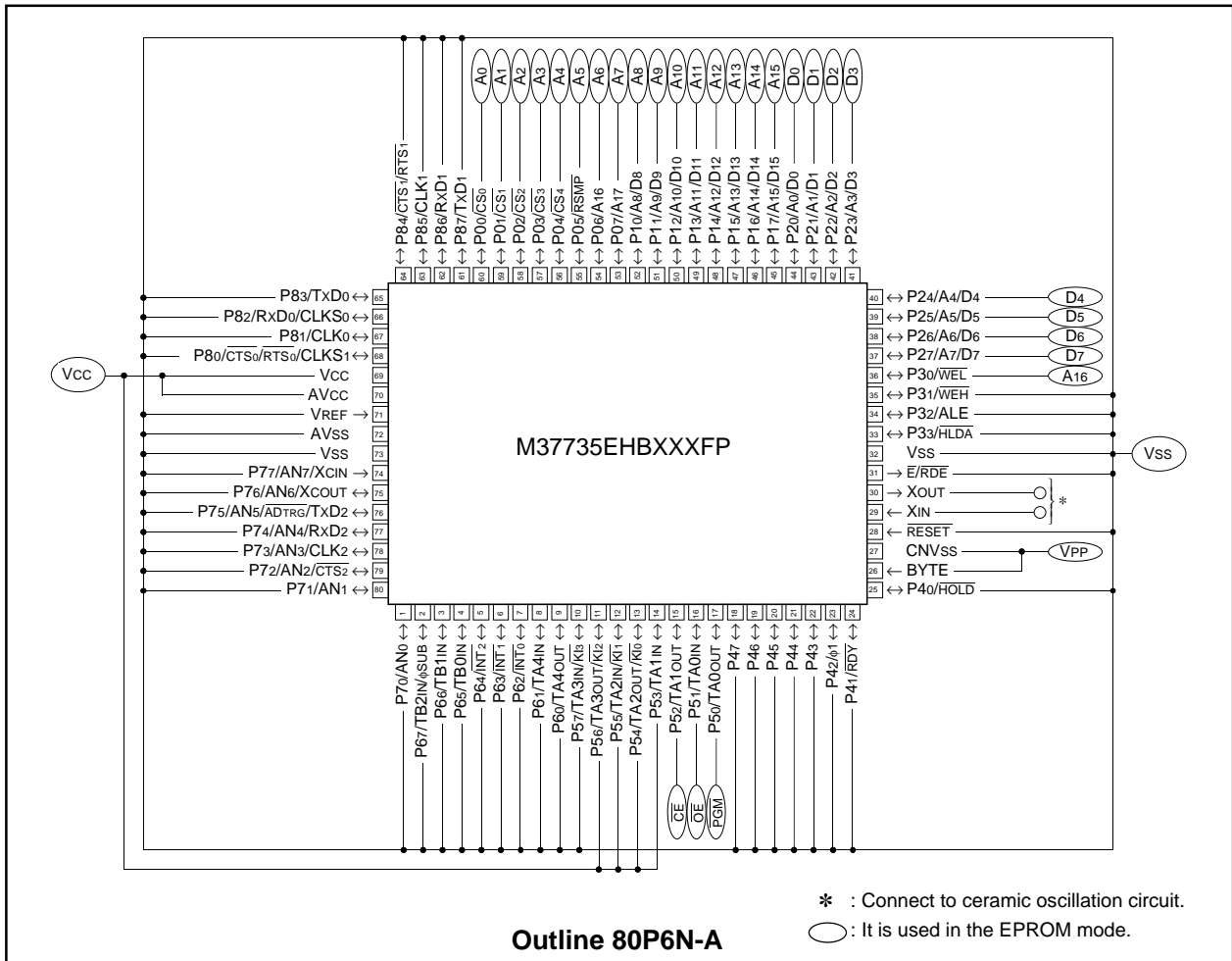


Fig. 4 Pin connection in EPROM mode

**FUNCTION IN EPROM MODE**  
**1M mode (equivalent to the M5M27C101K)**

**Reading**

To read the EPROM, set the  $\overline{CE}$  and  $\overline{OE}$  pins to a "L" level. Input the address of the data (A0 – A16) to be read, and the data will be output to the I/O pins D0 – D7. The data I/O pins will be floating when either the  $\overline{CE}$  or  $\overline{OE}$  pins are in the "H" state.

**Programming**

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the  $\overline{CE}$  pin to a "L" level and the  $\overline{OE}$  pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the VPP pin. The address to be programmed to is selected with pins A0 – A16, and the data to be programmed is input to pins D0 – D7. Set the  $\overline{PGM}$  pin to a "L" level to being programming.

**Erasing**

To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15 J/cm<sup>2</sup>.

**Programming operation**

To program the M37735EHBXXXFP, first set VCC = 6 V, VPP = 12.5 V, and set the address to 0100016. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 X X ms).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with VCC = VPP = 5 V (or VCC = VPP = 5.5 V).

Table 2. I/O signal in each mode

| Mode               | Pin             |                 |                  |        |     |          |
|--------------------|-----------------|-----------------|------------------|--------|-----|----------|
|                    | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | VPP    | VCC | Data I/O |
| Read-out           | VIL             | VIL             | X                | 5 V    | 5 V | Output   |
| Output             | VIL             | VIH             | X                | 5 V    | 5 V | Floating |
| Disable            | VIH             | X               | X                | 5 V    | 5 V | Floating |
| Programming        | VIL             | VIH             | VIL              | 12.5 V | 6 V | Input    |
| Programming Verify | VIL             | VIL             | VIH              | 12.5 V | 6 V | Output   |
| Program Disable    | VIH             | VIH             | VIH              | 12.5 V | 6 V | Floating |

**Note 1** : An X indicates either VIL or VIH.

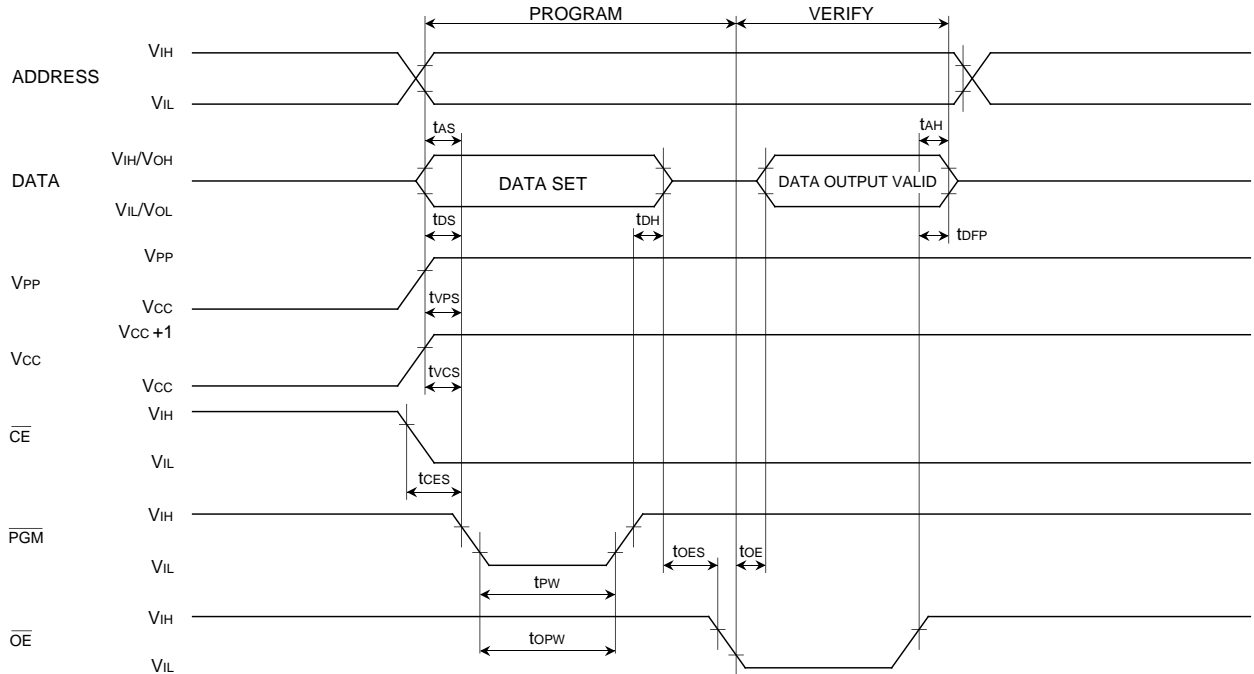
**Programming operation (equivalent to the M5M27C101K)**

AC ELECTRICAL CHARACTERISTICS (Ta = 25 ± 5 °C, VCC = 6 V ± 0.25 V, VPP = 12.5 ± 0.3 V, unless otherwise noted)

| Symbol | Parameter                                 | Test conditions | Limits |      |      | Unit |
|--------|---|-----------------|--------|------|------|------|
|        |   |                 | Min.   | Typ. | Max. |      |
| tAS    | Address setup time                        |                 | 2      |      |      | μs   |
| tOES   | $\overline{OE}$ setup time                |                 | 2      |      |      | μs   |
| tDS    | Data setup time                           |                 | 2      |      |      | μs   |
| tAH    | Address hold time                         |                 | 0      |      |      | μs   |
| tDH    | Data hold time                            |                 | 2      |      |      | μs   |
| tDFP   | Output enable to output float delay       |                 | 0      |      | 130  | ns   |
| tVCS   | VCC setup time                            |                 | 2      |      |      | μs   |
| tVPS   | VPP setup time                            |                 | 2      |      |      | μs   |
| tPW    | $\overline{PGM}$ pulse width              |                 | 0.19   | 0.2  | 0.21 | ms   |
| tOPW   | $\overline{PGM}$ over program pulse width |                 | 0.19   |      | 5.25 | ms   |
| tCES   | $\overline{CE}$ setup time                |                 | 2      |      |      | μs   |
| tOE    | Data valid from $\overline{OE}$           |                 |        |      | 150  | ns   |

**PRELIMINARY**  
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 Some parametric limits are subject to change.

**AC waveforms**



Test conditions for A.C. characteristics

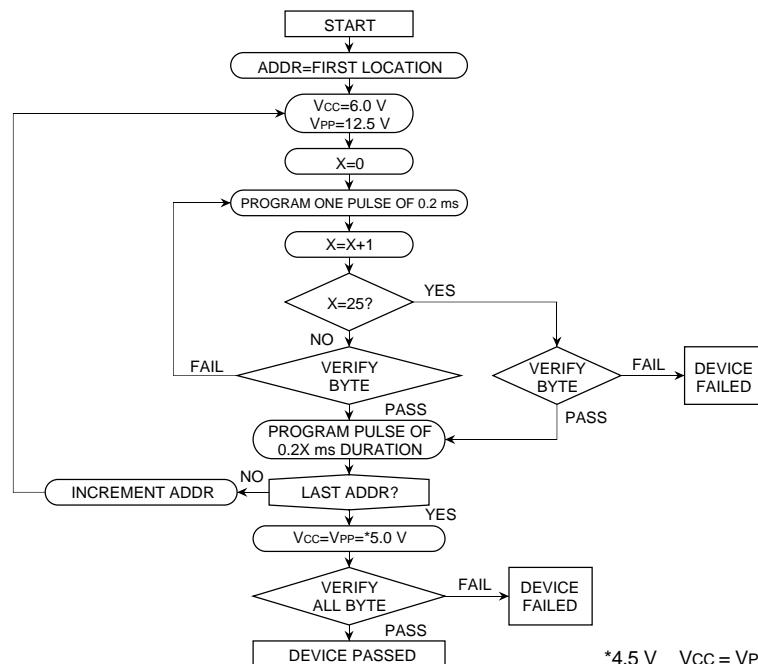
Input voltage : VIL = 0.45 V, VIH = 2.4 V

Input rise and fall times (10% - 90%) : 20 ns

Reference voltage at timing measurement : Input, Output

"L" = 0.8 V, "H" = 2 V

**Programming algorithm flow chart**



\*4.5 V VCC = VPP 5.5 V

**PRELIMINARY**  
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Some parametric limits are subject to change.

**SAFETY INSTRUCTIONS**

- (1) Sunlight and fluorescent lamp contain light that can erase written information. When using in read mode, be sure to cover the transparent glass portion with a seal or other materials (ceramic package product).
- (2) Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the read pins (ceramic package product).
- (3) Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet rays and may affect badly the erasure capability (ceramic package product).
- (4) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
- (5) The programmable M37735EHBFP that is shipped in blank is also provided. For the M37735EHBFP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.

**ADDRESSING MODES**

The M37735EHBXXXFP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

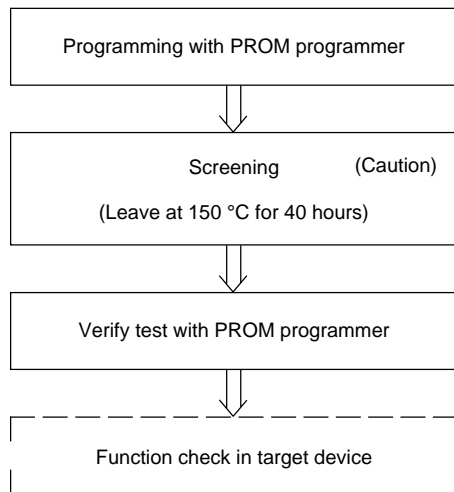
**MACHINE INSTRUCTION LIST**

The M37735EHBXXXFP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.

**DATA REQUIRED FOR PROM ORDERING**

Please send the following data for writing to PROM.

- (1) M37735EHBXXXFP writing to PROM order confirmation form
- (2) 80P6N mark specification form
- (3) ROM data (EPROM 3 sets)



Caution : Never expose to 150 °C exceeding 100 hours.

**PRELIMINARY**  
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**ABSOLUTE MAXIMUM RATINGS**

| Symbol           | Parameter   | Conditions             | Ratings                       | Unit |
|------------------|---|------------------------|-------------------------------|------|
| V <sub>cc</sub>  | Power source voltage  |                        | -0.3 to +7                    | V    |
| AV <sub>cc</sub> | Analog power source voltage   |                        | -0.3 to +7                    | V    |
| V <sub>i</sub>   | Input voltage RESET, CNV <sub>ss</sub> , BYTE   |                        | -0.3 to +12 (Note)            | V    |
| V <sub>i</sub>   | Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, V <sub>REF</sub> , X <sub>IN</sub> |                        | -0.3 to V <sub>cc</sub> + 0.3 | V    |
| V <sub>o</sub>   | Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X <sub>OUT</sub> , E              |                        | -0.3 to V <sub>cc</sub> + 0.3 | V    |
| P <sub>d</sub>   | Power dissipation   | T <sub>a</sub> = 25 °C | 300                           | mW   |
| T <sub>opr</sub> | Operating temperature   |                        | -20 to +85                    | °C   |
| T <sub>stg</sub> | Storage temperature   |                        | -40 to +150                   | °C   |

**Note.** When the EPROM is programmed, input voltage of pins CNV<sub>ss</sub> and BYTE is 13 V respectively.

**RECOMMENDED OPERATING CONDITIONS** (V<sub>cc</sub> = 5 V ± 10%, T<sub>a</sub> = -20 to +85 °C, unless otherwise noted)

| Symbol                | Parameter  |  | Limits              |                 |                     | Unit |
|-----------------------|--|--|---------------------|-----------------|---------------------|------|
|                       |  |  | Min.                | Typ.            | Max.                |      |
| V <sub>cc</sub>       | Power source voltage   | f(X <sub>IN</sub> ) : Operating                                  | 4.5                 | 5.0             | 5.5                 | V    |
|                       |  | f(X <sub>IN</sub> ) : Stopped, f(X <sub>CIN</sub> ) = 32.768 kHz | 2.7                 |                 | 5.5                 |      |
| AV <sub>cc</sub>      | Analog power source voltage  |  |                     | V <sub>cc</sub> |                     | V    |
| V <sub>ss</sub>       | Power source voltage   |  |                     | 0               |                     | V    |
| AV <sub>ss</sub>      | Analog power source voltage  |  |                     | 0               |                     | V    |
| V <sub>IH</sub>       | High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X <sub>IN</sub> , RESET, CNV <sub>ss</sub> , BYTE, X <sub>CIN</sub> (Note 3) |  | 0.8 V <sub>cc</sub> |                 | V <sub>cc</sub>     | V    |
| V <sub>IH</sub>       | High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)  |  | 0.8 V <sub>cc</sub> |                 | V <sub>cc</sub>     | V    |
| V <sub>IH</sub>       | High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)   |  | 0.5 V <sub>cc</sub> |                 | V <sub>cc</sub>     | V    |
| V <sub>IL</sub>       | Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X <sub>IN</sub> , RESET, CNV <sub>ss</sub> , BYTE, X <sub>CIN</sub> (Note 3)  |  | 0                   |                 | 0.2V <sub>cc</sub>  | V    |
| V <sub>IL</sub>       | Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)   |  | 0                   |                 | 0.2V <sub>cc</sub>  | V    |
| V <sub>IL</sub>       | Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)  |  | 0                   |                 | 0.16V <sub>cc</sub> | V    |
| I <sub>OH(peak)</sub> | High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87   |  |                     |                 | -10                 | mA   |
| I <sub>OH(avg)</sub>  | High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87  |  |                     |                 | -5                  | mA   |
| I <sub>OL(peak)</sub> | Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87  |  |                     |                 | 10                  | mA   |
| I <sub>OL(peak)</sub> | Low-level peak output current P44 – P47, P50 – P53   |  |                     |                 | 20                  | mA   |
| I <sub>OL(avg)</sub>  | Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87   |  |                     |                 | 5                   | mA   |
| I <sub>OL(avg)</sub>  | Low-level average output current P44 – P47, P50 – P53  |  |                     |                 | 15                  | mA   |
| f(X <sub>IN</sub> )   | Main-clock oscillation frequency (Note 4)  |  |                     |                 | 25                  | MHz  |
| f(X <sub>CIN</sub> )  | Sub-clock oscillation frequency  |  |                     | 32.768          | 50                  | kHz  |

- Notes**
1. Average output current is the average value of a 100 ms interval.
  2. The sum of I<sub>OL(peak)</sub> for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I<sub>OH(peak)</sub> for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I<sub>OL(peak)</sub> for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I<sub>OH(peak)</sub> for ports P4, P5, P6, and P7 must be 80 mA or less.
  3. Limits V<sub>IH</sub> and V<sub>IL</sub> for X<sub>CIN</sub> are applied when the sub clock external input selection bit = "1".
  4. The maximum value of f(X<sub>IN</sub>) = 12.5 MHz when the main clock division selection bit = "1".

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 25\text{ MHz}$ , unless otherwise noted)

| Symbol                            | Parameter  | Test conditions   | Limits     |      |             | Unit |
|-----------------------------------|--|---|------------|------|-------------|------|
|                                   |  |   | Min.       | Typ. | Max.        |      |
| V <sub>OH</sub>                   | High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87  | I <sub>OH</sub> = –10 mA  | 3          |      |             | V    |
| V <sub>OH</sub>                   | High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33   | I <sub>OH</sub> = –400 μA   | 4.7        |      |             | V    |
| V <sub>OH</sub>                   | High-level output voltage P30 – P32  | I <sub>OH</sub> = –10 mA<br>I <sub>CH</sub> = –400 μA   | 3.1<br>4.8 |      |             | V    |
| V <sub>OH</sub>                   | High-level output voltage $\bar{E}$  | I <sub>OH</sub> = –10 mA<br>I <sub>OH</sub> = –400 μA   | 3.4<br>4.8 |      |             | V    |
| V <sub>OL</sub>                   | Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P43, P54 – P57, P60 – P67, P70 – P75, P80 – P87   | I <sub>OL</sub> = 10 mA   |            |      | 2           | V    |
| V <sub>OL</sub>                   | Low-level output voltage P44 – P47, P50 – P53  | I <sub>OL</sub> = 20 mA   |            |      | 2           | V    |
| V <sub>OL</sub>                   | Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33  | I <sub>OL</sub> = 2 mA  |            |      | 0.45        | V    |
| V <sub>OL</sub>                   | Low-level output voltage P30 – P32   | I <sub>OL</sub> = 10 mA<br>I <sub>OL</sub> = 2 mA   |            |      | 1.9<br>0.43 | V    |
| V <sub>OL</sub>                   | Low-level output voltage $\bar{E}$   | I <sub>OL</sub> = 10 mA<br>I <sub>OL</sub> = 2 mA   |            |      | 1.6<br>0.4  | V    |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis $\overline{HOLD}$ , $\overline{RDY}$ , $\overline{TA0IN} - \overline{TA4IN}$ , $\overline{TB0IN} - \overline{TB2IN}$ , $\overline{INT0} - \overline{INT2}$ , $\overline{ADTRG}$ , $\overline{CTS0}$ , $\overline{CTS1}$ , $\overline{CTS2}$ , $\overline{CLK0}$ , $\overline{CLK1}$ , $\overline{CLK2}$ , $\overline{K10} - \overline{K13}$ |   | 0.4        |      | 1           | V    |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis $\overline{RESET}$  |   | 0.2        |      | 0.5         | V    |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis $\overline{XIN}$  |   | 0.1        |      | 0.4         | V    |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis $\overline{XCIN}$ (When external clock is input)  |   | 0.1        |      | 0.4         | V    |
| I <sub>IH</sub>                   | High-level input current<br>P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, $\overline{XIN}$ , $\overline{RESET}$ , $\overline{CNVSS}$ , $\overline{BYTE}$  | V <sub>I</sub> = 5 V  |            |      | 5           | μA   |
| I <sub>IL</sub>                   | Low-level input current<br>P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, $\overline{XIN}$ , $\overline{RESET}$ , $\overline{CNVSS}$ , $\overline{BYTE}$   | V <sub>I</sub> = 0 V  |            |      | –5          | μA   |
| I <sub>IL</sub>                   | Low-level input current P54 – P57, P62 – P64   | V <sub>I</sub> = 0 V,<br>without a pull-up transistor<br>V <sub>I</sub> = 0 V,<br>with a pull-up transistor |            |      | –5          | μA   |
| V <sub>RAM</sub>                  | RAM hold voltage   | When clock is stopped.  | 2          |      |             | V    |

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ , unless otherwise noted)

| Symbol          | Parameter            | Test conditions   | Limits  |      |      | Unit |               |
|-----------------|----------------------|---|---|------|------|------|---------------|
|                 |                      |   | Min.  | Typ. | Max. |      |               |
| I <sub>CC</sub> | Power source current | In single-chip mode, output pins are open, and other pins are V <sub>SS</sub> . | $V_{CC} = 5\text{ V}$ ,<br>$f(X_{IN}) = 25\text{ MHz}$ (square waveform),<br>( $f(f_2) = 12.5\text{ MHz}$ ),<br>$f(X_{CIN}) = 32.768\text{ kHz}$ ,<br>in operating (Note 1) |      | 9.5  | 19   | mA            |
|                 |                      |   | $V_{CC} = 5\text{ V}$ ,<br>$f(X_{IN}) = 25\text{ MHz}$ (square waveform),<br>( $f(f_2) = 1.5625\text{ MHz}$ ),<br>$f(X_{CIN}) = \text{Stopped}$ ,<br>in operating (Note 1)  |      | 1.3  | 2.6  | mA            |
|                 |                      |   | $V_{CC} = 5\text{ V}$ ,<br>$f(X_{IN}) = 25\text{ MHz}$ (square waveform),<br>$f(X_{CIN}) = 32.768\text{ kHz}$ ,<br>when a WIT instruction is executed (Note 2)              |      | 10   | 20   | $\mu\text{A}$ |
|                 |                      |   | $V_{CC} = 5\text{ V}$ ,<br>$f(X_{IN}) : \text{Stopped}$ ,<br>$f(X_{CIN}) : 32.768\text{ kHz}$ ,<br>in operating (Note 3)  |      | 50   | 100  | $\mu\text{A}$ |
|                 |                      |   | $V_{CC} = 5\text{ V}$ ,<br>$f(X_{IN}) : \text{Stopped}$ ,<br>$f(X_{CIN}) : 32.768\text{ kHz}$ ,<br>when a WIT instruction is executed (Note 4)                              |      | 5    | 10   | $\mu\text{A}$ |
|                 |                      |   | $T_a = 25\text{ }^\circ\text{C}$ ,<br>when clock is stopped   |      |      | 1    | $\mu\text{A}$ |
|                 |                      |   | $T_a = 85\text{ }^\circ\text{C}$ ,<br>when clock is stopped   |      |      | 20   | $\mu\text{A}$ |

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
  2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
  3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
  4. This applies when the X<sub>COUT</sub> drivability selection bit = "0" and the system clock stop bit at wait state = "1".

**A-D CONVERTER CHARACTERISTICS**

( $V_{CC} = AV_{CC} = 5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 25\text{ MHz}$  (Note), unless otherwise noted)

| Symbol            | Parameter            | Test conditions    | Limits |      |           | Unit          |
|-------------------|----------------------|--------------------|--------|------|-----------|---------------|
|                   |                      |                    | Min.   | Typ. | Max.      |               |
| —                 | Resolution           | $V_{REF} = V_{CC}$ |        |      | 10        | Bits          |
| —                 | Absolute accuracy    | $V_{REF} = V_{CC}$ |        |      | $\pm 3$   | LSB           |
| RLADDER           | Ladder resistance    | $V_{REF} = V_{CC}$ | 10     |      | 25        | k $\Omega$    |
| t <sub>CONV</sub> | Conversion time      |                    | 9.44   |      |           | $\mu\text{s}$ |
| V <sub>REF</sub>  | Reference voltage    |                    | 2      |      | $V_{CC}$  | V             |
| V <sub>IA</sub>   | Analog input voltage |                    | 0      |      | $V_{REF}$ | V             |

**Note.** This applies when the main clock division selection bit = "0" and  $f(f_2) = 12.5\text{ MHz}$ .

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**TIMING REQUIREMENTS** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 25\text{ MHz}$ , unless otherwise noted (Note))

**Notes 1.** This applies when the main clock division selection bit = "0" and  $f(f_2) = 12.5\text{ MHz}$ .

**2.** Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

**External clock input**

| Symbol     | Parameter  | Limits |      | Unit |
|------------|--|--------|------|------|
|            |  | Min.   | Max. |      |
| $t_c$      | External clock input cycle time (Note 3)             | 40     |      | ns   |
| $t_{w(H)}$ | External clock input high-level pulse width (Note 4) | 15     |      | ns   |
| $t_{w(L)}$ | External clock input low-level pulse width (Note 4)  | 15     |      | ns   |
| $t_r$      | External clock rise time                             |        | 8    | ns   |
| $t_f$      | External clock fall time                             |        | 8    | ns   |

**Notes 3.** When the main clock division selection bit = "1", the minimum value of  $t_c = 80\text{ ns}$ .

**4.** When the main clock division selection bit = "1", values of  $t_{w(H)} / t_c$  and  $t_{w(L)} / t_c$  must be set to values from 0.45 through 0.55.

**Single-chip mode**

| Symbol          | Parameter                | Limits |      | Unit |
|-----------------|--------------------------|--------|------|------|
|                 |                          | Min.   | Max. |      |
| $t_{su(P0D-E)}$ | Port P0 input setup time | 60     |      | ns   |
| $t_{su(P1D-E)}$ | Port P1 input setup time | 60     |      | ns   |
| $t_{su(P2D-E)}$ | Port P2 input setup time | 60     |      | ns   |
| $t_{su(P3D-E)}$ | Port P3 input setup time | 60     |      | ns   |
| $t_{su(P4D-E)}$ | Port P4 input setup time | 60     |      | ns   |
| $t_{su(P5D-E)}$ | Port P5 input setup time | 60     |      | ns   |
| $t_{su(P6D-E)}$ | Port P6 input setup time | 60     |      | ns   |
| $t_{su(P7D-E)}$ | Port P7 input setup time | 60     |      | ns   |
| $t_{su(P8D-E)}$ | Port P8 input setup time | 60     |      | ns   |
| $t_{h(E-P0D)}$  | Port P0 input hold time  | 0      |      | ns   |
| $t_{h(E-P1D)}$  | Port P1 input hold time  | 0      |      | ns   |
| $t_{h(E-P2D)}$  | Port P2 input hold time  | 0      |      | ns   |
| $t_{h(E-P3D)}$  | Port P3 input hold time  | 0      |      | ns   |
| $t_{h(E-P4D)}$  | Port P4 input hold time  | 0      |      | ns   |
| $t_{h(E-P5D)}$  | Port P5 input hold time  | 0      |      | ns   |
| $t_{h(E-P6D)}$  | Port P6 input hold time  | 0      |      | ns   |
| $t_{h(E-P7D)}$  | Port P7 input hold time  | 0      |      | ns   |
| $t_{h(E-P8D)}$  | Port P8 input hold time  | 0      |      | ns   |

**Memory expansion mode and microprocessor mode**

| Symbol                | Parameter             | Limits |      | Unit |
|-----------------------|-----------------------|--------|------|------|
|                       |                       | Min.   | Max. |      |
| $t_{su(D-RDE)}$       | Data input setup time | 32     |      | ns   |
| $t_{su(RDY-\phi_1)}$  | RDY input setup time  | 55     |      | ns   |
| $t_{su(HOLD-\phi_1)}$ | HOLD input setup time | 55     |      | ns   |
| $t_{h(RDE-D)}$        | Data input hold time  | 0      |      | ns   |
| $t_{h(\phi_1-RDY)}$   | RDY input hold time   | 0      |      | ns   |
| $t_{h(\phi_1-HOLD)}$  | HOLD input hold time  | 0      |      | ns   |



**Timer A input** (Count input in event counter mode)

| Symbol               | parameter                          | Limits |      | Unit |
|----------------------|------------------------------------|--------|------|------|
|                      |                                    | Min.   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIN input cycle time             | 80     |      | ns   |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width | 40     |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width  | 40     |      | ns   |

**Timer A input** (Gating input in timer mode)

| Symbol               | parameter                                 | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIN input cycle time (Note)             | 320    |      | ns   |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width (Note) | 160    |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width (Note)  | 160    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 19.

**Timer A input** (External trigger input in one-shot pulse mode)

| Symbol               | parameter                          | Limits |      | Unit |
|----------------------|------------------------------------|--------|------|------|
|                      |                                    | Min.   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIN input cycle time (Note)      | 320    |      | ns   |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width | 80     |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width  | 80     |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 19.

**Timer A input** (External trigger input in pulse width modulation mode)

| Symbol               | parameter                          | Limits |      | Unit |
|----------------------|------------------------------------|--------|------|------|
|                      |                                    | Min.   | Max. |      |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width | 80     |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width  | 80     |      | ns   |

**Timer A input** (Up-down input in event counter mode)

| Symbol                                | parameter                           | Limits |      | Unit |
|---------------------------------------|-------------------------------------|--------|------|------|
|                                       |                                     | Min.   | Max. |      |
| t <sub>c</sub> (UP)                   | TAiOUT input cycle time             | 2000   |      | ns   |
| t <sub>w</sub> (UPH)                  | TAiOUT input high-level pulse width | 1000   |      | ns   |
| t <sub>w</sub> (UPL)                  | TAiOUT input low-level pulse width  | 1000   |      | ns   |
| t <sub>su</sub> (UP-T <sub>IN</sub> ) | TAiOUT input setup time             | 400    |      | ns   |
| t <sub>h</sub> (T <sub>IN</sub> -UP)  | TAiOUT input hold time              | 400    |      | ns   |

**Timer A input** (Two-phase pulse input in event counter mode)

| Symbol                         | parameter               | Limits |      | Unit |
|--------------------------------|-------------------------|--------|------|------|
|                                |                         | Min.   | Max. |      |
| t <sub>c</sub> (TA)            | TAjIN input cycle time  | 800    |      | ns   |
| t <sub>su</sub> (TAjIN-TAjOUT) | TAjIN input setup time  | 200    |      | ns   |
| t <sub>su</sub> (TAjOUT-TAjIN) | TAjOUT input setup time | 200    |      | ns   |

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**Timer B input** (Count input in event counter mode)

| Symbol               | Parameter   | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>c</sub> (TB)  | TB <sub>iIN</sub> input cycle time (one edge count)               | 80     |      | ns   |
| t <sub>w</sub> (TBH) | TB <sub>iIN</sub> input high-level pulse width (one edge count)   | 40     |      | ns   |
| t <sub>w</sub> (TBL) | TB <sub>iIN</sub> input low-level pulse width (one edge count)    | 40     |      | ns   |
| t <sub>c</sub> (TB)  | TB <sub>iIN</sub> input cycle time (both edges count)             | 160    |      | ns   |
| t <sub>w</sub> (TBH) | TB <sub>iIN</sub> input high-level pulse width (both edges count) | 80     |      | ns   |
| t <sub>w</sub> (TBL) | TB <sub>iIN</sub> input low-level pulse width (both edges count)  | 80     |      | ns   |

**Timer B input** (Pulse period measurement mode)

| Symbol               | Parameter   | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>c</sub> (TB)  | TB <sub>iIN</sub> input cycle time (Note)             | 320    |      | ns   |
| t <sub>w</sub> (TBH) | TB <sub>iIN</sub> input high-level pulse width (Note) | 160    |      | ns   |
| t <sub>w</sub> (TBL) | TB <sub>iIN</sub> input low-level pulse width (Note)  | 160    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 19.

**Timer B input** (Pulse width measurement mode)

| Symbol               | Parameter   | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>c</sub> (TB)  | TB <sub>iIN</sub> input cycle time (Note)             | 320    |      | ns   |
| t <sub>w</sub> (TBH) | TB <sub>iIN</sub> input high-level pulse width (Note) | 160    |      | ns   |
| t <sub>w</sub> (TBL) | TB <sub>iIN</sub> input low-level pulse width (Note)  | 160    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 19.

**A-D trigger input**

| Symbol               | Parameter  | Limits |      | Unit |
|----------------------|--|--------|------|------|
|                      |  | Min.   | Max. |      |
| t <sub>c</sub> (AD)  | AD <sub>TRG</sub> input cycle time (minimum allowable trigger) | 1000   |      | ns   |
| t <sub>w</sub> (ADL) | AD <sub>TRG</sub> input low-level pulse width                  | 125    |      | ns   |

**Serial I/O**

| Symbol                | Parameter                                     | Limits |      | Unit |
|-----------------------|---|--------|------|------|
|                       |   | Min.   | Max. |      |
| t <sub>c</sub> (CK)   | CLK <sub>i</sub> input cycle time             | 200    |      | ns   |
| t <sub>w</sub> (CKH)  | CLK <sub>i</sub> input high-level pulse width | 100    |      | ns   |
| t <sub>w</sub> (CKL)  | CLK <sub>i</sub> input low-level pulse width  | 100    |      | ns   |
| t <sub>d</sub> (C-Q)  | TxD <sub>i</sub> output delay time            |        | 80   | ns   |
| t <sub>h</sub> (C-Q)  | TxD <sub>i</sub> hold time                    | 0      |      | ns   |
| t <sub>su</sub> (D-C) | RxD <sub>i</sub> input setup time             | 30     |      | ns   |
| t <sub>h</sub> (C-D)  | RxD <sub>i</sub> input hold time              | 90     |      | ns   |

**External interrupt INT<sub>i</sub> input, key input interrupt KI<sub>i</sub> input**

| Symbol               | Parameter                                     | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>w</sub> (INH) | INT <sub>i</sub> input high-level pulse width | 250    |      | ns   |
| t <sub>w</sub> (INL) | INT <sub>i</sub> input low-level pulse width  | 250    |      | ns   |
| t <sub>w</sub> (KIL) | KI <sub>i</sub> input low-level pulse width   | 250    |      | ns   |

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**DATA FORMULAS**

**Timer A input** (Gating input in timer mode)

| Symbol              | Parameter                          | Limits                                 |      | Unit |
|---------------------|------------------------------------|--|------|------|
|                     |                                    | Min.                                   | Max. |      |
| t <sub>c(TA)</sub>  | TAiIn input cycle time             | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w(TAH)</sub> | TAiIn input high-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w(TAL)</sub> | TAiIn input low-level pulse width  | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |

**Timer A input** (External trigger input in one-shot pulse mode)

| Symbol             | Parameter              | Limits                                 |      | Unit |
|--------------------|------------------------|--|------|------|
|                    |                        | Min.                                   | Max. |      |
| t <sub>c(TA)</sub> | TAiIn input cycle time | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |

**Timer B input** (In pulse period measurement mode or pulse width measurement mode)

| Symbol              | Parameter                          | Limits                                 |      | Unit |
|---------------------|------------------------------------|--|------|------|
|                     |                                    | Min.                                   | Max. |      |
| t <sub>c(TB)</sub>  | TBiIn input cycle time             | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w(TBH)</sub> | TBiIn input high-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w(TBL)</sub> | TBiIn input low-level pulse width  | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |

**Note.** f(f<sub>2</sub>) represents the clock f<sub>2</sub> frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85^\circ\text{C}$ ,  $f(X_{IN}) = 25\text{ MHz}$  (Note), unless otherwise noted)

**Single-chip mode**

| Symbol         | Parameter                      | Test conditions | Limits |      | Unit |
|----------------|--------------------------------|-----------------|--------|------|------|
|                |                                |                 | Min.   | Max. |      |
| $t_{d(E-P0Q)}$ | Port P0 data output delay time | Fig. 5          |        | 80   | ns   |
| $t_{d(E-P1Q)}$ | Port P1 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P2Q)}$ | Port P2 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P3Q)}$ | Port P3 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P4Q)}$ | Port P4 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P5Q)}$ | Port P5 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P6Q)}$ | Port P6 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P7Q)}$ | Port P7 data output delay time |                 |        | 80   | ns   |
| $t_{d(E-P8Q)}$ | Port P8 data output delay time |                 |        | 80   | ns   |

**Note.** This applies when the main clock division selection bit = "0" and  $f(f_2) = 12.5\text{ MHz}$ .

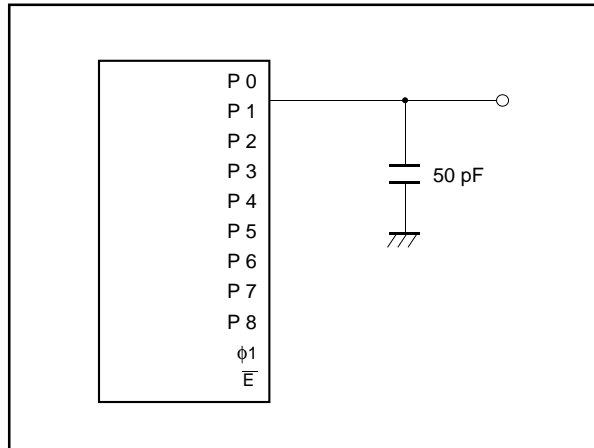


Fig. 5 Measuring circuit for ports P0 – P8 and  $\phi_1$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**Memory expansion mode and microprocessor mode**

(VCC = 5 V ± 10%, VSS = 0 V, Ta = -20 to 85 °C, f(XIN) = 25 MHz (Note 1), unless otherwise noted)

| Symbol       | Parameter                     | (Note 2)<br>Wait mode | Test conditions | Limits |      | Unit |
|--------------|-------------------------------|-----------------------|-----------------|--------|------|------|
|              |                               |                       |                 | Min.   | Max. |      |
| td(CS-WE)    | Chip-select output delay time | No wait               | Fig. 5          | 12     |      | ns   |
| td(CS-RDE)   |                               | Wait 1                |                 | 87     |      | ns   |
|              |                               | Wait 0                |                 |        |      |      |
| th(WE-CS)    | Chip-select hold time         |                       |                 | 4      |      | ns   |
| th(RDE-CS)   |                               |                       |                 |        |      |      |
| td(An-WE)    | Address output delay time     | No wait               |                 | 12     |      | ns   |
| td(An-RDE)   |                               | Wait 1                |                 | 87     |      | ns   |
|              |                               | Wait 0                |                 |        |      |      |
| td(A-WE)     | Address output delay time     | No wait               |                 | 12     |      | ns   |
| td(A-RDE)    |                               | Wait 1                |                 | 75     |      | ns   |
|              |                               | Wait 0                |                 |        |      |      |
| th(WE-An)    | Address hold time             |                       |                 | 18     |      | ns   |
| th(RDE-An)   |                               |                       |                 |        |      |      |
| tw(ALE)      | ALE pulse width               | No wait               |                 | 22     |      | ns   |
|              |                               | Wait 1                |                 | 57     |      | ns   |
|              |                               | Wait 0                |                 |        |      |      |
| tsu(A-ALE)   | Address output setup time     | No wait               | 5               |        | ns   |      |
|              |                               | Wait 1                | 45              |        | ns   |      |
|              |                               | Wait 0                |                 |        |      |      |
| th(ALE-A)    | Address hold time             | No wait               | 9               |        | ns   |      |
|              |                               | Wait 1                | 15              |        | ns   |      |
|              |                               | Wait 0                |                 |        |      |      |
| td(ALE-WE)   | ALE output delay time         | No wait               | 4               |        | ns   |      |
| td(ALE-RDE)  |                               | Wait 1                | 10              |        | ns   |      |
|              |                               | Wait 0                |                 |        |      |      |
| td(WE-DQ)    | Data output delay time        |                       |                 | 45     | ns   |      |
| th(WE-DQ)    | Data hold time                |                       |                 | 18     | ns   |      |
| tw(WE)       | WEL/WEH pulse width           | No wait               | 50              |        | ns   |      |
|              |                               | Wait 1                | 130             |        | ns   |      |
|              |                               | Wait 0                |                 |        |      |      |
| tpxz(RDE-DZ) | Floating start delay time     |                       |                 | 5      | ns   |      |
| tpzx(RDE-DZ) | Floating release delay time   |                       |                 | 20     | ns   |      |
| tw(RDE)      | RDE pulse width               | No wait               | 48              |        | ns   |      |
|              |                               | Wait 1                | 128             |        | ns   |      |
|              |                               | Wait 0                |                 |        |      |      |
| td(RSMP-WE)  | RSMP output delay time        |                       | 10              |        | ns   |      |
| td(RSMP-RDE) |                               |                       |                 |        |      |      |
| th(φ1-RSMP)  | RSMP hold time                |                       | 0               |        | ns   |      |
| td(WE-φ1)    | φ1 output delay time          |                       | 0               |        | ns   |      |
| td(RDE-φ1)   |                               |                       |                 | 18     |      |      |
| td(φ1-HLDA)  | HLDA output delay time        |                       |                 | 50     | ns   |      |

**Notes 1.** This applies when the main clock division selection bit = "0" and f(f2) = 12.5 MHz.

**2.** No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

**Memory expansion mode and microprocessor mode**

**Bus timing data formulas** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 25\text{ MHz}$  (Max., Note1), unless otherwise noted)

| Symbol                                  | Parameter                     | Wait mode | Limits                                      |      | Unit |
|---|-------------------------------|-----------|---|------|------|
|   |                               |           | Min.  | Max. |      |
| td(CS-WE)<br>td(CS-RDE)                 | Chip-select output delay time | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$ |      | ns   |
|   |                               | Wait 1    | $\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$ |      | ns   |
| th(WE-CS)<br>th(RDE-CS)                 | Chip-select hold time         |           | 4   |      | ns   |
|   |                               |           |   |      |      |
| td(An-WE)<br>td(An-RDE)                 | Address output delay time     | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$ |      | ns   |
|   |                               | Wait 1    | $\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$ |      | ns   |
| td(A-WE)<br>td(A-RDE)                   | Address output delay time     | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$ |      | ns   |
|   |                               | Wait 1    | $\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$ |      | ns   |
| th(WE-An)<br>th(RDE-An)                 | Address hold time             |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$ |      | ns   |
|   |                               |           |   |      |      |
| tw(ALE)                                 | ALE pulse width               | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$ |      | ns   |
|   |                               | Wait 1    | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$ |      | ns   |
| tsu(A-ALE)                              | Address output setup time     | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$ |      | ns   |
|   |                               | Wait 1    | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$ |      | ns   |
| th(ALE-A)                               | Address hold time             | No wait   | 9   |      | ns   |
|   |                               | Wait 1    | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$ |      | ns   |
| td(ALE-WE)<br>td(ALE-RDE)               | ALE output delay time         | No wait   | 4   |      | ns   |
|   |                               | Wait 1    | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$ |      | ns   |
| td(WE-DQ)                               | Data output delay time        |           |   | 45   | ns   |
| th(WE-DQ)                               | Data hold time                |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$ |      | ns   |
| tw(WE)                                  | WEL/WEH pulse width           | No wait   | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$ |      | ns   |
|   |                               | Wait 1    | $\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$ |      | ns   |
| tpxz(RDE-DZ)                            | Floating start delay time     |           |   | 5    | ns   |
| tpzx(RDE-DZ)                            | Floating release delay time   |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$ |      | ns   |
| tw(RDE)                                 | RDE pulse width               | No wait   | $\frac{2 \times 10^9}{2 \cdot f(f_2)} - 32$ |      | ns   |
|   |                               | Wait 1    | $\frac{4 \times 10^9}{2 \cdot f(f_2)} - 32$ |      | ns   |
| td(RSMP-WE)<br>td(RSMP-RDE)             | RSMP output delay time        |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$ |      | ns   |
| th( $\phi_1$ -RSMP)                     | RSMP hold time                |           | 0   |      | ns   |
| td(WE- $\phi_1$ )<br>td(RDE- $\phi_1$ ) | $\phi_1$ output delay time    |           | 0   | 18   | ns   |

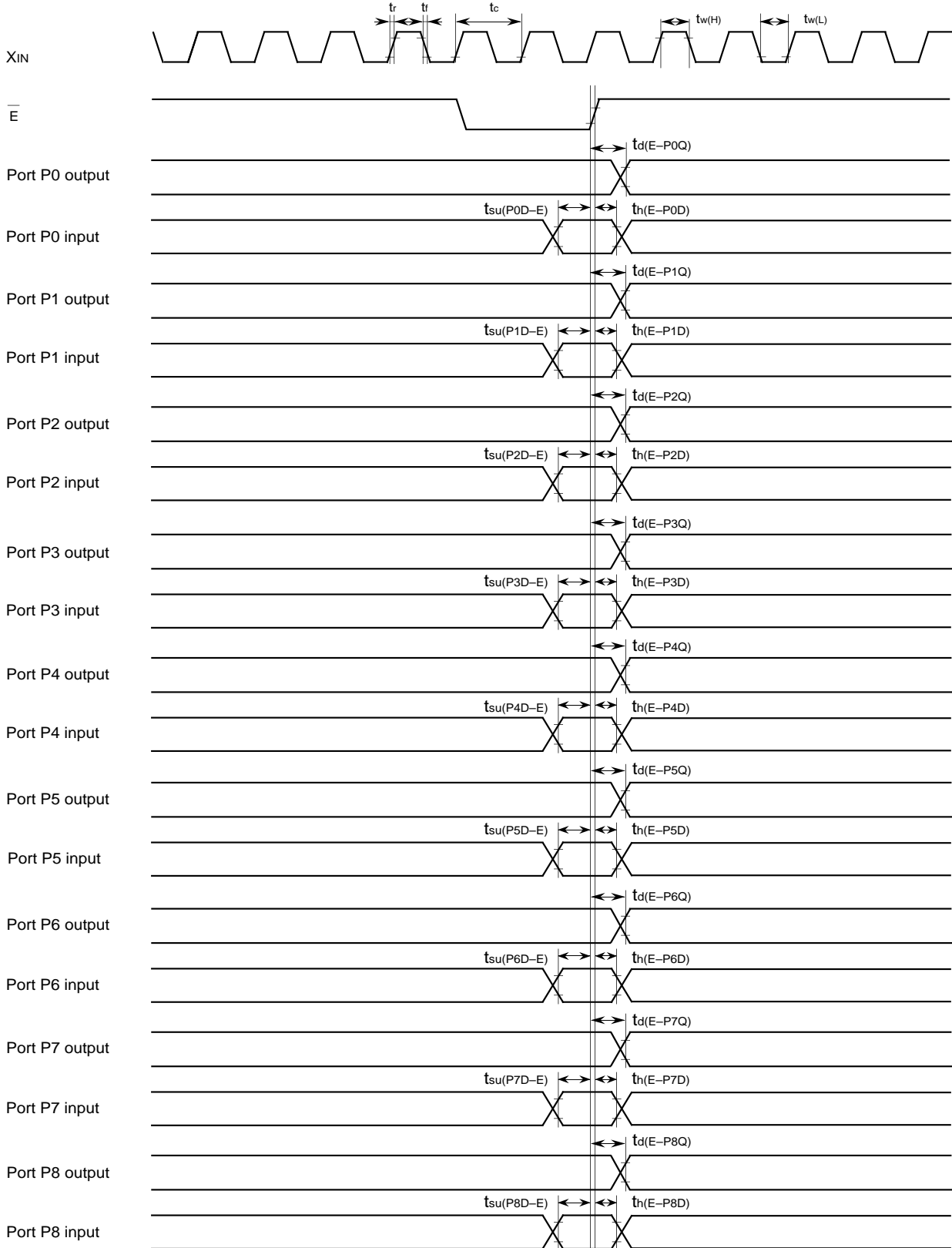
**Notes 1.** This applies when the main-clock division selection bit = "0".

**2.**  $f(f_2)$  represents the clock  $f_2$  frequency.

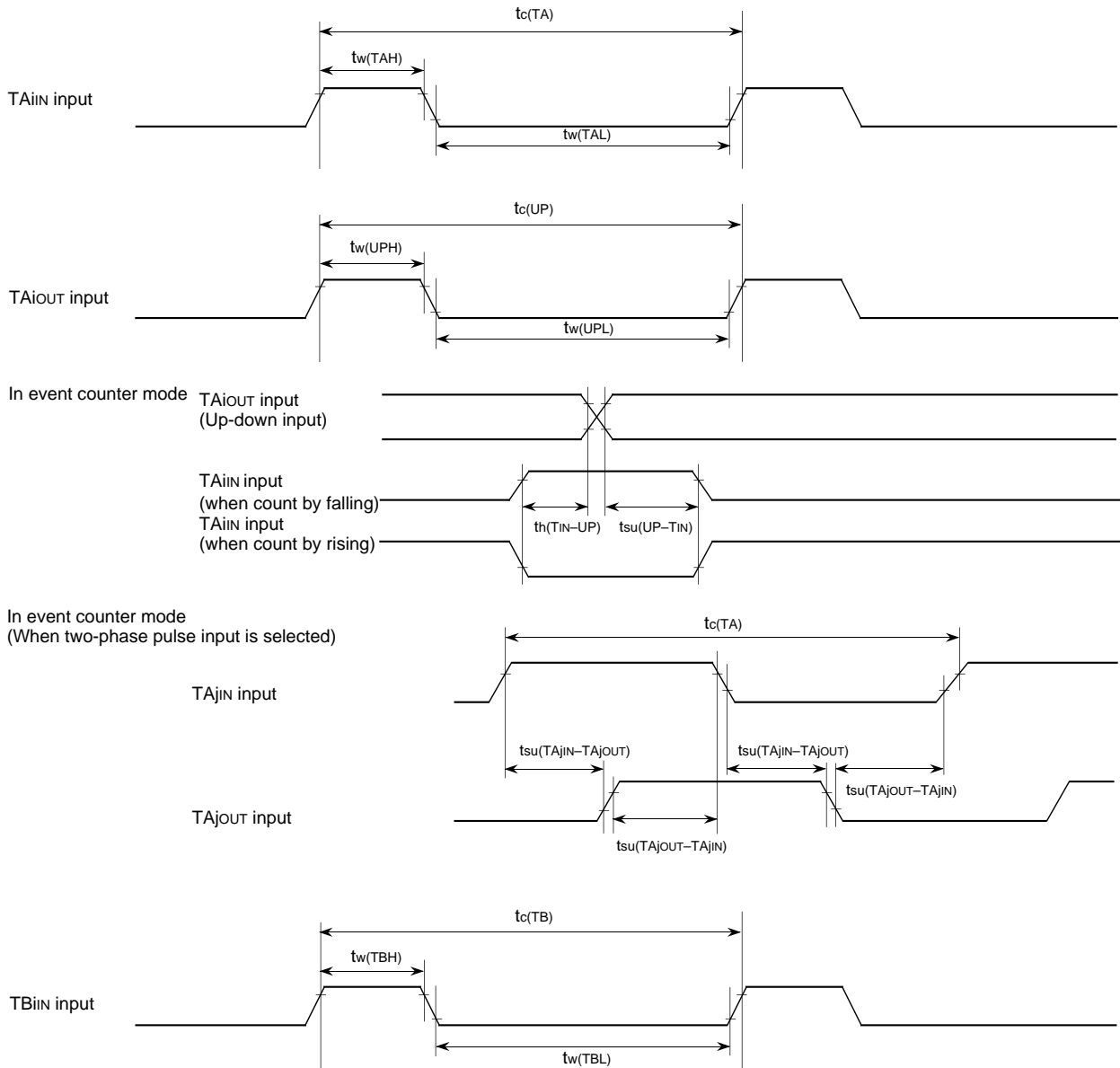
For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**TIMING DIAGRAM**



**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

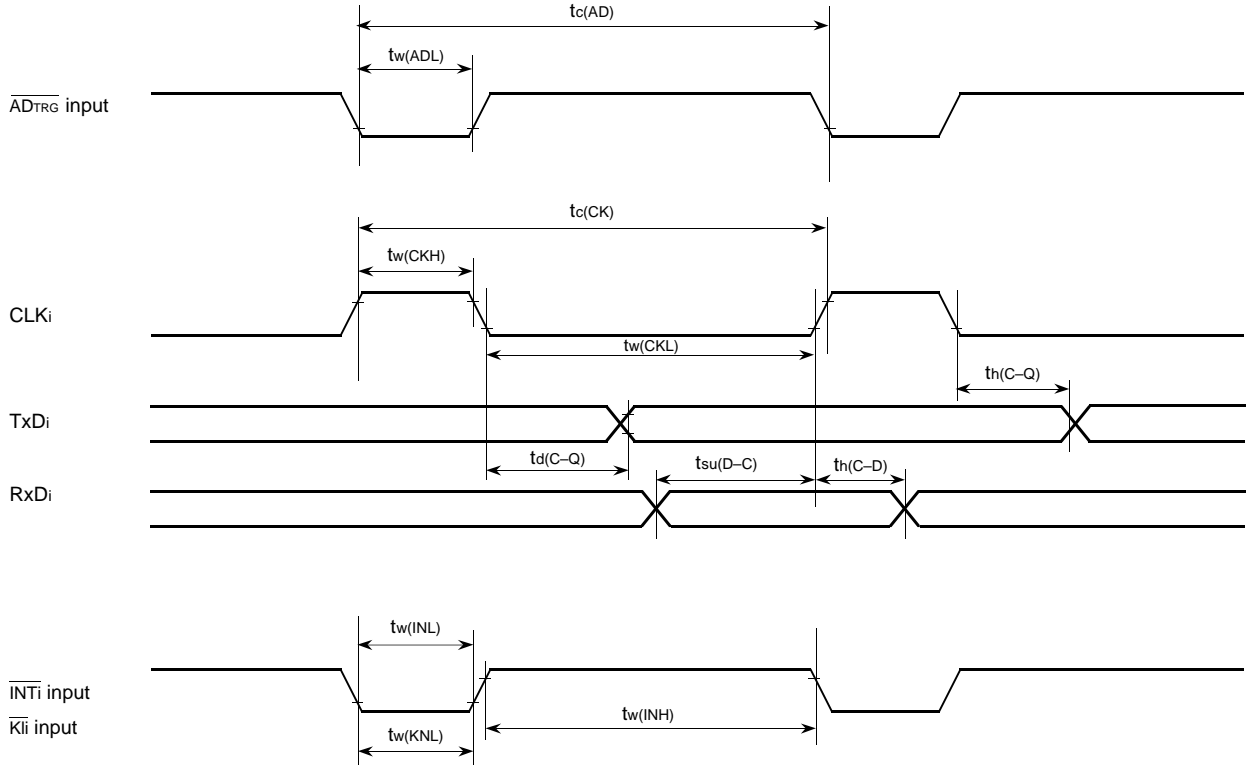




**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

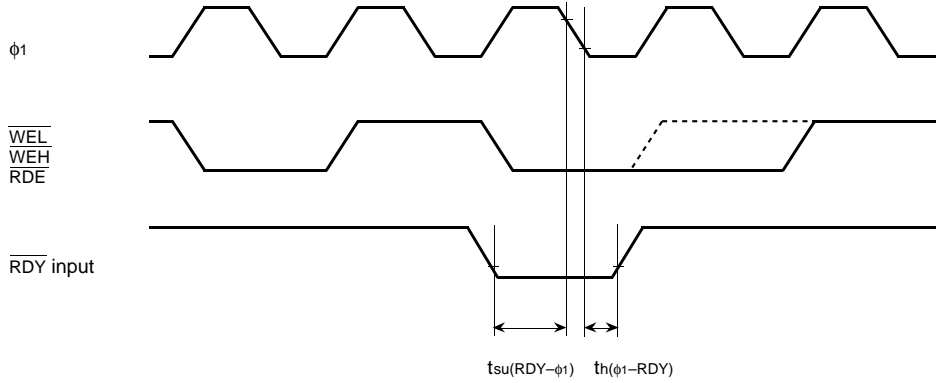
**M37735EHBXXXFP**  
**M37735EHBFS**

PROM VERSION OF M37735MHBXXXFP

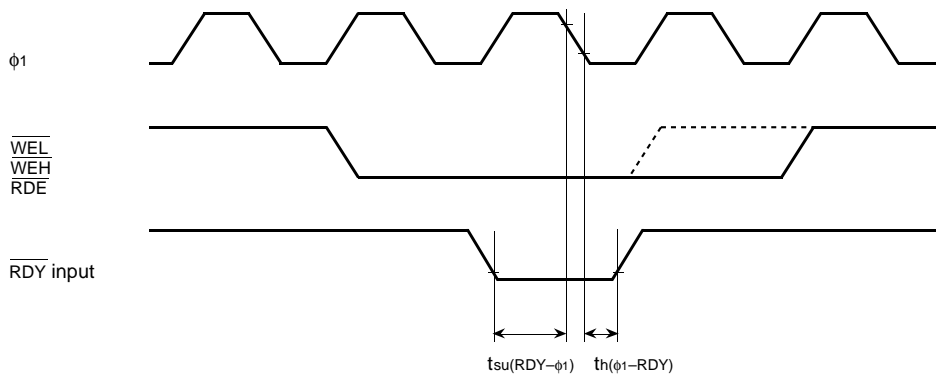


**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

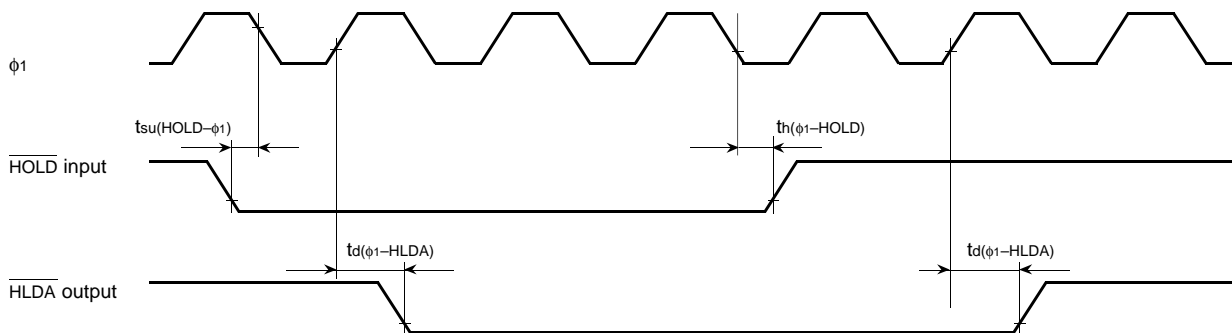
Memory expansion mode and microprocessor mode  
 (When wait bit = "1")



(When wait bit = "0")



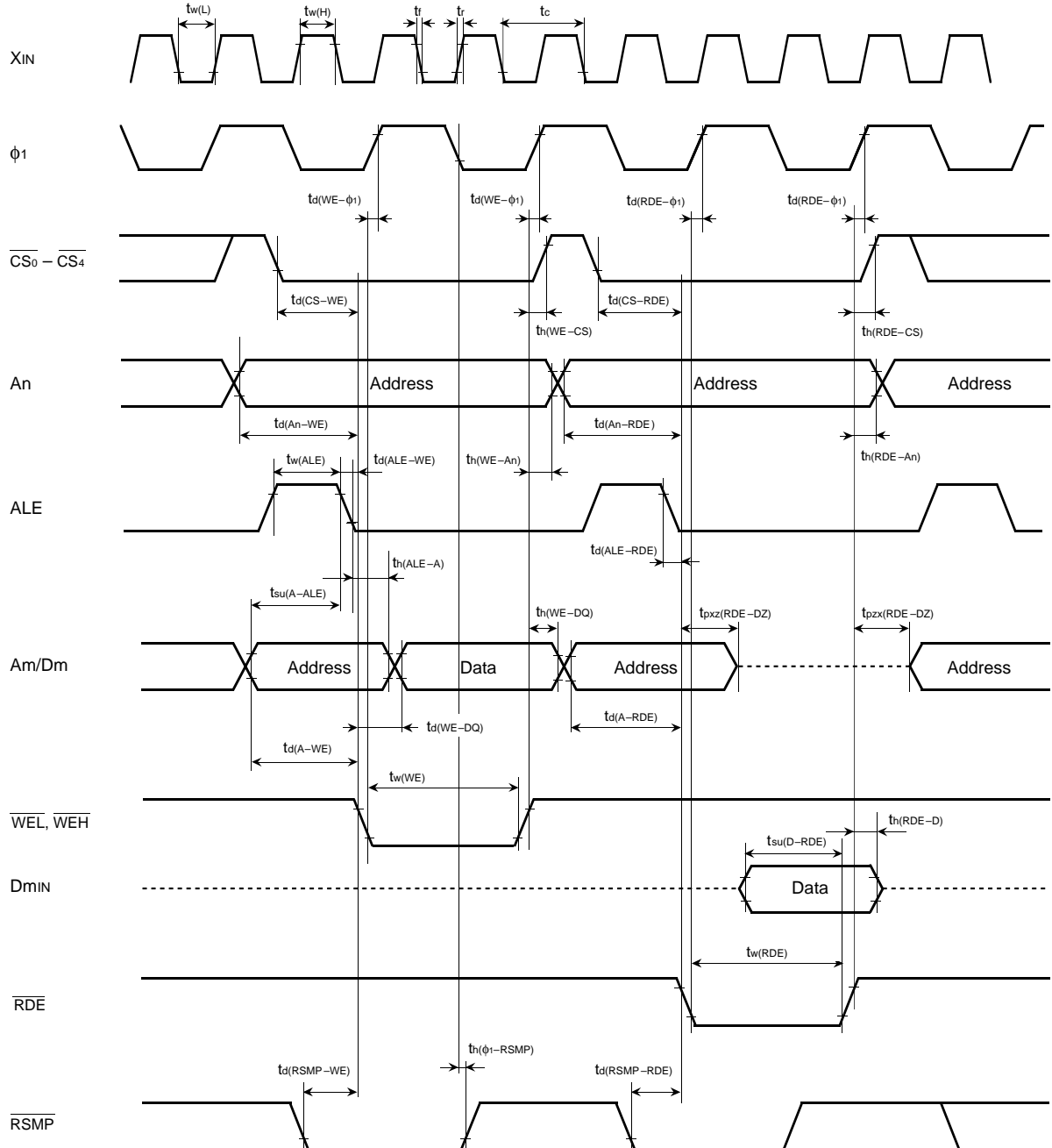
(When wait bit = "1" or "0" in common)



- Test conditions
- $V_{CC} = 5\text{ V} \pm 10\%$
  - Input timing voltage :  $V_{IL} = 1.0\text{ V}$ ,  $V_{IH} = 4.0\text{ V}$
  - Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode  
 (No wait : When wait bit = "1")



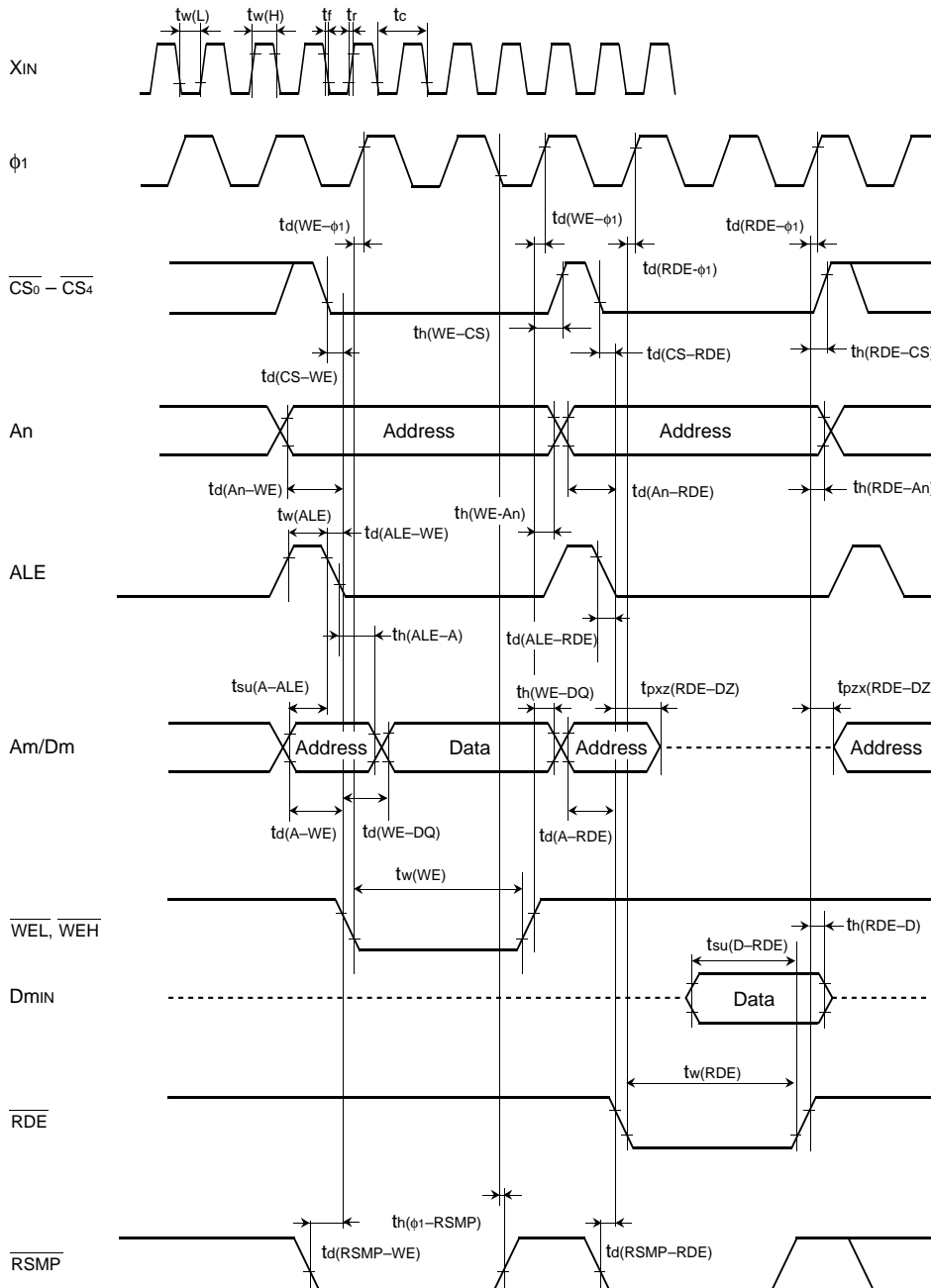
Test conditions

- $V_{CC} = 5 V \pm 10\%$
- Output timing voltage :  $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input Dmin :  $V_{IL} = 0.8 V, V_{IH} = 2.5 V$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(Wait 1 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)



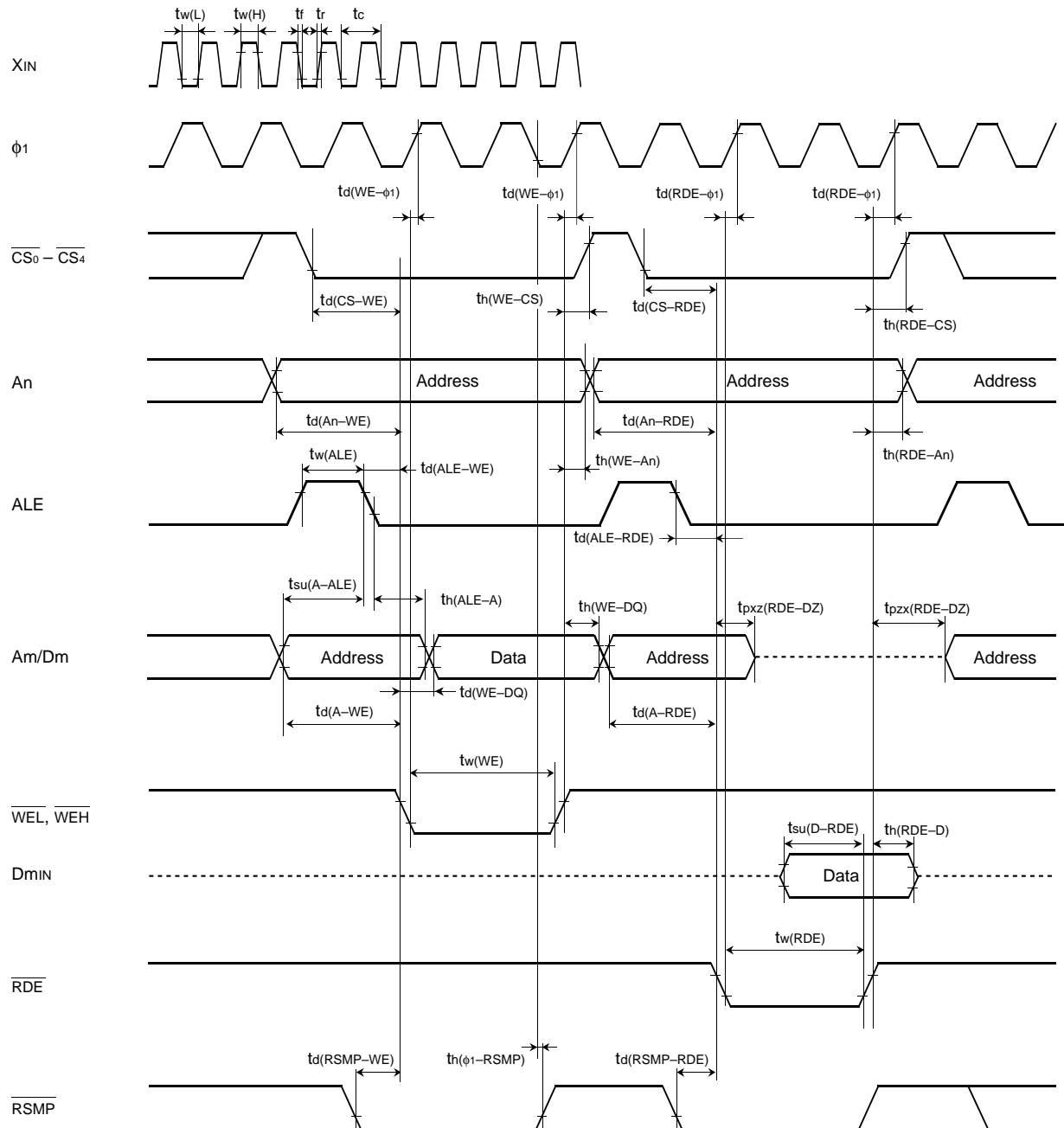
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$
- Data input  $D_{min}$  :  $V_{IL} = 0.8\text{ V}$ ,  $V_{IH} = 2.5\text{ V}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$
- Data input  $\overline{Dmin}$  :  $V_{IL} = 0.8\text{ V}$ ,  $V_{IH} = 2.5\text{ V}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**M37735EHBXXXFP**  
**M37735EHBFS**

PROM VERSION OF M37735MHBXXXFP

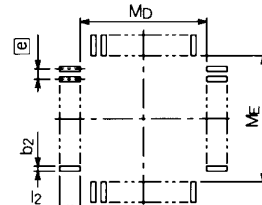
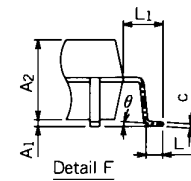
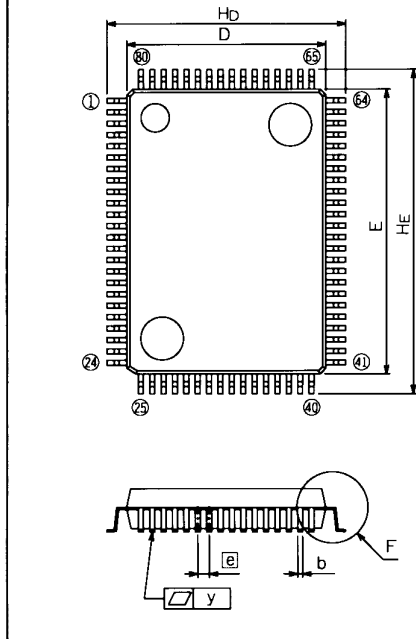
**PACKAGE OUTLINE**

**80P6N-A**

Plastic 80pin 14x20mm body QFP

|                   |            |            |               |
|-------------------|------------|------------|---------------|
| EIAJ Package Code | JEDEC Code | Weight (g) | Lead Material |
| QFP80-P-1420-0.80 | -          | 1.58       | Alloy 42      |

Scale : 2/1



Recommended Mount Pad

| Symbol | Dimension in Millimeters |      |      |
|--------|--------------------------|------|------|
|        | Min                      | Nom  | Max  |
| A      | -                        | -    | 3.05 |
| A1     | 0                        | 0.1  | 0.2  |
| A2     | -                        | 2.8  | -    |
| b      | 0.3                      | 0.35 | 0.45 |
| c      | 0.13                     | 0.15 | 0.2  |
| D      | 13.8                     | 14.0 | 14.2 |
| E      | 19.8                     | 20.0 | 20.2 |
| e      | -                        | 0.8  | -    |
| Hd     | 16.5                     | 16.8 | 17.1 |
| HE     | 22.5                     | 22.8 | 23.1 |
| L      | 0.4                      | 0.6  | 0.8  |
| L1     | -                        | 1.4  | -    |
| y      | -                        | -    | 0.1  |
| theta  | 0°                       | -    | 10°  |
| b2     | -                        | 0.5  | -    |
| l2     | 1.3                      | -    | -    |
| MD     | -                        | 14.6 | -    |
| ME     | -                        | 20.6 | -    |

**7700 FAMILY WRITING TO PROM ORDER CONFIRMATION FORM  
SINGLE-CHIP 16-BIT MICROCOMPUTER  
M37735EHBXXXFP  
MITSUBISHI ELECTRIC**

|            |  |
|------------|--|
| ROM number |  |
|------------|--|

|         |                        |                      |
|---------|------------------------|----------------------|
| Receipt | Date:                  |                      |
|         | Section head signature | Supervisor signature |
|         |                        |                      |

Note : Please fill in all items marked ※

|   |          |              |                              |                     |                     |            |
|---|----------|--------------|------------------------------|---------------------|---------------------|------------|
| ※ | Customer | Company name | TEL (                      ) | Issuance signatures | Responsible officer | Supervisor |
|   |          | Date issued  | Date:                        |                     |                     |            |

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain the identical data, we will produce writing to PROM based on this data. We shall assume the responsibility for errors only if the written PROM data on the products we produce differ from this data.

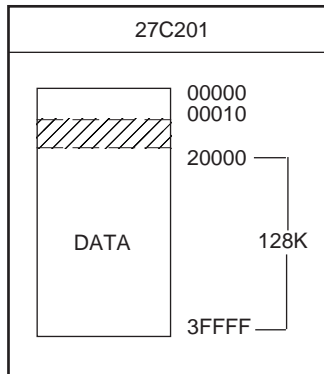
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas 

|  |  |  |  |
|--|--|--|--|
|  |  |  |  |
|--|--|--|--|

 (hexadecimal notation)

EPROM Type :



Note : Make sure that address 01FFFF<sub>16</sub> of the microcomputer's internal ROM corresponds to address 3FFFF<sub>16</sub> of EPROM.

(1) Set "FF<sub>16</sub>" in the shaded area.

(2) Address 0<sub>16</sub> to 0F<sub>16</sub> are the area for storing the data on model designation. This area must be written with the data shown below.

Address and data are written in hexadecimal notation.

| Address |   | Address |   |
|---------|---|---------|---|
| 4D      | 0 | 42      | 8 |
| 33      | 1 | FF      | 9 |
| 37      | 2 | FF      | A |
| 37      | 3 | FF      | B |
| 33      | 4 | FF      | C |
| 35      | 5 | FF      | D |
| 45      | 6 | FF      | E |
| 48      | 7 | FF      | F |

※2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6N Mark Specification Form (for M37735EHBXXXFP) and attach to the Writing to PROM Order Confirmation Form.

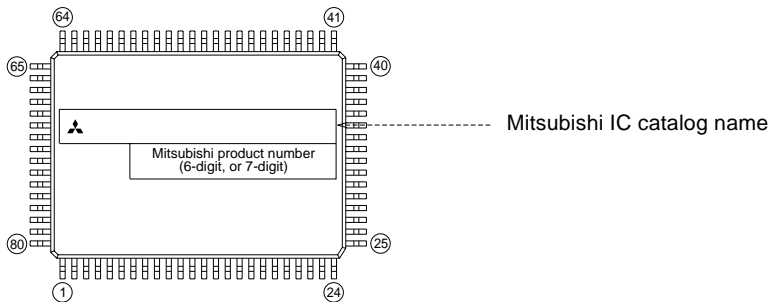
※3. Comments

## 80P6N (80-PIN QFP) MARK SPECIFICATION FORM

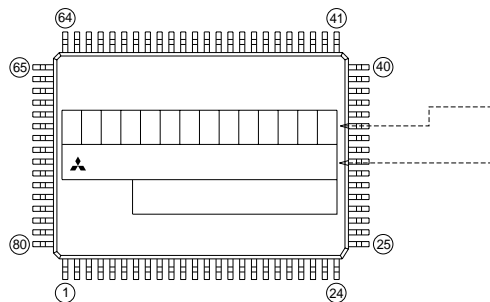
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

### A. Standard Mitsubishi Mark



### B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Notes 1 : The mark field should be written right aligned.

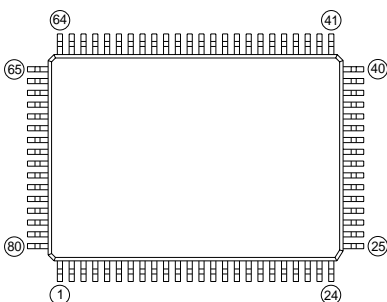
2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's parts number can be up to 14 alphanumeric characters for capital letters, hyphens, commas, periods and so on.

4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

### C. Special Mark Required



Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.

Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.

2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.

For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required



**PRELIMINARY**

Notice: This is not a final specification.  
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

**M37735EHBXXXFP**  
**M37735EHBFS**

PROM VERSION OF M37735MHBXXXFP

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- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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REVISION DESCRIPTION LIST

M37735EBXXXXFP, M37735EBBFS Datasheet

| Rev. No. | Revision Description   |   | Rev. date |   |
|----------|--|---|-----------|---|
| 1.00     | First Edition  |   | 970604    |   |
| 1.01     | The following are added: <ul style="list-style-type: none"> <li>• PROM ORDER CONFIRMATION FORM</li> <li>• MARK SPECIFICATION FORM</li> </ul> |   | 980526    |   |
| 2.00     | The following are revised:   |   | 980731    |   |
|          | Page   | Previous Version  |           | Revised Version   |
|          | P12<br>Right column<br>Line 2  | The M37735EBXXXXFP has 28 powerful addressing modes. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for the details of each addressing mode.<br><br><b>MACHINE INSTRUCTION LIST</b><br>The M37735EBXXXXFP has 103 machine instructions. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for details. |           | The M37735EBXXXXFP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.<br><br><b>MACHINE INSTRUCTION LIST</b><br>The M37735EBXXXXFP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details. |