

## 16.1 Absolute Maximum Ratings

Table 16-1 lists the absolute maximum ratings.

**Table 16-1. Absolute Maximum Ratings (Preliminary)**

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Programming voltage	V <sub>PP</sub>	-0.3 to +13.5	V
Input voltage	Ports 1 – 6, 8, 9	V <sub>in</sub>	-0.3 to V <sub>CC</sub> + 0.3
	Port 7	V <sub>in</sub>	-0.3 to AV <sub>CC</sub> + 0.3
Analog supply voltage	AV <sub>CC</sub>	-0.3 to +7.0	V
Analog input voltage	V <sub>AN</sub>	-0.3 to AV <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	Regular specifications:	-20 to +75 °C
		Wide-range specifications:	-40 to +85 °C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

Note: Exceeding the absolute maximum ratings shown in table 16-1 can permanently destroy the chip.

## 16.2 Electrical Characteristics

### 16.2.1 DC Characteristics

Table 16-2 lists the DC characteristics of the 5V version. Table 16-3 lists the DC characteristics of the 3V version. Table 16-4 gives the allowable current output values of the 5V version.

Table 16-5 gives the allowable current output values of the 3V version.

**Table 16-2. DC Characteristics (5V Version) (Preliminary)**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%*$ ,  $V_{SS} = AV_{SS} = 0V$ ,

$T_a = -20$  to  $75^\circ C$  (regular specifications),  $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Measurement
							conditions
Schmitt trigger input voltage (1)	P67 – P62, P60,	$V_{T^-}$	1.0	–	–	V	
	P86 – P80,	$V_{T^+}$	–	–	$V_{CC} \times 0.7$	V	
	P97, P94 – P90	$V_{T^+} - V_{T^-}$	0.4	–	–	V	
Input High voltage (2)	$\overline{RES}$ , $\overline{STBY}$ , $\overline{NMI}$	$V_{IH}$	$V_{CC} - 0.7$	–	$V_{CC} + 0.3$	V	
	MD1, MD0						
	$\overline{EXTAL}$						
	P77 – P70		2.0	–	$AV_{CC} + 0.3$	V	
Input High voltage	Input pins other than (1) and (2)	$V_{IH}$	2.0	–	$V_{CC} + 0.3$	V	
Input Low voltage (3)	$\overline{RES}$ , $\overline{STBY}$	$V_{IL}$	–0.3	–	0.5	V	
	MD1, MD0						
Input Low voltage	Input pins other than (1) and (3) above	$V_{IL}$	–0.3	–	0.8	V	
Output High voltage	All output pins	$V_{OH}$	$V_{CC} - 0.5$	–	–	V	$I_{OH} = -200\mu A$
			3.5	–	–	V	$I_{OH} = -1.0mA$
Output Low voltage	All output pins Ports 1 and 2	$V_{OL}$	–	–	0.4	V	$I_{OL} = 1.6mA$
			–	–	1.0	V	$I_{OL} = 10.0mA$
Input leakage current	$\overline{RES}$	$I_{inl}$	–	–	10.0	$\mu A$	$V_{in} = 0.5V$ to $V_{CC} - 0.5V$
	$\overline{STBY}$ , $\overline{NMI}$ ,		–	–	1.0	$\mu A$	
	MD1, MD0						
	P77 – P70		–	–	1.0	$\mu A$	$V_{in} = 0.5V$ to $AV_{CC} - 0.5V$
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9	$I_{Tstl}$	–	–	1.0	$\mu A$	$V_{in} = 0.5V$ to $V_{CC} - 0.5V$
Input pull-up MOS current	Ports 1, 2, 3	$-I_p$	30	–	250	$\mu A$	$V_{in} = 0V$

Note: \* Connect  $AV_{CC}$  to the power supply (+5V) even when the A/D and D/A converters are not used.

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**Table 16-2. DC Characteristics (5V Version) (cont.)**

Conditions:  $V_{CC} = AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_a = -20$  to  $75^\circ C$  (regular specifications)  
 $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$ (VPP)	$C_{in}$	–	–	60	pF	$V_{in} = 0V$
	$\overline{NMI}$		–	–	30	pF	$f = 1MHz$
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	$T_a = 25^\circ C$
Current dissipation*1	Normal operation	$I_{cc}$	–	12	25	mA	$f = 6MHz$
			–	16	30	mA	$f = 8MHz$
			–	20	40	mA	$f = 10MHz$
	Sleep mode		–	8	15	mA	$f = 6MHz$
			–	10	20	mA	$f = 8MHz$
			–	12	25	mA	$f = 10MHz$
Analog supply current	During A/D or D/A conversion	$A_{Icc}$	–	2.0	5.0	mA	
	Waiting		–	0.01	5.0	$\mu A$	
RAM standby voltage		$V_{RAM}$	2.0	–	–	V	

Notes: \*1 Current dissipation values assume that  $V_{IH\ min} = V_{CC} - 0.5V$ ,  $V_{IL\ max} = 0.5V$ , all output pins are in the no-load state, and all input pull-up transistors are off.

\*2 For these values it is assumed that  $V_{RAM} \leq V_{CC} < 4.5V$  and  $V_{IH\ min} = V_{CC} \times 0.9$ ,  $V_{IL\ max} = 0.3V$ .

**Table 16-3. DC Characteristics (3V Version) (preliminary)**

 Conditions:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%^{*1}$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_a = -20$  to  $70^{\circ}C$ 

Item	Symbol	Min	Typ	Max	Unit	Measurement conditions	
Schmitt trigger input voltage*2 (1)	P67 – P62, P60, $V_{T-}$	$V_{CC} \times 0.15$	–	–	V		
	P86 – P80, $V_{T+}$	–	–	$V_{CC} \times 0.7$	V		
	P97, P94 – P90 $V_{T+} - V_{T-}$	0.2	–	–	V		
Input High voltage*2 (2)	$\overline{RES}$ , $\overline{STBY}$	$V_{CC} \times 0.9$	–	$V_{CC} + 0.3$	V		
	MD1, MD0						
	$\overline{EXTAL}$ , $\overline{NMI}$						
	P77 – P70	$V_{CC} \times 0.7$	–	$AV_{CC} + 0.3$	V		
Input pins other than (1) and (2) above		$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V		
Input Low voltage*2 (3)	$\overline{RES}$ , $\overline{STBY}$	$V_{IL}$	–0.3	–	$V_{CC} \times 0.1$	V	
	MD1, MD0						
	Input pins other than (1) and (3) above		–0.3	–	$V_{CC} \times 0.15$	V	
Output High voltage	All output pins	$V_{OH}$	$V_{CC} - 0.4$	–	–	V	$I_{OH} = -200\mu A$
			$V_{CC} - 0.9$	–	–	V	$I_{OH} = -1.0mA$
Output Low voltage	All output pins Ports 1 and 2	$V_{OL}$	–	–	0.4	V	$I_{OL} = 0.8mA$
			–	–	0.4	V	$I_{OL} = 1.6mA$
Input leakage current	$\overline{RES}$	$I_{inl}$	–	–	10.0	$\mu A$	$V_{in} = 0.5$ to
	$\overline{STBY}$ , $\overline{NMI}$ , MD1, MD0		–	–	1.0	$\mu A$	$V_{CC} - 0.5V$
	P77 – P70		–	–	1.0	$\mu A$	$V_{in} = 0.5$ to $AV_{CC} - 0.5V$
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9	$ I_{TSI} $	–	–	1.0	$\mu A$	$V_{in} = 0.5$ to $V_{CC} - 0.5V$
Input pull-up MOS current	Ports 1, 2, 3	$-I_p$	3	–	120	$\mu A$	$V_{in} = 5.0V$

 Notes: \*1 Connect  $AV_{CC}$  to the power supply (+3V) even when the A/D converter is not used.

 \*2 In the range  $3.3V < V_{CC} < 4.5V$ , for the input levels of  $V_{IH}$  and  $V_{T+}$ , apply the higher of the values given for the 5V and 3V versions. For  $V_{IL}$  and  $V_{T-}$ , apply the lower of the values given for the 5V and 3V versions.

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**Table 16-3. DC Characteristics (3V Version) (preliminary) (cont.)**

Conditions:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ \*1,  $V_{SS} = AV_{SS} = 0V$ ,  $T_a = -20$  to  $70^\circ C$

Item		Symbol	Min	Typ	Max	Unit	Measurement conditions
Input capacitance	RES	$C_{in}$	–	–	60	pF	$V_{in} = 0V$
	NMI		–	–	30	pF	$f = 1MHz$
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	$T_a = 25^\circ C$
Current dissipation*1	Normal operation	$I_{CC}$	–	6	–	mA	$f = 3MHz$
			–	10	20	mA	$f = 5MHz$
	Sleep mode		–	4	–	mA	$f = 3MHz$
			–	6	12	mA	$f = 5MHz$
			Standby modes*2	–	0.01	5.0	$\mu A$
Analog supply current	During A/D or D/A conversion	$A_{I_{CC}}$	–	2.0	5.0	mA	
	Waiting		–	0.01	5.0	$\mu A$	
RAM backup voltage (in standby modes)		$V_{RAM}$	2.0	–	–	V	

Notes: \*1 Current dissipation values assume that  $V_{IH\ min} = V_{CC} - 0.5V$ ,  $V_{IL\ max} = 0.5V$ , all output pins are in the no-load state, and all input pull-up transistors are off.

\*2 For these values it is assumed that  $V_{RAM} \leq V_{CC} < 2.7V$  and  $V_{IH\ min} = V_{CC} \times 0.9$ ,  $V_{IL\ max} = 0.3V$ .

**Table 16-4. Allowable Output Current Sink Values (5V Version) (Preliminary)**

Conditions:  $V_{CC} = AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_a = -20$  to  $75^\circ C$  (regular specifications)  
 $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

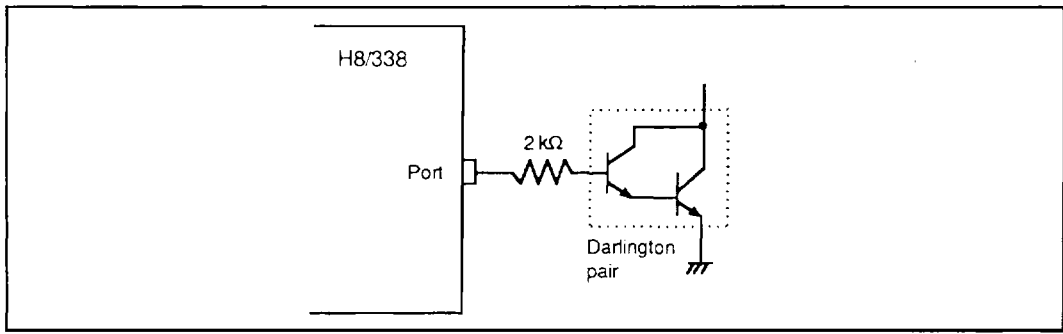
Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	IOL	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	$\Sigma IOL$	–	–	80	mA
	Total of all output		–	–	120	mA
Allowable output High current sink (per pin)	All output pins	–IOH	–	–	2.0	mA
Allowable output High current sink (total)	Total of all output	$\Sigma -IOH$	–	–	40	mA

**Table 16-5. Allowable Output Current Sink Values (3V Version) (Preliminary)**

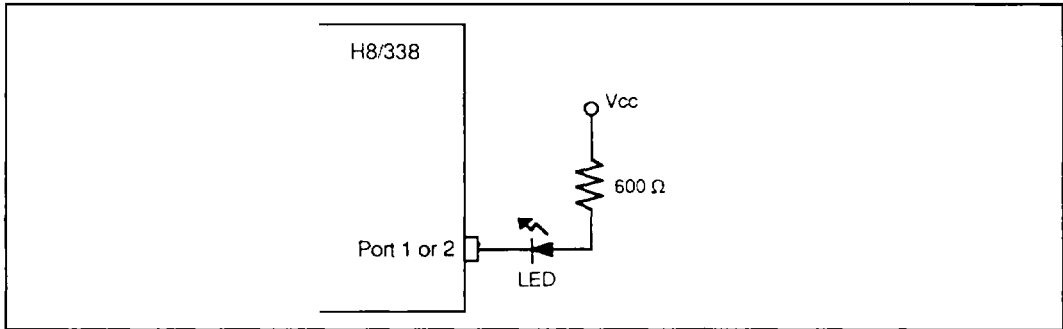
Conditions:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_a = -20$  to  $75^\circ C$

Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	IOL	–	–	2	mA
	Other output pins		–	–	1	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	$\Sigma IOL$	–	–	40	mA
	Total of all output		–	–	60	mA
Allowable output High current sink (per pin)	All output pins	–IOH	–	–	2	mA
Allowable output High current sink (total)	Total of all output	$\Sigma -IOH$	–	–	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in tables 16-4 and 16-5. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 16-1 and 16-2.



**Figure 16-1. Example of Circuit for Driving a Darlington Pair (5V Version)**



**Figure 16-2. Example of Circuit for Driving an LED (5V Version)**

## 16.2.2 AC Characteristics

The AC characteristics are listed in three tables. Bus timing parameters are given in table 16-6, control signal timing parameters in table 16-7, and timing parameters of the on-chip supporting modules in table 16-8.

**Table 16-6. Bus Timing (Preliminary)**

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5MHz$  to maximum operating frequency,  
 $T_a = -20$  to  $75^\circ C$  (regular specifications),  
 $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5MHz$  to maximum operating frequency,  
 $T_a = -20$  to  $75^\circ C$

Item	Symbol	Condition B		Condition A				Unit	Measurement conditions		
		5MHz	6MHz	8MHz	10MHz	Min	Max				
Clock cycle time	$t_{cyc}$	200	2000	166.7	2000	125	2000	100	2000	ns	Fig. 16-4
Clock pulse width Low	$t_{CL}$	70	-	65	-	45	-	35	-	ns	Fig. 16-4
Clock pulse width High	$t_{CH}$	70	-	65	-	45	-	35	-	ns	Fig. 16-4
Clock rise time	$t_{Cr}$	-	25	-	15	-	15	-	15	ns	Fig. 16-4
Clock fall time	$t_{Cf}$	-	25	-	15	-	15	-	15	ns	Fig. 16-4
Address delay time	$t_{AD}$	-	90	-	70	-	60	-	50	ns	Fig. 16-4
Address hold time	$t_{AH}$	30	-	30	-	25	-	20	-	ns	Fig. 16-4
Address strobe delay time	$t_{ASD}$	-	80	-	70	-	60	-	40	ns	Fig. 16-4
Write strobe delay time	$t_{WSD}$	-	80	-	70	-	60	-	50	ns	Fig. 16-4
Strobe delay time	$t_{SD}$	-	90	-	70	-	60	-	50	ns	Fig. 16-4
Write strobe pulse width*	$t_{WSW}$	200	-	200	-	150	-	120	-	ns	Fig. 16-4
Address setup time 1*	$t_{AS1}$	25	-	25	-	20	-	15	-	ns	Fig. 16-4
Address setup time 2*	$t_{AS2}$	105	-	105	-	80	-	65	-	ns	Fig. 16-4
Read data setup time	$t_{RDS}$	90	-	70	-	50	-	35	-	ns	Fig. 16-4
Read data hold time*	$t_{RDH}$	0	-	0	-	0	-	0	-	ns	Fig. 16-4
Read data access time*	$t_{ACC}$	-	300	-	270	-	210	-	170	ns	Fig. 16-4
Write data delay time	$t_{WDD}$	-	125	-	85	-	75	-	75	ns	Fig. 16-4
Write data setup time	$t_{WDS}$	10	-	20	-	10	-	5	-	ns	Fig. 16-4
Write data hold time	$t_{WDH}$	30	-	30	-	25	-	20	-	ns	Fig. 16-4
Wait setup time	$t_{WTS}$	60	-	40	-	40	-	40	-	ns	Fig. 16-5
Wait hold time	$t_{WTH}$	20	-	10	-	10	-	10	-	ns	Fig. 16-5

Note: \* Values at maximum operating frequency



**Table 16-7. Control Signal Timing (Preliminary)**

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5MHz$  to maximum operating frequency,

$T_a = -20$  to  $75^\circ C$  (regular specifications),

$T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5MHz$  to maximum operating frequency,

$T_a = -20$  to  $75^\circ C$

Item	Symbol	Condition B		Condition A				Measurement Unit conditions			
		5MHz		6MHz		8MHz			10MHz		
		Min	Max	Min	Max	Min	Max		Min	Max	
RES setup time	t <sub>RESS</sub>	300	-	200	-	200	-	200	-	ns	Fig. 16-6
RES pulse width	t <sub>RESW</sub>	10	-	10	-	10	-	10	-	tcyc	Fig. 16-6
NMI setup time ( $\overline{NMI}$ , $\overline{IRQ_0}$ to $\overline{IRQ_7}$ )	t <sub>NMIS</sub>	300	-	150	-	150	-	150	-	ns	Fig. 16-7
NMI hold time ( $\overline{NMI}$ , $\overline{IRQ_0}$ to $\overline{IRQ_7}$ )	t <sub>NMIH</sub>	10	-	10	-	10	-	10	-	ns	Fig. 16-7
Interrupt pulse width for recovery from software standby mode ( $\overline{NMI}$ , $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	t <sub>NMIW</sub>	300	-	200	-	200	-	200	-	ns	Fig. 16-7
Crystal oscillator settling time (reset)	t <sub>OSC1</sub>	20	-	20	-	20	-	20	-	ms	Fig. 16-8
Crystal oscillator settling time (software standby)	t <sub>OSC2</sub>	10	-	10	-	10	-	10	-	ms	Fig. 16-9

**Table 16-8. Timing Conditions of On-Chip Supporting Modules (Preliminary)**

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5MHz$  to maximum operating frequency,  
 $T_a = -20$  to  $75^\circ C$  (regular specifications),  
 $T_a = -40$  to  $85^\circ C$  (wide-range specifications)  
 Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5MHz$  to maximum operating frequency,  
 $T_a = -20$  to  $75^\circ C$

Item	Symbol	Condition B		Condition A				Unit	Measurement conditions			
		Min	Max	Min	Max	Min	Max					
FRT	Timer output delay time	tFOD	-	150	-	100	-	100	-	100	ns	Fig. 16-10
	Timer input setup time	tFIS	80	-	50	-	50	-	50	-	ns	Fig. 16-10
	Timer clock input setup time	tFICS	80	-	50	-	50	-	50	-	ns	Fig. 16-11
	Timer clockpulse width	tFTCWH tFTCWL	1.5	-	1.5	-	1.5	-	1.5	-	t <sub>cy</sub>	Fig. 16-11
TMR	Timer output delay time	tTOD	-	150	-	100	-	100	-	100	ns	Fig. 16-12
	Timer reset input setup time	tTMRs	80	-	50	-	50	-	50	-	ns	Fig. 16-14
	Timer clock input setup time	tTMCs	80	-	50	-	50	-	50	-	ns	Fig. 16-13
	Timer clock pulse width (single edge)	tTMCWH	1.5	-	1.5	-	1.5	-	1.5	-	t <sub>cy</sub>	Fig. 16-13
	Timer clock pulse width (both edges)	tTMCWL	2.5	-	2.5	-	2.5	-	2.5	-	t <sub>cy</sub>	Fig. 16-13
PWM	Timer output delay time	tPWOD	-	150	-	100	-	100	-	100	ns	Fig. 16-15
SCI	Input clock cycle (Async)	t <sub>cy</sub>	2	-	2	-	2	-	2	-	t <sub>cy</sub>	Fig. 16-16
	Input clock cycle (Sync)	t <sub>cy</sub>	6	-	6	-	6	-	6	-	t <sub>cy</sub>	Fig. 16-16
	Transmit data delay time (Sync)	tTXD	-	200	-	100	-	100	-	100	ns	Fig. 16-16
	Receive data setup time (Sync)	tRXS	150	-	100	-	100	-	100	-	ns	Fig. 16-16
	Receive data hold time (Sync)	tRXH	150	-	100	-	100	-	100	-	ns	Fig. 16-16
	Input clock pulse width	tSCKW	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>cy</sub>	Fig. 16-17
Ports	Output data delay time	tPWD	-	150	-	100	-	100	-	100	ns	Fig. 16-18
	Input data setup time	tPRS	80	-	50	-	50	-	50	-	ns	Fig. 16-18
	Input data hold time	tPRH	80	-	50	-	50	-	50	-	ns	Fig. 16-18

• Measurement Conditions for AC Characteristics

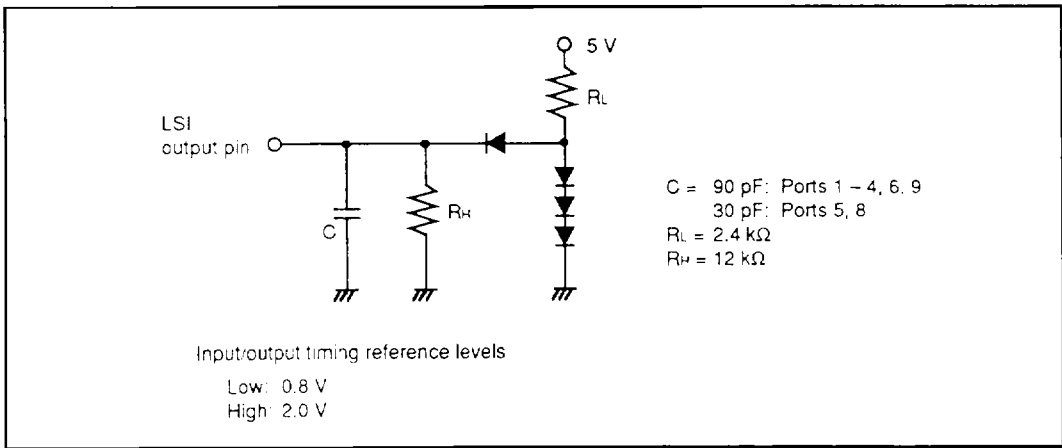


Figure 16-3. Output Load Circuit

16.2.3 A/D Converter Characteristics

Table 16-9 lists the characteristics of the on-chip A/D converter.

Table 16-9. A/D Converter Characteristics (Preliminary)

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $\emptyset = 0.5\text{MHz}$  to maximum operating frequency,  $T_a = -20$  to  $75^\circ\text{C}$  (regular specifications),

$T_a = -40$  to  $85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $\emptyset = 0.5\text{MHz}$  to maximum operating frequency,  $T_a = -20$  to  $75^\circ\text{C}$

Item	Condition B			Condition A								Unit	
	5MHz			6MHz			8MHz			10MHz			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ		Max
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)*	---	---	24.4	---	---	20.4	---	---	15.25	---	---	12.2	$\mu\text{s}$
Analog input capacitance	---	---	20	---	---	20	---	---	20	---	---	20	pF
Allowable signal source impedance	---	---	10	---	---	10	---	---	10	---	---	10	k $\Omega$
Nonlinearity error	---	---	$\pm 1$	---	---	$\pm 1$	---	---	$\pm 1$	---	---	$\pm 1$	LSB
Offset error	---	---	$\pm 1$	---	---	$\pm 1$	---	---	$\pm 1$	---	---	$\pm 1$	LSB
Full-scale error	---	---	$\pm 1$	---	---	$\pm 1$	---	---	$\pm 1$	---	---	$\pm 1$	LSB
Quantizing error	---	---	$\pm 0.5$	---	---	$\pm 0.5$	---	---	$\pm 0.5$	---	---	$\pm 0.5$	LSB
Absolute accuracy	---	---	$\pm 1.5$	---	---	$\pm 1.5$	---	---	$\pm 1.5$	---	---	$\pm 1.5$	LSB

Note: \* Values at maximum operating frequency

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## 16.2.4 D/A Converter Characteristics

Table 16-10 lists the characteristics of the on-chip D/A converter.

**Table 16-10. D/A Converter Characteristics**

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $\emptyset = 0.5MHz$  to maximum operating frequency,  $T_a = -20$  to  $75^\circ C$  (regular specifications),

$T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $\emptyset = 0.5MHz$  to maximum operating frequency,  $T_a = -20$  to  $75^\circ C$

Item	Condition B			Condition A								Unit	Measurement conditions	
	5MHz			6MHz			8MHz			10MHz				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ			Max
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits	
Conversion time	—	—	10.0	—	—	10.0	—	—	10.0	—	—	10.0	$\mu s$	30pF load capacitance
Absolute accuracy	—	$\pm 1$	$\pm 1.5$	—	$\pm 1$	$\pm 1.5$	—	$\pm 1$	$\pm 1.5$	—	$\pm 1$	$\pm 1.5$	LSB	2M $\Omega$ load resistance
	—	—	$\pm 1$	—	—	$\pm 1$	—	—	$\pm 1$	—	—	$\pm 1$	LSB	4M $\Omega$ load resistance

## 16.3 MCU Operational Timing

This section provides the following timing charts:

16.3.1 Bus Timing	Figures 16-4 to 16-5
16.3.2 Control Signal Timing	Figures 16-6 to 16-9
16.3.3 16-Bit Free-Running Timer Timing	Figures 16-10 to 16-11
16.3.4 8-Bit Timer Timing	Figures 16-12 to 16-14
16.3.5 PWM Timer Timing	Figure 16-15
16.3.6 SCI Timing	Figures 16-16 to 16-17
16.3.7 I/O Port Timing	Figure 16-18

### 16.3.1 Bus Timing

#### (1) Basic Bus Cycle (without Wait States) in Expanded Modes

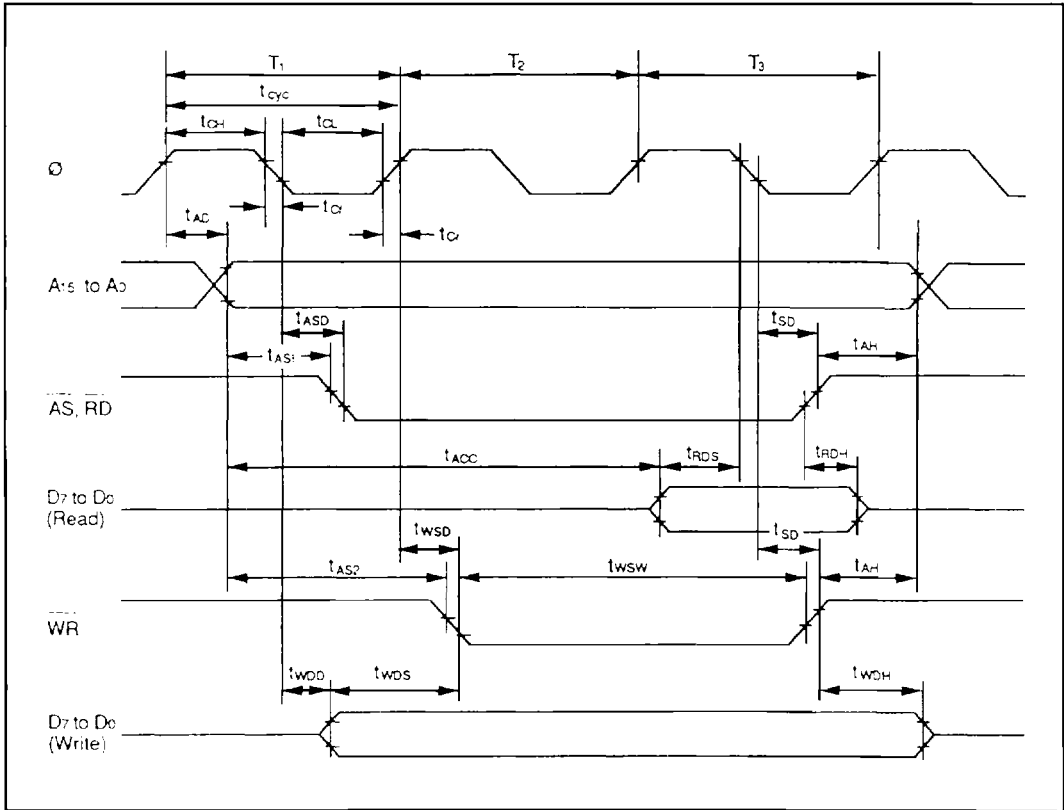
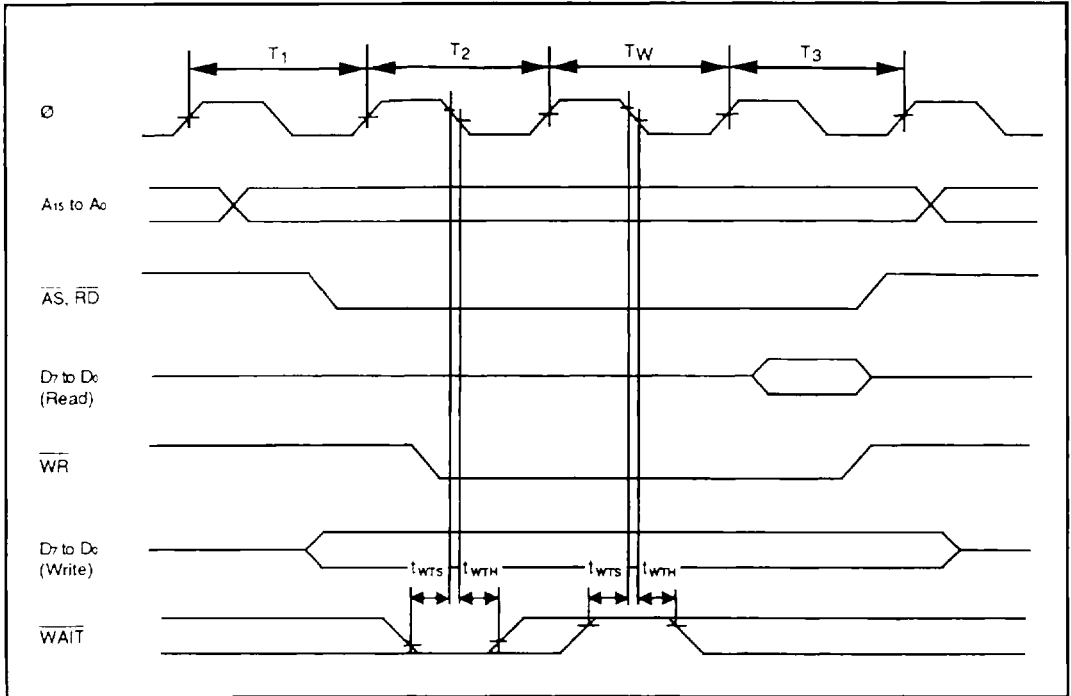


Figure 16-4. Basic Bus Cycle (without Wait States) in Expanded Modes

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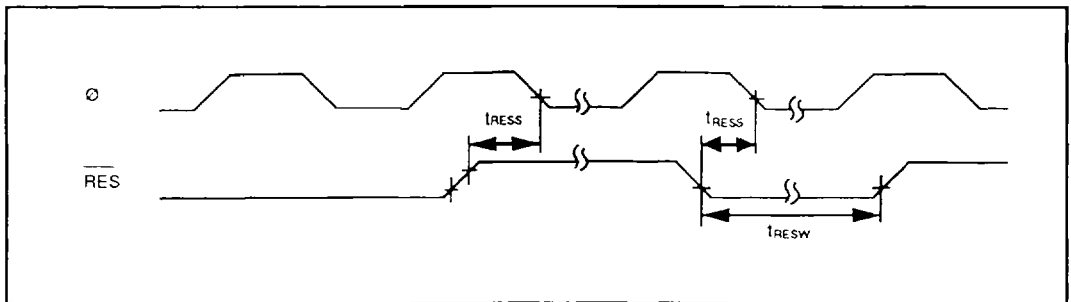
**(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes**



**Figure 16-5. Basic Bus Cycle (with 1 Wait State) in Expanded Modes**

**16.3.2 Control Signal Timing**

**(1) Reset Input Timing**



**Figure 16-6. Reset Input Timing**

## (2) Interrupt Input Timing

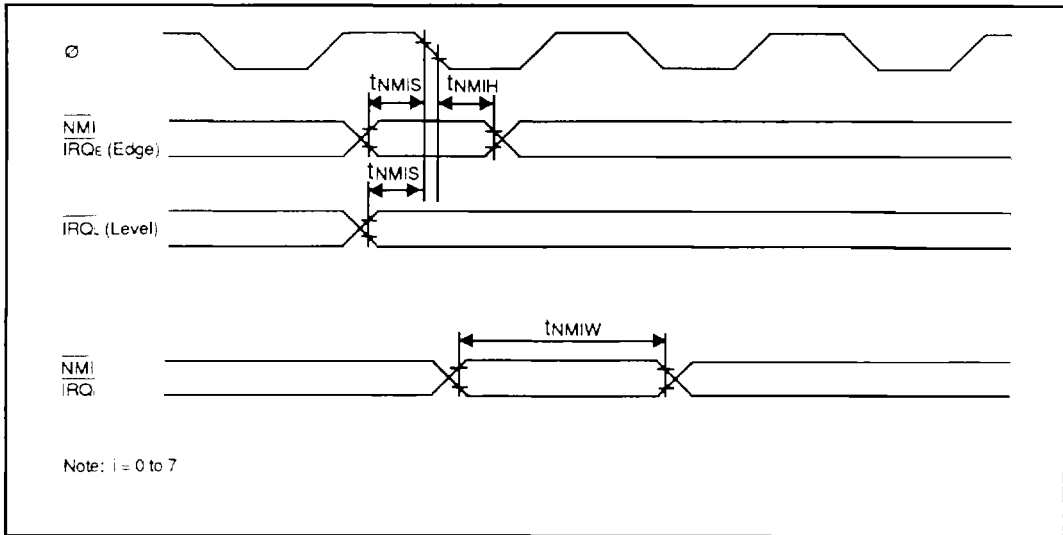


Figure 16-7. Interrupt Input Timing

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### (3) Clock Settling Timing

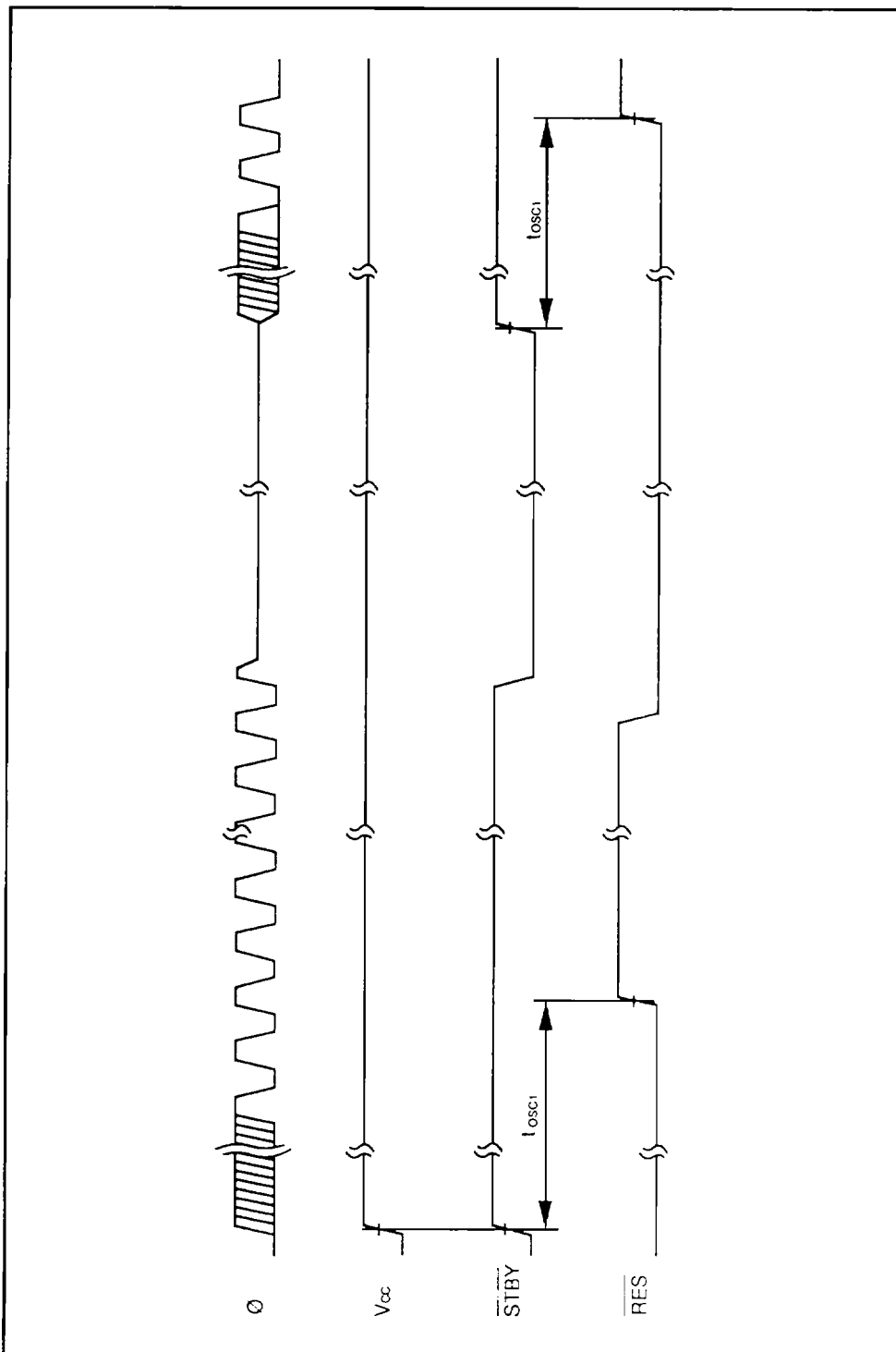
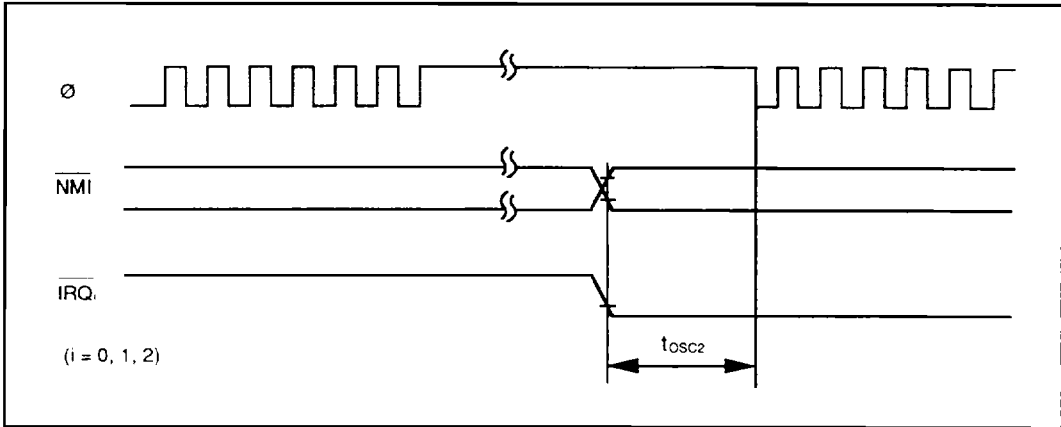


Figure 16-8. Clock Settling Timing



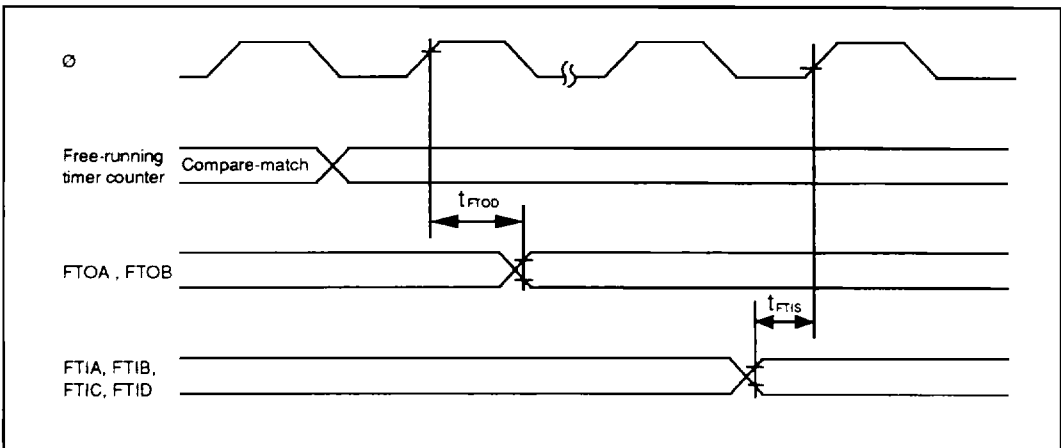
**(4) Clock Settling Timing for Recovery from Software Standby Mode**



**Figure 16-9. Clock Settling Timing for Recovery from Software Standby Mode**

**16.3.3 16-Bit Free-Running Timer Timing**

**(1) Free-Running Timer Input/Output Timing**



**Figure 16-10. Free-Running Timer Input/Output Timing**

(2) External Clock Input Timing for Free-Running Timer

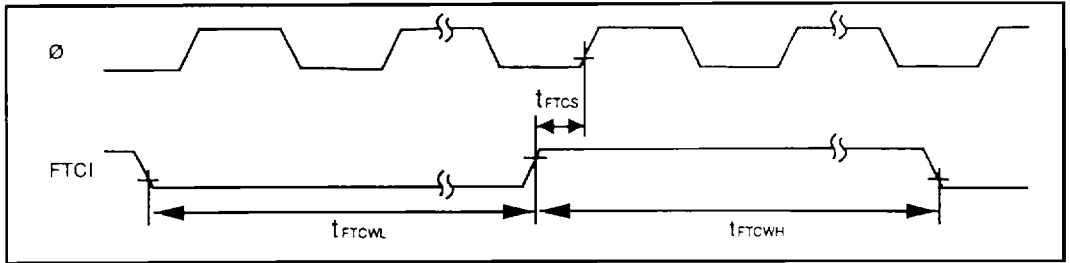


Figure 16-11. External Clock Input Timing for Free-Running Timer

16.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

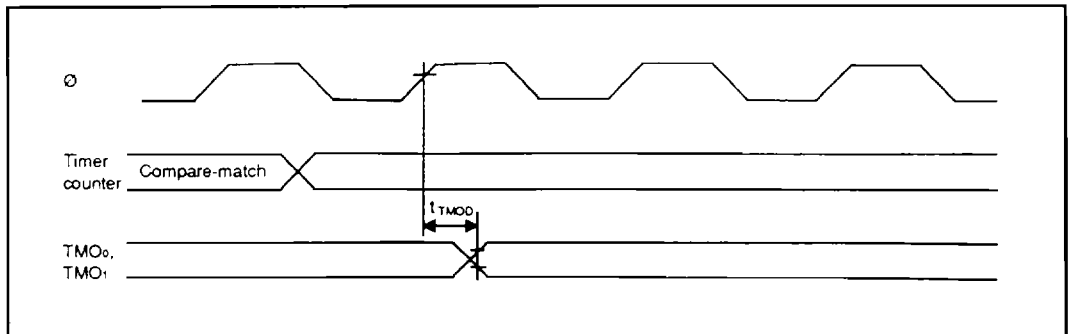


Figure 16-12. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

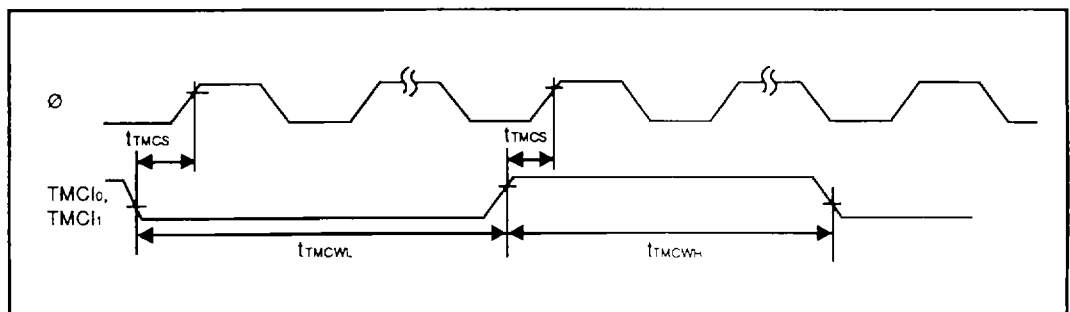


Figure 16-13. 8-Bit Timer Clock Input Timing

### (3) 8-Bit Timer Reset Input Timing

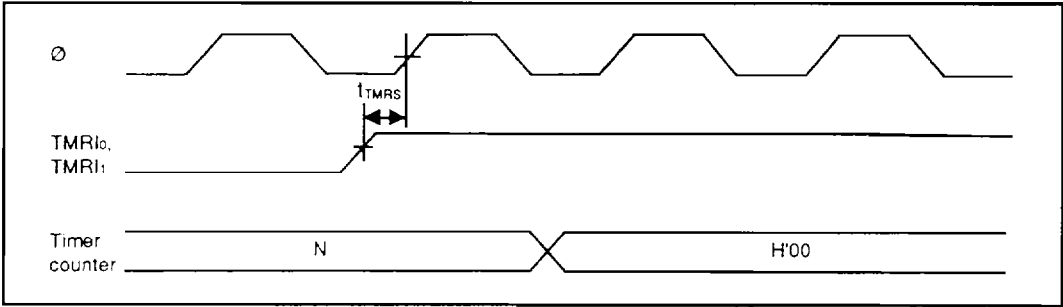


Figure 16-14. 8-Bit Timer Reset Input Timing

### 16.3.5 Pulse Width Modulation Timer Timing

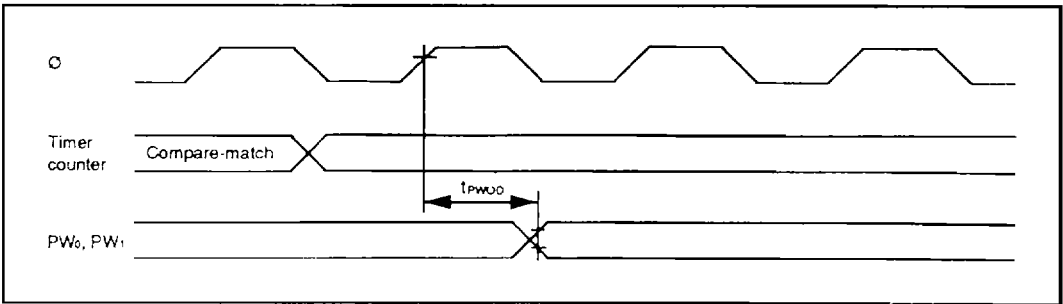


Figure 16-15. PWM Timer Output Timing

### 16.3.6 Serial Communication Interface Timing

#### (1) SCI Input/Output Timing

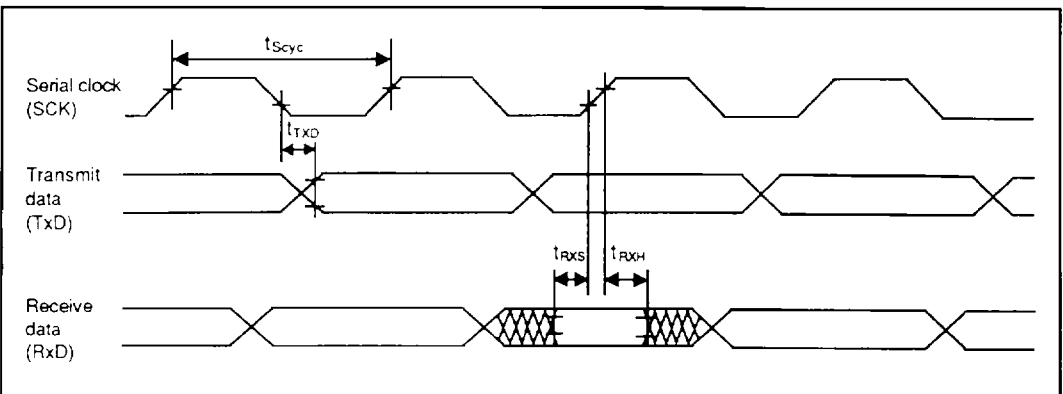


Figure 16-16. SCI Input/Output Timing (Synchronous Mode)

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## (2) SCI Input Clock Timing

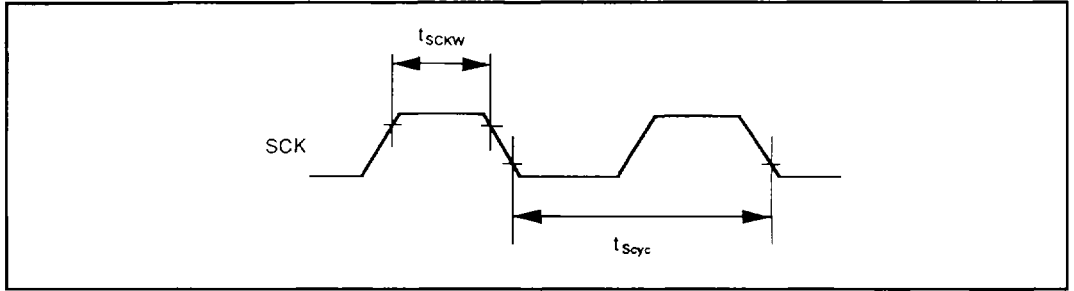


Figure 16-17. SCI Input Clock Timing

## 16.3.7 I/O Port Timing

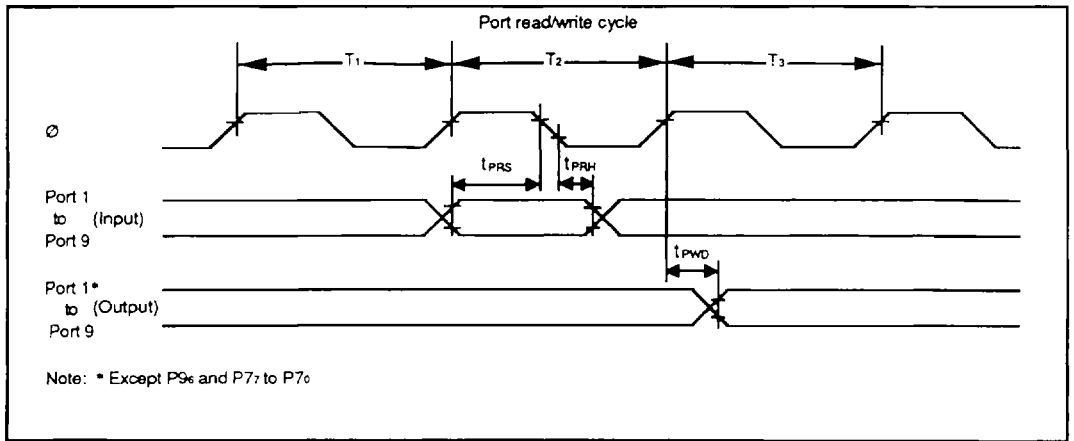


Figure 16-18. I/O Port Input/Output Timing