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PowerPC™

Advance Information

MPC860 Family Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC860 family. These same specifications also apply to the MPC860P. In this document, the term 'MPC860' generally refers to all MPC860 family members including the MPC860P.

This document contains the following topics:

MOTOROLA

1.1 Overview

The MPC860 PowerPC™ Quad Integrated Communications Controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in both communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this manual.

The MPC860 is a PowerPC architecture-based derivative of Motorola's MC68360 Quad Integrated Communications Controller (QUICC™), referred to here as the QUICC. The CPU on the MPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller (I^2C) channel. Digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

1.2 Features

The following list summarizes the key MPC860 features:

- Embedded PowerPC core
- Single-issue, 32-bit version of the core (compatible the PowerPC architecture definition) with 32, 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4-Kbyte data cache and 4-Kbyte instruction cache
  - Instruction and data caches are two-way, set-associative, physical address, least recently used (LRU) replacement, lockable on-line granularity
  - MMUs with 32 entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Complete static design (0–40 MHz operation)
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROM, flash EPROM, and other memory devices.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)

  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - PowerPC decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 5 Kbytes of dual-port RAM
  - 16 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- On-chip 16x16 multiply accumulate controller (MAC)
  - One operation per clock (two clock latency, one clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop: four clocks per four multiplies
- Four baud-rate generators (BRGs)
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- Four serial communications controllers (SCCs)

  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation (Available only on specially programmed devices)
  - HDLC/SDLC (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^2C (inter-integrated circuit) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, clocking
  - Allows dynamic changes
  - Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported

- Low power support
  - Full on—All units fully powered
  - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—All units disabled except RTC and PIT, PLL active for fast wake up
  - Deep sleep—All units disabled including PLL except RTC and PIT
  - Power down mode— All units powered down except PLL, RTC, PIT, time base and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watch-point can generate a break-point internally
- 3.3 V operation with 5-V TTL compatibility
- 357-pin ball grid array (BGA) package

1.3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC860. Table 4 provides the maximum ratings.

Table 4. Maximum Ratings

(GND = 0V)

Rating	Symbol	Value	Unit
Supply voltage[1]	VDDH	-0.3 to 4.0	V
	VDDL	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input voltage[2]	V_{in}	GND-0.3 to VDDH + 2.5V	V
Temperature [3] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature [3] (extended)	$T_{A(min)}$	-40	°C
	$T_{j(max)}$	95	°C
Storage temperature range	T_{stg}	-55 to +150	°C

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 7. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

[3] Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused

inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}). Table 5 provides the package thermal characteristics for the MPC860.

1.4 Thermal Characteristics

Table 5 shows the thermal characteristics for the MPC860.

Table 5. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA[1]	θ_{JA}	47[2]	°C/W
	θ_{JA}	30[3]	°C/W
	θ_{JA}	15[4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	4.9	°C/W

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, *Plastic Ball Grid Array Application Note* available from your local Motorola sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias, 1-W MPC860 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias,1-W MPC860 dissipation, and a board temperature rise of 10°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins.

Table 6 provides power dissipation information.

Table 6. Power Dissipation (P_D)

Die Revision	Frequency	Typical[1]	Maximum[2]	Unit
A.3 and previous	25 MHz	450	550	mW
	40 MHz	700	850	mW
	50 MHz	870	1050	mW
B.1 and later	33 MHz	375	TBD	mW
	50 MHz	575	TBD	mW
	66 MHz	750	TBD	mW

[1] Maximum power dissipation is measured at 3.65V.

[2] Typical power dissipation is measured at 3.3V.

Table 7 provides the DC electrical characteristics for the MPC860.

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, VDDSYN	3.0	3.6	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH - 0.4	VDDH	V

Table 7. DC Electrical Specifications (Continued)

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH - 0.4	VDDH	V
Input High Voltage (all inputs except EXTAL and EXTCLK)	VIH	2.0	5.5	V
Input Low Voltage	VIL	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input Leakage Current, Vin = 5.5V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{in}	—	100	μA
Input Leakage Current, Vin = 3.6V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	μA
Input Leakage Current, Vin = 0V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{In}	—	10	μA
Input Capacitance	C_{in}	—	20	pF
Output High Voltage, IOH = -2.0 mA, VDDH = 3.0V Except XTAL, XFC, and Open drain pins	VOH	2.4	—	V
Output Low Voltage IOL = 2.0 mA CLKOUT IOL = 3.2 mA[1] IOL = 5.3 mA[2] IOL = 7.0 mA TXD1/PA14, TXD2/PA12 IOL = 8.9 mA $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	VOL	—	0.5	V

[1] A(0:31), TSIZ0/$\overline{\text{REG}}$, TSIZ1, D(0:31), DP(0:3)/$\overline{\text{IRQ}}$(3:6), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, $\overline{\text{RSV}}$/$\overline{\text{IRQ2}}$, IP_B(0:1)/IWP(0:1)/ VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/ PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/ BRGO1/CLK1/PA7, BRGCLK1/$\overline{\text{TOUT1}}$/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{\text{TOUT2}}$/CLK4/PA4, TIN3/ BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/$\overline{\text{TOUT3}}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/$\overline{\text{TOUT4}}$/CLK8/PA0, $\overline{\text{REJCT1}}$/$\overline{\text{SPISEL}}$/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/ I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/$\overline{\text{SDACK1}}$/PB23, $\overline{\text{SMSYN2}}$/$\overline{\text{SDACK2}}$/PB22, SMTXD2/ L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/$\overline{\text{RTS1}}$/PB19, L1ST2/$\overline{\text{RTS2}}$/PB18, L1ST3/$\overline{\text{L1RQB}}$/PB17, L1ST4/ $\overline{\text{L1RQA}}$/PB16, BRGO3/PB15, $\overline{\text{RSTRT1}}$/PB14, L1ST1/$\overline{\text{RTS1}}$/$\overline{\text{DREQ0}}$/PC15, L1ST2/$\overline{\text{RTS2}}$/$\overline{\text{DREQ1}}$/PC14, L1ST3/ $\overline{\text{L1RQB}}$/PC13, L1ST4/$\overline{\text{L1RQA}}$/PC12, $\overline{\text{CTS1}}$/PC11, $\overline{\text{TGATE1}}$/$\overline{\text{CD1}}$/PC10, $\overline{\text{CTS2}}$/PC9, $\overline{\text{TGATE2}}$/$\overline{\text{CD2}}$/PC8, $\overline{\text{SDACK2}}$/ L1TSYNCB/PC7, L1RSYNCB/PC6, $\overline{\text{SDACK1}}$/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3

[2] $\overline{\text{BDIP}}$/$\overline{\text{GPL\_B}}$(5), $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/$\overline{\text{IRQ6}}$, $\overline{\text{CS}}$(0:5), $\overline{\text{CS}}$(6)/$\overline{\text{CE}}$(1)_B, $\overline{\text{CS}}$(7)/$\overline{\text{CE}}$(2)_B, $\overline{\text{WE0}}$/$\overline{\text{BS\_B0}}$/$\overline{\text{IORD}}$, $\overline{\text{WE1}}$/$\overline{\text{BS\_B1}}$/ $\overline{\text{IOWR}}$, $\overline{\text{WE2}}$/$\overline{\text{BS\_B2}}$/$\overline{\text{PCOE}}$, $\overline{\text{WE3}}$/$\overline{\text{BS\_B3}}$/$\overline{\text{PCWE}}$, $\overline{\text{BS\_A}}$(0:3), $\overline{\text{GPL\_A0}}$/$\overline{\text{GPL\_B0}}$, $\overline{\text{OE}}$/$\overline{\text{GPL\_A1}}$/$\overline{\text{GPL\_B1}}$, $\overline{\text{GPL\_A}}$(2:3)/ $\overline{\text{GPL\_B}}$(2:3)/$\overline{\text{CS}}$(2:3), UPWAITA/$\overline{\text{GPL\_A4}}$, UPWAITB/$\overline{\text{GPL\_B4}}$, $\overline{\text{GPL\_A5}}$, ALE_A, $\overline{\text{CE1\_A}}$, $\overline{\text{CE2\_A}}$, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/$\overline{\text{STS}}$, OP3/MODCK2/DSDO, BADDR(28:30)

1.5 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (P_D \bullet q_{JA})(1)$$

where

T_A = Ambient temperature, °C

q_{JA} = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + q_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

1.5.1 Layout Practices

Each V_{CC} pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

1.6 Bus Signal Timing

Table 8 provides the bus operation timing for the MPC860 (devices marked with date code 9829 and later) at 33 MHz and 50 MHz. Timing information for other bus speeds can be interpolated by equation using the *MPC860 Electrical Specifications Spreadsheet v2.0* found at http://www.mot.com/netcomm. For devices marked with date codes earlier than 9829, refer to the *MPC860 Electrical Specifications Spreadsheet v1.1*.

The maximum bus speed supported by the MPC860 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. For loads other than 50 pF, maximum delays can be derated by 1 ns per 10 pF. Derating calculations can also be performed using either version of the *MPC860 Electrical Specifications Spreadsheet*.

When operating at frequencies other than the frequency marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the 'FFACT.' column. AC parameters without an FFactor entry are not frequency-dependent and therefore do not need to be recalculated.

To calculate the AC parameters for a frequency F, the following equation should be applied to each one of the above parameters:

for minima:

$$D = D_{50} + \frac{FFACTOR(1000 - 20 \times F)}{F}$$

where

D is the parameter value in nanoseconds for the frequency required

F is the operation frequency in MHz

D50 is the parameter defined for 50 MHz

FFACTOR is the one defined for each on of the parameters in the table.

Table 8 shows the bus operation timings for the MPC860.

Table 8. Bus Operation Timings

Num	Characteristic	50 MHz		33 MHz[1]		Unit	FFACT.
		Min	Max	Min	Max		
B1	CLKOUT period	20		30.30		ns	
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	ns	
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	ns	
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [2]	-0.60	0.60	-0.60	0.60	ns	
B1d	CLKOUT phase jitter [2]	-2.00	2.00	-2.00	2.00	ns	
B1e	CLKOUT frequency jitter (MF < 10) [2]		0.50		0.50	%	
B1f	CLKOUT frequency jitter (10 < MF < 500) [2]		2.00		2.00	%	
B1g	CLKOUT frequency jitter (MF > 500) [2]		3.00		3.00	%	
B1h	Frequency jitter on EXTCLK [3]		0.50		0.50	%	
B2	CLKOUT pulse width low	8.00		12.12		ns	
B3	CLKOUT width high	8.00		12.12		ns	
B4	CLKOUT rise time		4.00		4.00	ns	
B5	CLKOUT fall time		4.00		4.00	ns	
B6							
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) invalid	5.00		7.58		ns	0.250
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR invalid	5.00		7.58		ns	0.250
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ invalid [4]	5.00		7.58		ns	0.250
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid	5.00	11.75	7.58	14.33	ns	0.250
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3) $\overline{BDIP}$, PTR valid	5.00	11.75	7.58	14.33	ns	0.250
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid [4]	5.00	11.75	7.58	14.33	ns	0.250
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z	5.00	11.75	7.58	14.33	ns	0.250
B10							
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion	5.00	11.00	7.58	13.58	ns	0.250

Table 8. Bus Operation Timings (Continued)

Num	Characteristic	50 MHz		33 MHz[1]		Unit	FFACT.
		Min	Max	Min	Max		
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	ns	
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation	5.00	11.75	7.58	14.33	ns	0.250
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	ns	
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z	5.00	19.00	7.58	21.58	ns	0.250
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	ns	
B14	CLKOUT to $\overline{TEA}$ assertion	2.50	10.00	2.50	10.00	ns	
B15	CLKOUT to $\overline{TEA}$ High-Z	2.50	15.00	2.50	15.00	ns	
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time)	9.75		9.75		ns	
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time)	10.00		10.00		ns	
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [5]	8.50		8.50		ns	
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time).	1.00		1.00		ns	
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time)	2.00		2.00		ns	
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [6]	6.00		6.00		ns	
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [6]	1.00		1.00		ns	
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [7]	4.00		4.00		ns	
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [7]	2.00		2.00			
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	ns	0.250
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0		8.00		8.00	ns	
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	ns	0.250
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.13	10.86	17.99	ns	0.375
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	ns	
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0.	3.00		5.58		ns	0.250
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0	8.00		13.15		ns	0.500
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted		9.00		9.00	ns	
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	ns	
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	23.00		35.88		ns	1.250
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	28.00		43.45		ns	1.500
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0		9.00		9.00	ns	
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0	5.00	11.75	7.58	14.33	ns	0.250
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0		11.75		14.33	ns	0.250

Table 8. Bus Operation Timings (Continued)

Num	Characteristic	50 MHz		33 MHz[1]		Unit	FFACT.
		Min	Max	Min	Max		
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.13	10.86	17.99	ns	0.375
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1		14.13		17.99	ns	0.375
B29	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0	3.00		5.58		ns	0.250
B29a	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0	8.00		13.15		ns	0.500
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00		5.58		ns	0.250
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0	8.00		13.15		ns	0.500
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00		43.45		ns	1.500
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0	28.00		43.45		ns	1.500
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1	5.00		8.86		ns	0.375
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1	5.00		8.86		ns	0.375
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1	24.50		38.67		ns	1.375
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	24.50		38.67		ns	1.375
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM write access [8]	3.00		5.58		ns	0.250
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0	8.00		13.15		ns	0.500
B30b	$\overline{WE}$(0:3) negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0	28.00		43.45		ns	1.500
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1	4.50		8.36		ns	0.375
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	24.50		38.67		ns	1.375
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	ns	

Table 8. Bus Operation Timings (Continued)

Num	Characteristic	50 MHz		33 MHz[1]		Unit	FFACT.
		Min	Max	Min	Max		
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	ns	
B31c	CLKOUT rising edge to S valid- as requested by control bit CST3 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1	9.40	14.13	13.26	17.99	ns	0.375
B32	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	ns	
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0	5.00	11.75	7.58	14.33	ns	0.250
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	ns	
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1	9.40	14.13	13.26	17.99	ns	0.375
B33	CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	ns	
B33a	CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	3.00		5.58		ns	0.250
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	8.00		13.15		ns	0.500
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM	13.00		20.73		ns	0.750
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM	3.00		5.58		ns	0.250
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM	8.00		13.15		ns	0.500
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	13.00		20.73		ns	0.750
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM	3.00		5.58		ns	0.250
B37	UPWAIT valid to CLKOUT falling edge [9]	6.00		6.00		ns	
B38	CLKOUT falling edge to UPWAIT valid [9]	1.00		1.00		ns	
B39	$\overline{AS}$ valid to CLKOUT rising edge [10]	7.00		7.00		ns	
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge	7.00		7.00		ns	
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00		7.00		ns	
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00		2.00		ns	

Table 8. Bus Operation Timings (Continued)

Num	Characteristic	50 MHz		33 MHz[1]		Unit	FFACT.
		Min	Max	Min	Max		
B43	$\overline{AS}$ negation to memory controller signals negation		TBD			ns	

[1] The values in the 33 MHz column are derived from the 50 MHz values.

[2] Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

[3] If the rate of change of the frequency of EXTAL is slow (I.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (I.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

[4] The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

[5] The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

[6] The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

[7] The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the Memory Controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

[8] The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

[9] The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 16.

[10] The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 19.

Figure 1 is the control timing diagram.

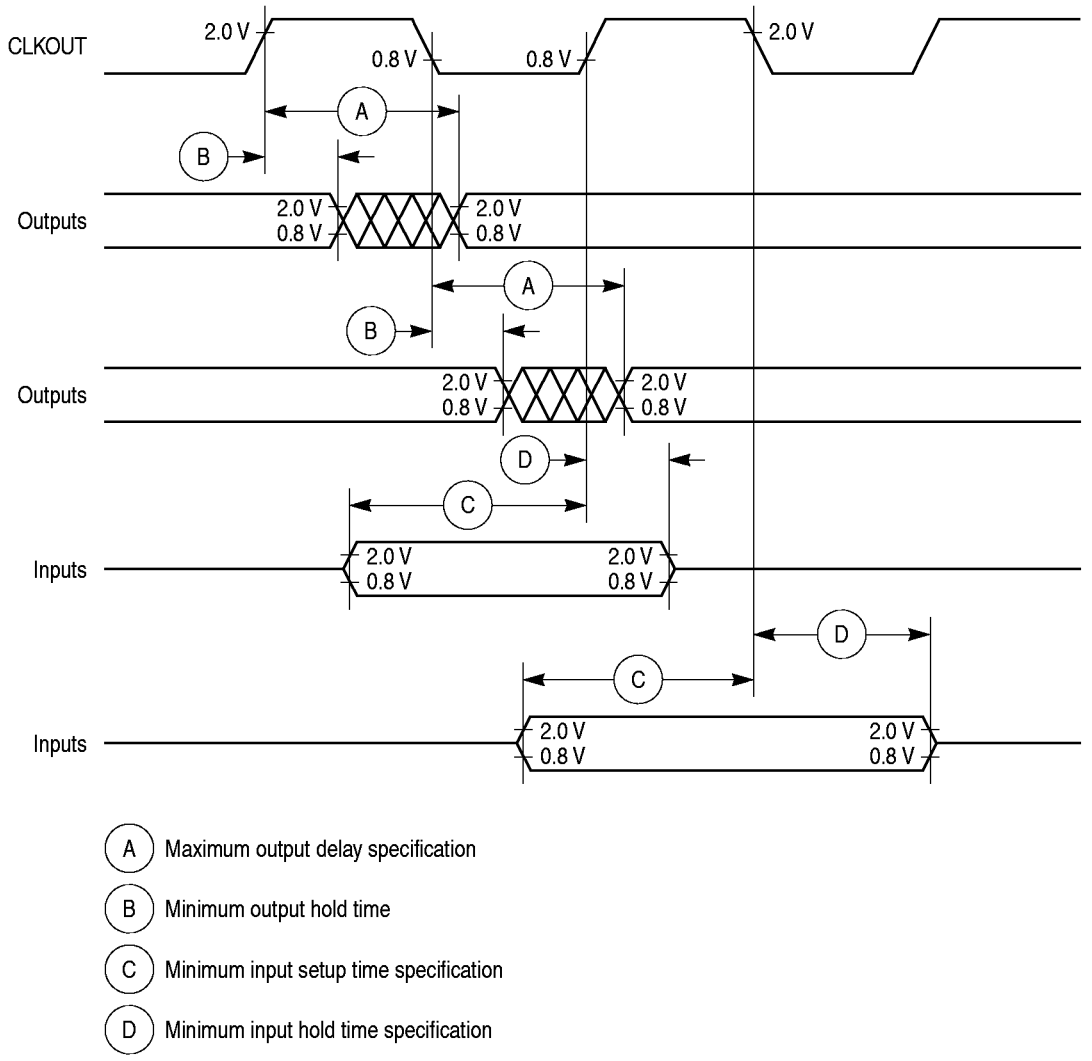


Figure 1. Control Timing

Figure 2 provides the timing for the external clock.

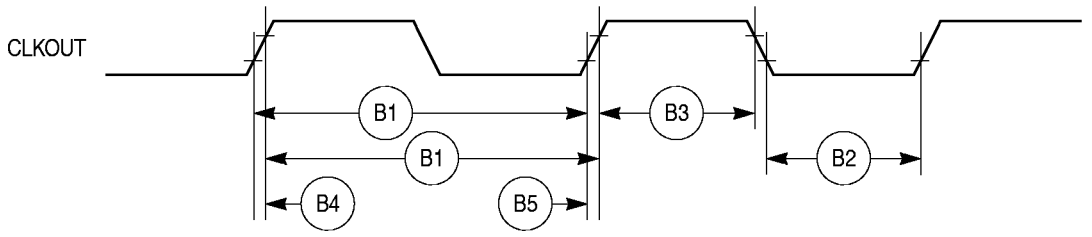


Figure 2. External Clock Timing

Figure 3 provides the timing for the synchronous output signals.

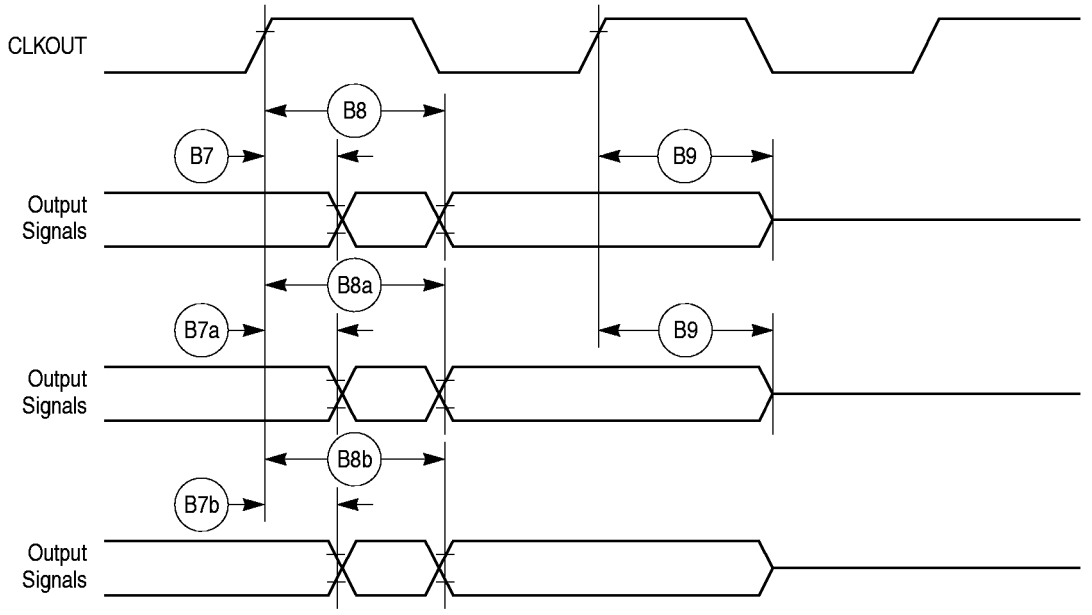


Figure 3. Synchronous Output Signals Timing

Figure 4 provides the timing for the synchronous active pull-up and open-drain output signals.

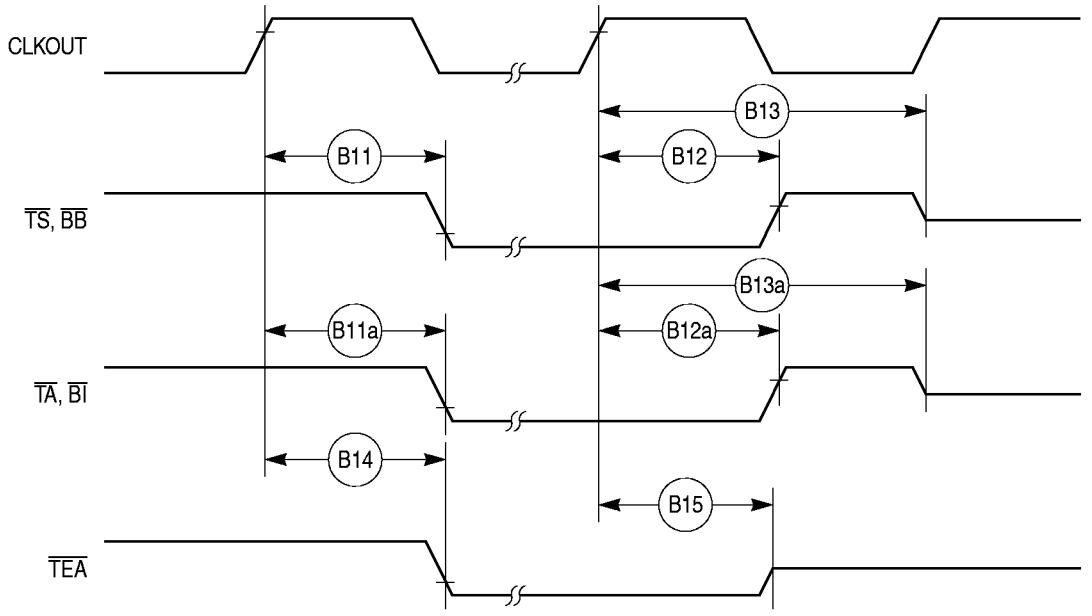


Figure 4. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 5 provides the timing for the synchronous input signals.

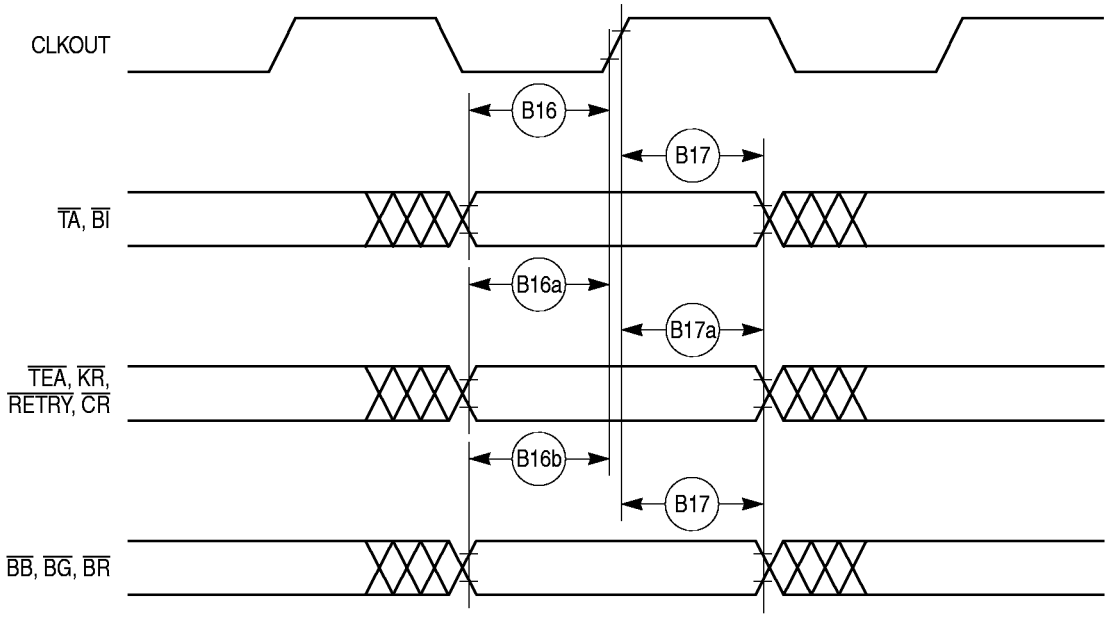


Figure 5. Synchronous Input Signals Timing

Figure 6 provides normal case timing for input data.

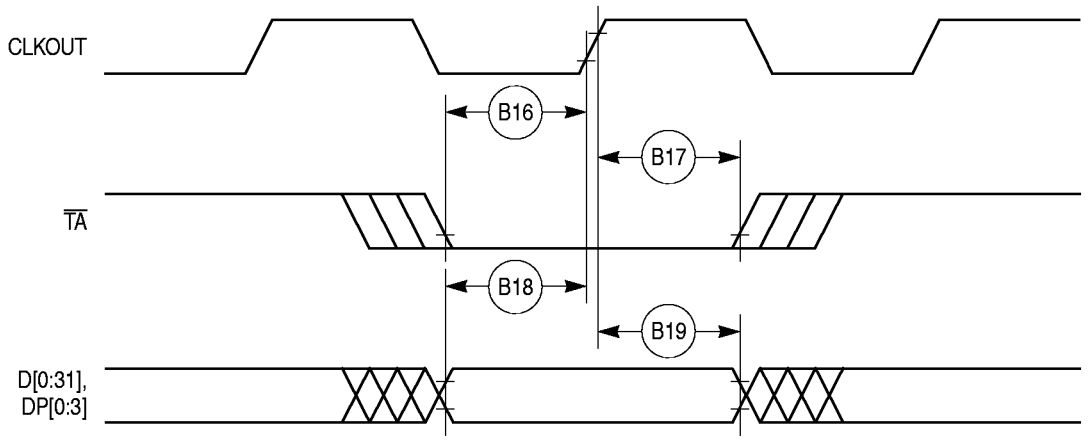


Figure 6. Input Data Timing in Normal Case

Figure 7 provides the timing for the input data controlled by the UPM in the memory controller.

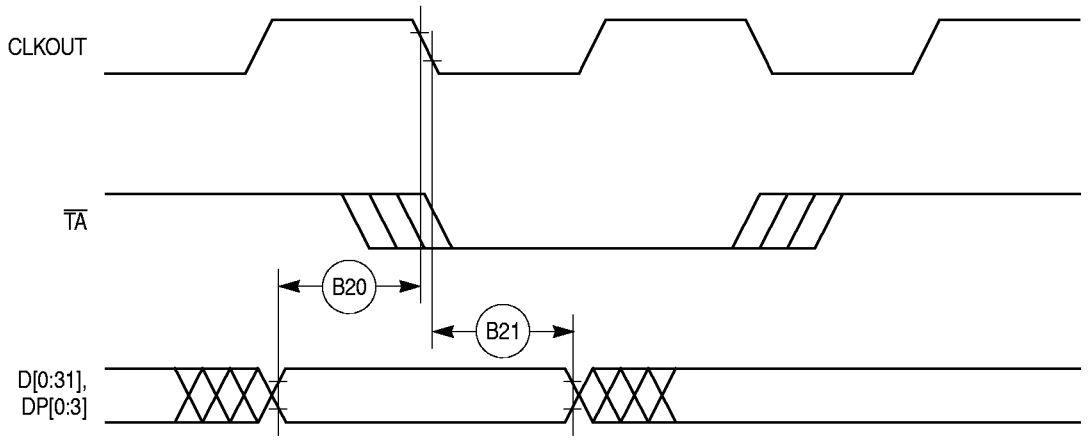


Figure 7. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 8 through Figure 11 provide the timing for the external bus read controlled by various GPCM factors.

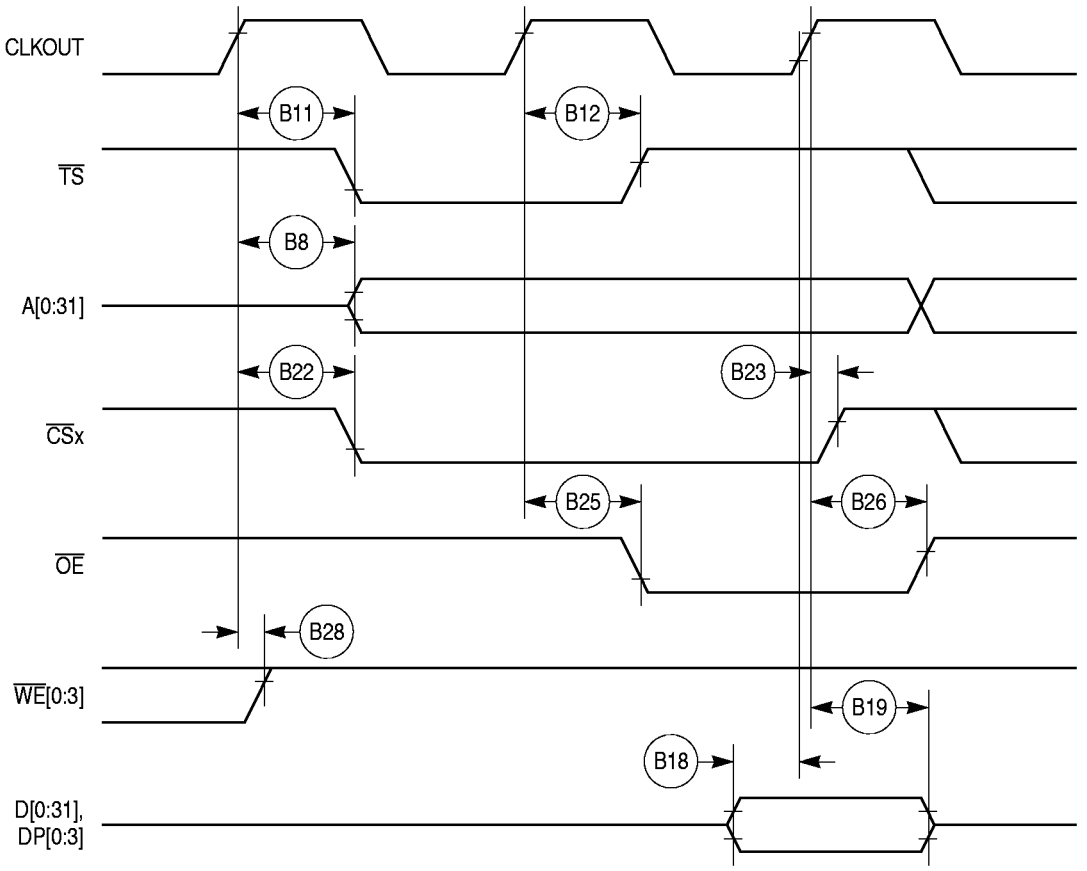


Figure 8. External Bus Read Timing (GPCM Controlled—ACS = 00)

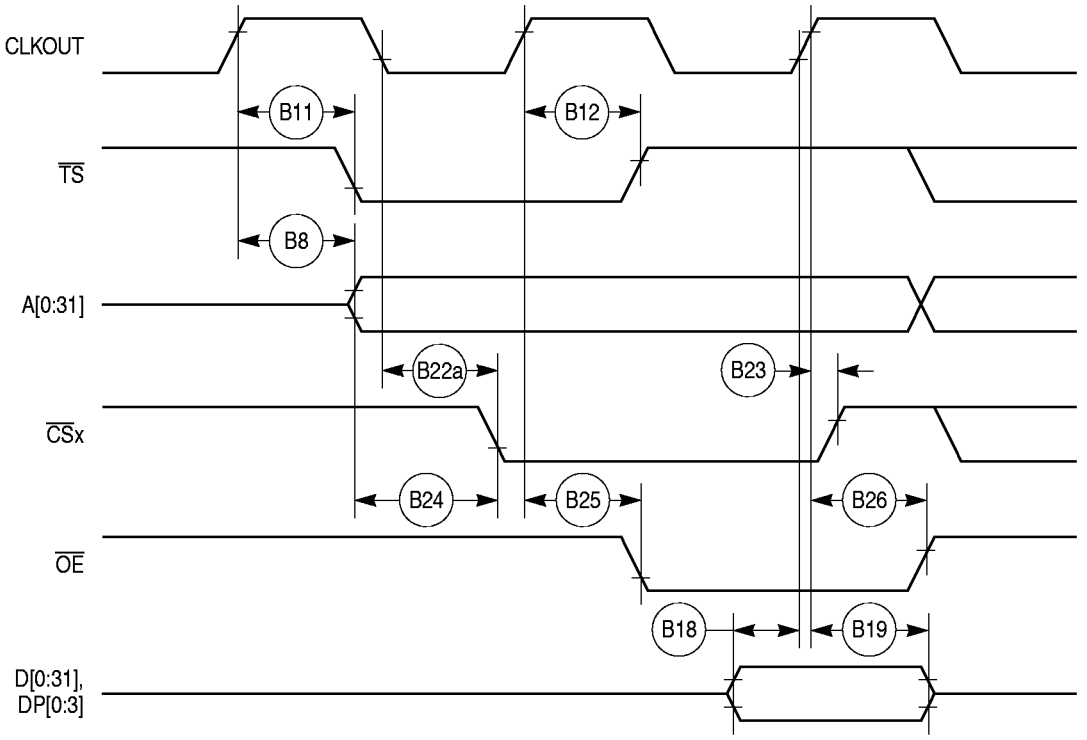


Figure 9. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

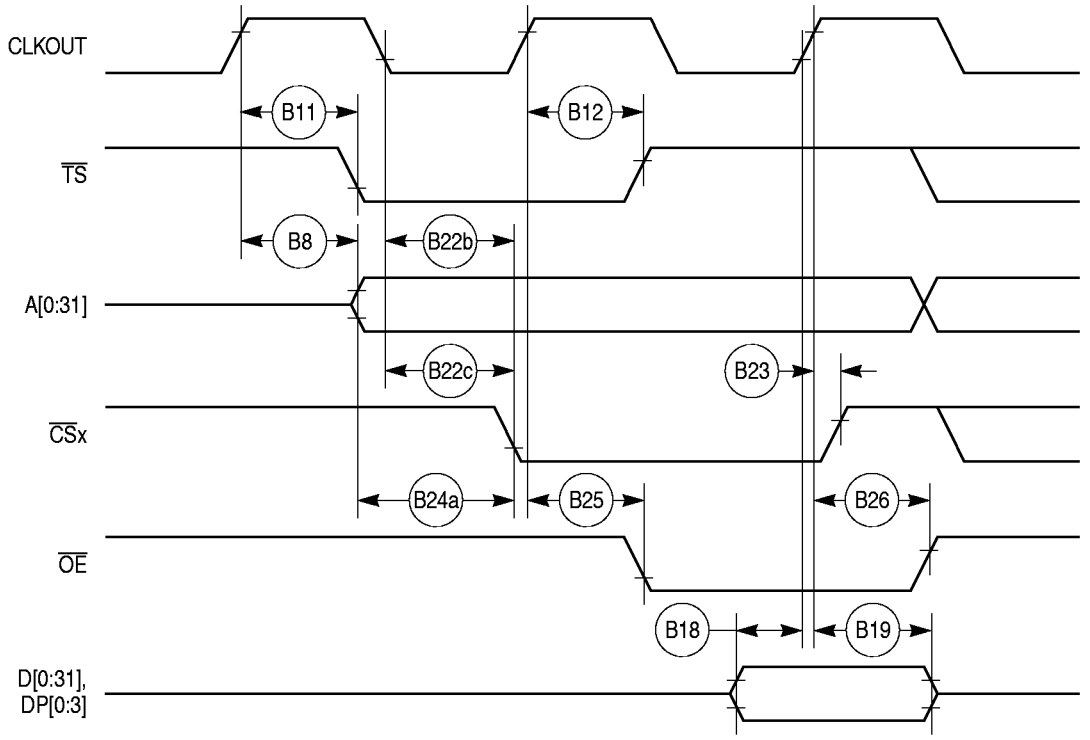


Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

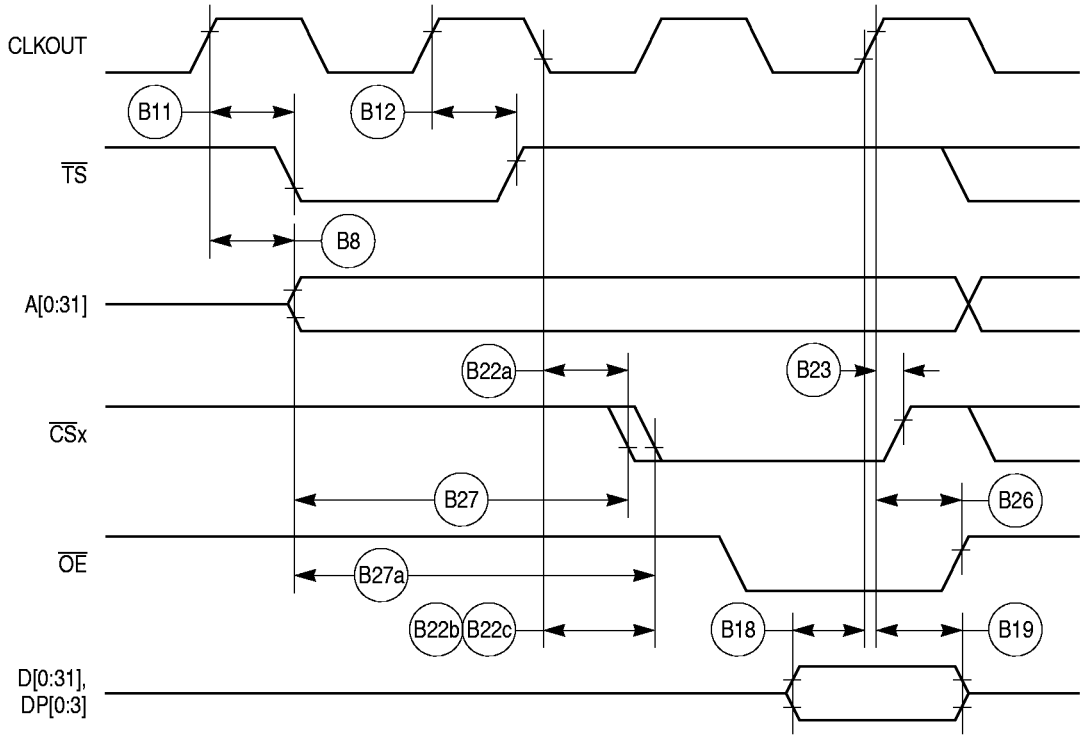


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 12 through Figure 14 provide the timing for the external bus write controlled by various GPCM factors.

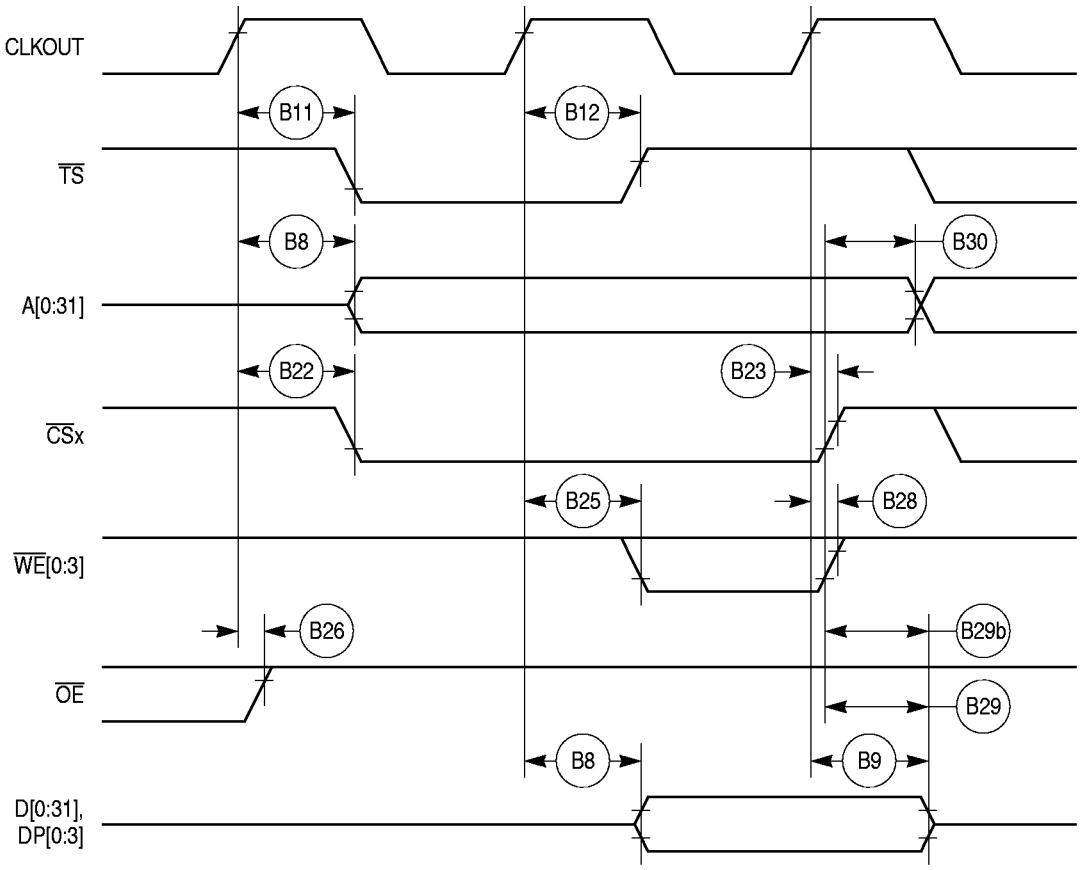


Figure 12. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

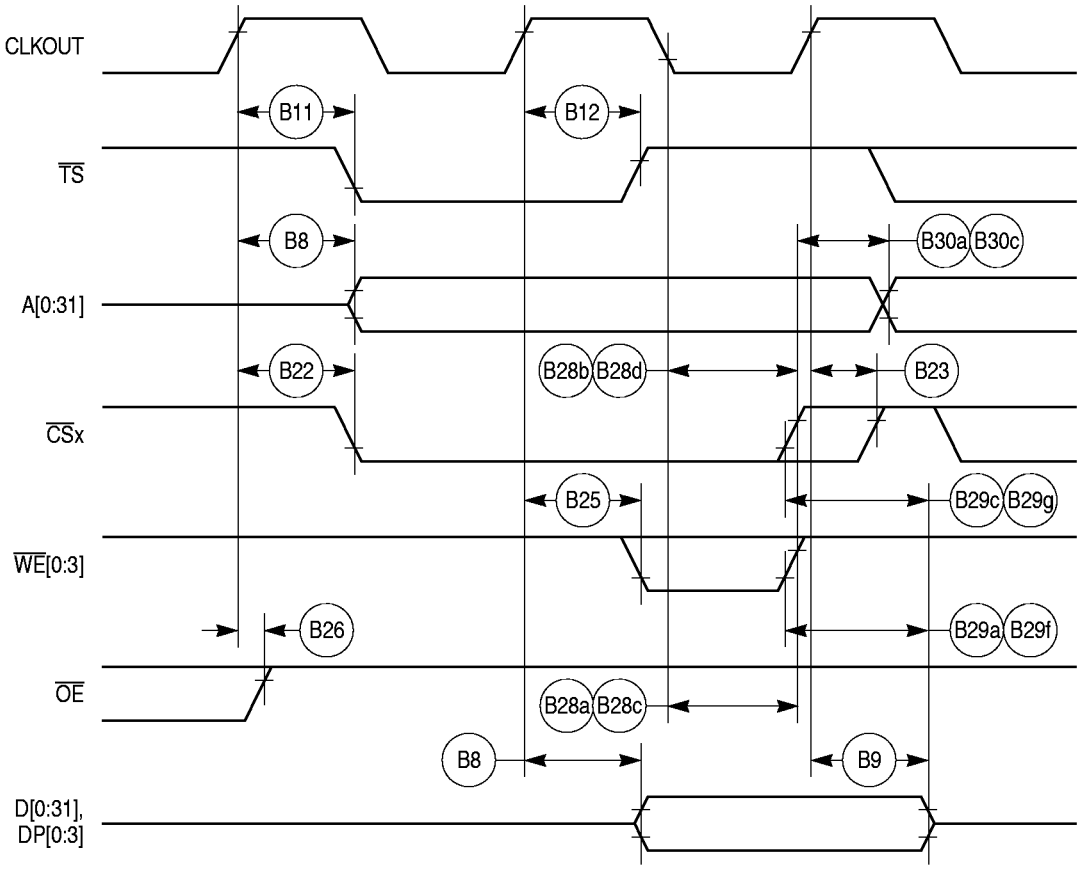


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

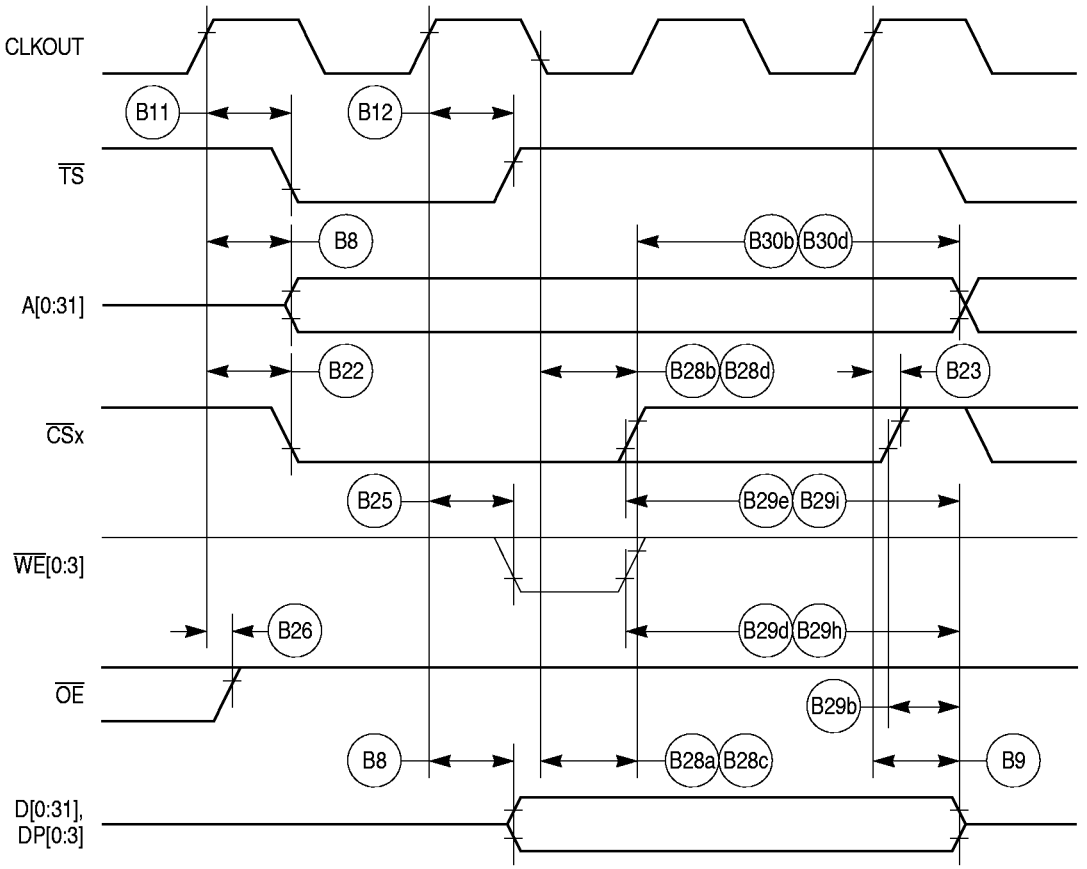


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 15 provides the timing for the external bus controlled by the UPM.

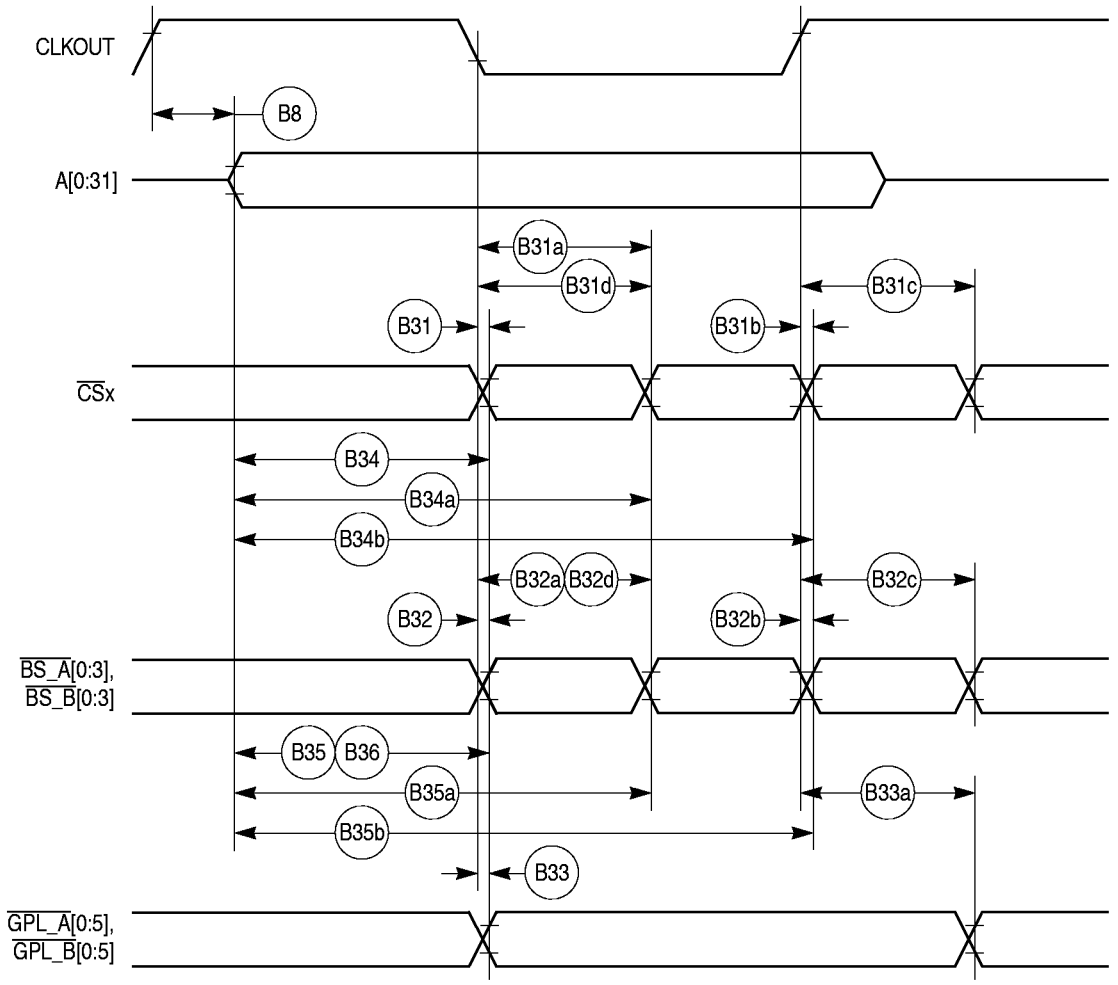


Figure 15. External Bus Timing (UPM Controlled Signals)

Figure 16 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

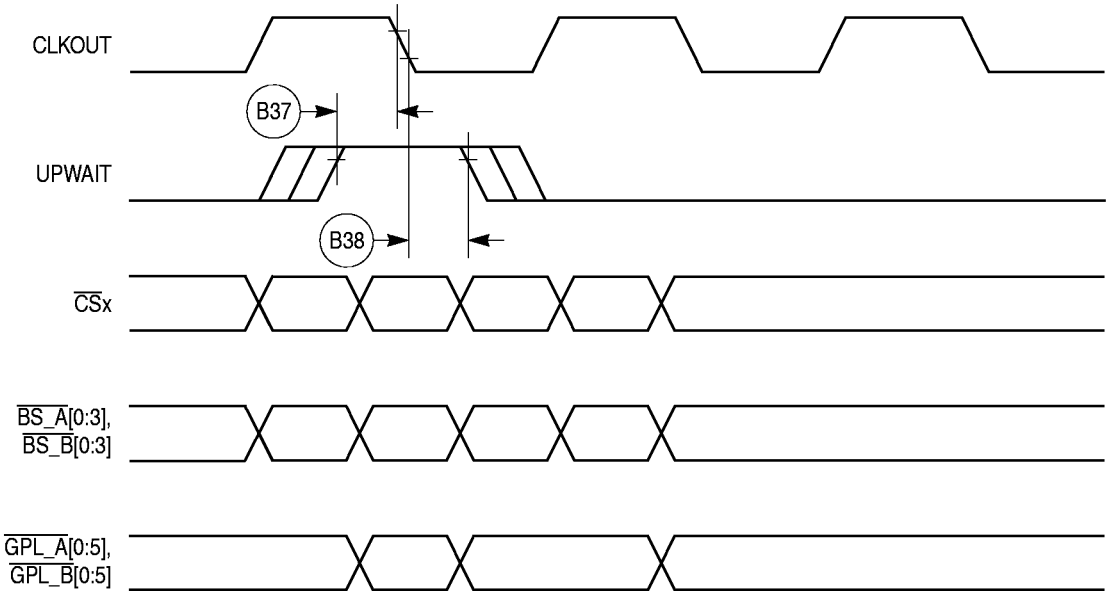


Figure 16. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 17 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

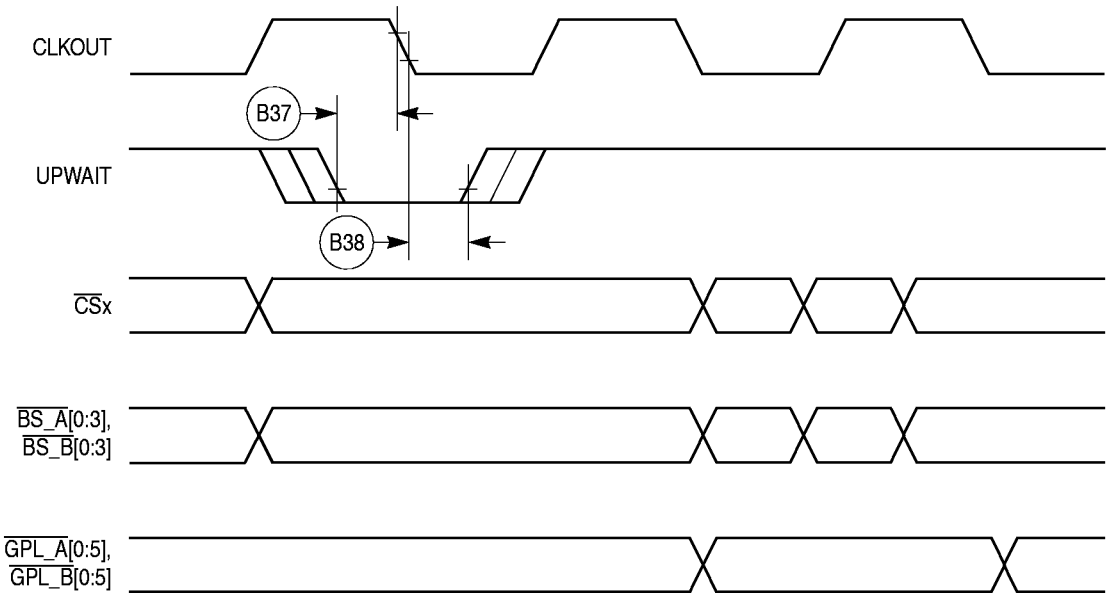


Figure 17. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 18 provides the timing for the synchronous external master access controlled by the GPCM.

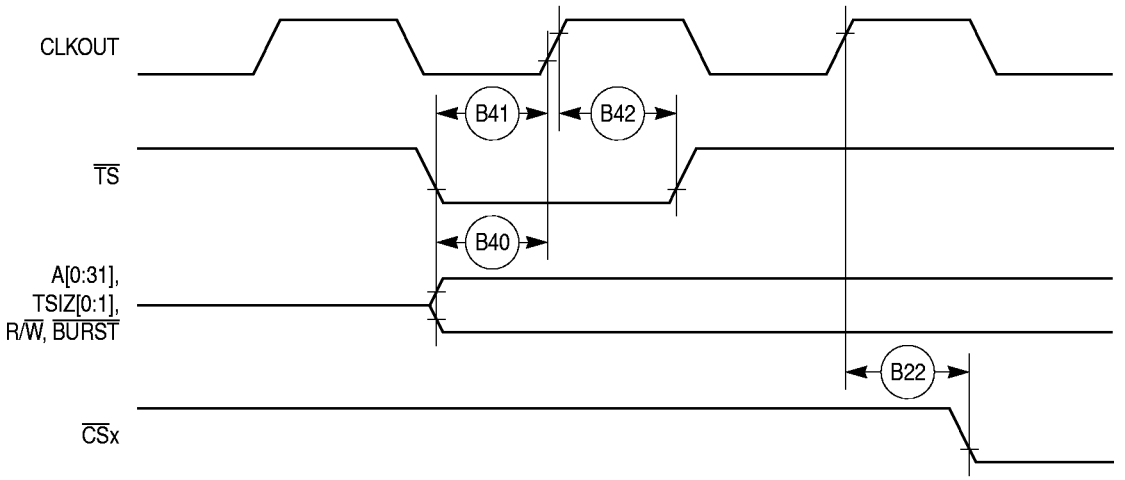


Figure 18. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 19 provides the timing for the asynchronous external master memory access controlled by the GPCM.

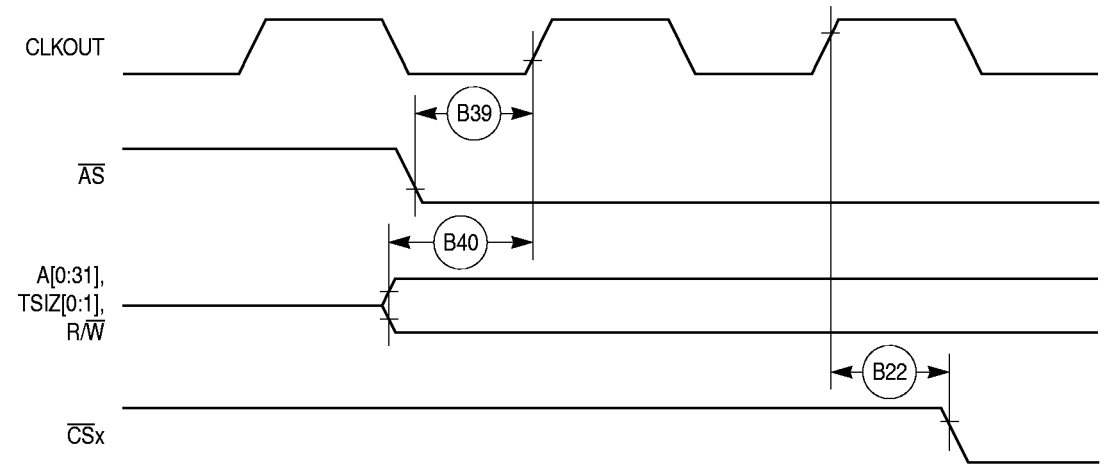


Figure 19. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 20 provides the timing for the asynchronous external master control signals negation.

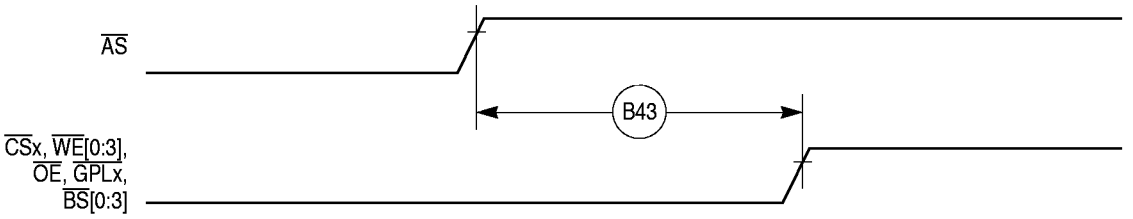


Figure 20. Asynchronous External Master—Control Signals Negation Timing

Table 9 provides interrupt timing for the MPC860.

Table 9. Interrupt Timing

Num	Characteristic[1]	33 MHz		50 MHz		Unit
		Min	Max	Min	Max	
I39	$\overline{IRQ}$x valid to CLKOUT rising edge (set up time)	6.00		6.00		ns
I40	$\overline{IRQ}$x hold time after CLKOUT	2.00		2.00		ns
I41	$\overline{IRQ}$x pulse width low	3.00		3.00		ns
I42	$\overline{IRQ}$x pulse width high	3.00		3.00		ns
I43	$\overline{IRQ}$x edge-to-edge time	$4xT_{CLOCKOUT}$		$4xT_{CLOCKOUT}$		—

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 21 provides the interrupt detection timing for the external level-sensitive lines.

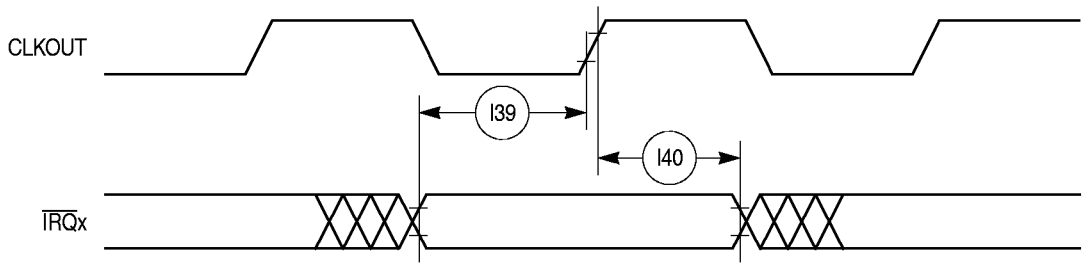


Figure 21. Interrupt Detection Timing for External Level Sensitive Lines

Figure 22 provides the interrupt detection timing for the external edge-sensitive lines.

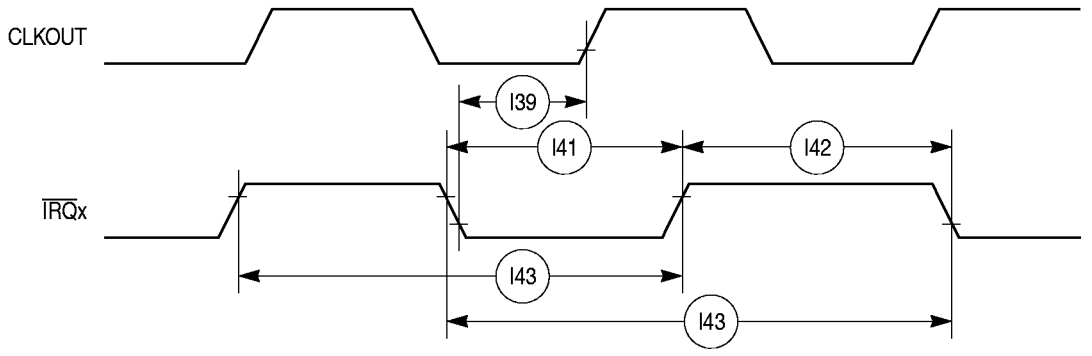


Figure 22. Interrupt Detection Timing for External Edge Sensitive Lines

Table 10 shows the PCMCIA timing for the MPC860.

Table 10. PCMCIA Timing

Num	Characteristic	33 MHz		50 MHz		FFACTOR	Unit
		Min	Max	Min	Max		
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted.[1]	20.73		13.00		0.750	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation.[1]	28.30		18.00		1.000	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	7.58	15.58	5.00	13.00	0.250	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid.	8.58		6.00		0.250	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted.	7.58	15.58	5.00	13.00	0.250	
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated.	7.58	15.58	5.00	13.00	0.250	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time.		11.00		11.00		ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time.	2.00	11.00	2.00	11.00		ns
P52	CLKOUT to ALE assert time	7.58	15.58	5.00	13.00	0.250	ns
P53	CLKOUT to ALE negate time		15.58		13.00	0.250	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid.[1]	5.58		3.00		0.250	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge.[1]	8.00		8.00			ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid.[1]	2.00		2.00			ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC860 PowerQUICC User s Manual*.

Figure 23 provides the PCMCIA access cycle timing for the external bus read.

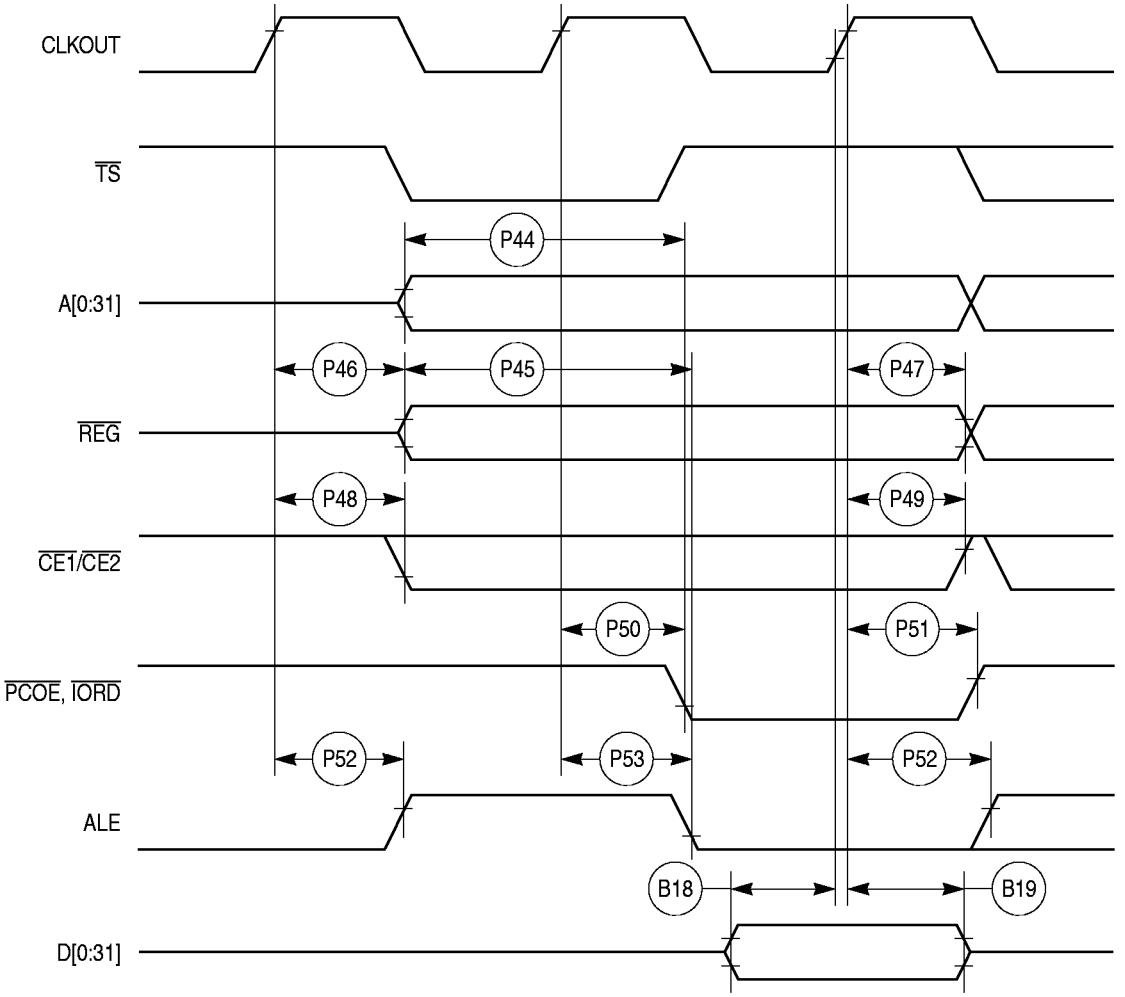


Figure 23. PCMCIA Access Cycles Timing External Bus Read

Figure 24 provides the PCMCIA access cycle timing for the external bus write.

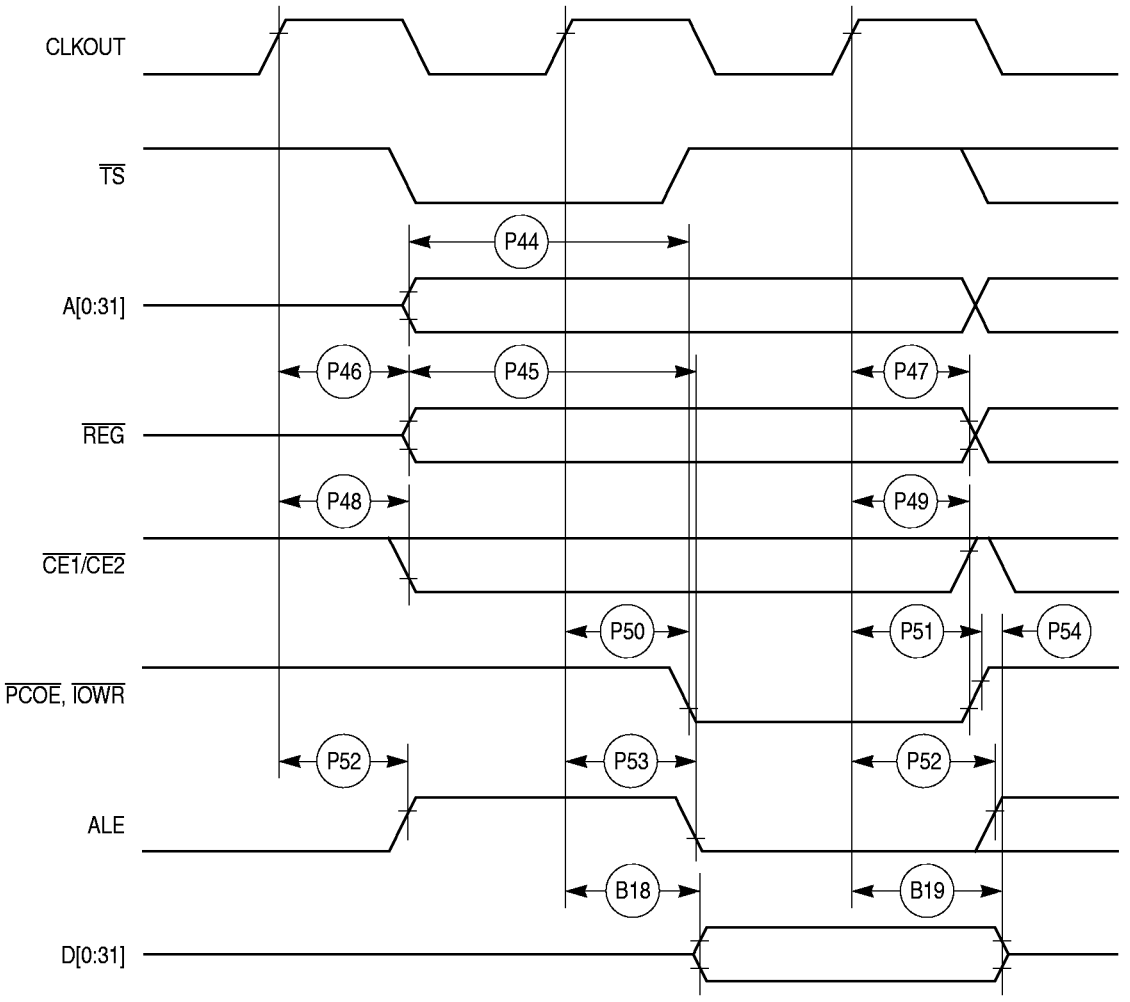


Figure 24. PCMCIA Access Cycles Timing External Bus Write

Figure 25 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

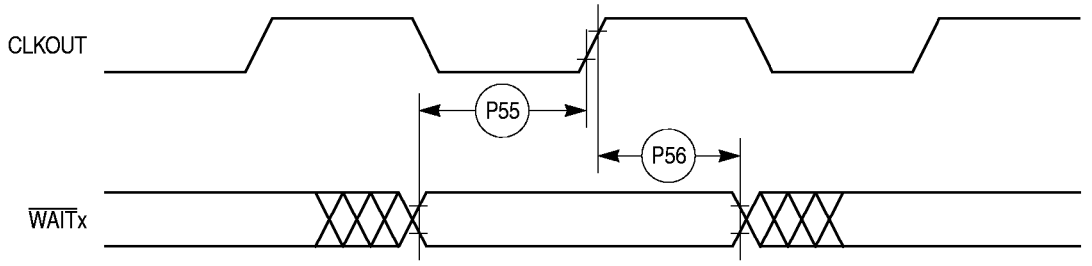


Figure 25. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 11 shows the PCMCIA port timing for the MPC860.

Table 11. PCMCIA Port Timing

Num	Characteristic	33 MHz		50 MHz		FFactor	Unit
		Min	Max	Min	Max		
P57	CLKOUT to OPx Valid		19.00		19.00		ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1]	25.73		18.00		0.75	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00		5.00			ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00		1.00			ns

[1] OP2 and OP3 only.

Figure 26 provides the PCMCIA output port timing for the MPC860.

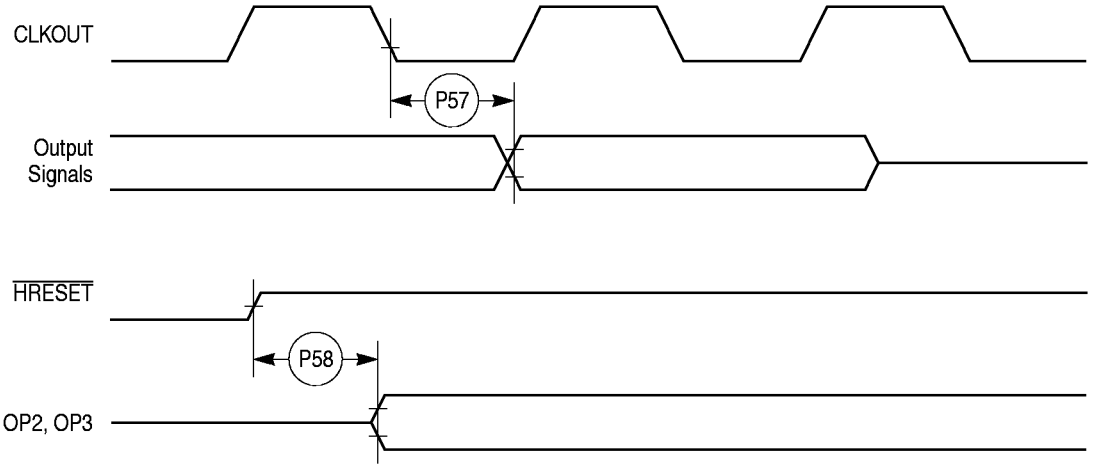


Figure 26. PCMCIA Output Port Timing

Figure 27 provides the PCMCIA output port timing for the MPC860.

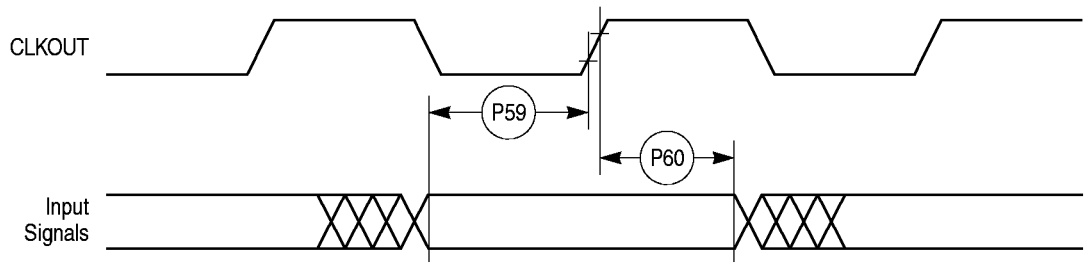


Figure 27. PCMCIA Input Port Timing

Table 12 shows the debug port timing for the MPC860.

Table 12. Debug Port Timing

Num	Characteristic	33 MHz		50 MHz		Unit
		Min	Max	Min	Max	
D61	DSCK cycle time	$3xT_{CLOCKOUT}$		$3xT_{CLOCKOUT}$		ns
D62	DSCK clock pulse width	$1.25xT_{CLOCKOUT}$		$1.25xT_{CLOCKOUT}$		ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00		8.00		ns
D65	DSDI data hold time	5.00		5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	ns

Figure 28 provides the input timing for the debug port clock.

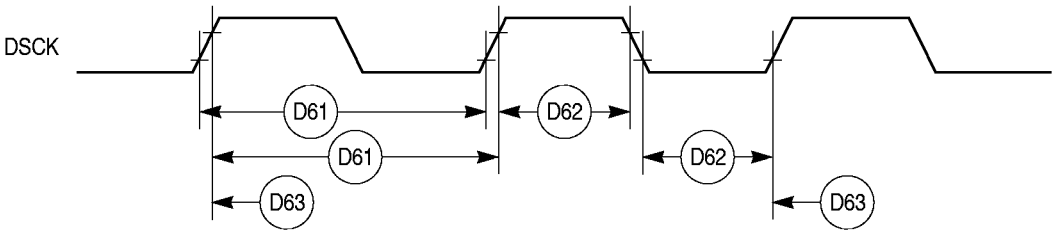


Figure 28. Debug Port Clock Input Timing

Figure 29 provides the timing for the debug port.

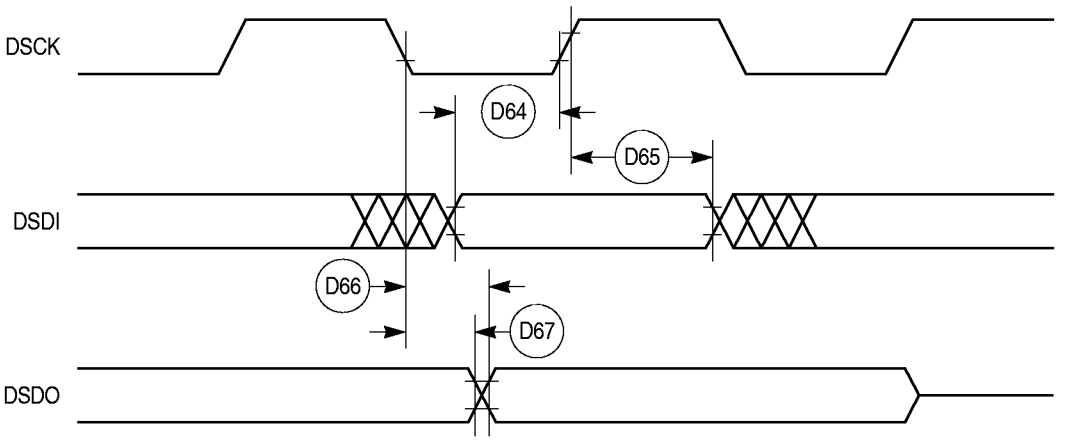


Figure 29. Debug Port Timings

Table 13 shows the reset timing for the MPC860.

Table 13. Reset Timing

Num	Characteristic	33 MHz		50 MHz		FFACTOR	Unit
		Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance		20.00		20.00		ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance		20.00		20.00		ns
R71	$\overline{\text{RSTCONF}}$ pulse width	515.15		340.00		17.000	ns
R72							
R73	Configuration data to HRESET rising edge set up time	504.55		350.00		15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00		350.00			ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00		0.00			ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00		0.00			ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive		25.00		25.00		ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.		25.00		25.00		ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance.		25.00		25.00		ns
R80	DSDI, DSCK set up	90.91		60.00		3.000	ns
R81	DSDI, DSCK hold time	0.00		0.00			ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	242.42		160.00		8.000	ns

Figure 30 shows the reset timing for the data bus configuration.

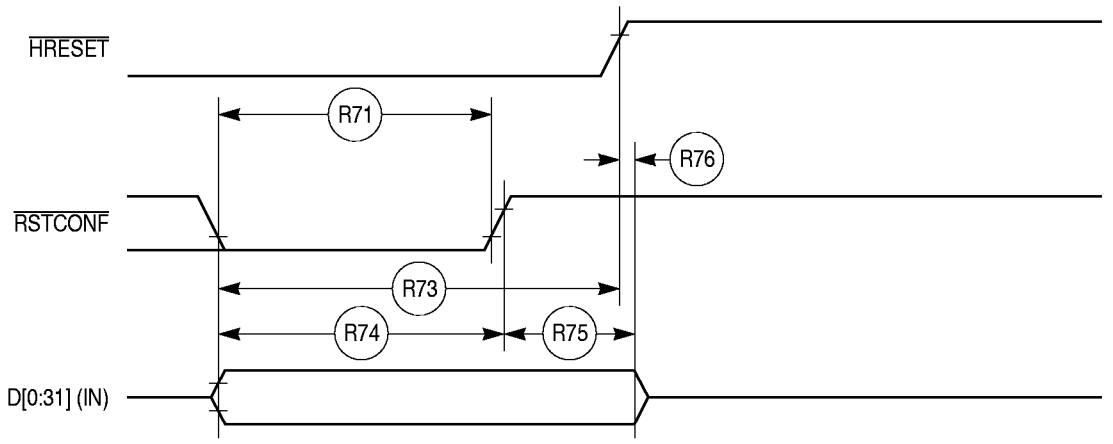


Figure 30. Reset Timing—Configuration from Data Bus

Figure 31 provides the reset timing for the data bus weak drive during configuration.

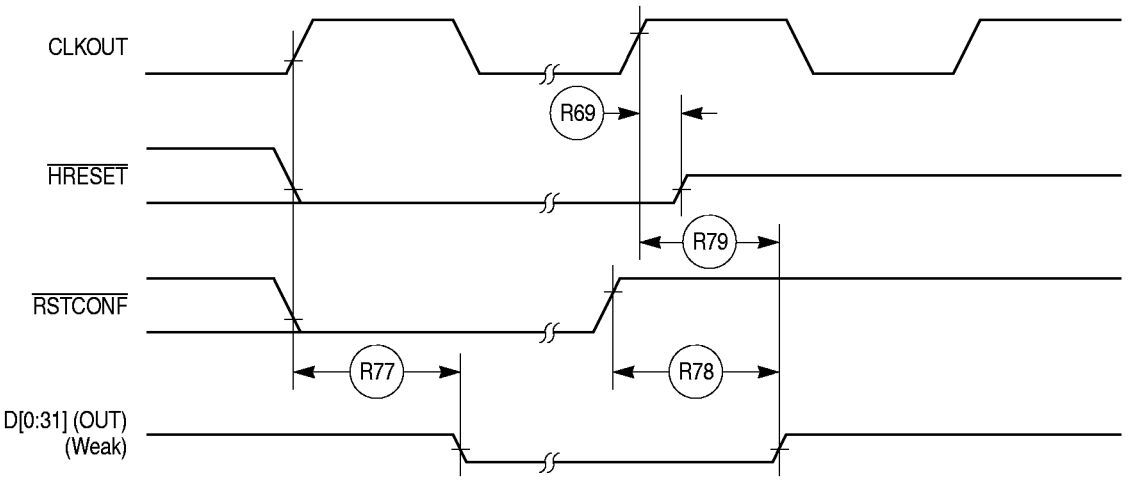


Figure 31. Reset Timing—Data Bus Weak Drive during Configuration

Figure 32 provides the reset timing for the debug port configuration.

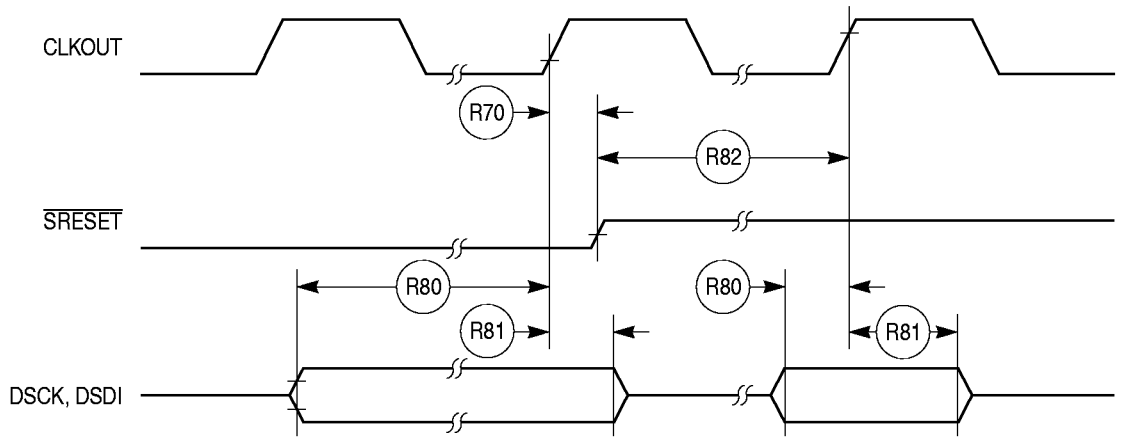


Figure 32. Reset Timing—Debug Port Configuration

1.7 IEEE 1149.1 Electrical Specifications

Table 14 provides the JTAG timings for the MPC860 shown in Figure 33 to Figure 36.

Table 14. JTAG Timing

Num	Characteristic	33 MHz		50 MHz		Unit
		Min	Max	Min	Max	
J82	TCK cycle time	100.00		100.00		ns
J83	TCK clock pulse width measured at 1.5 V	40.00		40.00		ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00		5.00		ns
J86	TMS, TDI data hold time	25.00		25.00		ns
J87	TCK low to TDO data valid		27.00		27.00	ns
J88	TCK low to TDO data invalid	0.00		0.00		ns

Table 14. JTAG Timing (Continued)

Num	Characteristic	33 MHz		50 MHz		Unit
		Min	Max	Min	Max	
J89	TCK low to TDO high impedance		20.00		20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00		100.00		ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00		40.00		ns
J92	TCK falling edge to output valid		50.00		50.00	ns
J93	TCK falling edge to output valid out of high impedance		50.00		50.00	ns
J94	TCK falling edge to output high impedance		50.00		50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00		50.00		ns
J96	TCK rising edge to boundary scan input invalid	50.00		50.00		ns

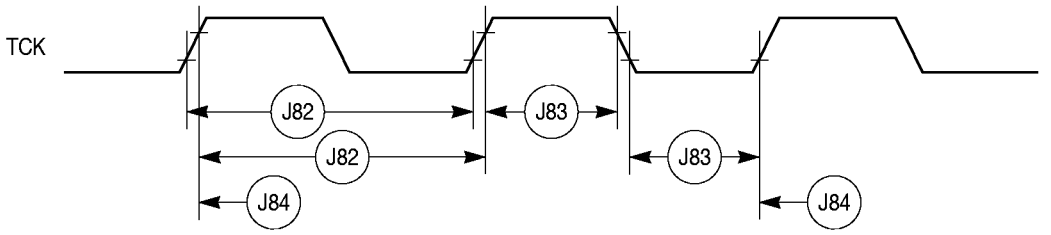


Figure 33. JTAG Test Clock Input Timing

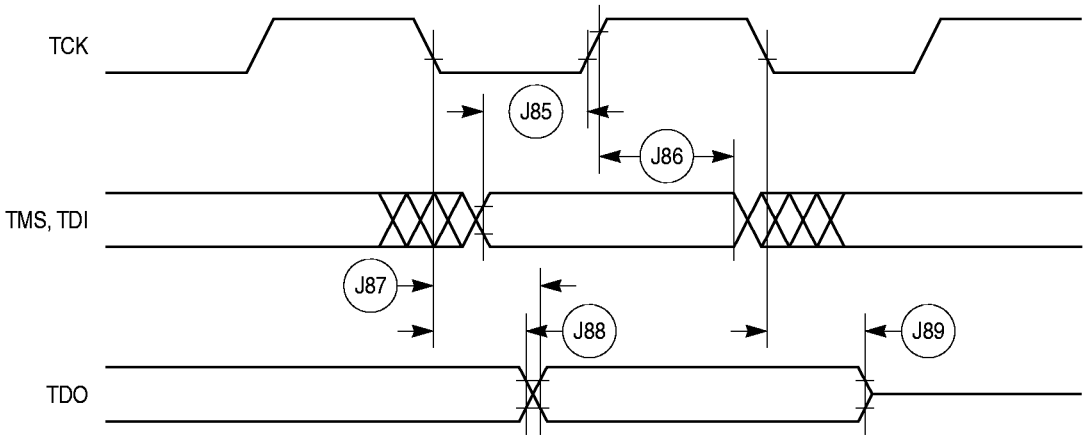


Figure 34. JTAG Test Access Port Timing Diagram

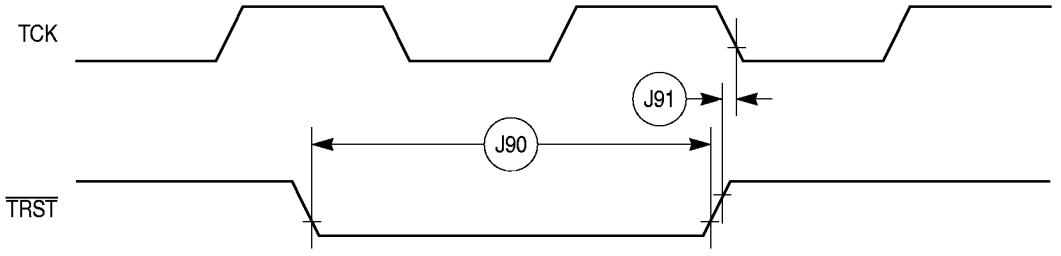


Figure 35. JTAG $\overline{\text{TRST}}$ Timing Diagram

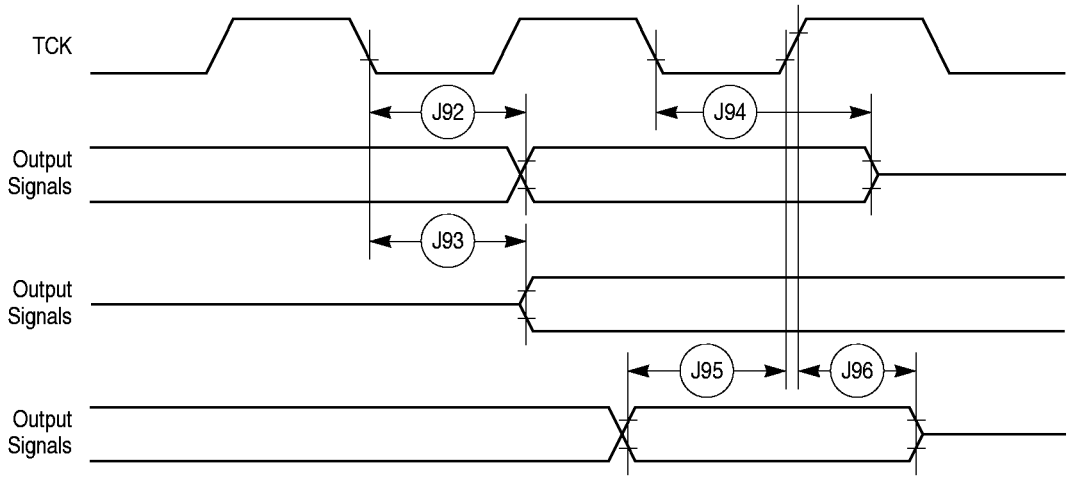


Figure 36. Boundary Scan (JTAG) Timing Diagram

1.8 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

1.8.1 PIP/PIO AC Electrical Specifications

Table 15 provides the PIP/PIO AC timings as shown in Figure 37 to Figure 41.

Table 15. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-In hold time to STBI high	2.5 – t3[1]	—	clk
23	STBI pulse width	1.5	—	clk
24	STBO pulse width	1 clk – 5ns	—	ns
25	Data-out setup time to STBO low	2	—	clk
26	Data-out hold time from STBO high	5	—	clk
27	STBI low to STBO low (Rx interlock)	—	2	clk
28	STBI low to STBO high (Tx interlock)	2	—	clk
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

[1] t3 = Specification 23

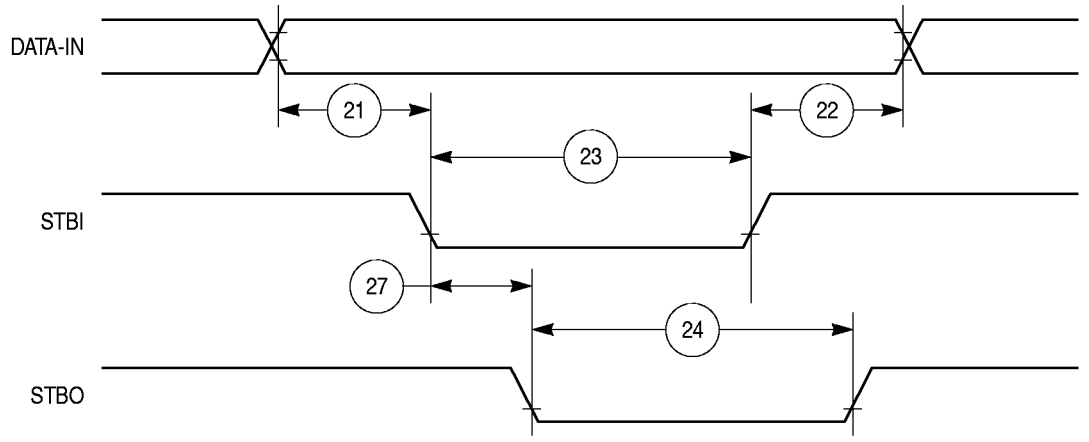


Figure 37. PIP RX (Interlock Mode) Timing Diagram

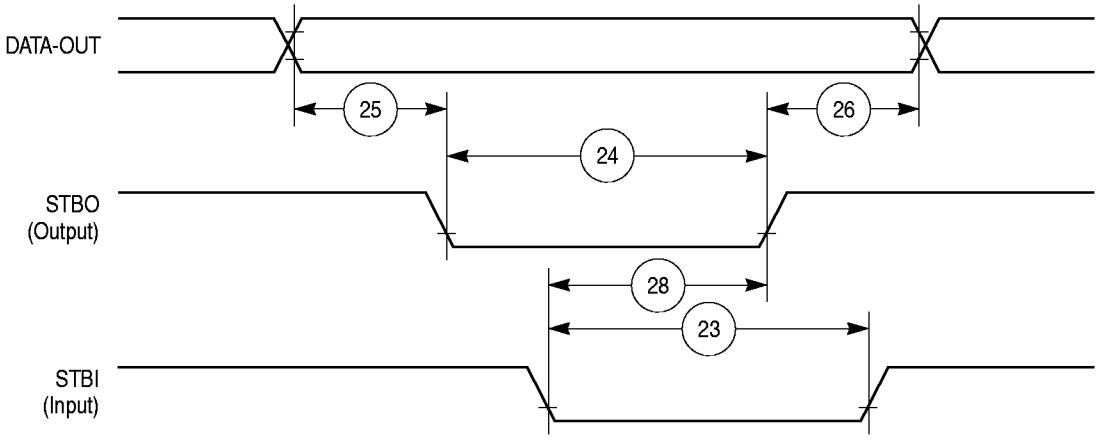


Figure 38. PIP TX (Interlock Mode) Timing Diagram

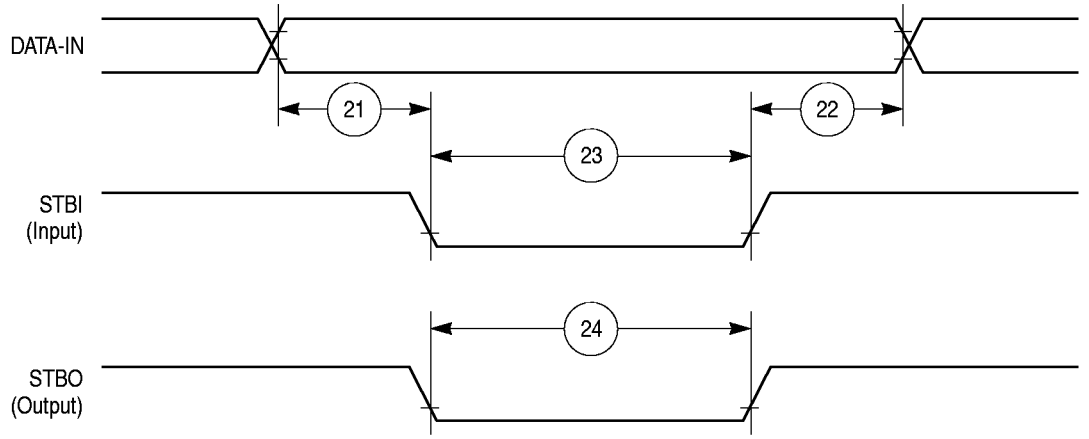


Figure 39. PIP RX (Pulse Mode) Timing Diagram

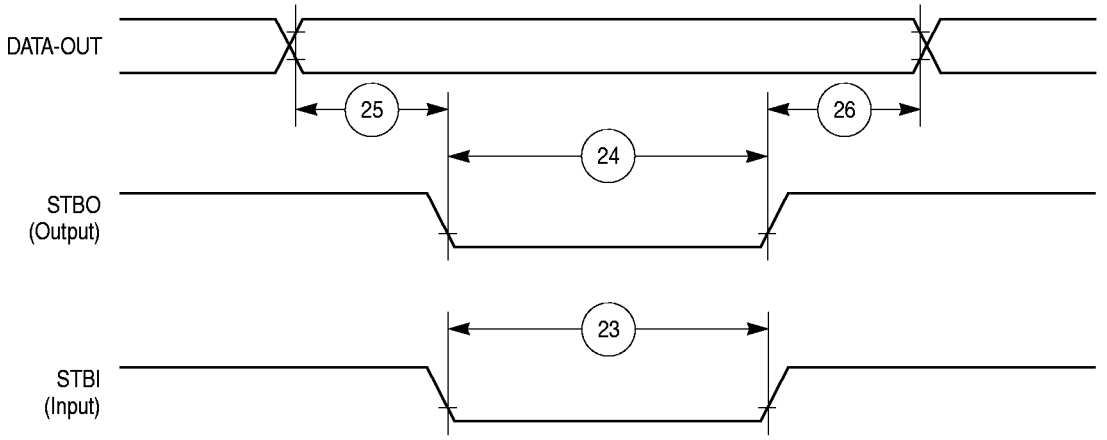


Figure 40. PIP TX (Pulse Mode) Timing Diagram

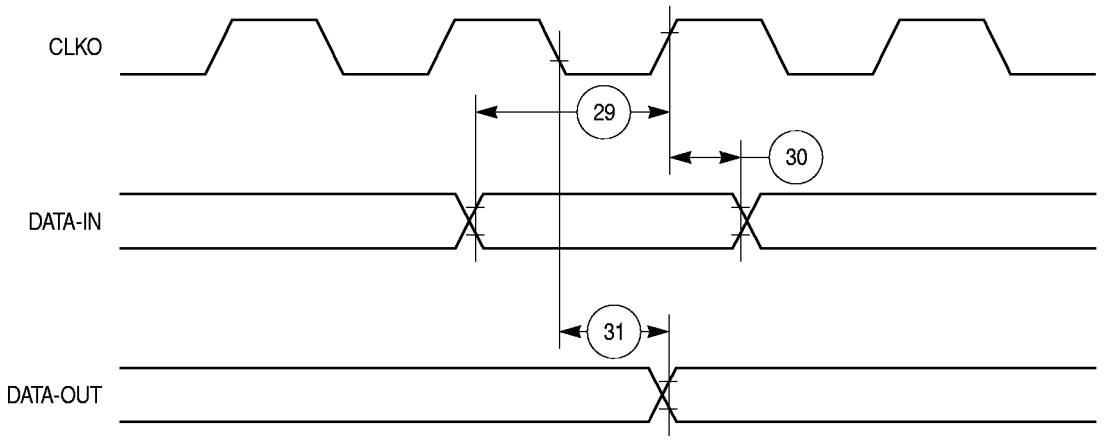


Figure 41. Parallel I/O Data-In/Data-Out Timing Diagram

1.8.2 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 42 to Figure 45.

Table 16. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

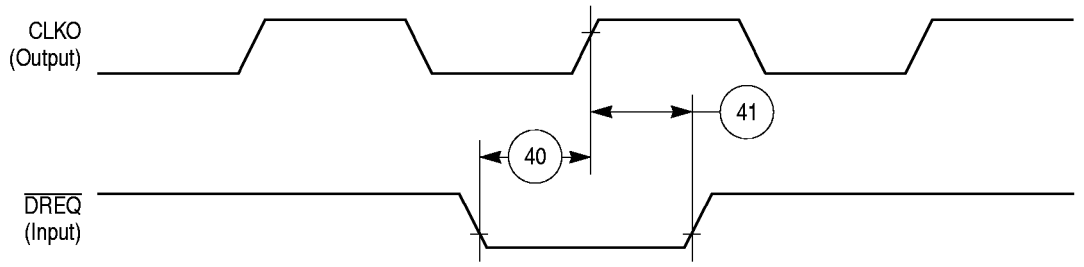


Figure 42. IDMA External Requests Timing Diagram

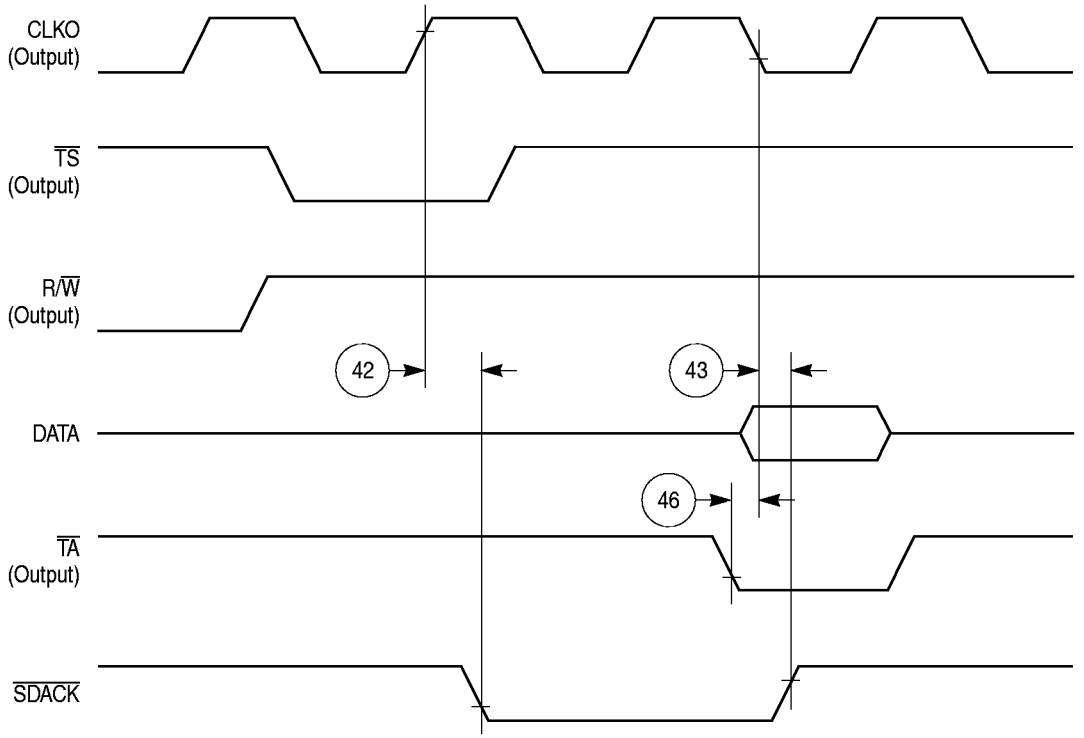


Figure 43. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

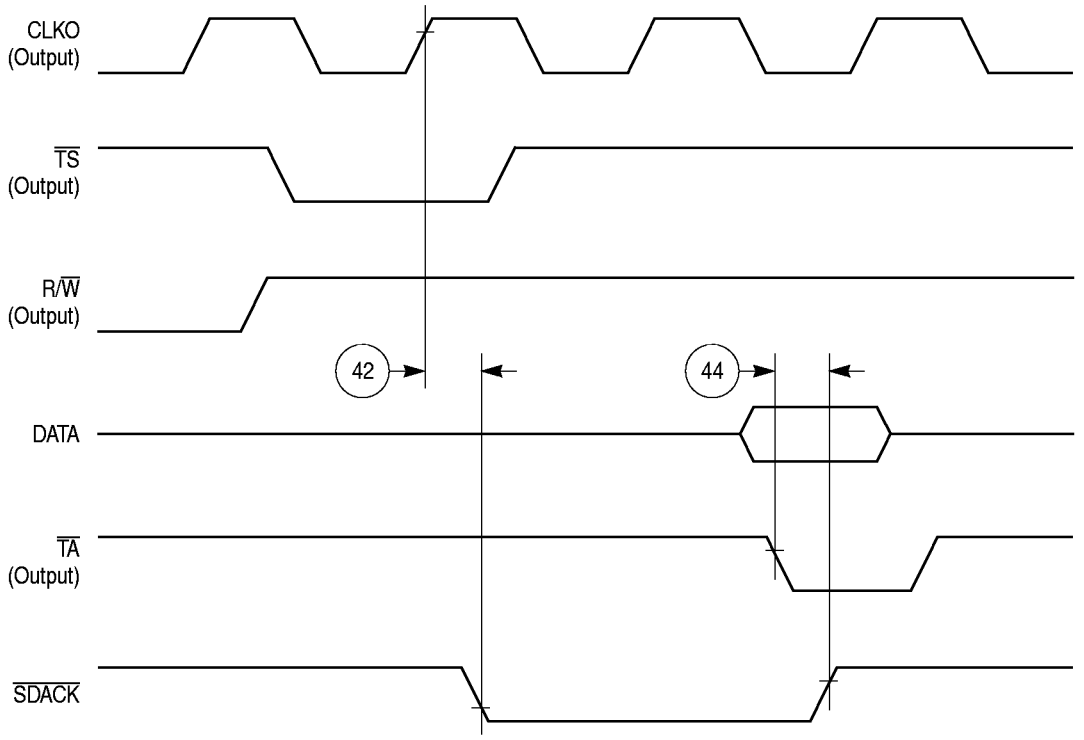


Figure 44. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock

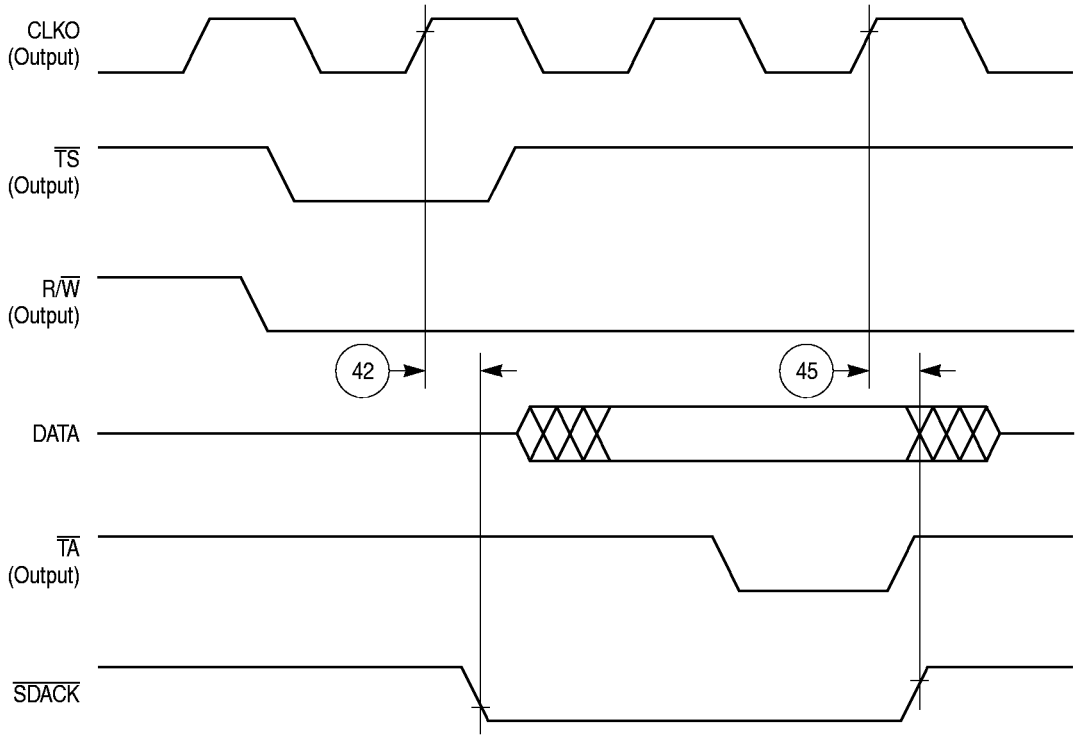


Figure 45. SDACK Timing Diagram—Peripheral Read

1.8.3 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 46.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

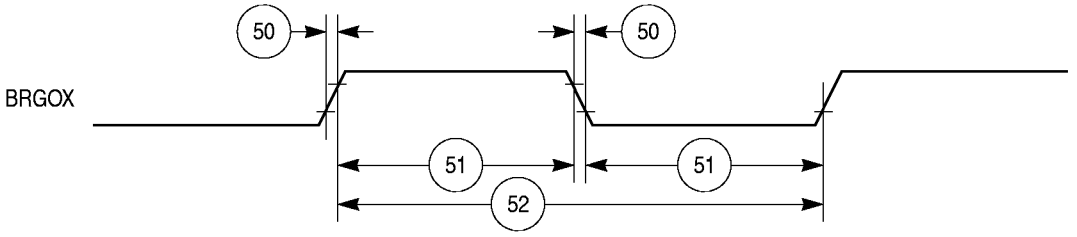


Figure 46. Baud Rate Generator Timing Diagram

1.8.4 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 47.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

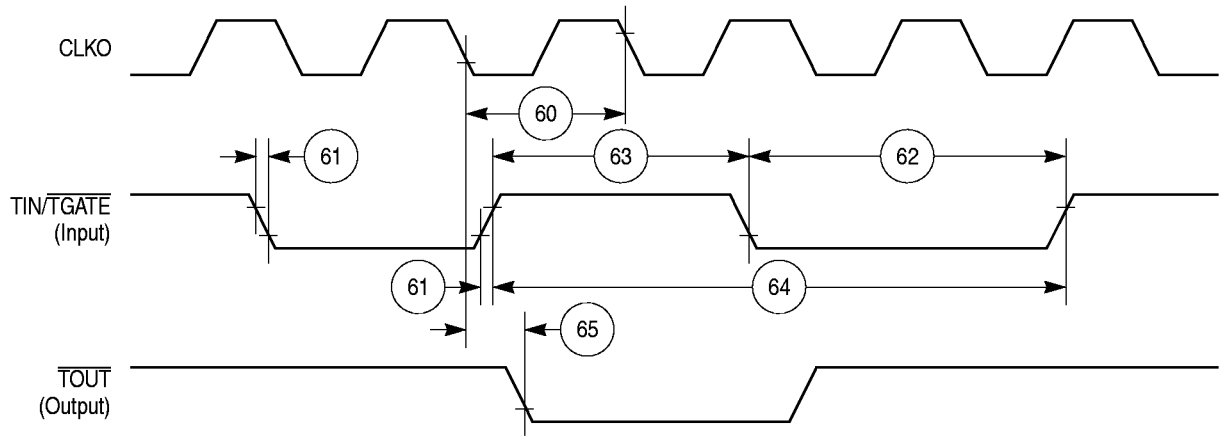


Figure 47. CPM General-Purpose Timers Timing Diagram

1.8.5 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 48 to Figure 52.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0)[1, 2]		SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10		ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10		ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time		15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge Edge (SYNC setup time)	20.00		ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00		ns
75	L1RSYNC, L1TSYNC rise/fall time		15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00		ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00		ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)		16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10		ns
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10		ns
84	L1CLK edge to L1CLKO valid (DSC = 1)		30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00		L1TCLK
86	L1GR setup time[2]	42.00		ns
87	L1GR hold time	42.00		ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)		0.00	ns

[1] The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

[2] These specs are valid for IDL mode only.

[3] Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

[4] These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

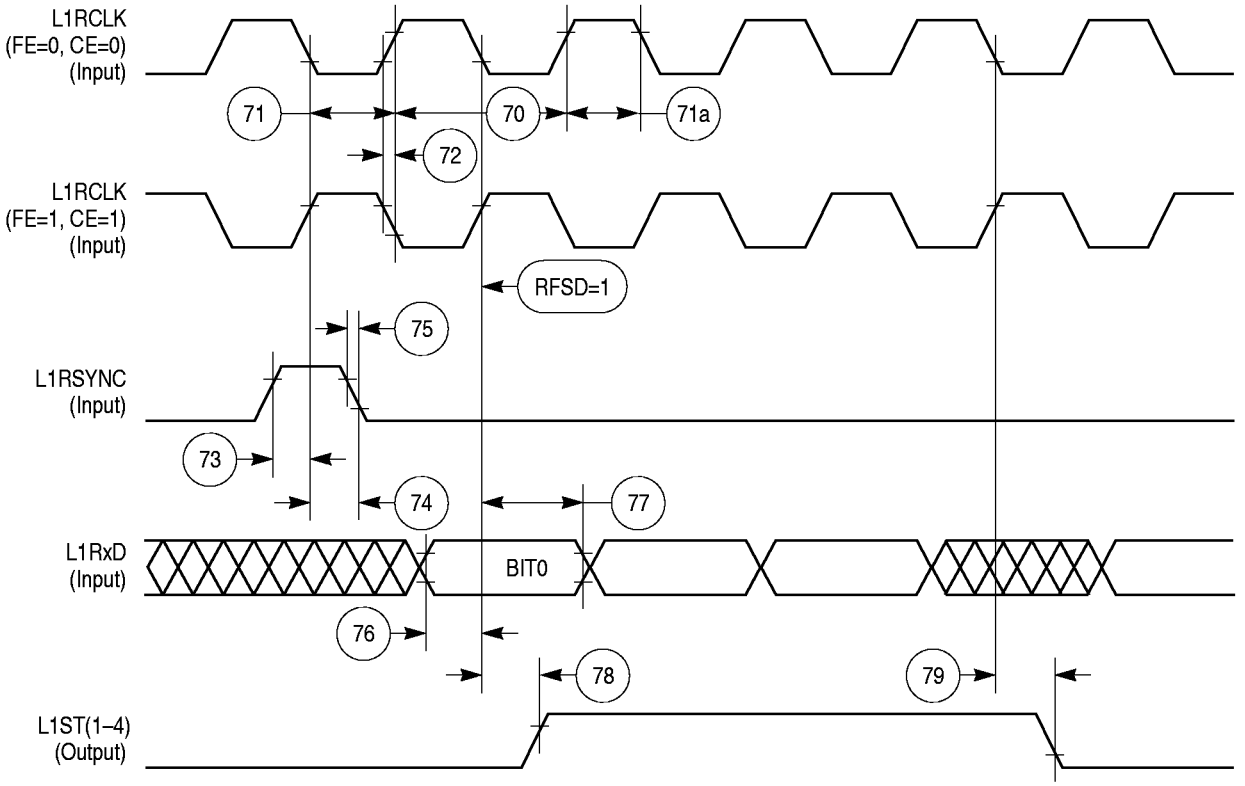


Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

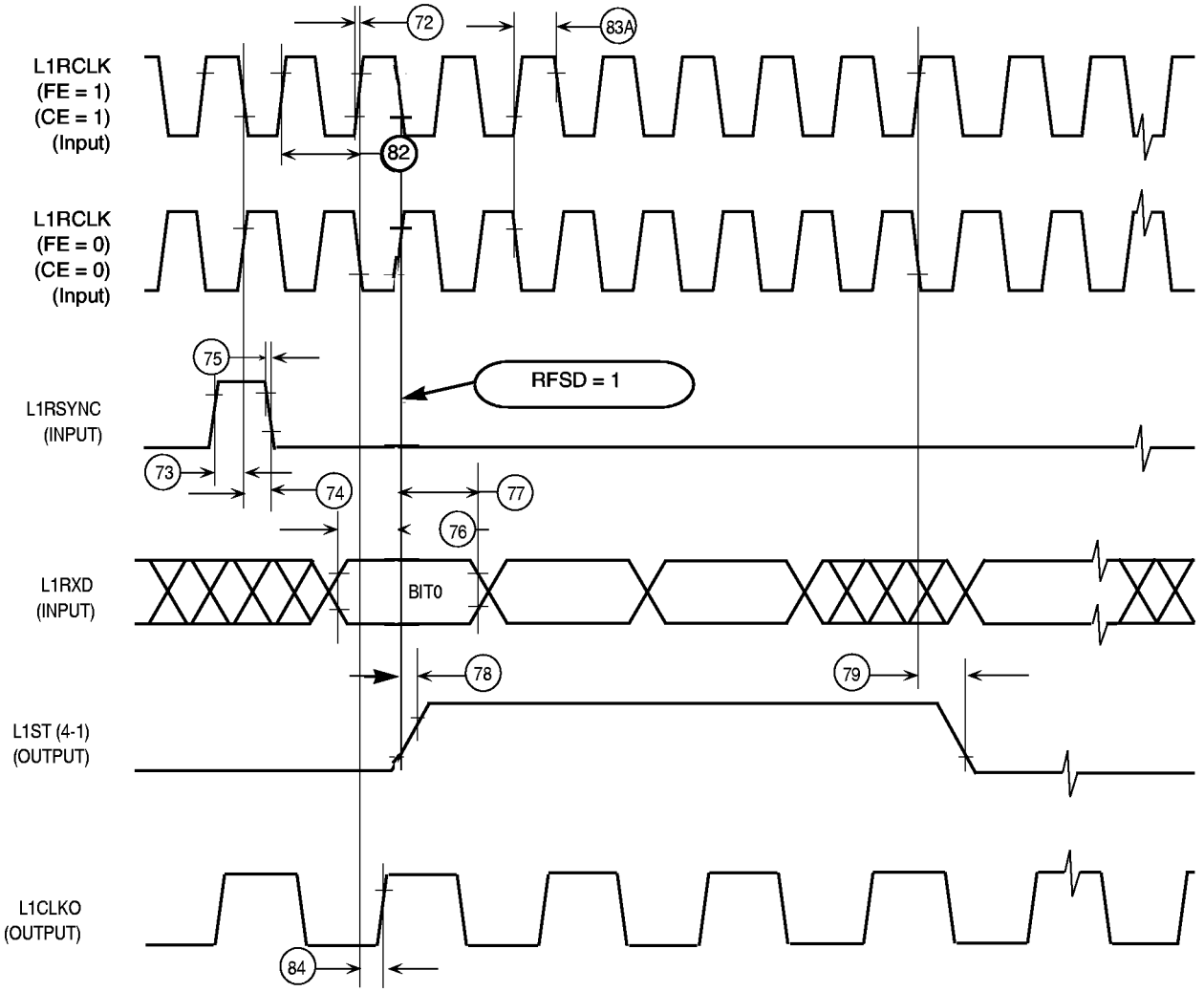


Figure 49. SI Receive Timing with Double-Speed Clocking (DSC = 1)

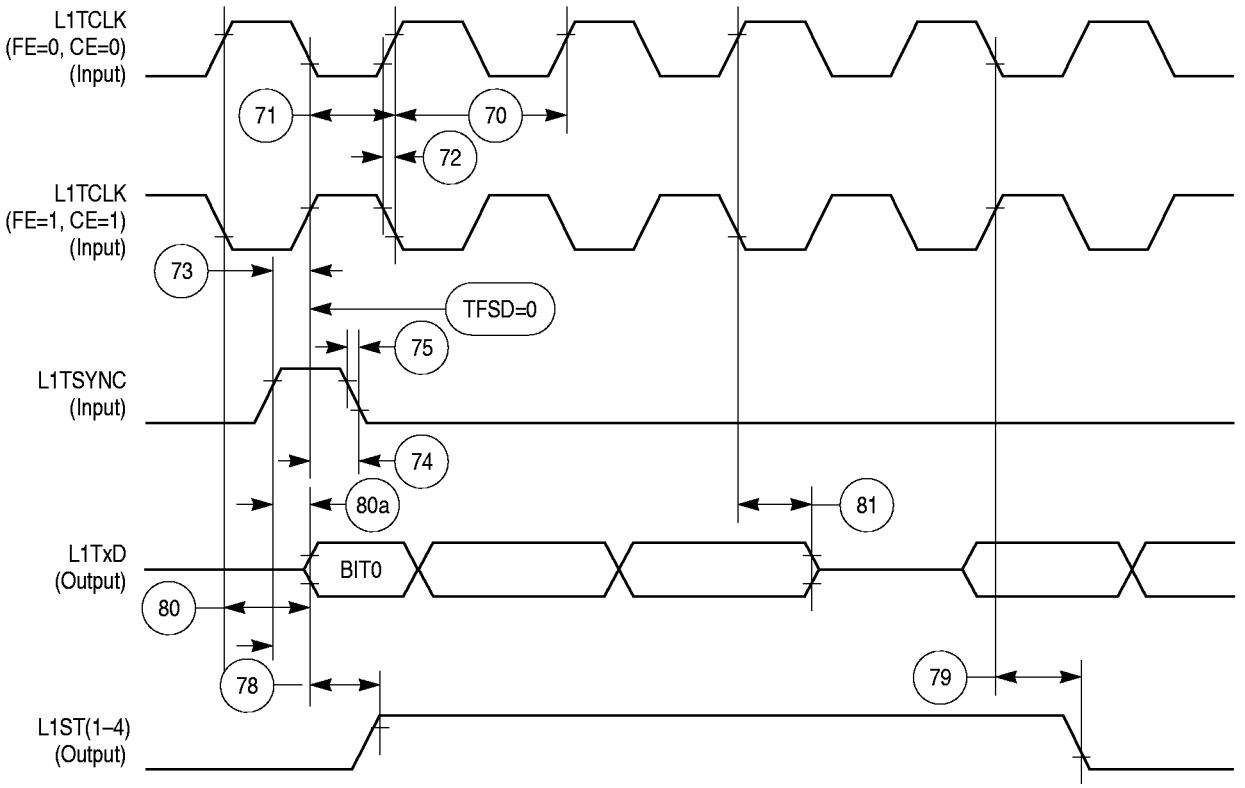


Figure 50. SI Transmit Timing Diagram (DSC = 0)

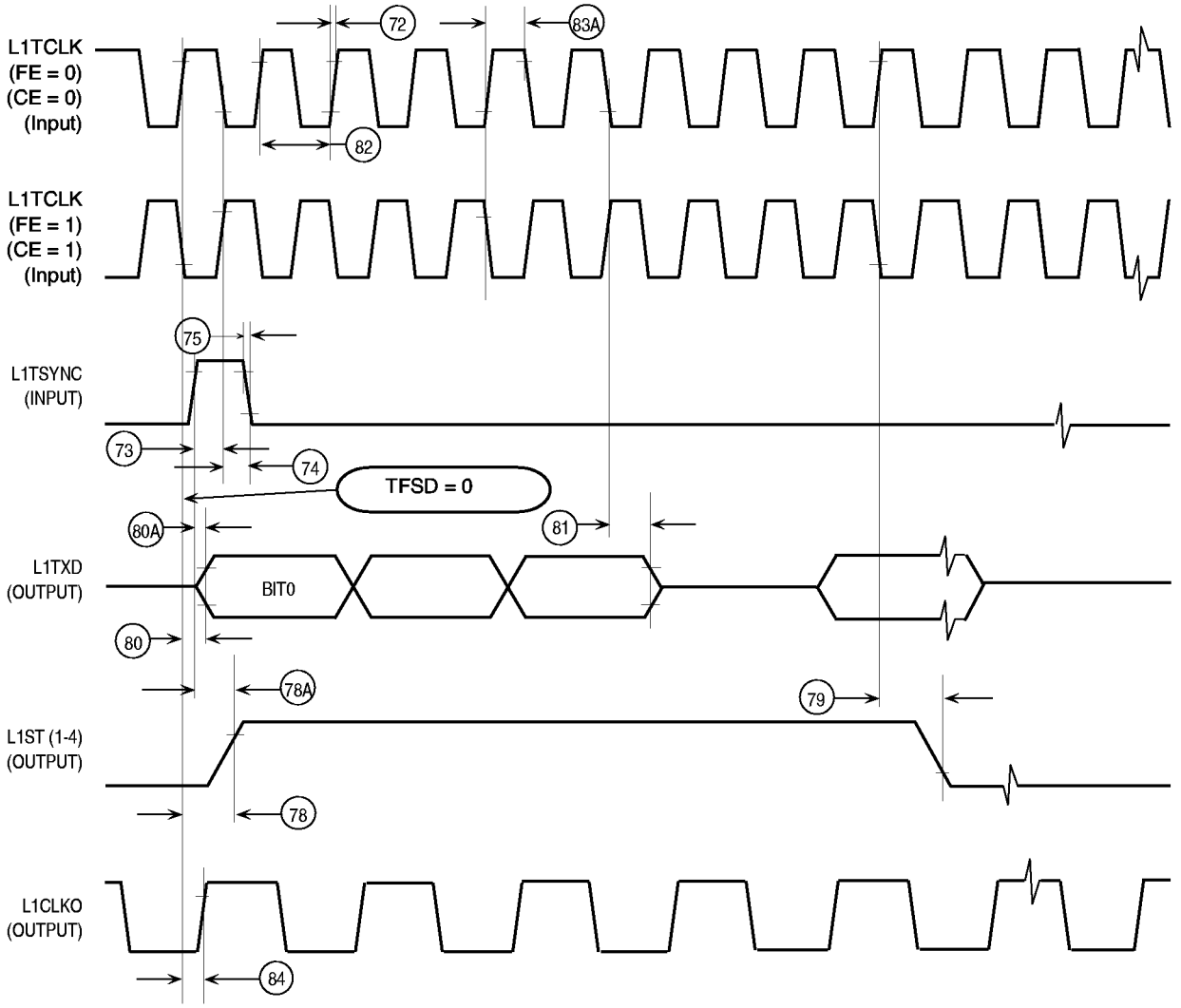


Figure 51. SI Transmit Timing with Double Speed Clocking (DSC = 1)

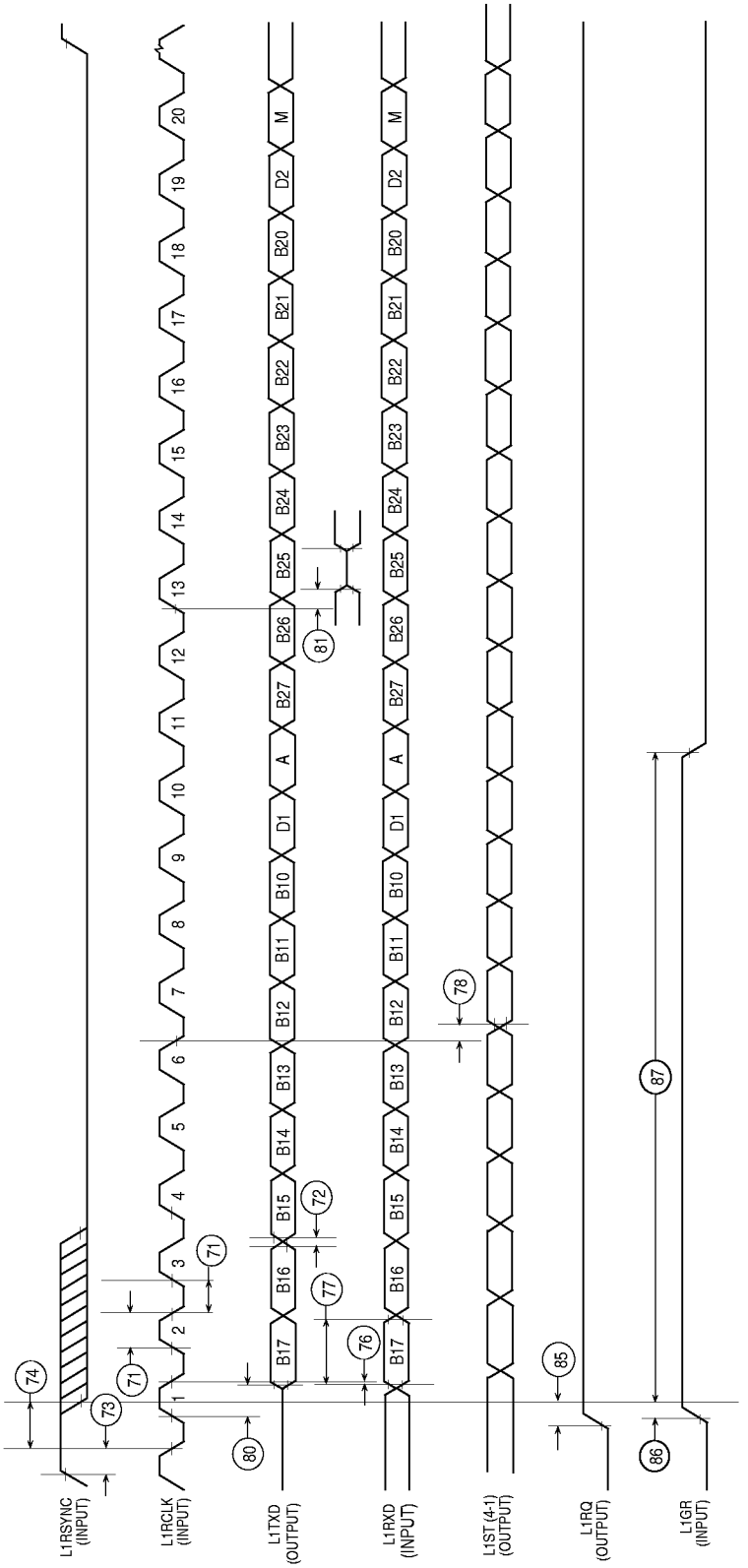


Figure 52. IDL Timing

1.8.6 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK		ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5		ns
102	RCLK1 and TCLK1 rise/fall time		15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00		ns
106	RXD1 setup time to RCLK1 rising edge	5.00		ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00		ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00		ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time			ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00		ns
106	RXD1 setup time to RCLK1 rising edge	40.00		ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00		ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00		ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Figure 53 through Figure 55 show the NMSI timings.

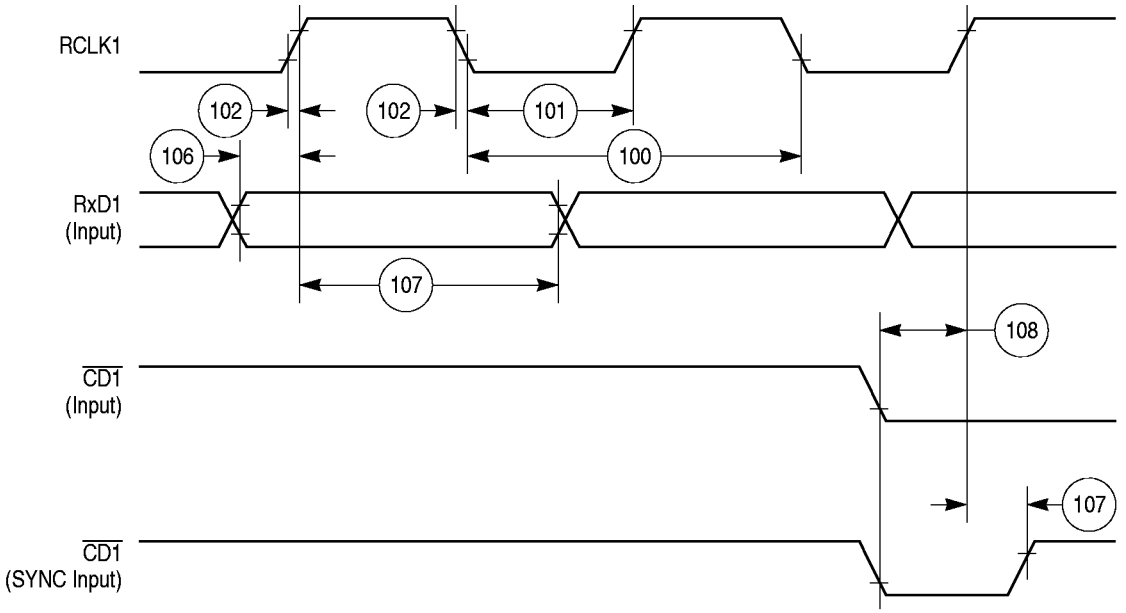


Figure 53. SCC NMSI Receive Timing Diagram

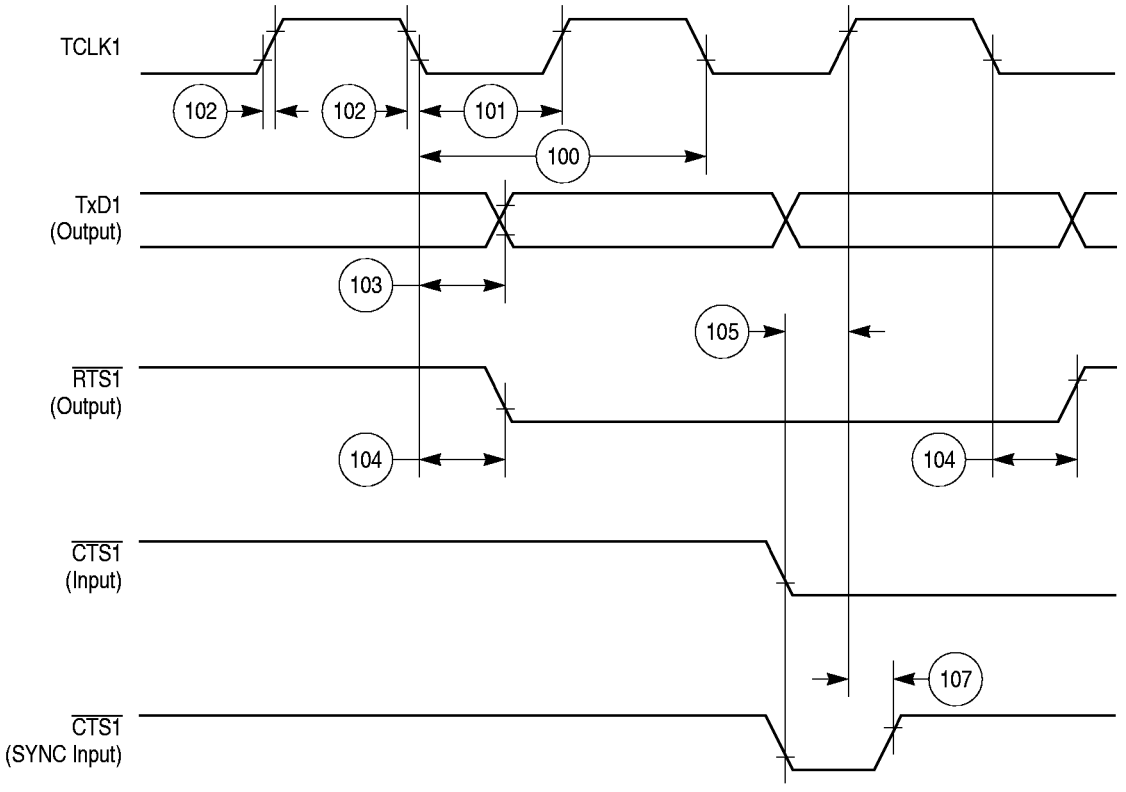


Figure 54. SCC NMSI Transmit Timing Diagram

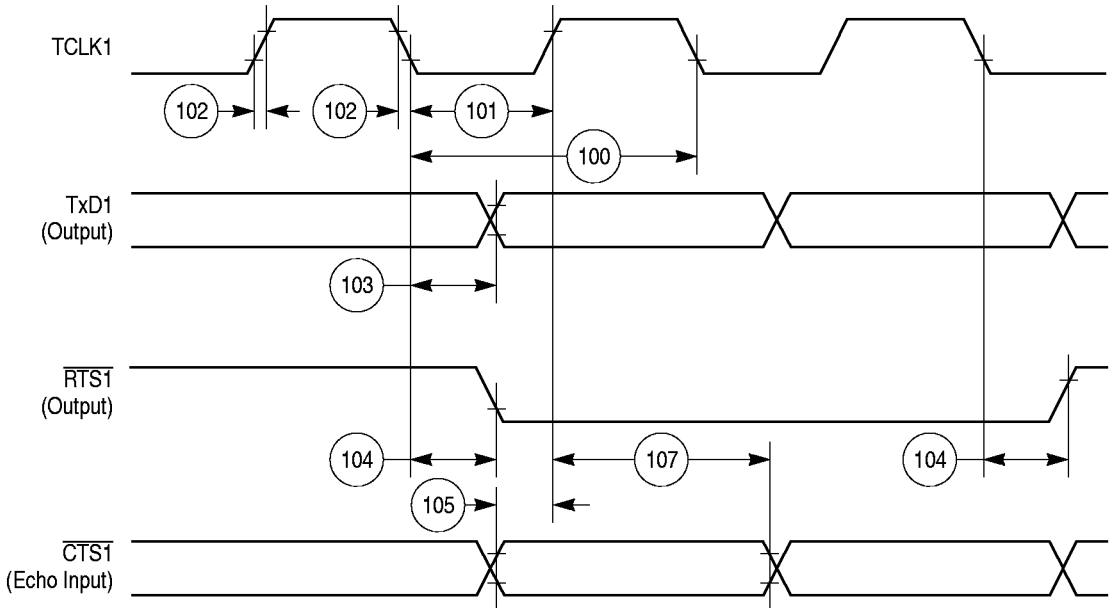


Figure 55. HDLC Bus Timing Diagram

1.8.7 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 56 to Figure 60.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

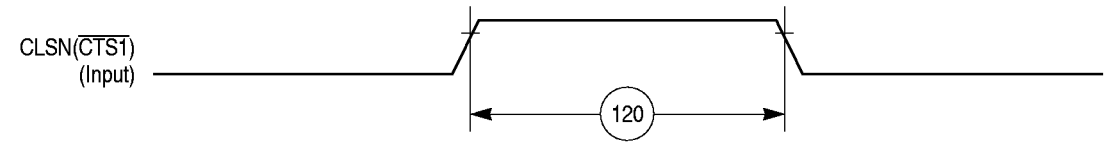


Figure 56. Ethernet Collision Timing Diagram

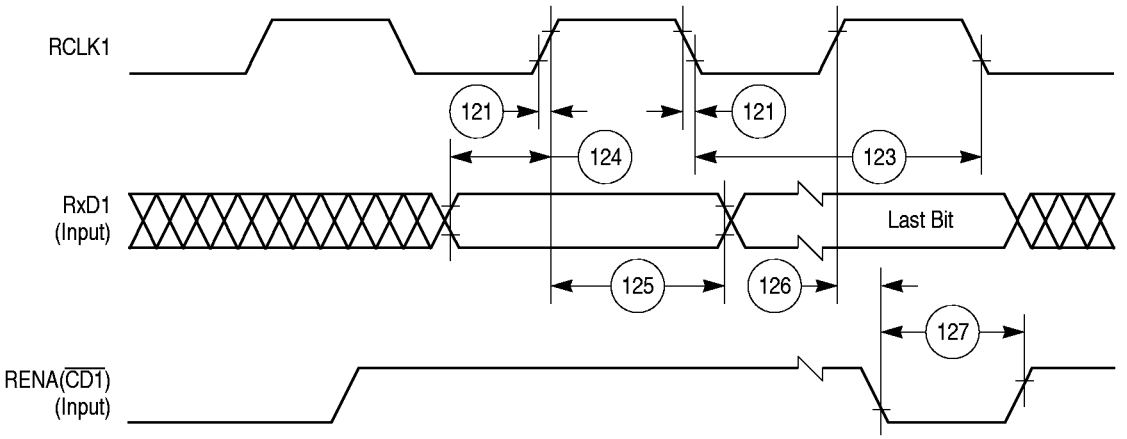
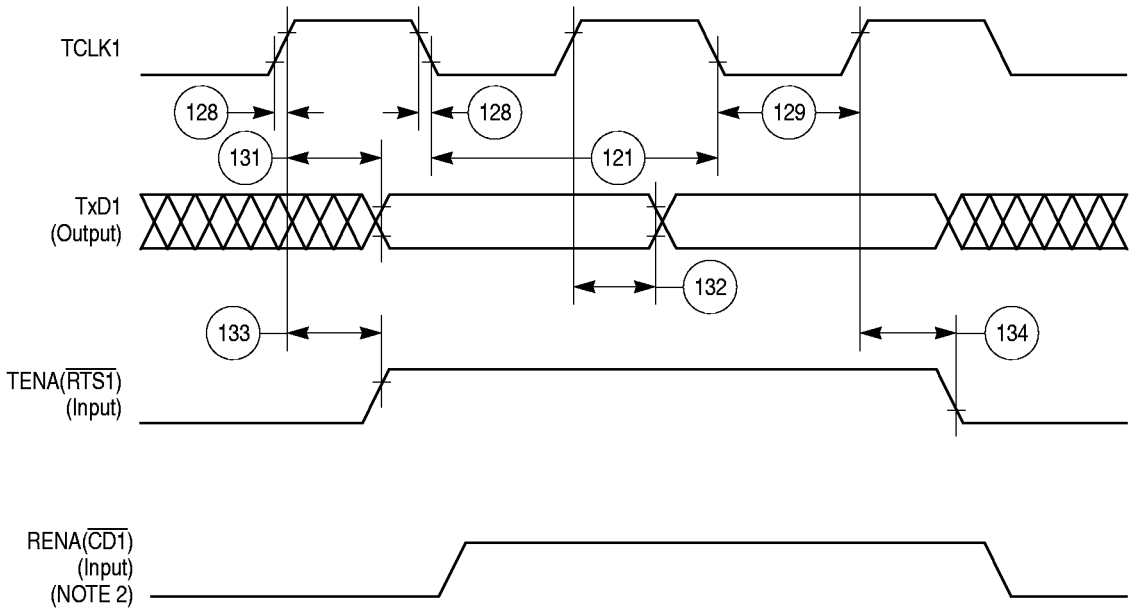


Figure 57. Ethernet Receive Timing Diagram



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 58. Ethernet Transmit Timing Diagram

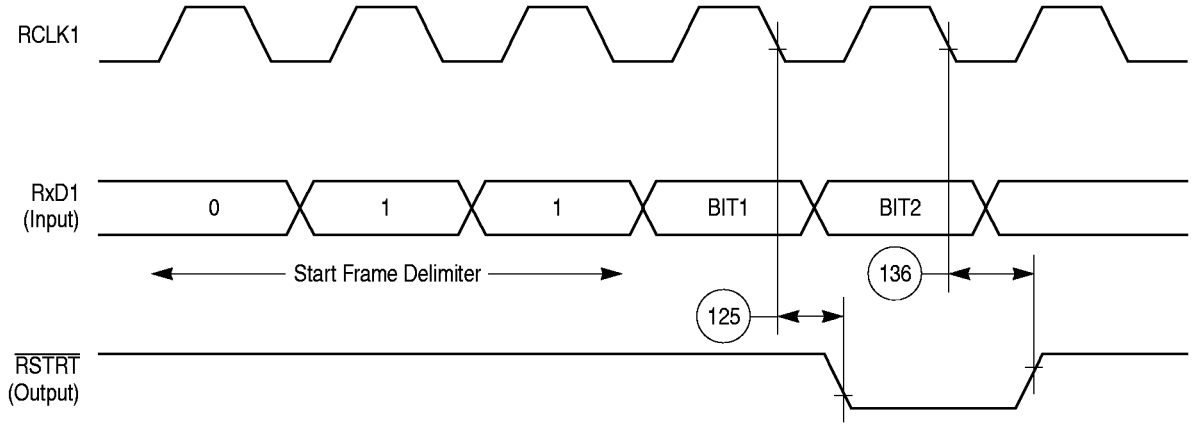


Figure 59. CAM Interface Receive Start Timing Diagram

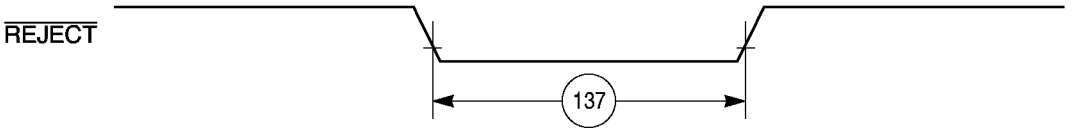


Figure 60. CAM Interface $\overline{\text{REJECT}}$ Timing Diagram

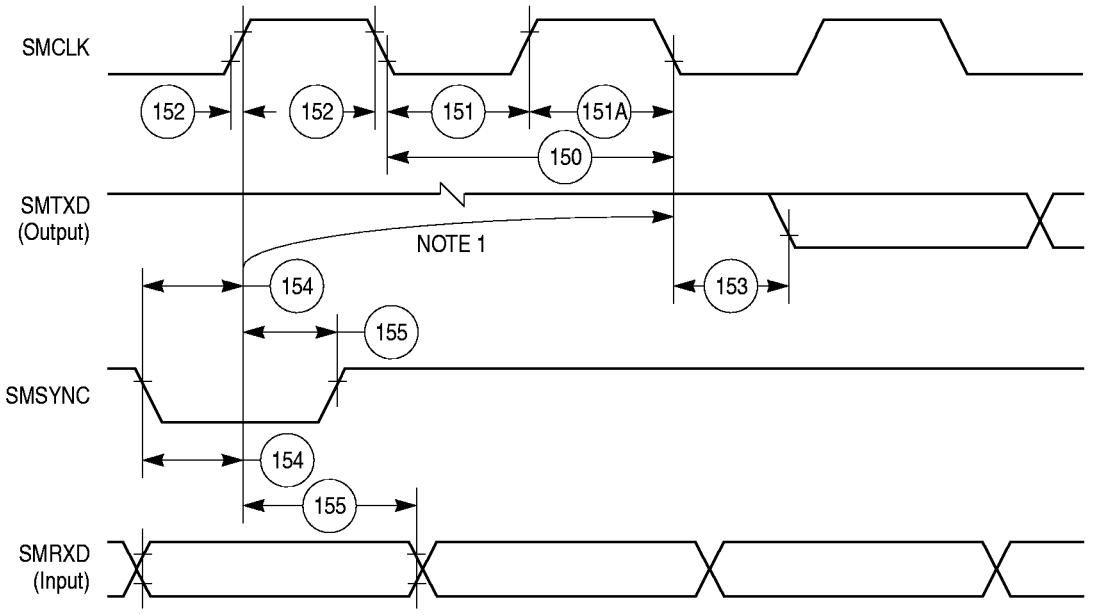
1.8.8 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 61.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] SyncCLK must be at least twice as fast as SMCLK.



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 61. SMC Transparent Timing Diagram

1.8.9 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 62 and Figure 63.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	20	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

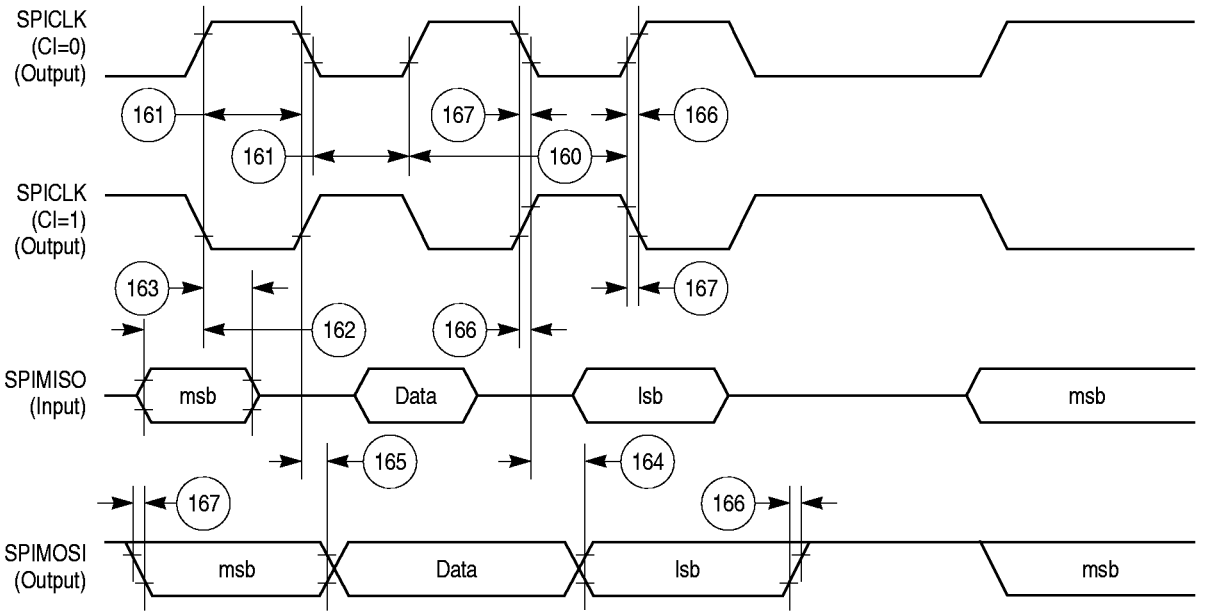


Figure 62. SPI Master (CP = 0) Timing Diagram

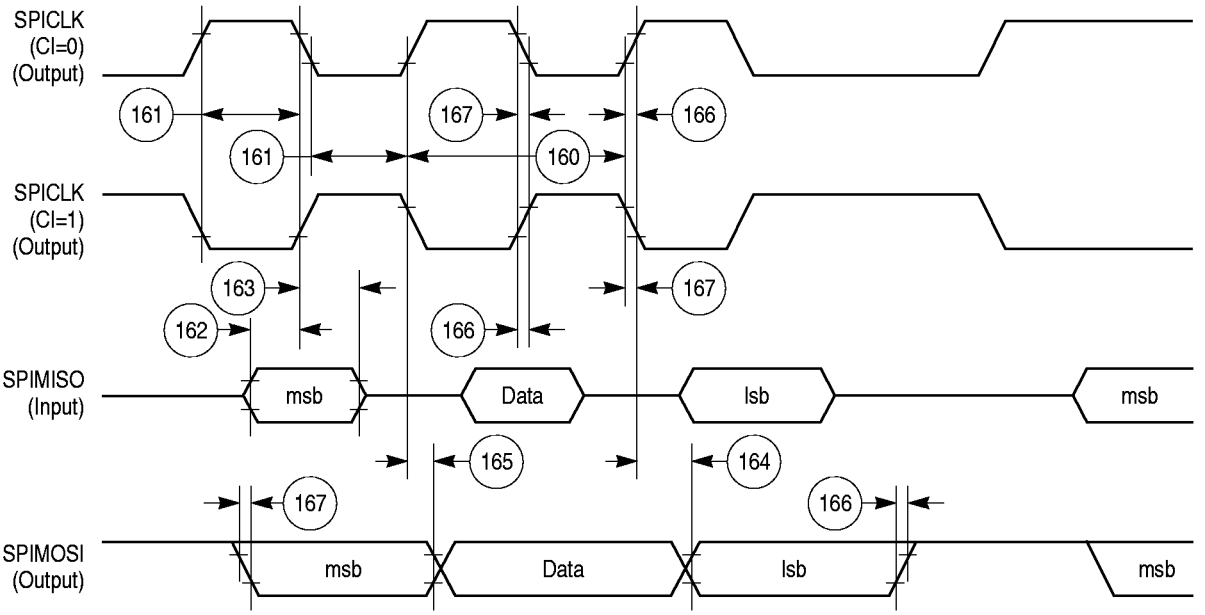


Figure 63. SPI Master (CP = 1) Timing Diagram

1.8.10 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 64 and Figure 65.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

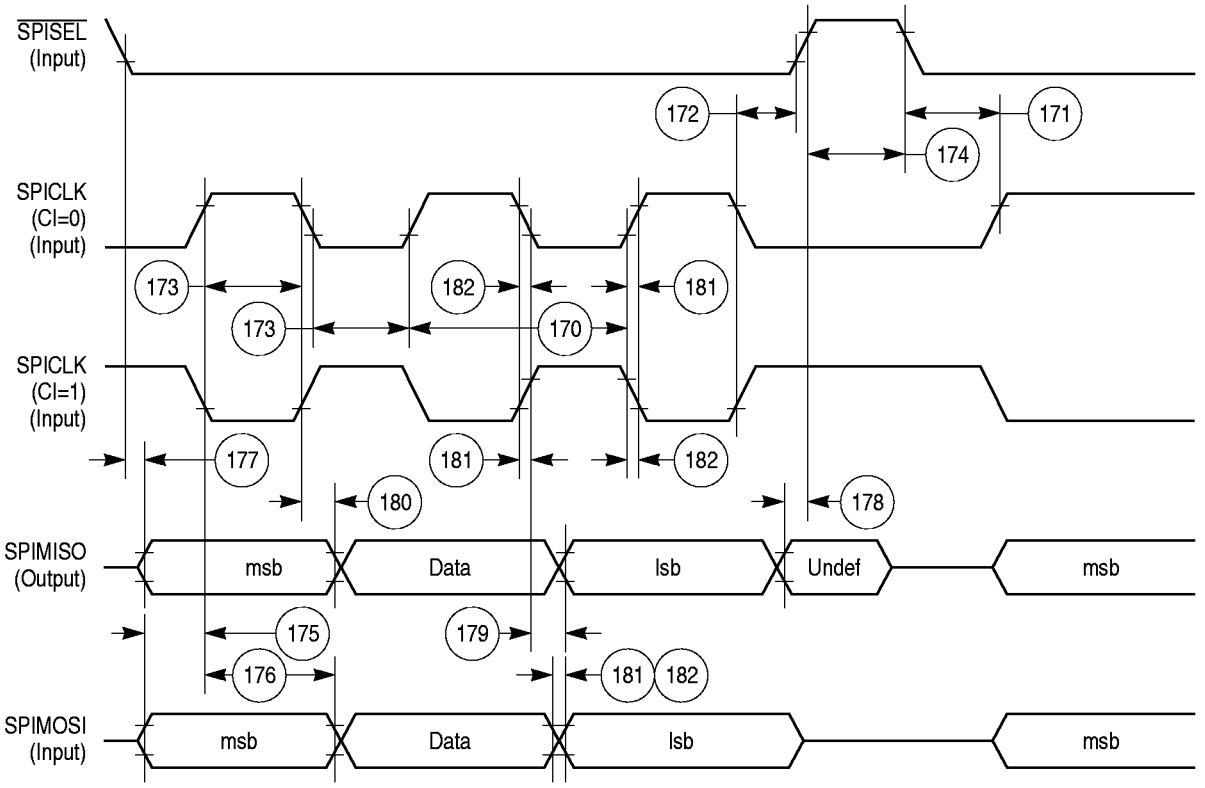


Figure 64. SPI Slave (CP = 0) Timing Diagram

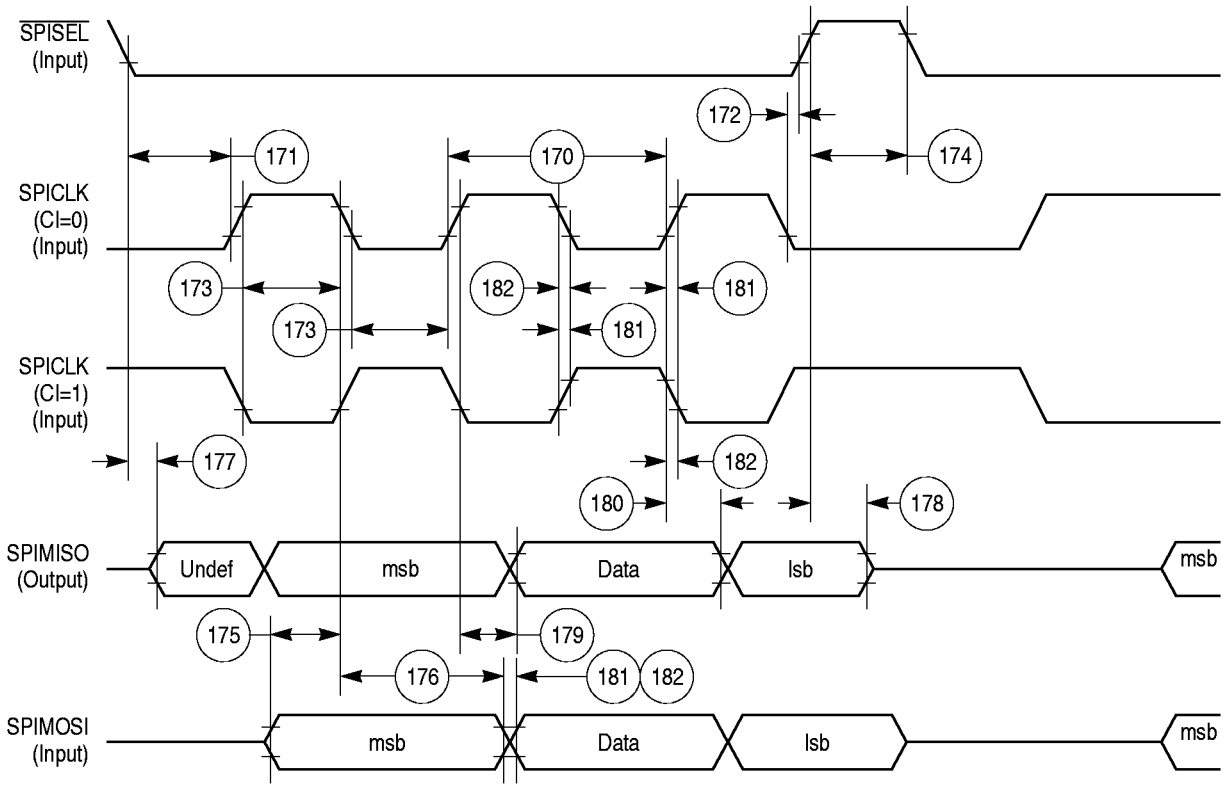


Figure 65. SPI Slave (CP = 1) Timing Diagram

1.8.11 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 KHz) timings.

Table 26. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	KHz
200	SCL clock frequency (master)[1]	1.5	100	KHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 KHz) timings.

Table 27. I^2C Timing (SCL > 100 KHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 66 shows the I^2C bus timing.

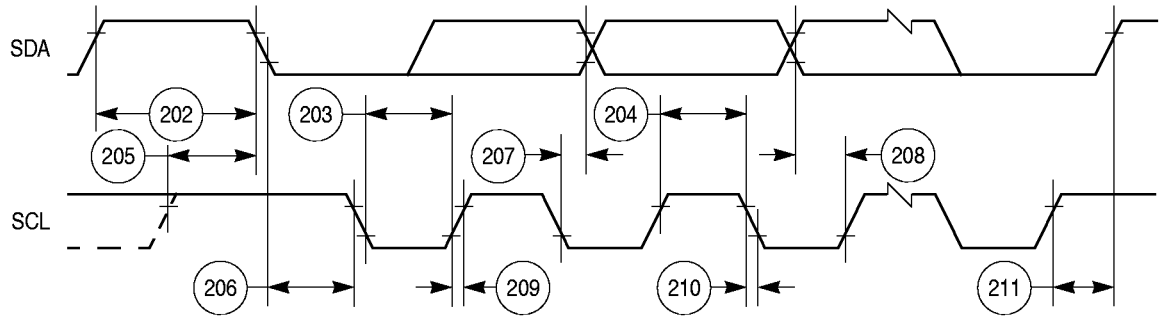


Figure 66. I^2C Bus Timing Diagram

1.9 Mechanical Data and Ordering Information

Table 28 provides information on the MPC860 revision C.1 derivative devices.

Table 28. MPC860 Revision C.1 Derivatives

Device	Number of SCCs[1]	Ethernet Support	Multi-Channel HDLC Support[2]	ATM Support
MPC860DC	Two	SCC1	N/A	N/A
MPC860DE		Yes	N/A	N/A
MPC860DH		Yes	Yes	N/A
MPC860	Four	N/A	N/A	N/A
MPC860EN		Yes	N/A	N/A
MPC860MH		Yes	Yes	N/A
MPC860SR		Yes	Yes	Yes

[1] Serial communications controller (SCC)

[2] 50-MHz version supports 64 time slots on a time-division multiplexed line using one SCC

Table 29 provides information on the MPC860 revision D.3 derivative devices.

Table 29. MPC860 Revision D.3 Derivatives

Device	Number of SCCs[1]	Ethernet Support	Multi-Channel HDLC Support	ATM Support
MPC860DE	Two	10 Mbps	N/A	N/A
MPC860DT		10/100 Mbps	Yes	Yes
MPC860DP		10/100 Mbps	Yes	Yes
MPC860EN	Four	10 Mbps	N/A	N/A
MPC860SR		10 Mbps	Yes	Yes
MPC860T		10/100 Mbps	Yes	Yes
MPC860P		10/100 Mbps	Yes	Yes

[1] Serial communications controller (SCC)

Table 30 identifies the packages and operating frequencies available for the MPC860 revision C.1.

Table 30. MPC860 Revision C.1 Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
Ball grid array (ZP suffix)	33	0°C to 95°C	XPC860ZP33C1 XPC860ENZP33C1 XPC860MHZP33C1 XPC860DCZP33C1 XPC860DEZP33C1 XPC860DHZP33C1 XPC860SRZP33C1
	50	0°C to 95°C	XPC860ZP50C1 XPC860ENZP50C1 XPC860MHZP50C1 XPC860DCZP50C1 XPC860DEZP50C1 XPC860DHZP50C1 XPC860SRZP50C1
	66	0°C to 95°C	XPC860ZP66C1 XPC860ENZP66C1 XPC860MHZP66C1 XPC860DCZP66C1 XPC860DEZP66C1 XPC860DHZP66C1 XPC860SRZP66C1
Ball grid array (CZP suffix)	33	-40°C to 95°C	XPC860CZP33C1 XPC860ENCZP33C1 XPC860MHCZP33C1 XPC860DCCZP33C1 XPC860DECZP33C1 XPC860DHCZP33C1 XPC860SRCZP33C1
	50		XPC860CZP50C1 XPC860ENCZP50C1 XPC860MHCZP50C1 XPC860DCCZP50C1 XPC860DECZP50C1 XPC860DHCZP50C1 XPC860SRCZP50C1

Table 31 identifies the packages and operating frequencies available for the MPC860 revision D.3.

Table 31. MPC860 Revision D.3 Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
Ball grid array (ZP suffix)	50	0°C to 95°C	XPC860DEZP50D3 XPC860DTZP50D3 XPC860ENZP50D3 XPC860SRZP50D3 XPC860TZP50D3
	66	0°C to 95°C	XPC860DEZP66D3 XPC860DTZP66D3 XPC860ENZP66D3 XPC860SRZP66D3 XPC860TZP66D3
	80	0°C to 95°C	XPC860DEZP80D3 XPC860DTZP80D3 XPC860ENZP80D3 XPC860SRZP80D3 XPC860TZP80D3
Ball grid array (CZP suffix)	50	-40°C to 95°C	XPC860DECZP50D3 XPC860DTCZP50D3 XPC860ENCZP50D3 XPC860SRCZP50D3 XPC860TCZP50D3
	66	-40°C to 95°C	XPC860DECZP66D3 XPC860DTCZP66D3 XPC860ENCZP66D3 XPC860SRCZP66D3 XPC860TCZP66D3

Table 32 identifies the packages and operating frequencies available for the MPC860P.

Table 32. MPC860P Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
Ball grid array (ZP suffix)	50	0°C to 95°C	XPC860DPZP50D3 XPC860PZP50D3
	66	0°C to 95°C	XPC860DPZP66D3 XPC860PZP66D3
	80	0°C to 95°C	XPC860DPZP80D3 XPC860PZP80D3
Ball grid array (CZP suffix)	50	-40°C to 95°C	XPC860DPCZP50D3 XPC860PCZP50D3
	66	-40°C to 95°C	XPC860DPCZP66D3 XPC860PCZP66D3

1.9.1 Pin Assignments

Figure 67 shows the pinout of the PBGA package as viewed from the top surface.

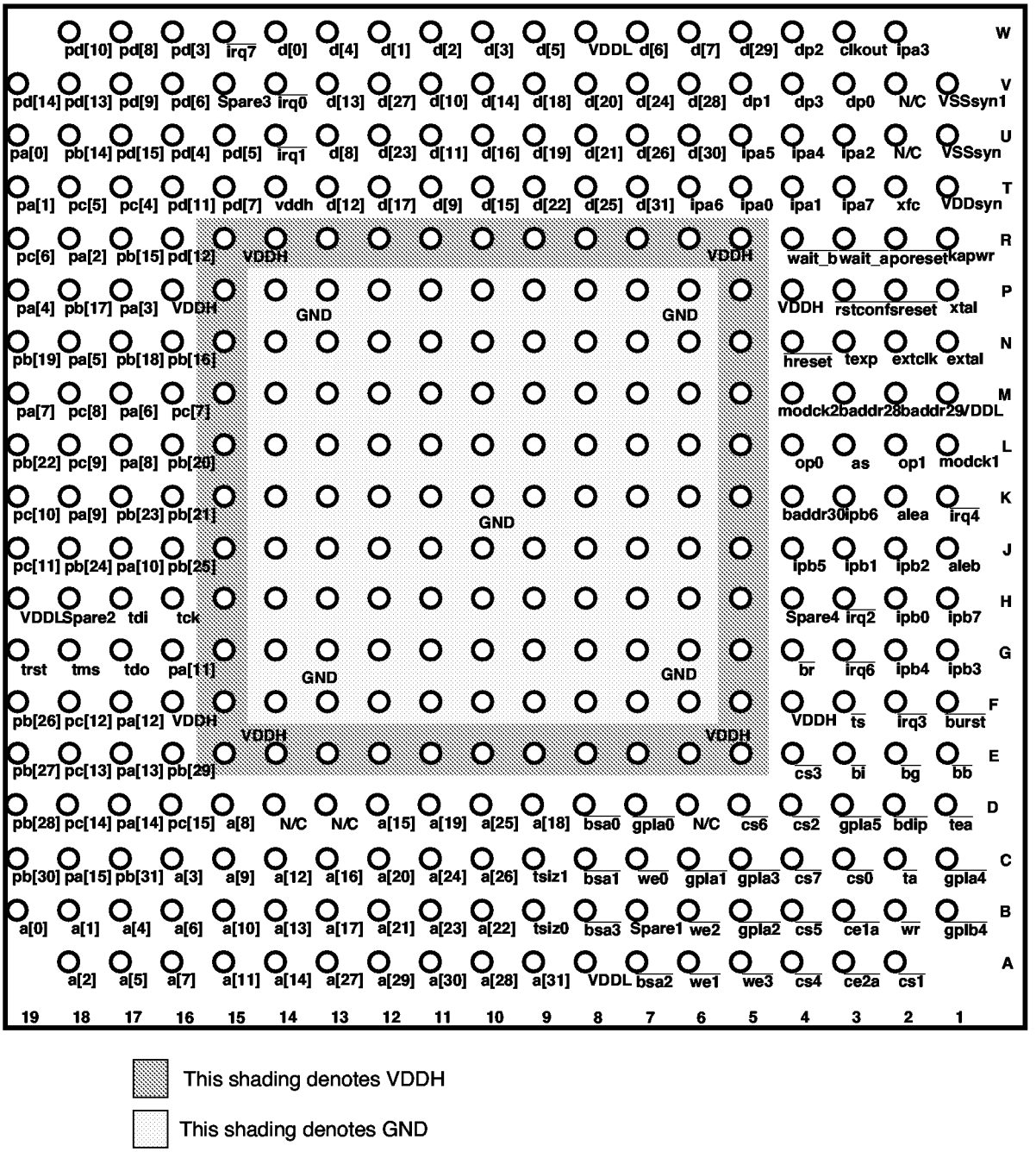
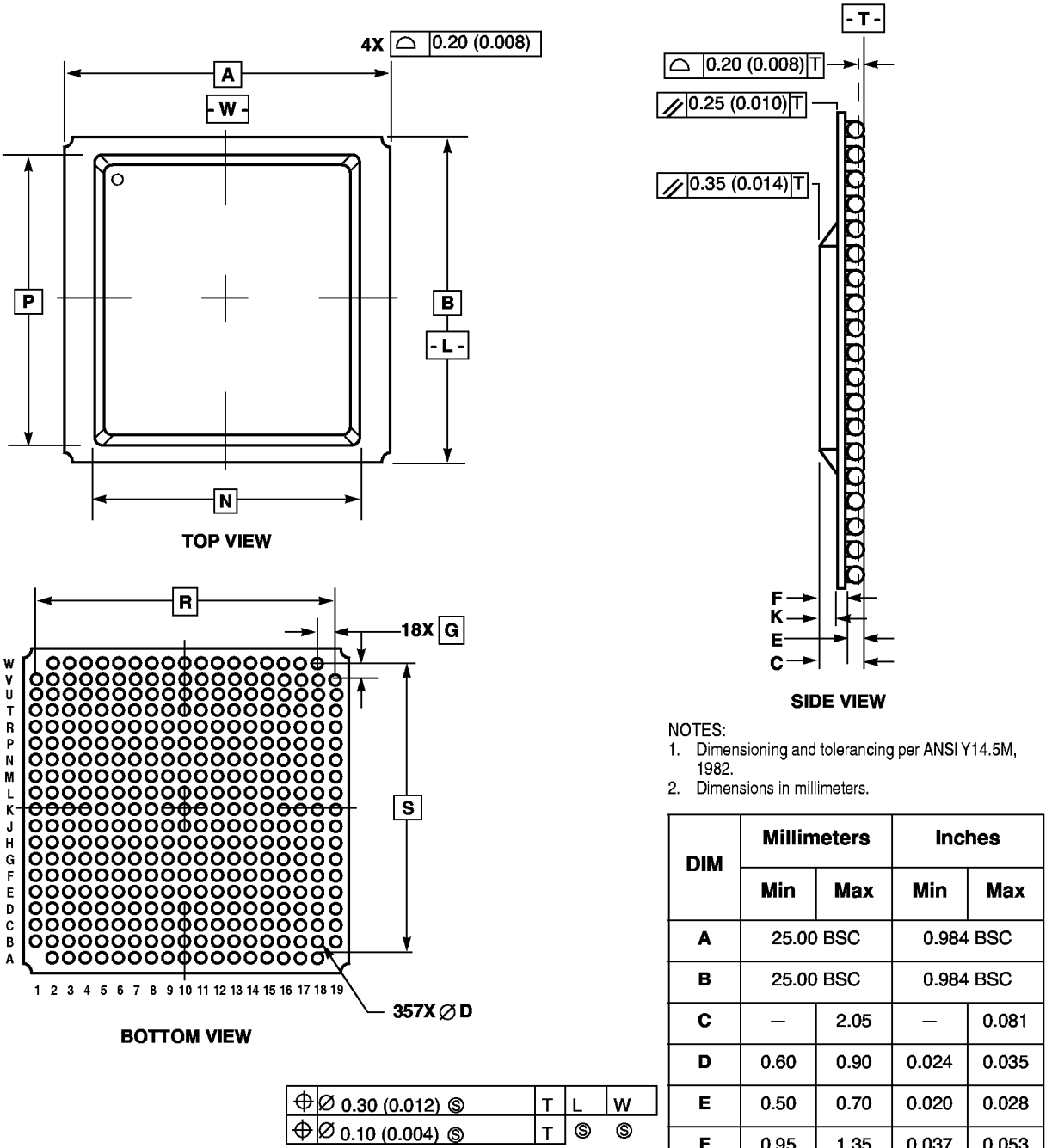


Figure 67. Pinout of the PBGA Package as Viewed from the Top Surface

1.9.2 Mechanical Dimensions of the PBGA

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Motorola sales office.



NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Dimensions in millimeters.

DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	—	2.05	—	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

Figure 68. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package