SECTION 2
ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS}, see Notes 1 and 2)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	− 0.5	7	V
Input Voltage, All Inputs	V_{in}	− 0.5	V_{DD} + 0.5	V
Output Voltage, All Outputs	V_{out}	− 0.5	V_{DD} + 0.5	V
Power Dissipation	P_D	—	1	W
Storage Temperature	T_{stg}	− 55	150	°C
Electrostatic Discharge (All except SCSI pins) (Note 3)	ESD	± 4000	—	V
Electrostatic Discharge (All SCSI pins) (Note 3)	ESD	± 4000	—	V

NOTES:
1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or pin descriptions section.
2. These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
   Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). except for inputs with pullup devices. Unused outputs must be left open.
3. Tested using human body model (100 pF @ 1.5 kΩ)

2.2 OPERATING CONDITIONS

Parameter	Test Condition	Symbol	Min	Max	Unit
DC Supply Voltage		V_{DD}	4.75	5.25	V
Supply Current	Static (Note 1)	I_{DD}	—	10	mA
Supply Current	Dynamic	I_{DD}	—	50	mA
Ambient Temperature		T_A	0	70	°C

NOTE:
1. Static conditions: All inputs at V_{SS}, all outputs floating, and all I/O pins configured as inputs.

2.3 DC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.75 V to 5.25 V, T_A = 0°C to 70°C)

2.3.1 Bidirectional Pins with Pullup Resistors (DB0–DB7, DBP, see Note 1)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\|I_{out}\| \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IH}	2	—	V
Maximum Input Low Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\|I_{out}\| \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IL}	—	0.8	V
Minimum Output High-Level Voltage	$I_{OH(Source)}$ = – 2 mA V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL(Sink)}$ = 4 mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OL}	—	0.4	V
Input Low Pullup Current	V_{in} = 0 V, V_{DD} = 5.25 V	$I_{IL(PU)}$	– 400	—	µA
Input High Pullup Current	V_{in} = V_{IH} min, V_{DD} = 5.25 V	$I_{IH(PU)}$	– 250	—	µA
Hi-Z Pullup Current	Output in High Impedance State, V_{out} = V_{DD} or V_{SS}, V_{in} = V_{DD} or V_{SS}, V_{DD} = 5.25 V	$I_{OZ(PU)}$	– 400	5	µA
Maximum I/O Pin Capacitance		C_{IO}	—	12	pF

NOTE:
1. The MCCS53C90A does not support the DBP signal.

2.3.2 Non-SCSI Input Pins (A0–A3, $\overline{CS}$, $\overline{DACK}$, $\overline{RD}$, $\overline{WR}$, DIFFM, RESET, CLOCK; see Note 1)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\|I_{out}\| \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IH}	2	—	V
Maximum Input Low Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\|I_{out}\| \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IL}	—	0.8	V
Input Leakage Current	V_{in} = V_{DD} or V_{SS}, V_{DD} = 5.25 V	I_{in}	– 1	1	µA
Maximum Input Pin Capacitance		C_{in}	—	12	pF

NOTE:
1. The MCCS53C90B does not support the DIFFM signal.

2.3.3 Bidirectional TGS with Pullup Resistor

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\|I_{out}\| \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IH}	3.1	—	V
Maximum Input Low Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\|I_{out}\| \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IL}	—	0.8	V
Minimum Output High-Level Voltage	$I_{OH(Source)} = -4$ mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL(Sink)}$ = 8 mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OL}	—	0.4	V
Input Low Pullup Current	V_{in} = 0 Volts, V_{DD} = 5.25 V	$I_{IL(PU)}$	– 400	—	µA
Input High Pullup Current	$V_{in} = V_{IH(min)}$, V_{DD} = 5.25 V	$I_{IH(PU)}$	– 250	—	µA
Hi-Z Pullup Current	Output in High Impedance State, V_{out} = V_{DD} or V_{SS}, V_{in} = V_{DD} or V_{SS}, V_{DD} = 5.25 V	$I_{OZ(PU)}$	– 400	5	µA
Maximum I/O Pin Capacitance		$C_{I/O}$	—	12	pF

2.3.4 Outputs DREQ, IGS

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Output High-Level Voltage	$I_{OH(Source)} = -2$ mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL(Sink)}$ = 4 mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, V_{out} = V_{DD} or V_{SS}, V_{in} = V_{DD} or V_{SS}, V_{DD} = 5.25 V	I_{OZ}	– 5	5	µA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.3.5 Output RESETO

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Output High-Level Voltage	$I_{OH(Source)} = -4$ mA, $V_{in} = V_{DD}$ or V_{SS}, $V_{DD} = 4.75$ V	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL(Sink)} = 8$ mA, $V_{in} = V_{DD}$ or V_{SS}, $V_{DD} = 4.75$ V	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{out} = V_{DD}$ or V_{SS}, $V_{in} = V_{DD}$ or V_{SS}, $V_{DD} = 5.25$ V	I_{OZ}	−5	5	µA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.3.6 Output $\overline{INT}$ (Open Drain)

Parameter	Test Condition	Symbol	Min	Max	Unit
Maximum Output Low-Level Voltage	$I_{OL(Sink)} = 8$ mA, $V_{in} = V_{DD}$ or V_{SS}, $V_{DD} = 4.75$ V	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{out} = V_{DD}$ or V_{SS}, $V_{in} = V_{DD}$ or V_{SS}, $V_{DD} = 5.25$ V	I_{OZ}	−5	5	µA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.3.7 SCSI Control Input Pins ($\overline{SELI}$, $\overline{BSYI}$, $\overline{REQI}$, $\overline{ACKI}$, $\overline{MSGI}$, $\overline{C\_DI}$, $\overline{I\_OI}$, $\overline{ATNI}$, $\overline{RSTI}$)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	$V_{out} = 0.1$ V or $V_{DD} - 0.1$ V, $\lvert I_{out} \rvert \leq 20$ µA, $V_{DD} = 4.75$ or 5.25 V	V_{IH}	2	—	V
Maximum Input Low Voltage	$V_{out} = 0.1$ V or $V_{DD} - 0.1$ V, $\lvert I_{out} \rvert \leq 20$ µA, $V_{DD} = 4.75$ or 5.25 V	V_{IL}	—	0.8	V
Minimum Hysterisis Voltage	$V_{out} = 0.1$ V or $V_{DD} - 0.1$ V, $\lvert I_{out} \rvert \leq 20$ µA, $V_{DD} = 4.75$ V	V_H	200	—	mV
Input Leakage Current	$V_{in} = V_{DD}$ or V_{SS}, $V_{DD} = 5.25$ V	I_{in}	−1	1	µA
Maximum Input Pin Capacitance		C_{in}	—	12	pF

2.3.8 SCSI Bidirectional Pins ($\overline{SDI7}$–$\overline{SDI0}$, $\overline{SDIP}$)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\lvert I_{out} \rvert \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IH}	2	—	V
Maximum Input Low Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\lvert I_{out} \rvert \leq 20\ \mu A$, V_{DD} = 4.75 or 5.25 V	V_{IL}	—	0.8	V
Minimum Hysterisis Voltage	V_{out} = 0.1 V or V_{DD} – 0.1 V $\lvert I_{out} \rvert \leq 20\ \mu A$, V_{DD} = 4.75 V	V_H	200	—	mV
Minimum Output High-Level Voltage	$I_{OH(Source)}$ = – 2 mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL(Sink)}$ = 4 mA V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, V_{out} = V_{DD} or V_{SS}, V_{in} = V_{DD} or V_{SS}, V_{DD} = 5.25 V	I_{OZ}	– 5	5	µA
Maximum I/O Pin Capacitance		$C_{I/O}$	—	12	pF

2.3.9 SCSI Output Pins ($\overline{SDO0}$–$\overline{SDO7}$, $\overline{SDOP}$, $\overline{SELO}$, $\overline{BSYO}$, $\overline{REQO}$, $\overline{ACKO}$, $\overline{MSGO}$, $\overline{C\_DO}$, $\overline{I\_OO}$, $\overline{ATNO}$, $\overline{RSTO}$)

Parameter	Test Condition	Symbol	Min	Max	Unit
Maximum Output High-Level Voltage	$I_{OH(Source)}$ = 16 mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL(Sink)}$ = 48 mA, V_{in} = V_{DD} or V_{SS}, V_{DD} = 4.75 V	V_{OL}	—	0.5	V
Hi-Z Leakage Current	Output in High Impedance State, V_{out} = V_{DD} or V_{SS}, V_{in} = V_{DD} or V_{SS}, V_{DD} = 5.25 V	I_{OZ}	– 5	5	µA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.4 AC ELECTRICAL CHARACTERISTICS (0°–70°C, V_{DD} = 4.75 to 5.25 V)

2.4.1 Pad Termination

Pin	Termination
RESETO, DREQ, TGS, IGS	50 pF
$\overline{SDIP}$, $\overline{SDI7}$ . . . $\overline{SDI0}$	50 pF
$\overline{INT}$	50 pF 1 kΩ pullup
DB7 . . . DB0, DBP	85 pF
$\overline{RSTO}$, $\overline{SELO}$, $\overline{BSYO}$, $\overline{ATNO}$, $\overline{MSGO}$, $\overline{CDO}$, $\overline{IOO}$, $\overline{REQO}$, $\overline{ACKO}$, SDO7. . . SDO0, $\overline{SDOP}$	200 pF 110 Ω pullup, 165 Ω pulldown

2.4.2 Clock

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_1	Clock Period	t_{CP}	25	—	ns	
t_2	Clock Frequency	f_{CP}	—	40	MHz	1, 3
t_3	Clock High Time	t_{CH}	0.4 × t_{CP}	—	ns	2
t_4	Clock Low Time	t_{CL}	0.4 × t_{CP}	—	ns	2

NOTES:
1. There are no minimum frequency requirements. 40 MHz is recommended for FAST SCSI synchronous mode.
2. For synchronous mode and an odd sync period, $| t_{CL} - t_{CH} | \leq 5$ nanoseconds.
3. For $f_{CP} > 25$ MHz set prescale bit (clock conversion register).

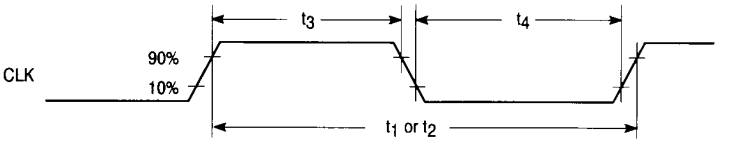

Figure 2.1. Clock Timing

2.4.3 Reset Input

Time	Parameter	Symbol	Min	Max	Unit
t_5	RESET Pulse Width	$t_{W(RST)}$	80	—	ns
t_6	RESET High to RESETO High	t_{RH}	—	50	ns
t_7	RESET Low to RESETO Low	t_{RL}	—	55	ns

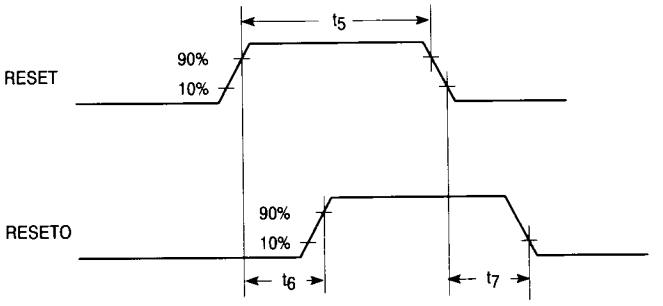

Figure 2.2. Reset Input Timing

2.4.4 Interrupt Output

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_8	$\overline{INT}$ to $\overline{RD}$ (Interrupt Reg read)	t_{IR}	0	—	ns	1, 2
t_9	$\overline{RD}$ Low to $\overline{INT}$ High ($\overline{CS}$ active)	t_{RI}	—	100	ns	1, 2
t_{10}	$\overline{RD}$ High to $\overline{INT}$ Low ($\overline{CS}$ active)	t_{RDI}	—	100	ns	1, 2

NOTES:
1. All timing based on an Interrupt Register read. Reference Register Read timing information for control line timing information.
2. The Interrupt register should not be read when $\overline{INT}$ is inactive.

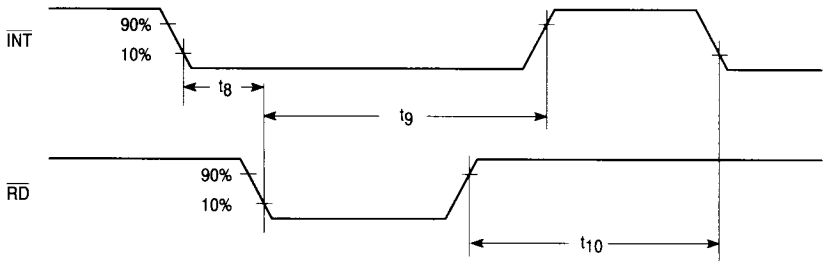

Figure 2.3. Interrupt Output Timing

2.4.5 Register Write

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_{11}	Address Setup to $\overline{CS}$ Low	$t_{su(AD)}$	0	—	ns	1, 2
t_{12}	$\overline{CS}$ Setup to $\overline{WR}$	$t_{su(WR)}$	0	—	ns	1, 3
t_{13}	$\overline{WR}$ Pulse Width	$t_{w(WR)}$	40	—	ns	1
t_{14}	Data Setup to $\overline{WR}$ High	$t_{su(DW)}$	11	—	ns	1, 3
t_{15}	Address Hold Time from $\overline{CS}$	$t_{h(ACS)}$	50	—	ns	1, 2
t_{16}	Data Hold Time from $\overline{WR}$ High	$t_{h(DWR)}$	2	—	ns	1, 3
t_{17}	$\overline{WR}$ High to $\overline{CS}$ High	t_{WC}	0	—	ns	1, 3
t_{18}	$\overline{CS}$ High to $\overline{CS}$ Low	$t_{c(CS)}$	40	—	ns	1, 3
t_{19}	$\overline{WR}$ High to $\overline{WR}$ Low	$t_{c(WR)}$	60	—	ns	1

NOTES:
1. $\overline{DACK}$ must be inactive during all register I/O cycles.
2. $\overline{CS}$ must cycle to capture a new register address.
3. $\overline{WR}$ edges may precede or follow $\overline{CS}$ edges. If $\overline{WR}$ is held low, data setup to $\overline{CS}$ high is 25 ns minimum; data hold from $\overline{CS}$ high is 60 ns minimum; and $t_{c(CS)}$ is 60 ns minimum.

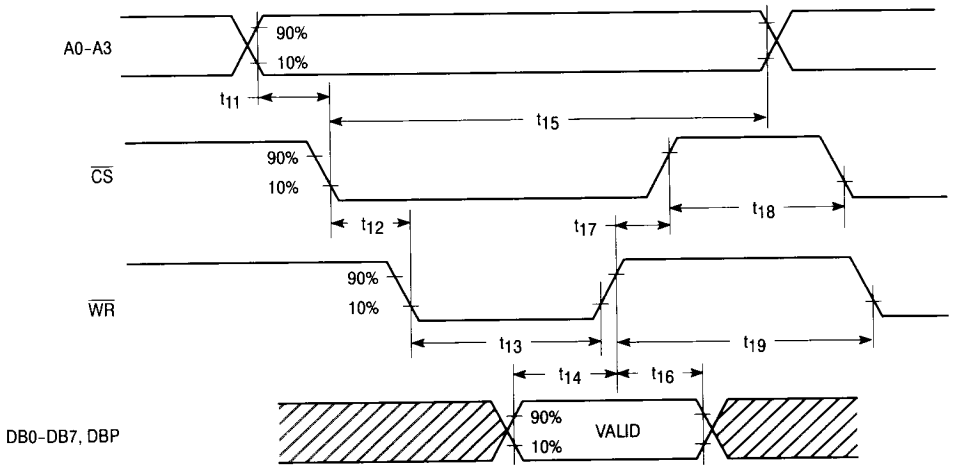

Figure 2.4. Register Write Timing

2.4.6 Register Read

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_{20}	Address Setup to $\overline{CS}$ Low	$t_{su(AD)}$	0	—	ns	1, 2
t_{21}	$\overline{CS}$ Setup to $\overline{RD}$	$t_{su(RD)}$	0	—	ns	1, 3
t_{22}	$\overline{RD}$ Pulse Width	$t_{w(WR)}$	50	—	ns	1
t_{23}	$\overline{RD}$ to Data Valid	$t_{su(DW)}$	—	50	ns	1, 3
t_{24}	$\overline{CS}$ to Data Valid	$t_{h(CSD)}$	—	70	ns	1
t_{25}	Address Hold Time from $\overline{CS}$	$t_{h(ACS)}$	50	—	ns	1, 2
t_{26}	Data Release Time	$t_{h(D)}$	2	40	ns	1, 3
t_{27}	$\overline{RD}$ High to $\overline{CS}$ High	$t_{c(RDCS)}$	0	—	ns	1, 3
t_{28}	$\overline{CS}$ High to $\overline{CS}$ Low	$t_{c(CD)}$	40	—	ns	1

NOTES:
1. $\overline{DACK}$ must be inactive during all register I/O cycles.
2. $\overline{CS}$ must cycle to capture a new register address.
3. $\overline{RD}$ edges may precede or follow $\overline{CS}$ edges. If $\overline{RD}$ is held low, the time from $\overline{CS}$ low to stable data is $t_{h(CSD)}$ and the data release time from $\overline{CS}$ high is $t_{h(D)}$.

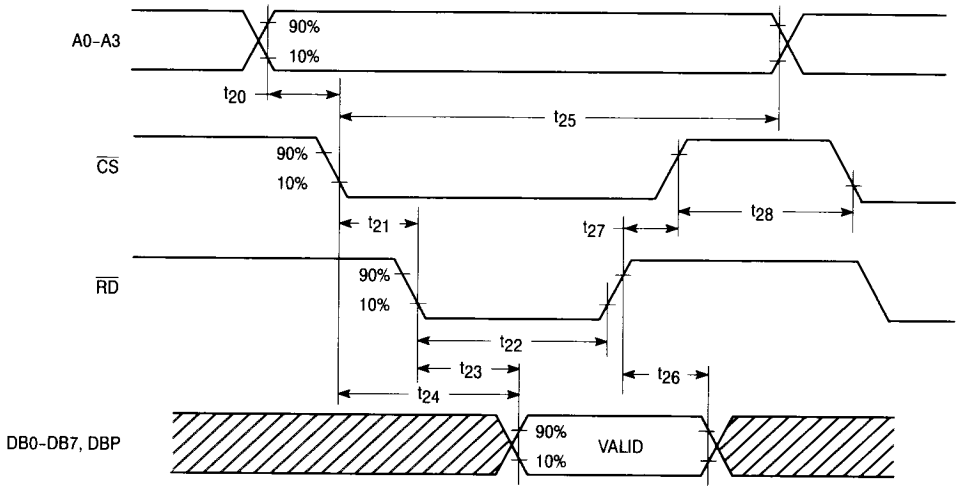

Figure 2.5. Register Read Timing

2.4.7 DMA Write

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_{29}	$\overline{DACK}$ Low to DREQ Low (Negation Pending)	t_{DADRL}	0	38	ns	1
t_{30}	$\overline{DACK}$ Low to $\overline{WR}$ Low	t_{DAWR}	0	—	ns	1, 3
t_{31}	$\overline{WR}$ Pulse Width	$t_{w(WR)}$	40	—	ns	1
t_{32}	Data Setup to $\overline{WR}$ High	t_{DWR}	11	—	ns	1, 3
t_{33}	$\overline{WR}$ High to $\overline{DACK}$ High	t_{WRDA}	0	—	ns	1, 3
t_{34}	Data Hold Time to $\overline{WR}$ High	$t_{h(D)}$	2	—	ns	1, 3
t_{35}	$\overline{DACK}$ High to $\overline{DACK}$ Low	$t_{wh(DACK)}$	12	—	ns	1, 2, 3
t_{36}	$\overline{DACK}$ High to DREQ High (Assertion Pending)	t_{DADRH}	0	50	ns	1, 3
t_{37}	$\overline{DACK}$ Pulse Width	$t_{w(DACK)}$	50	—	ns	1, 2, 3, 4
t_{38}	$\overline{WR}$ High to $\overline{WR}$ Low	$t_{w(WR)}$	40	—	ns	1

NOTES:
1. $\overline{CS}$ must be inactive during all DMA accesses.
2. $\overline{ACK}$ must be cycled once for each DMA access.
3. $\overline{WR}$ may precede or follow $\overline{DACK}$ edges. If $\overline{WR}$ is held low, the data setup to DACK high is 15 ns and $t_{wh(DACK)}$ is 40 ns minimum.
4. DREQ will remain true as long as the FIFO has room for at least one more byte. If the current write cycle fills the FIFO, DREQ will go false. If the SCSI bus then removes a byte from the FIFO, DREQ will not go true until $\overline{DACK}$ goes false.
5. For synchronous mode, there are no additional requirements as regards chip clock CLOCK.

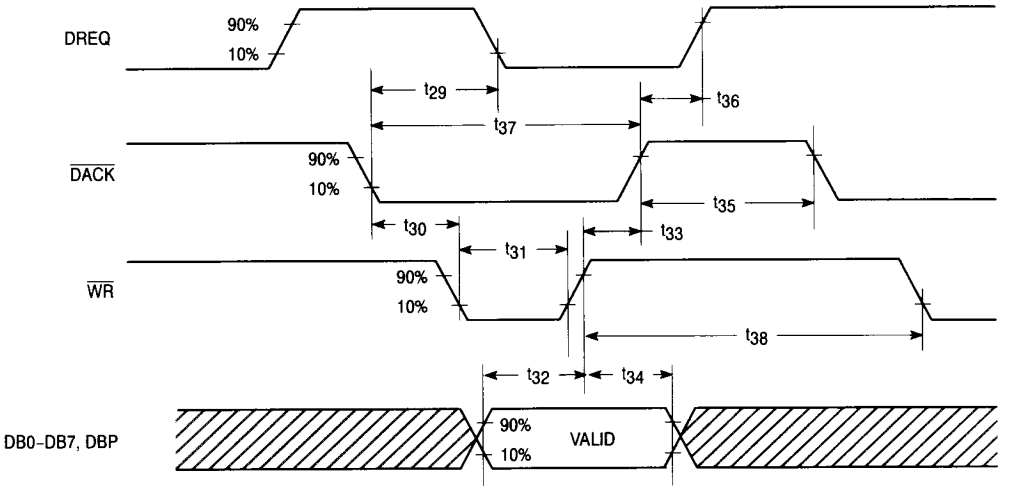

Figure 2.6. DMA Write Timing

2.4.8 DMA Read

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_{39}	$\overline{DACK}$ Low to DREQ Low (Negation Pending)	t_{DADRL}	0	38	ns	1
t_{40}	$\overline{DACK}$ Low to $\overline{RD}$ Low	t_{DARD}	0	—	ns	1, 3
t_{41}	$\overline{RD}$ Pulse Width	$t_{w(RD)}$	50	—	ns	1
t_{42}	$\overline{RD}$ to Data Valid	t_{DRD}	—	41	ns	1, 3
t_{43}	$\overline{DACK}$ to Data Valid	t_{DAD}	—	41	ns	1, 3
t_{44}	$\overline{RD}$ High to $\overline{DACK}$ High	t_{RDDA}	0	—	ns	1, 3
t_{45}	Data Hold Time	$t_{h(D)}$	2	40	ns	1, 2, 3
t_{46}	$\overline{DACK}$ High to $\overline{DACK}$ Low	$t_{wh(DACK)}$	12	—	ns	1, 4
t_{47}	$\overline{DACK}$ High to DREQ High (Assertion Pending)	t_{DADRH}	0	50	ns	1
t_{48}	$\overline{DACK}$ Pulse Width	$t_{w(DACK)}$	50	—	ns	1, 2

NOTES:
1. $\overline{CS}$ must be inactive during all DMA accesses.
2. $\overline{ACK}$ must be cycled once for each DMA access.
3. $\overline{RD}$ may precede or follow $\overline{DACK}$ edges. If $\overline{RD}$ is held low, the time from $\overline{DACK}$ low to stable data is t_{DAD} and data release time is $t_{h(D)}$.
4. If $t_{wh(DACK)}$ is ≤ 18 ns, then t_{DAD} is 45 ns max.
5. DREQ will remain true if there are more bytes in the FIFO. If the current read cycle empties the FIFO, DREQ will go false. If the SCSI bus then loads another byte into the FIFO, DREQ will not be asserted until $\overline{DACK}$ goes false.
6. For synchronous mode, there are no additional requirements as regards chip clock CLOCK.

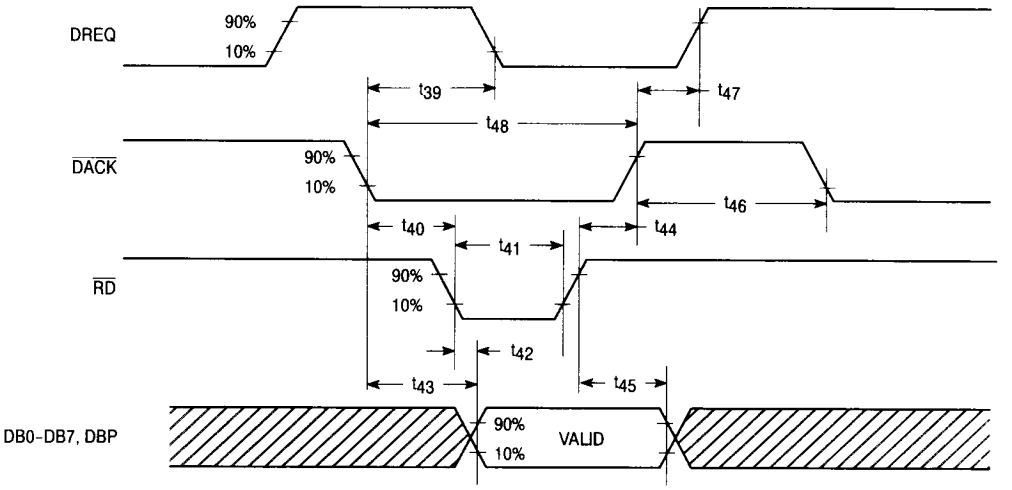

Figure 2.7. DMA Read Timing

2.4.9 Initiator Asynchronous Send

Time	Parameter	Symbol	Min	Max	Unit
t_{49}	Data Out Stable to $\overline{ACKO}$ Low	t_{DACL}	55	—	ns
t_{50}	$\overline{REQI}$ High to $\overline{ACKO}$ High	t_{REACH}	—	43	ns
t_{51}	$\overline{REQI}$ High to Next Data Byte Valid (FIFO bottom full)	t_{RED}	—	75	ns
t_{52}	$\overline{REQI}$ Low to $\overline{ACKO}$ Low (Data Previously Setup)	t_{REACL}	—	47	ns

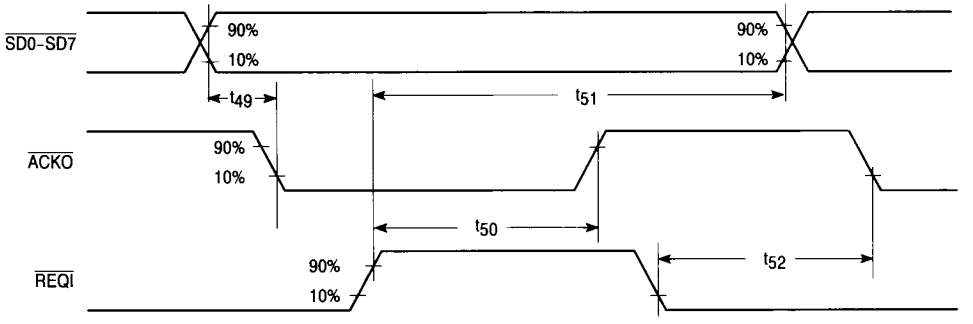

Figure 2.8. Initiator Asynchronous Send Timing

2.4.10 Initiator Asynchronous Read

Time	Parameter	Symbol	Min	Max	Unit
t_{53}	Data Setup to $\overline{REQI}$ Low	$t_{su(SREQ)}$	20	—	ns
t_{54}	$\overline{REQI}$ High to $\overline{ACKO}$ High	t_{REACH}	—	43	ns
t_{55}	$\overline{REQI}$ Low to $\overline{ACKO}$ Low (FIFO not full)	t_{REACL}	—	47	ns

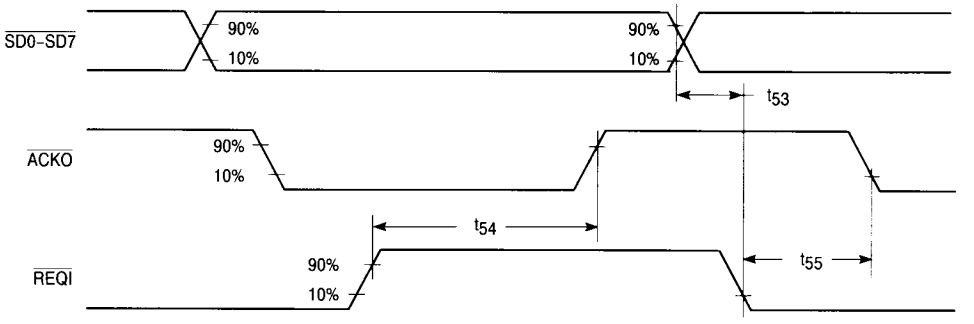

Figure 2.9. Initiator Asynchronous Receive Timing

2.4.11 Target Asynchronous Send

Time	Parameter	Symbol	Min	Max	Unit
t_{56}	Data Out Stable to $\overline{REQO}$ Low	t_{DREL}	55	—	ns
t_{57}	$\overline{ACKI}$ Low to $\overline{REQO}$ High	t_{ACREH}	—	43	ns
t_{58}	$\overline{ACKI}$ Low to Next Data Byte Valid (FIFO bottom full)	t_{ACD}	—	78	ns
t_{59}	$\overline{ACKI}$ High to $\overline{REQO}$ Low (data previously setup)	t_{ACREL}	—	45	ns

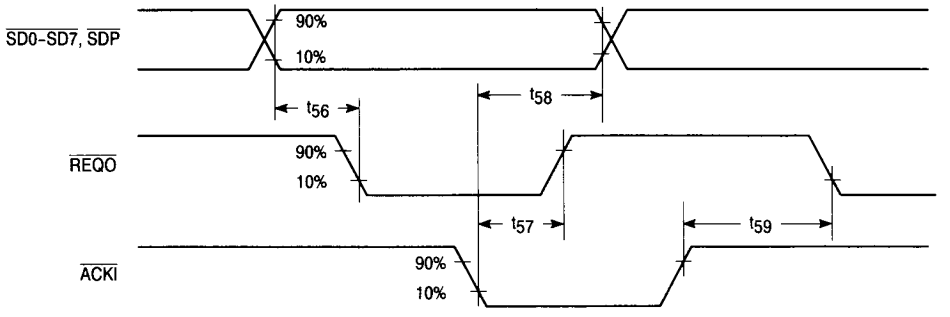

Figure 2.10. Target Asynchronous Send Timing

2.4.12 Target Asynchronous Receive

Time	Parameter	Symbol	Min	Max	Unit
t_{60}	Data Setup to $\overline{ACKI}$ Low	$t_{su(SACK)}$	20	—	ns
t_{61}	$\overline{ACKI}$ Low to $\overline{REQO}$ High	t_{ACREH}	—	43	ns
t_{62}	$\overline{ACKO}$ High to $\overline{REQO}$ Low (FIFO not full)	t_{ACREL}	—	45	ns

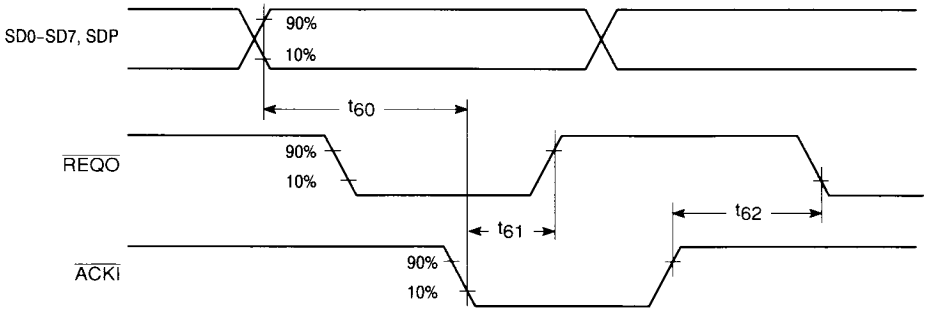

Figure 2.11. Target Asynchronous Receive Timing

2.4.13 Synchronous Receive

Time	Parameter	Symbol	Min	Max	Unit
t_{63}	Data Setup to $\overline{ACKI}$ Low (Target Mode)	$t_{su(SACK)}$	20	—	ns
t_{64}	Data Hold to $\overline{ACKI}$ Low (Target Mode)	$t_{h(SACK)}$	10	—	ns
t_{65}	$\overline{ACKI}$ Low to $\overline{ACKI}$ Low Cycle Time (Target Mode)	$t_{cyc(SACK)}$	100	—	ns
t_{66}	$\overline{ACKI}$ Assertion Period (Target Mode)	$t_{ast(SACK)}$	30	—	ns
t_{67}	$\overline{ACKI}$ Negation Period (Target Mode)	$t_{neg(SACK)}$	30	—	ns
t_{68}	Data Setup to $\overline{REQI}$ Low (Initiator Mode)	$t_{su(SREQ)}$	20	—	ns
t_{69}	Data Hold to $\overline{REQI}$ Low (Initiator Mode)	$t_{h(SREQ)}$	10	—	ns
t_{70}	$\overline{REQI}$ Low to $\overline{REQI}$ Low Cycle Time (Initiator Mode)	$t_{cyc(SREQ)}$	100	—	ns
t_{71}	$\overline{REQI}$ Assertion Period (Initiator Mode)	$t_{ast(SREQ)}$	30	—	ns
t_{72}	$\overline{REQI}$ Negation Period (Initiator Mode)	$t_{neg(SREQ)}$	30	—	ns

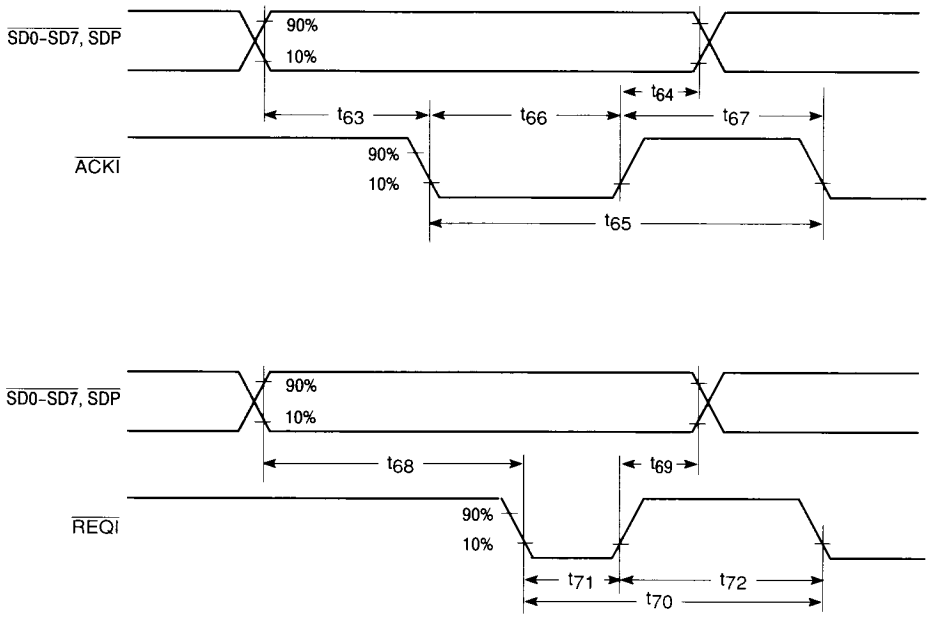

Figure 2.12. Synchronous Receive Timing

2.4.14 Synchronous Transmit (see Note 1)

Time	Parameter	Symbol	Min	Max	Unit
t_{73}	Data Valid from CLOCK High	t_{DCK}	—	60	ns
t_{74}	$\overline{REQO}$ Low from CLOCK High (Target Mode)	t_{RELCKH}	—	42	ns
t_{75}	$\overline{REQO}$ High from CLOCK High (Target Mode)	t_{REHCKH}	—	42	ns
t_{76}	$\overline{REQO}$ Low from CLOCK Low (Target Mode)	t_{RELCKL}	—	42	ns
t_{77}	$\overline{ACKO}$ Low from CLOCK High (Initiator Mode)	t_{ACLCKH}	—	42	ns
t_{78}	$\overline{ACKO}$ High from CLOCK High (Initiator Mode)	t_{ACHCKK}	—	42	ns
t_{79}	$\overline{ACKO}$ Low from CLOCK Low (Initiator Mode)	t_{ACLCKL}	—	42	ns

NOTE:
1. SCSI data setup and hold times are the same as asynchronous transfers.

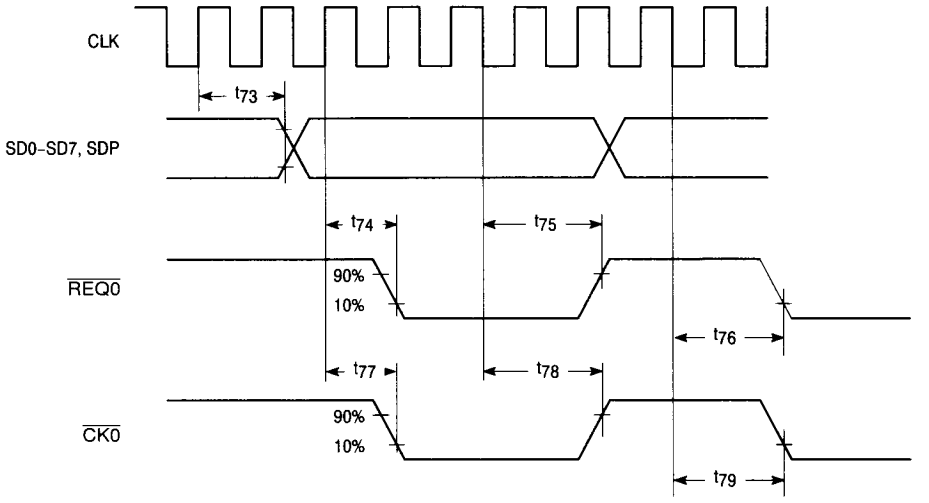

Figure 2.13. Synchronous Transmit Timing