## 5.1 Electrical Characteristics

### 5.1.1 Absolute maximum ratings

Absolute Maximum Ratings

| Symbol | Parameter | | Conditions | Ratings | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | All voltages measured with reference to the $V_{SS}$ pin, output transistors isolated. | -0.3~7.0 | V |
| $V_I$ | Input voltage | $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, $V_{REF}$ | | -0.3~$V_{CC}$+0.3 | V |
| $V_I$ | Input voltage | RESET, $X_{IN}$ | | -0.3~$V_{CC}$+0.3 | V |
| $V_I$ | Input voltage | $CNV_{SS}$ | | -0.3~13 | V |
| $V_O$ | Output voltage | $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, $X_{OUT}$ | | -0.3~$V_{CC}$+0.3 | V |
| Pd | Power dissipation | | Ta=25°C | 500 | mW |
| Topr | Operating temperature | | | -20~85 | °C |
| Tstg | Storage temperature | | | -40~125 | °C |

### 5.1.2 Recommended operating conditions

Recommended Operating Conditions ($V_{CC}$ = 4.0 to 5.5V, Ta = −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Power supply voltage | | 4.0 | 5.0 | 5.5 | V |
| $V_{SS}$ | Power supply voltage | | | 0 | | V |
| $V_{REF}$ | Analog reference voltage (when A-D converter is used) | | 2.0 | | $V_{CC}$ | V |
| | Analog reference voltage (when D-A converter is used) | | 4.0 | | $V_{CC}$ | V |
| AVss | Analog power supply voltage | | | 0 | | V |
| $V_{IA}$ | Analog input voltage | $AN_0$~$AN_7$ | AVss | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage | $\overline{RESET}$,$X_{IN}$,CNVss | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage | $\overline{RESET}$ | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage | $X_{IN}$ | 0 | | 0.16$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage | CNVss | 0 | | 0.2$V_{CC}$ | V |
| $\Sigma I_{OH1}$(peak) | "H" peak output total current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$ | | | -80 | mA |
| $\Sigma I_{OH2}$(peak) | "H" peak output total current | $P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$ | | | -80 | mA |
| $\Sigma I_{OL1}$(peak) | "L" peak output total current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$ | | | 80 | mA |
| $\Sigma I_{OL2}$(peak) | "L" peak output total current | $P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$, $P7_0$~$P7_7$ | | | 80 | mA |
| $\Sigma I_{OH1}$(avg) | "H" average output total current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$ (Note 1) | | | -40 | mA |
| $\Sigma I_{OH2}$(avg) | "H" average output total current | $P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$ (Note 1) | | | -40 | mA |
| $\Sigma I_{OL1}$(avg) | "L" average output total current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$ (Note 1) | | | 40 | mA |
| $\Sigma I_{OL2}$(avg) | "L" average output total current | $P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$, $P7_0$~$P7_7$ (Note 1) | | | 40 | mA |
| $I_{OH}$(peak) | "H" peak output current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ | | | -10 | mA |
| $I_{OL}$(peak) | "L" peak output current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ | | | 10 | mA |
| $I_{OH}$(avg) | "H" average output current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ (Note 1) | | | -5 | mA |
| $I_{OL}$(avg) | "L" average output current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ (Note 1) | | | 5 | mA |
| f($X_{IN}$) | Internal clock oscillation frequency | | | | 5 | MHz |

Note 1 : The average output currents are average values measured over 100ms.

### 5.1.3 Electrical characteristics

Electrical Characteristics ($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = 0V, Ta = −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | "H" output voltage | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P8_0$~$P8_7$ (Note 2) | $I_{OH}$=-10mA | Vcc-2.0 | | | V |
| $V_{OL}$ | "L" output voltage | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ | $I_{OL}$=10mA | | | 2.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $CNTR_0$,$CNTR_1$,$INT_0$~$INT_4$ | | | 0.4 | | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $R_xD$,$S_{CLK}$ | | | 0.5 | | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | | 0.5 | | V |
| $I_{IH}$ | "H" input current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ | $V_I$=Vcc | | | 5.0 | μA |
| $I_{IH}$ | "H" input current | $\overline{RESET}$,$CNV_{SS}$ | $V_I$=Vcc | | | 5.0 | μA |
| $I_{IH}$ | "H" input current | $X_{IN}$ | $V_I$=Vcc | | 4 | | μA |
| $I_{IL}$ | "L" input current | $P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ $\overline{RESET}$,$CNV_{SS}$ | $V_I$=Vss | | | -5.0 | μA |
| $I_{IL}$ | "L" input current | $X_{IN}$ | $V_I$=Vss | | -4 | | μA |
| $V_{RAM}$ | RAM retention voltage | | Clock is stopped | 2.0 | | 5.5 | V |
| Icc | Power supply current (Note 3) | f($X_{IN}$)=5MHz | | | 4 | 8 | mA |
| | | f($X_{IN}$)=5MHz (wait mode) | | | 1 | | mA |
| | | With all oscillation stopped (stop mode) | Ta=25°C | | 0.1 | 1 | μA |
| | | | Ta=85°C | | | 10 | |

Note 2 : $P4_5$ is measured when the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".

Note 3 : Not including the current flowing through the $V_{REF}$ pin. The A-D converter has completed conversion. Output transistors isolated.

### 5.1.4 A-D converter characteristics

A-D Converter Characteristics ($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $V_{REF}$ = 2.0V to $V_{CC}$, Ta= −20 to 85°C, f($X_{IN}$) = 5MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy (disregarding quantization error) | | | ±1 | ±2.5 | LSB |
| $t_{CONV}$ | Conversion time | | | | 50 | $tc(\phi)$ |
| $R_{LADDER}$ | Ladder resistor | | | 35 | | kΩ |
| $I_{VREF}$ | Reference power supply input current | (Note 4) | 50 | 150 | 200 | μA |
| $I_{I(AD)}$ | A-D port input current | | | 0.5 | | μA |

Note 4 : When D-A conversion registers (addresses $0036_{16}$ and $0037_{16}$) are at "$00_{16}$".

### 5.1.5 D-A converter characteristics

D-A Converter Characteristics ($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $V_{REF}$ = 4.0V to $V_{CC}$, Ta= −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy | | | | 1.0 | % |
| tsu | Setting time | | | | 3 | μs |
| Ro | Output resistor | | 1 | 2.5 | 4 | kΩ |
| $I_{VREF}$ | Reference power supply input current | (Note 5) | | | 3.2 | mA |

Note 5 : Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "$00_{16}$", and not including the ladder resistor of A-D converter.

### 5.1.6 Timing requirements and switching characteristics

Timing Requirements

($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = 0V, Ta = −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{w(\overline{RESET})}$ | Reset input "L" pulse width | 2 | | | μs |
| $t_{c(X_{IN})}$ | External clock input cycle time | 200 | | | ns |
| $t_{WH(X_{IN})}$ | External clock input "H" pulse width | 50 | | | ns |
| $t_{WL(X_{IN})}$ | External clock input "L" pulse width | 50 | | | ns |
| tc(CNTR) | $CNTR_0$, $CNTR_1$ input cycle time | 200 | | | ns |
| tWH(CNTR) | $CNTR_0$, $CNTR_1$, $INT_0$ to $INT_4$ input "H" pulse width | 80 | | | ns |
| tWL(CNTR) | $CNTR_0$, $CNTR_1$, $INT_0$ to $INT_4$ input "L" pulse width | 80 | | | ns |
| $t_{c(S_{CLK1})}$ | Serial clock input 1 cycle time | 800 | | | ns |
| $t_{c(S_{CLK2})}$ | Serial clock input 2 cycle time | 1000 | | | ns |
| $t_{WH(S_{CLK1})}$ | Serial clock input 1 "H" pulse width (Note 6) | 370 | | | ns |
| $t_{WH(S_{CLK2})}$ | Serial clock input 2 "H" pulse width | 400 | | | ns |
| $t_{WL(S_{CLK1})}$ | Serial clock input 1 "L" pulse width (Note 6) | 370 | | | ns |
| $t_{WL(S_{CLK2})}$ | Serial clock input 2 "L" pulse width | 400 | | | ns |
| $t_{su(R_{XD}-S_{CLK1})}$ | Serial input 1 setup time | 220 | | | ns |
| $t_{su(S_{IN2}-S_{CLK2})}$ | Serial input 2 setup time | 200 | | | ns |
| $t_{h(S_{CLK1}-R_{XD})}$ | Serial input 1 hold time | 100 | | | ns |
| $t_{h(S_{CLK2}-S_{IN2})}$ | Serial input 2 hold time | 200 | | | ns |

Note 6 : When $f(X_{IN})$ = 5MHz and bit 6 of address $001A_{16}$ is "1". The minimum time is quarter of the value when $f(X_{IN})$ = 5MHz and bit 6 of address $001A_{16}$ is "0".

Switching Characteristics

($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = 0V, Ta = −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{WH(S_{CLK1})}$ | Serial clock output 1 "H" pulse width | $t_{c(S_{CLK1})}/2-30$ | | | ns |
| $t_{WL(S_{CLK1})}$ | Serial clock output 1 "L" pulse width | $t_{c(S_{CLK1})}/2-30$ | | | ns |
| $t_{WH(S_{CLK2})}$ | Serial clock output 2 "H" pulse width | $t_{c(S_{CLK2})}/2-160$ | | | ns |
| $t_{WL(S_{CLK2})}$ | Serial clock output 2 "L" pulse width | $t_{c(S_{CLK2})}/2-160$ | | | ns |
| $t_{d(S_{CLK1}-T_{XD})}$ | Serial output delay time (Note 7) | | | 140 | ns |
| $t_{d(S_{CLK2}-S_{OUT2})}$ | Serial output delay time | | | 0.2tc | |
| $t_{v(S_{CLK1}-T_{XD})}$ | Serial output hold time (Note 7) | -30 | | | ns |
| $t_{v(S_{CLK2}-S_{OUT2})}$ | Serial output hold time | 0 | | | |
| tr | Total CMOS pin rise time (Note 8) | | 10 | 30 | ns |
| tf | Total CMOS pin fall time (Note 8) | | 10 | 30 | ns |

Note 7 : When the $P4_5/T_{XD}$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is at "0".

Note 8 : $X_{OUT}$ pin excluded.

Memory Expansion Mode and Microprocessor Mode Timing Requirements
($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = 0V, Ta = −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| tsu($\overline{ONW}$- $\phi$) | $\overline{ONW}$ input setup time | -20 | | | ns |
| th($\phi$ -$\overline{ONW}$) | $\overline{ONW}$ input hold time | -20 | | | ns |
| tsu(DB- $\phi$) | Data bus setup time | 60 | | | ns |
| th($\phi$ -DB) | Data bus hold time | 0 | | | ns |

Memory Expansion Mode and Microprocessor mode Switching Characteristics
($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = 0V, Ta = −20 to 85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| tc($\phi$) | $\phi$ clock cycle time | | 2×tc($X_{IN}$) | | ns |
| $t_{WH}$($\phi$) | $\phi$ clock "H" pulse width | tc($X_{IN}$)-10 | | | ns |
| $t_{WL}$($\phi$) | $\phi$ clock "L" pulse width | tc($X_{IN}$)-10 | | | ns |
| td($\phi$ -AH) | $AD_{15}$ to $AD_8$ delay time | | 20 | 40 | ns |
| tv($\phi$ -AH) | $AD_{15}$ to $AD_8$ valid time | 6 | 10 | | ns |
| td($\phi$ -AL) | $AD_7$ to $AD_0$ delay time | | 25 | 45 | ns |
| tv($\phi$ -AL) | $AD_7$ to $AD_0$ valid time | 6 | 10 | | ns |
| td($\phi$ -SYNC) | SYNC delay time | | 20 | | ns |
| tv($\phi$ -SYNC) | SYNC valid time | | 10 | | ns |
| td($\phi$ -$\overline{WR}$) | $\overline{RD}$ and $\overline{WR}$ delay time | | 10 | 20 | ns |
| tv($\phi$ -$\overline{WR}$) | $\overline{RD}$ and $\overline{WR}$ valid time | 3 | 5 | 10 | ns |
| td($\phi$ -DB) | Data bus delay time | | 20 | 70 | ns |
| tv($\phi$ -DB) | Data bus valid time | 15 | | | ns |
| td($\overline{RESET}$-$\overline{RESET_{OUT}}$) | $\overline{RESET_{OUT}}$ output delay time (Note 9) | | | 200 | ns |
| tv($\phi$ -$\overline{RESET}$) | $\overline{RESET_{OUT}}$ output valid time (Note 9,10) | 0 | | 200 | ns |

Note 9 : This is valid only in microprocessor mode.
Note 10 : The $\overline{RESET_{OUT}}$ output goes "H" with the rise of the $\phi$ clock, between 1 cycle and 19 cycles after the $\overline{RESET}$ input goes "H".

### 5.1.7 Test conditions

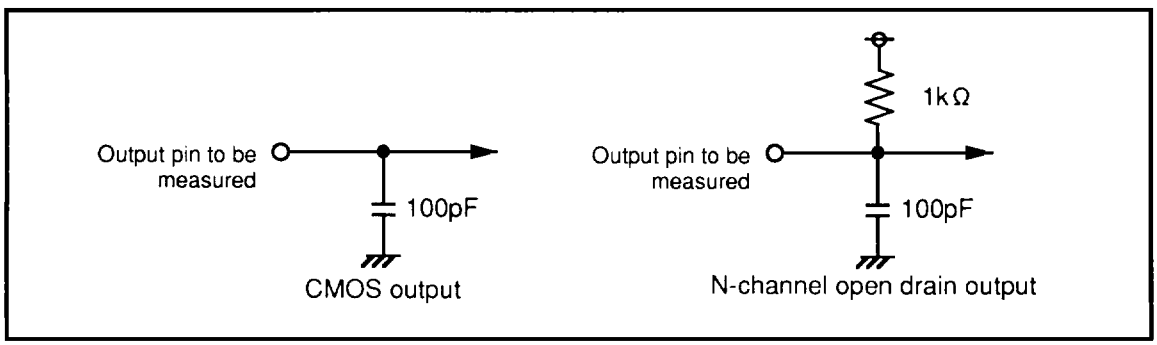
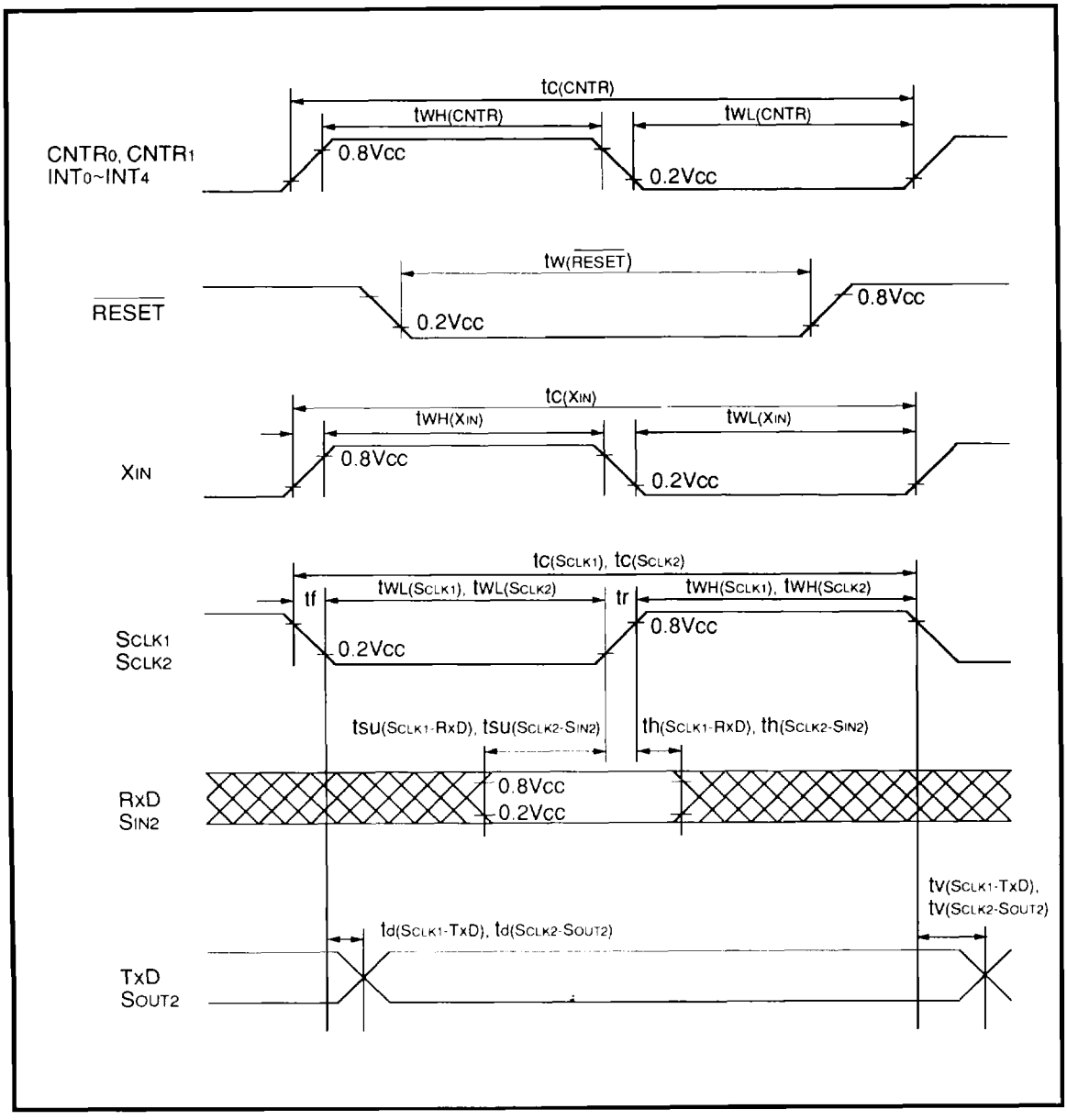


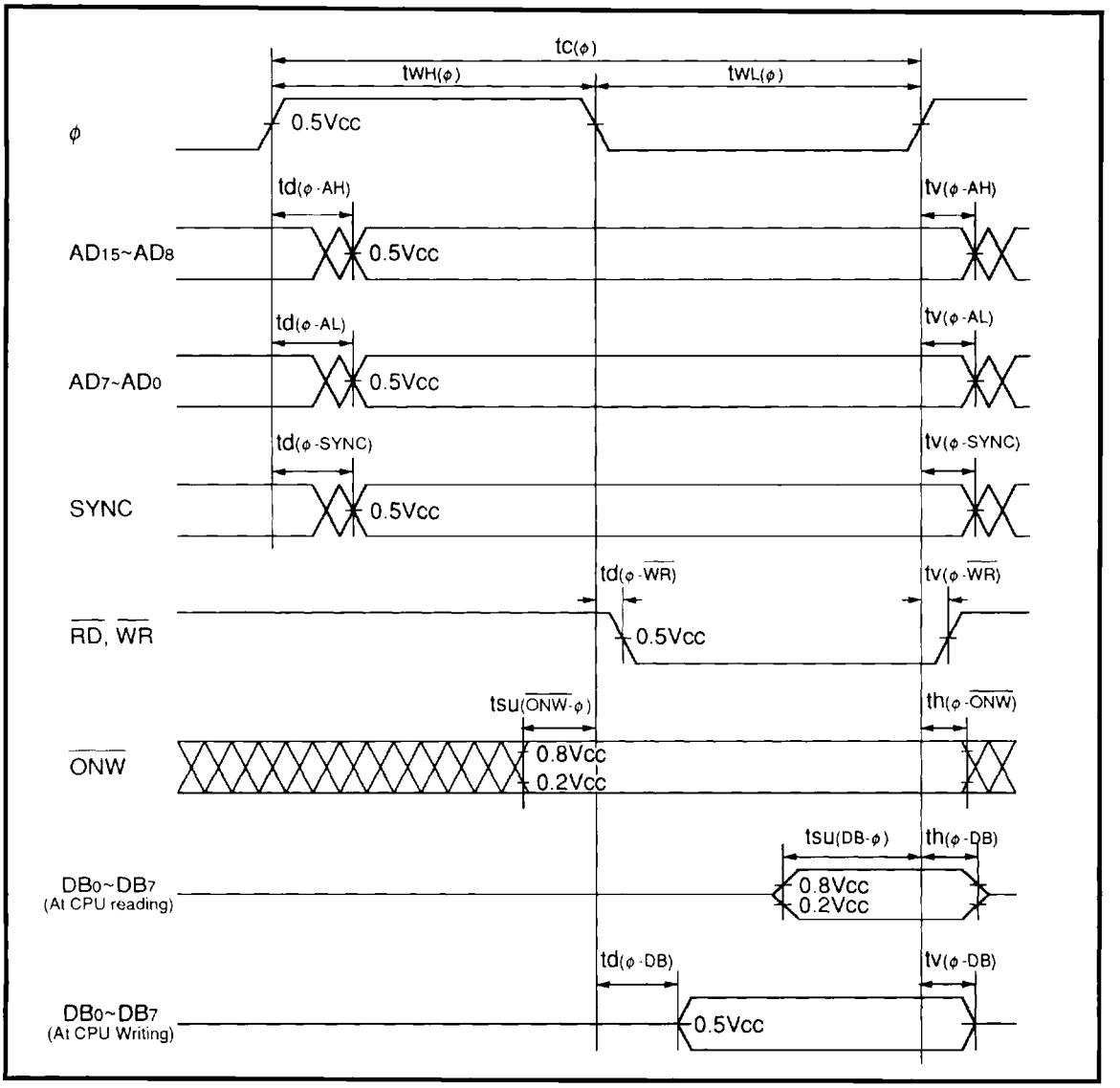

Fig. 5.1.1 Circuit for Measuring Output Switching Characteristics

### 5.1.8 Timing diagram

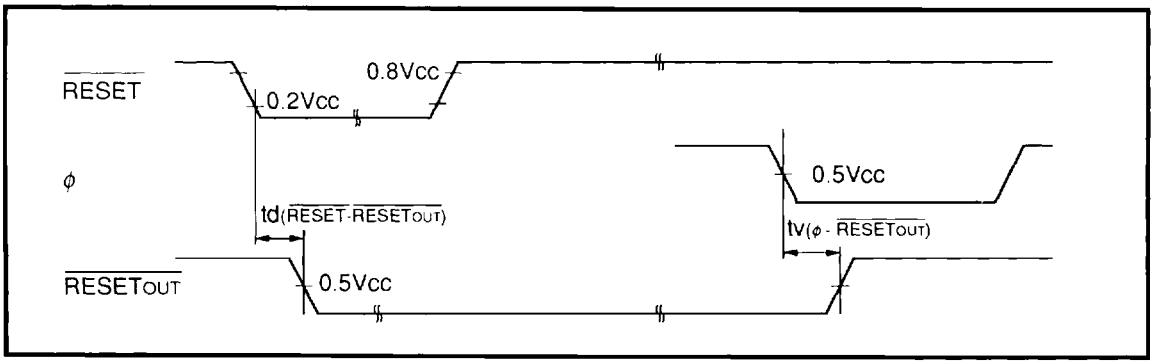
(1) Timing diagram



(2) Memory expansion mode, microprocessor mode




(3) Microprocessor mode



## 5.2 Typical Characteristics

### 5.2.1 Typical current consumption

The typical current consumption of the M38063M6-XXXFP/GP is as shown in Figure 5.2.1.

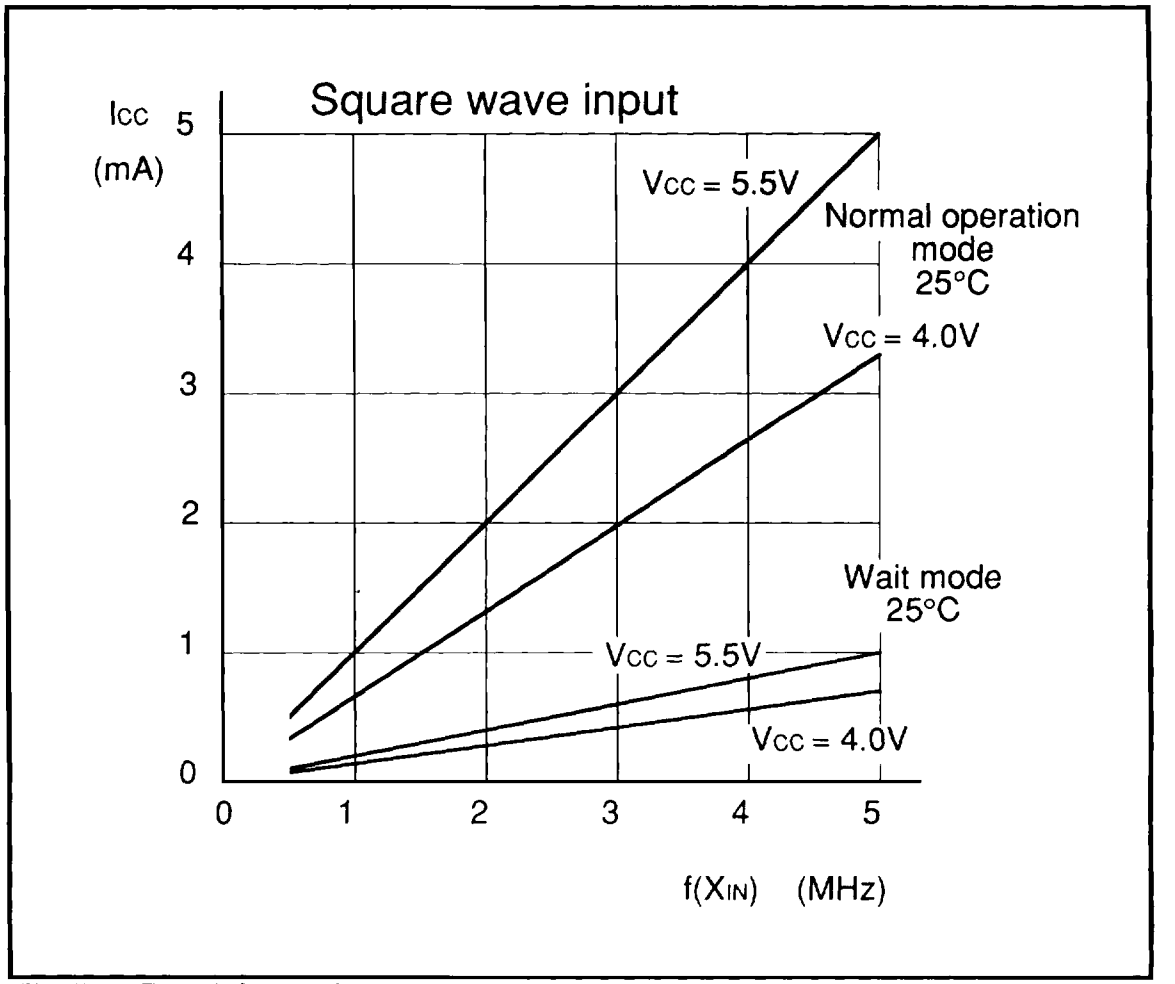



Fig. 5.2.1 Typical Current Consumption

### 5.2.2 Typical port characteristics

Typical port characteristics of the M38063M6-XXXFP/GP are shown in Figures 5.2.2 and 5.2.3

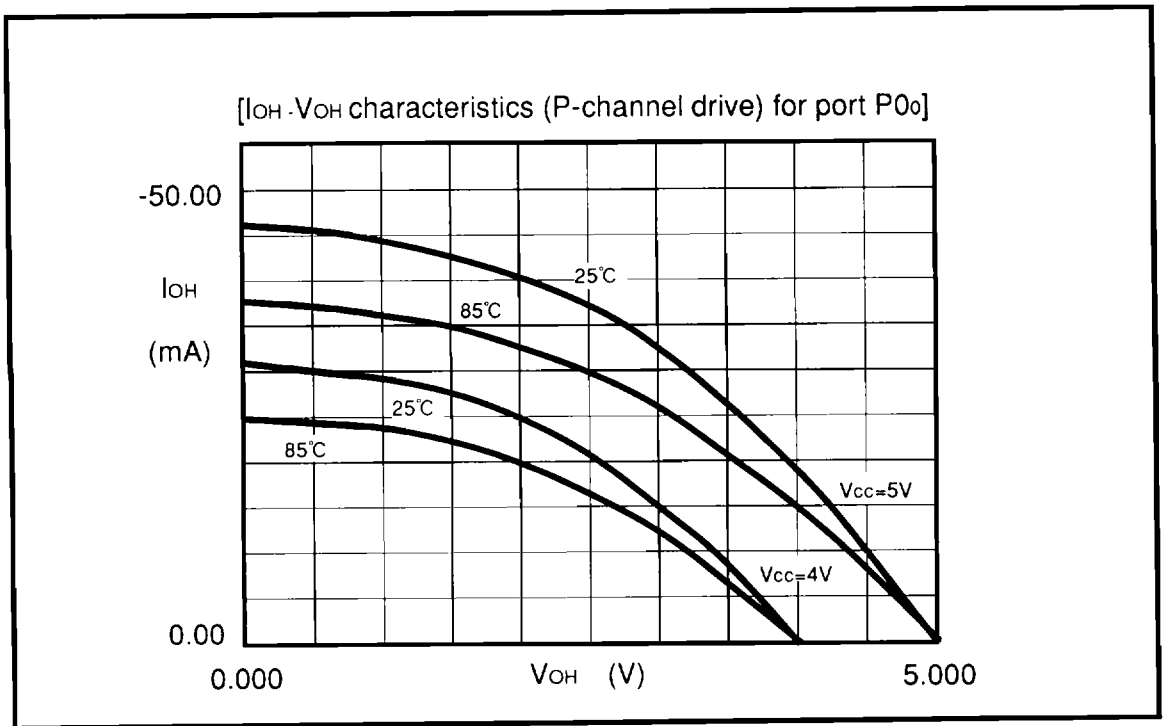



Fig. 5.2.2 Typical Characteristics of Port P0 P-Channel Output Transistor

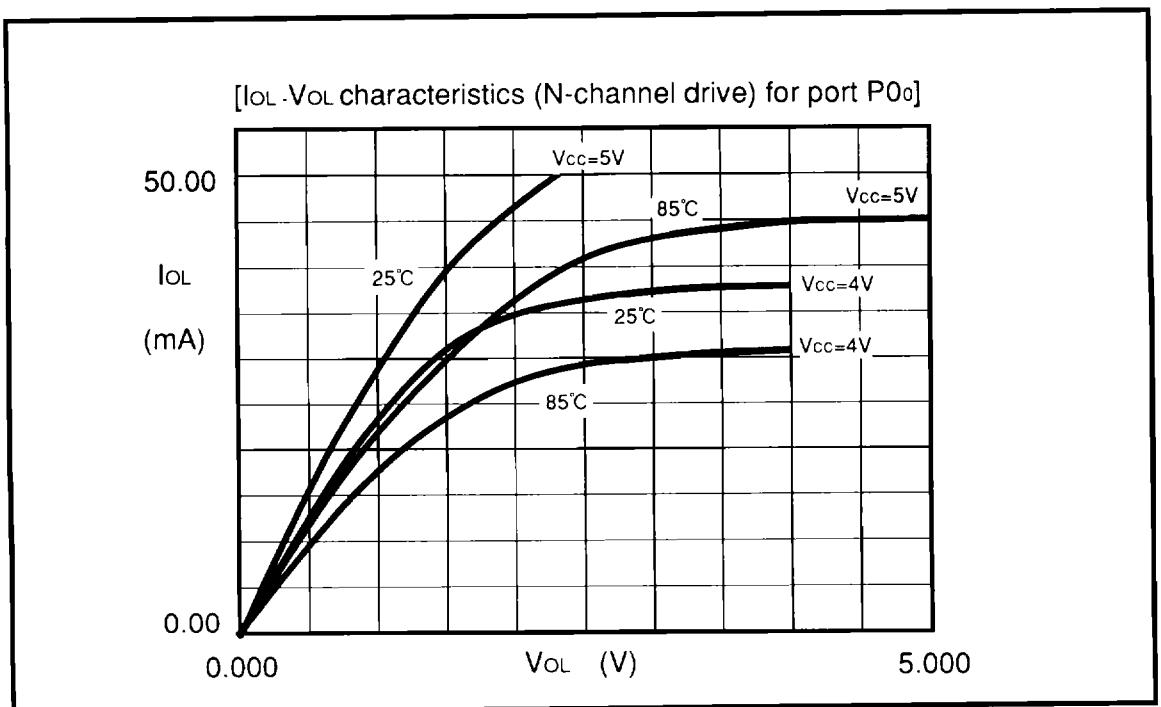
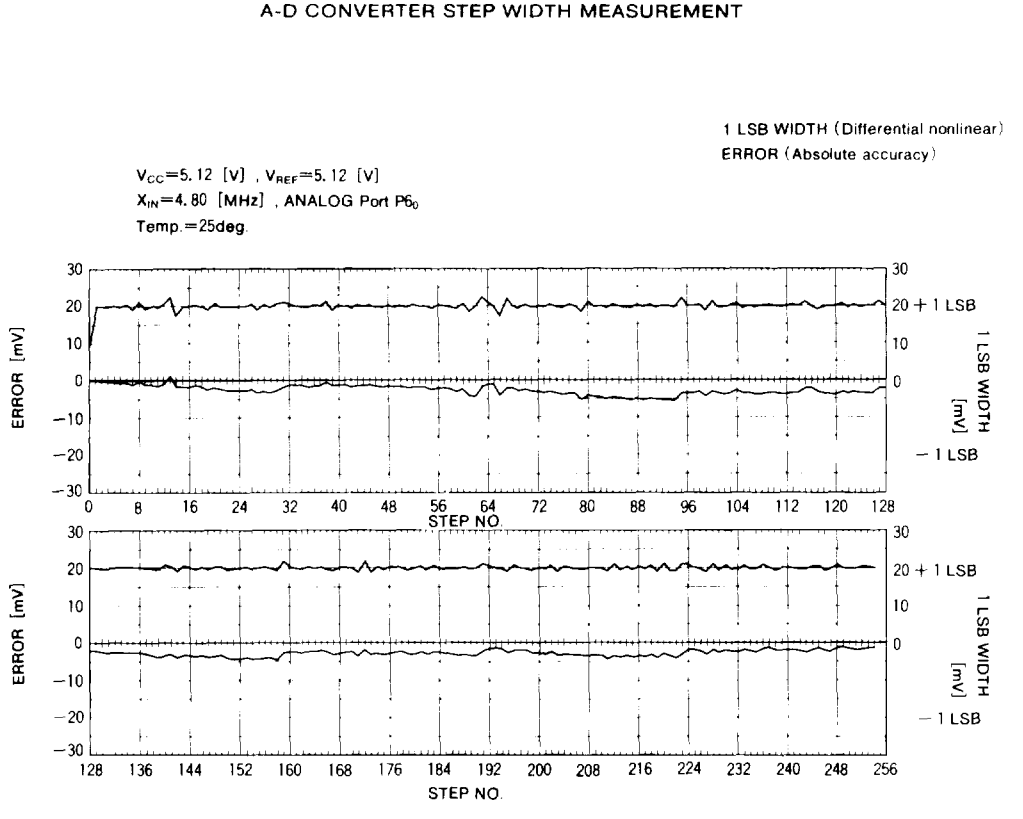



Fig. 5.2.3 Typical Characteristics of Port P0 N-Channel Output Transistor

### 5.2.3 Typical A-D conversion characteristics

Typical A-D conversion characteristics of the M38063M6-XXXFP/GP are shown in Figure 5.2.4. The line in the lower part of the graph shows the absolute accuracy error. This indicates the deviation from the ideal value at the point that the A-D output changes. For example, the change in the A-D output from $00_{16}$ to $01_{16}$ should ideally occur at the point that $AN_1$ = 10mV, but since it changes at 0mV, the error is: 10 − 0 = 10mV.

The line in the upper part of the graph shows the step width of the input voltage at any given A-D output value. For example, the measured step width of the input voltage is 22mV when the A-D code is $0D_{16}$, and the non-linearity error is 22 − 20 = 2mV (0.3 LSB).

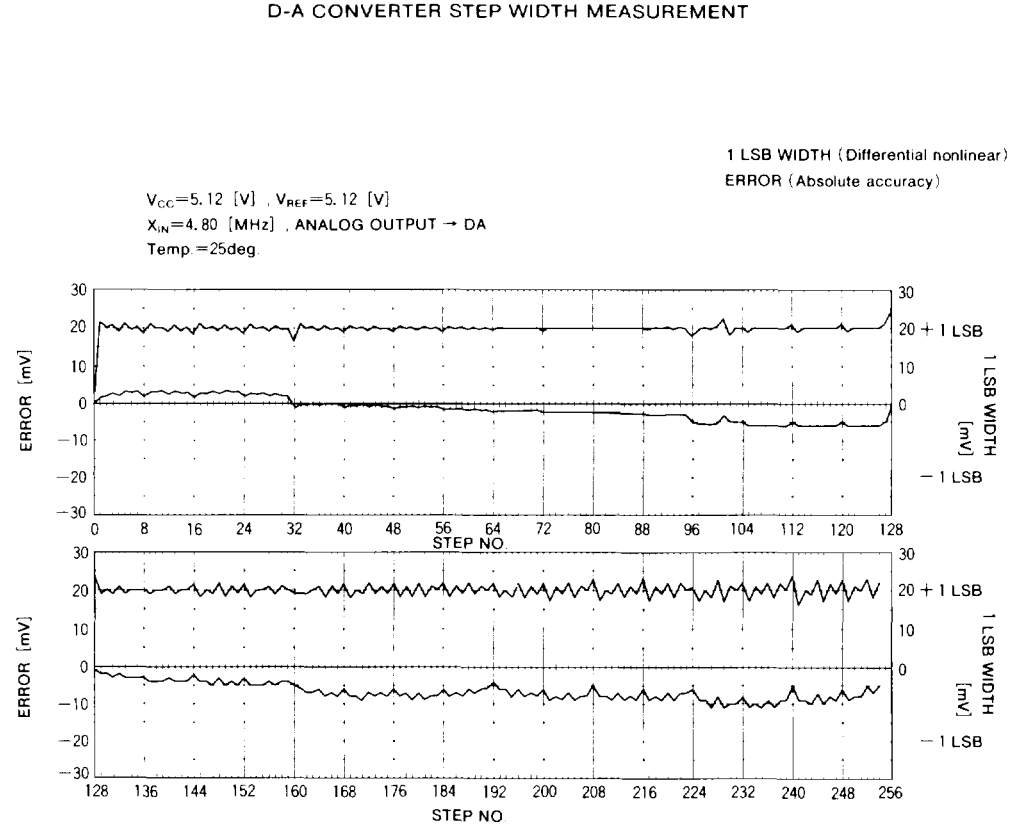



Measured after the power source has stabilized during operation in single-chip mode

Fig. 5.2.4 Typical A-D Conversion Characteristics

### 5.2.4 Typical D-A conversion characteristics

Typical D-A conversion characteristics of the M38063M6-XXXFP/GP are shown in Figure 5.2.5.
The line in the lower part of the graph shows absolute accuracy error. This indicates the difference between the ideal analog output and the measured output value.
The line in the upper part of the graph shows the step width of the output analog value for a one-bit change in the value input to the D-A converter.




Measured after the power source has stabilized during operation in single-chip mode

Fig. 5.2.5 Typical D-A Conversion Characteristics