4.1 Overview

In addition to the mask ROM versions, there are other members of the 7470 Series called built-in programmable ROM versions which are microcomputers with built-in programmable ROM. One version, the window-type EPROM version, has an built-in EPROM that can be written to and erased. Another version is a one-time programmable microcomputer whose built-in PROM can be written to but not erased. Since the functions of the built-in EPROM and one-time programmable versions are exactly the same, apart from whether the ROM contents can be erased, they are both referred to as built-in PROM versions in this manual.
The built-in PROM versions have functions similar to those of the mask ROM versions, but they also have a EPROM mode that enables writing to built-in PROM.
Seven built-in PROM versions of the 7470 Series are available: the M37470E4-XXXSP (one-time programmable), the M37470E8–XXXSP (one-time programmable), the M37471E4-XXXSP/FP (one-time programmable), the M37471E8–XXXSP/FP (one-time programmable), and the M37471E8SS (window version). A brief outline of the specifications of these microcomputers is given in Table 4.1.1.

Table 4.1.1 Functions of built-in PROM versions (M37470E4-XXXSP, M37470E8-XXXSP, M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, and M37471E8SS)

Parameter			Functions		
			M37470E4-XXXSP and M37470E8-XXXSP	M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS	M37471E4-XXXFP and M37471E8-XXXFP
Basic instructions			69		
Instruction execution time			1.0μs (minimum instructions, at 4MHz)		
Clock frequency			4MHz		
Memory size	PROM (Note 4)		8192 bytes (Note 1)		
	RAM		192 bytes (Note 2)		
Input/Output ports	P0, P1	I/O	8-bit × 2	8-bit × 2	
	P2	I/O	4-bit × 1	8-bit × 1	
	P3	Input	4-bit × 1	4-bit × 1	
	P4	I/O	2-bit × 1	4-bit × 1	
	P5	Input	—	4-bit × 1	
Serial I/O			8-bit × 1		
Timer			8-bit × 4 (with 8-bit latch)		
A-D converter			8-bit × 1 (4-channel)	8-bit × 1 (8-channel)	
Subroutine nesting			96 (max.) (Note 3)		
Interrupt			External 5, internal 6 and software 1		
Clock generating circuit			1 built-in (with external ceramic or quartz crystal oscillator)	2 built-in (with external ceramic or quartz crystal oscillator)	
Power supply			2.7 to 5.5V		
Power dissipation (typ.)			17.5mW (at 4MHz)		
Input/Output characteristics	Input/Output voltage		5V		
	Output current		–5 to 10mA (P0, P1, P2 and P4: CMOS 3-state)		
Operating temperature range			–20 to 85°C		
Device structure			CMOS silicon gate		
Package	One-time programmable		32-pin shrink plastic molded DIP	42-pin shrink plastic molded DIP	56-pin plastic molded QFP
	Window type		—	42-pin shrink ceramic DIP	—

Note 1 : 16384 bytes for M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS.
2 : 384 bytes for M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS.
3 : 192 (max.) for M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS.
4 : Voltage of writing to PROM is 12.5V (corresponding to M5L27256).

4.2 Pin configuration

Figure 4.2.1 shows the pin configuration of M37470E4-XXXSP and M37470E8-XXXSP, Figure 4.2.2 shows the pin configuration of M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS, and Figure 4.2.3 shows the pin configuration of M37471E4-XXXFP and M37471E8-XXXFP. The built-in PROM versions have pin-compatibility with the mask ROM version.

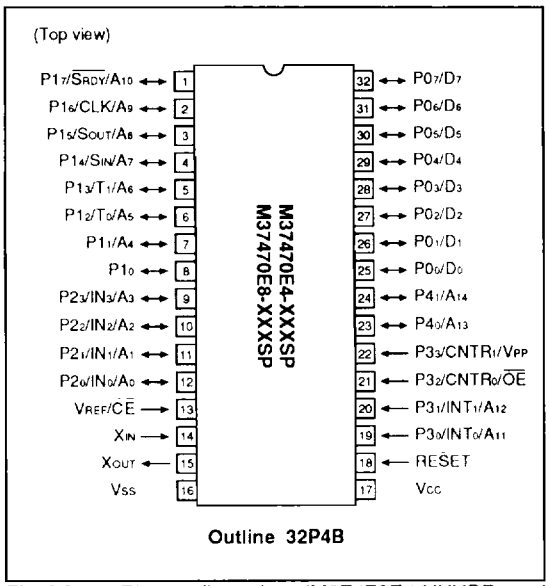

Fig.4.2.1 Pin configuration (M37470E4-XXXSP and M37470E8-XXXSP)

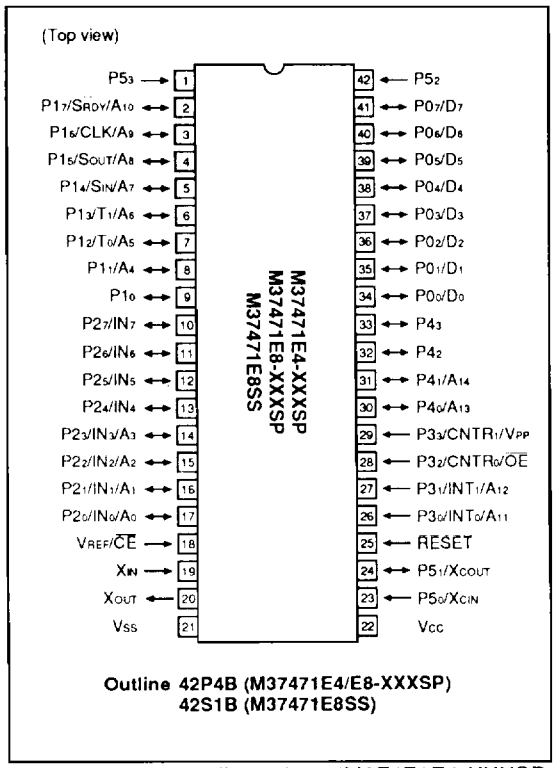

Fig.4.2.2 Pin configuration (M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS)

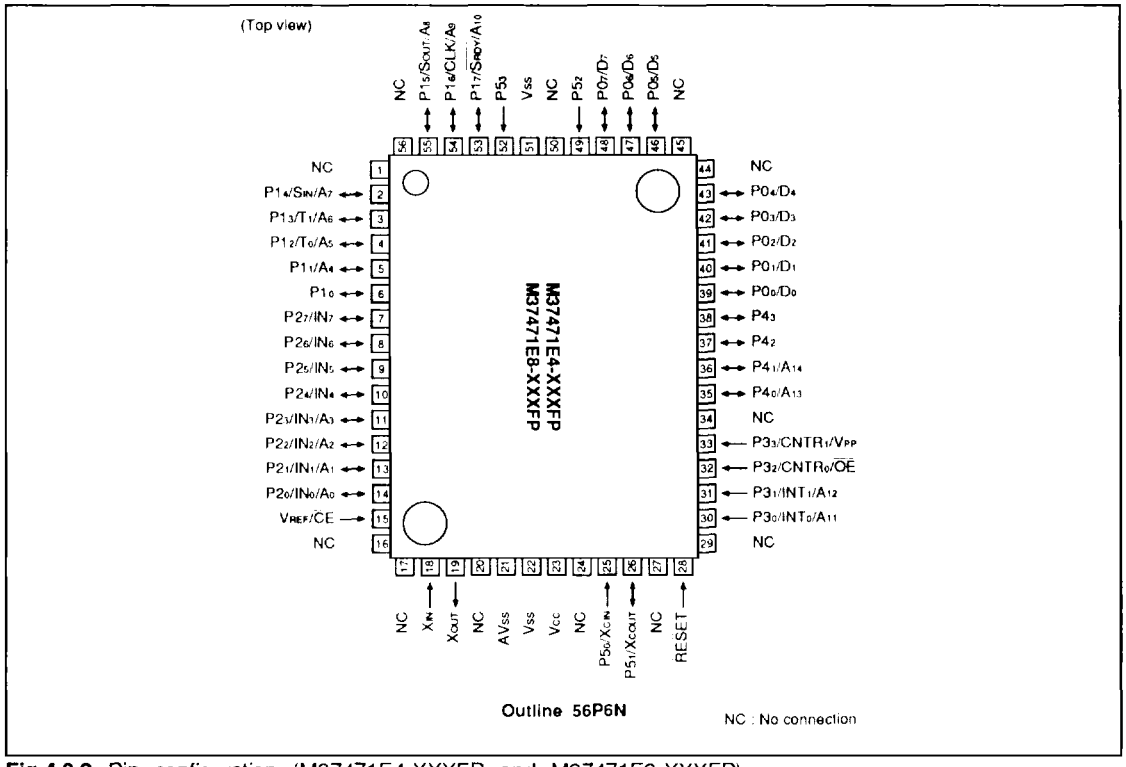

Fig.4.2.3 Pin configuration (M37471E4-XXXFP and M37471E8-XXXFP)

4.3 Block diagram

Figures 4.3.1 to 4.3.3 shows the block diagrams of M37470E4-XXXSP, M37470E8-XXXSP, M37471E4-XXXSP, M37471E8-XXXSP, M37471E8SS, M37471E4-XXXFP, and M37471E8-XXXFP.

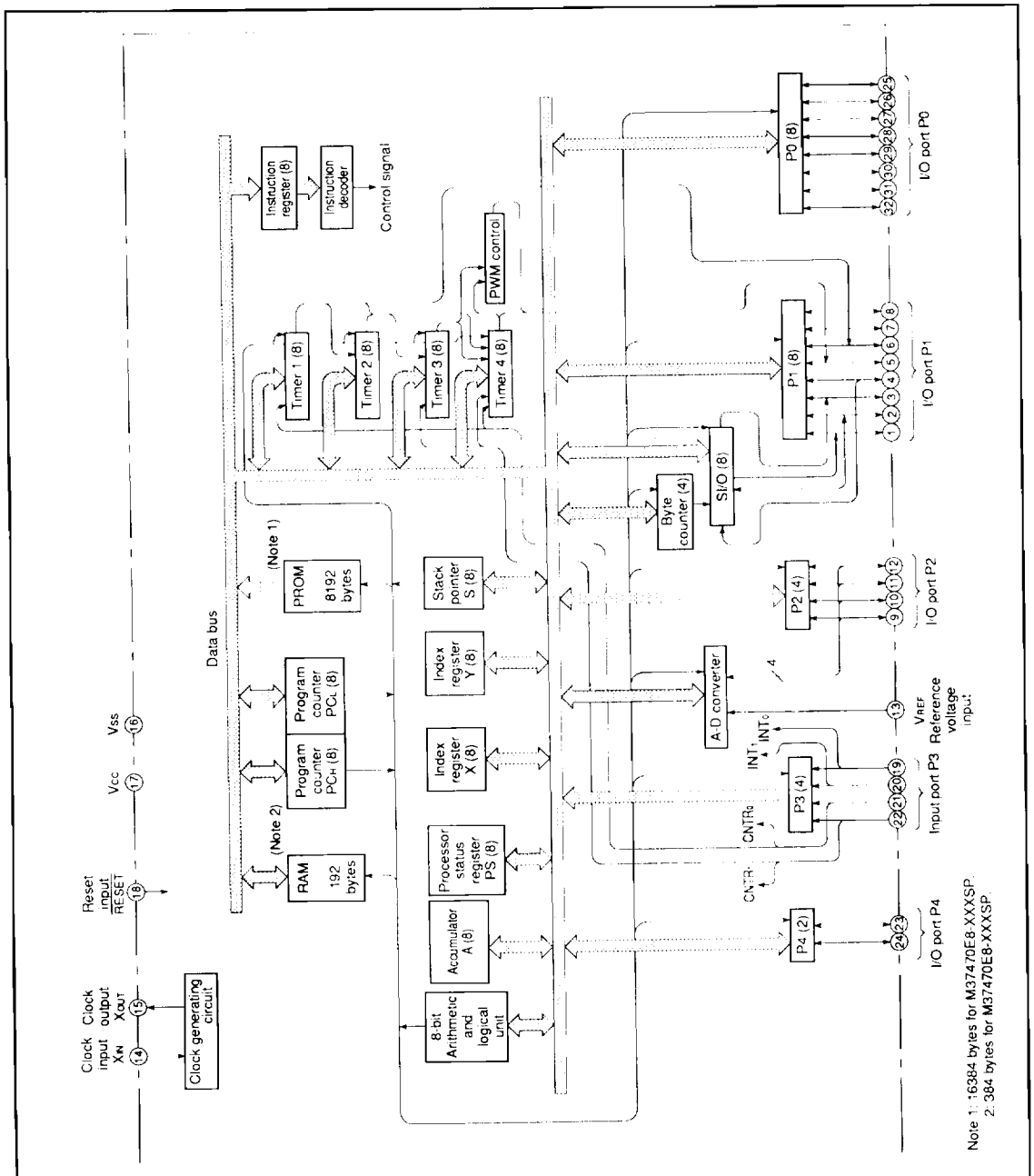

Fig.4.3.1 Block diagram of M37470E4-XXXSP and M37470E8-XXXSP

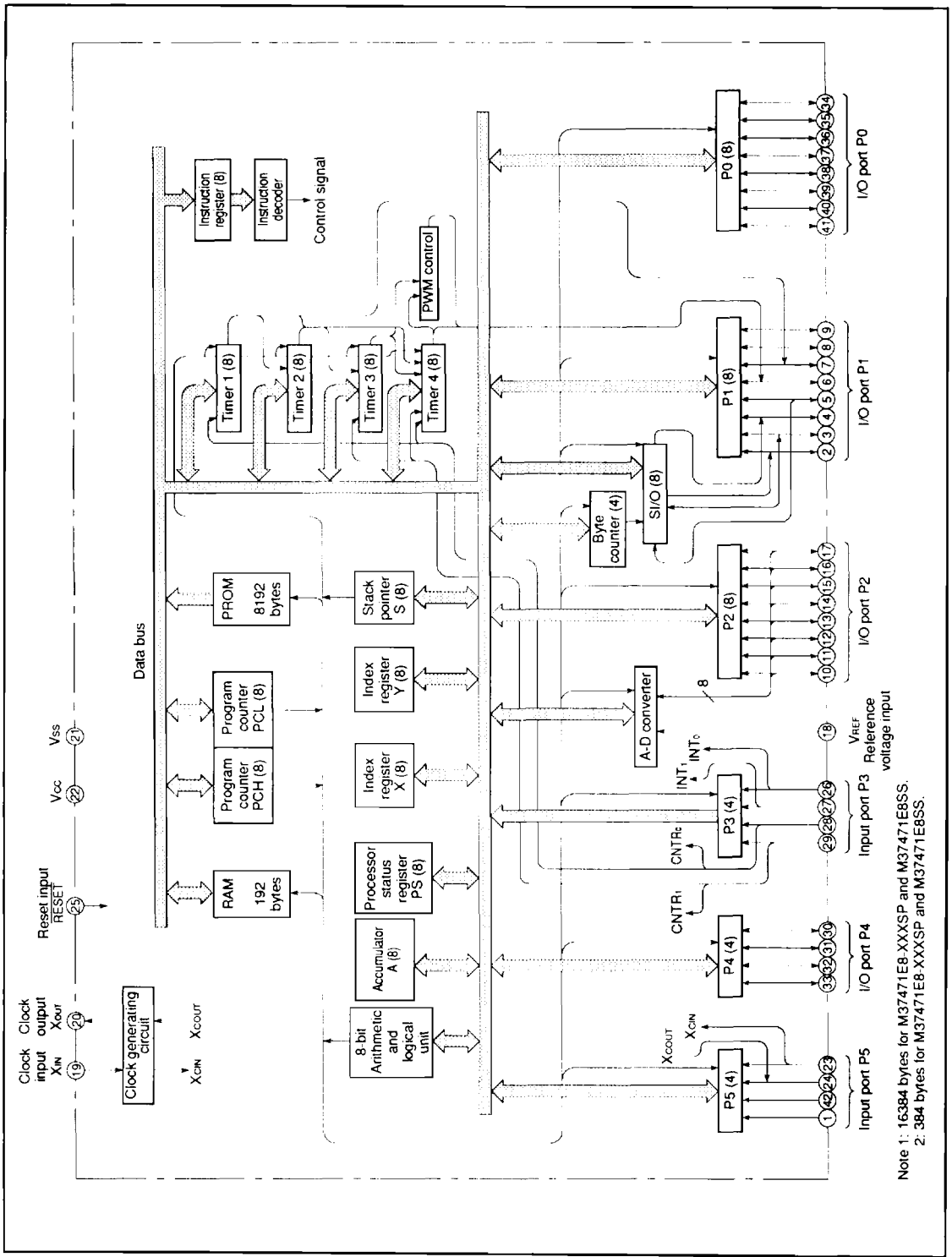

Fig.4.3.2 Block diagram of M37471E4-XXXSP and M37471E8-XXXSP(M37471E8SS)

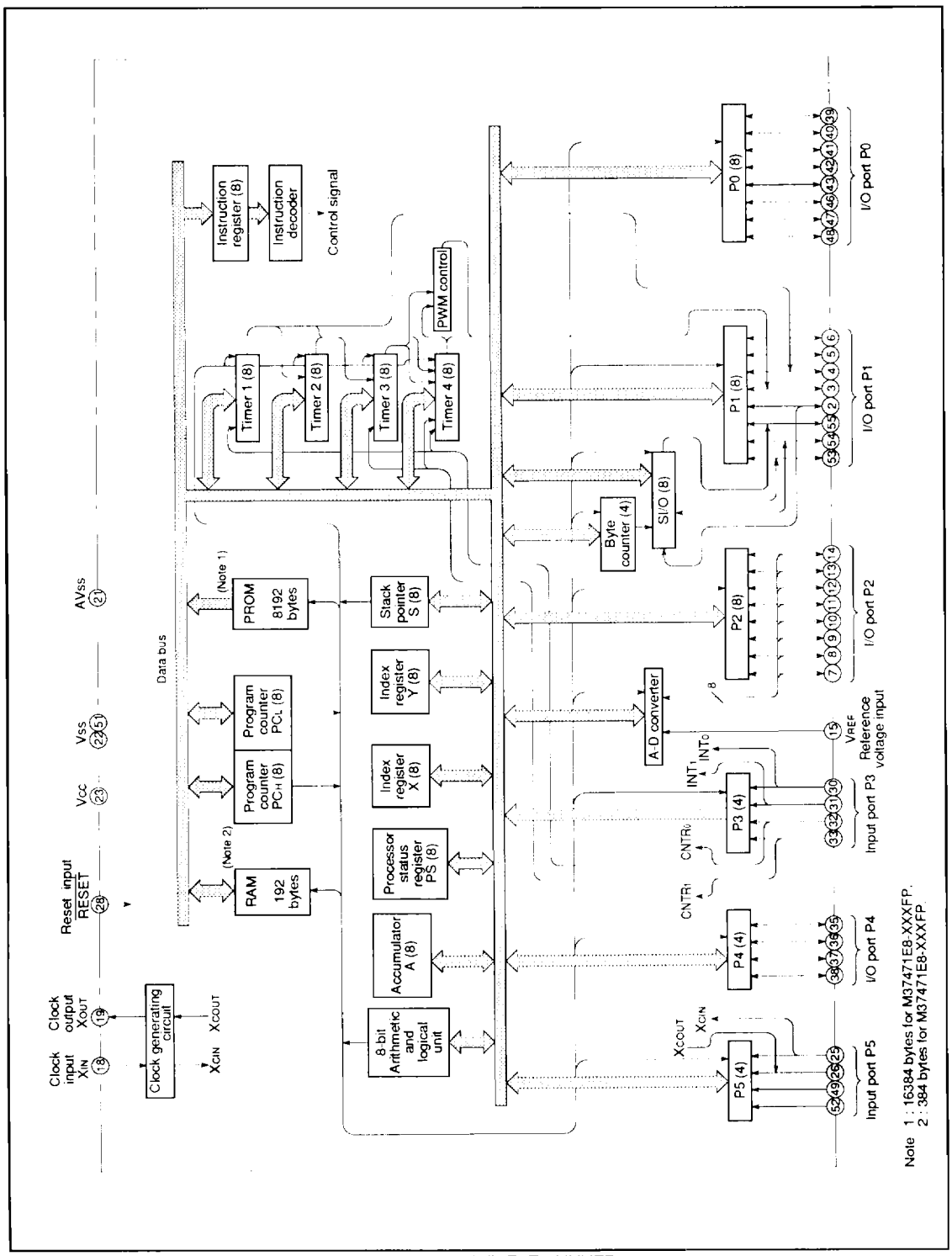

Fig.4.3.3 Block diagram of M37471E4-XXXFP and M37471E8-XXXFP

4.4 EPROM mode

4.4.1 EPROM mode

The built-in PROM versions of the 7470 Series have an EPROM mode in addition to the ordinary operating mode. Use EPROM mode to write to, read from, and erase built-in PROM, in the same way as in the M5L27256 (EPROM device).

The pin assignments in EPROM mode are shown in Table 4.4.1, and pin connection diagrams are shown in Figures 4.4.1 to 4.4.3.

Table 4.4.1 Pin correspondence at the EPROM mode

Device type name	Built-in PROM version	M5L27256
Pin name	V_{CC}	V_{CC}
	$P3_3$	V_{PP}
	V_{SS}	V_{SS}
	$P1_1$ to $P1_7$, $P2_0$ to $P2_3$ $P3_0$, $P3_1$, $P4_0$, $P4_1$	A_0 to A_{14}
	$P0_0$ to $P0_7$	D_0 to D_7
	V_{REF}	$\overline{CE}$
	$P3_2$	$\overline{OE}$

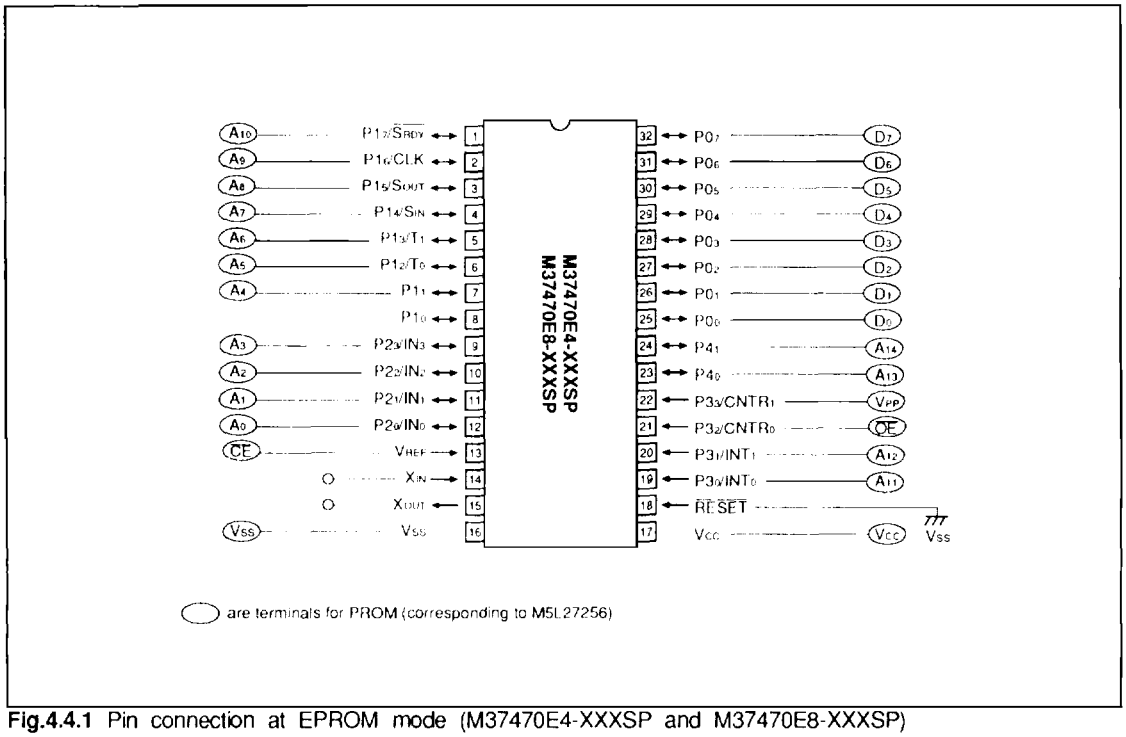

Fig.4.4.1 Pin connection at EPROM mode (M37470E4-XXXSP and M37470E8-XXXSP)

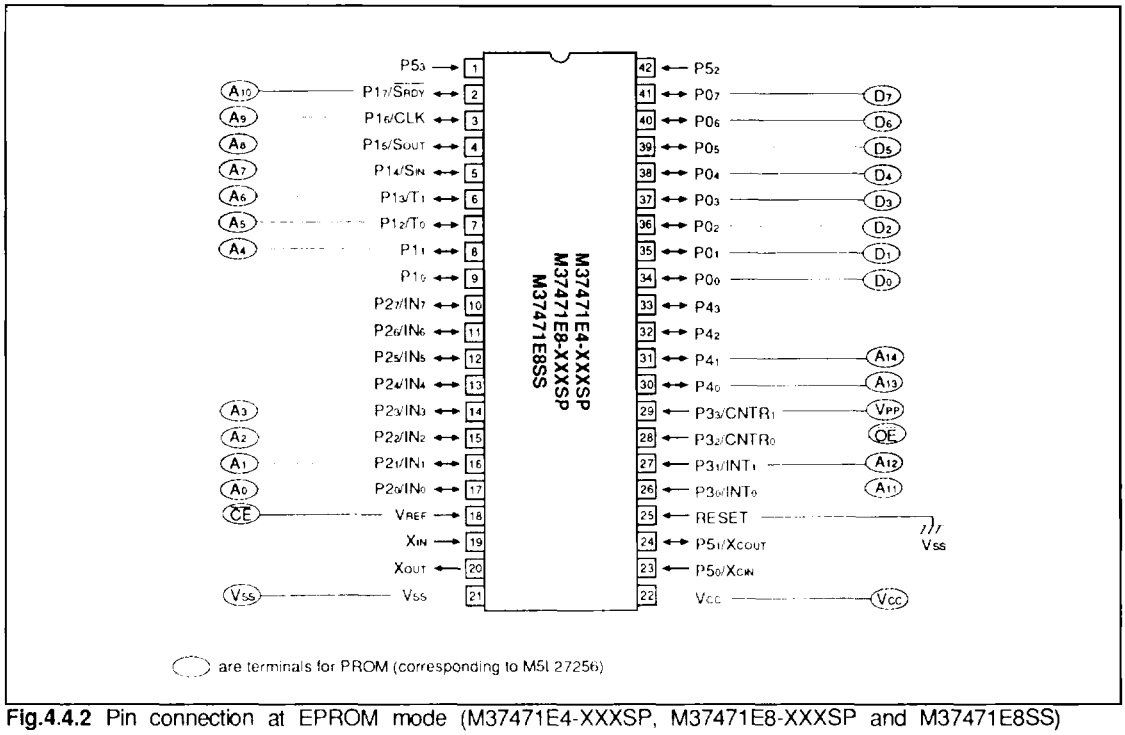

Fig.4.4.2 Pin connection at EPROM mode (M37471E4-XXXSP, M37471E8-XXXSP and M37471E8SS)

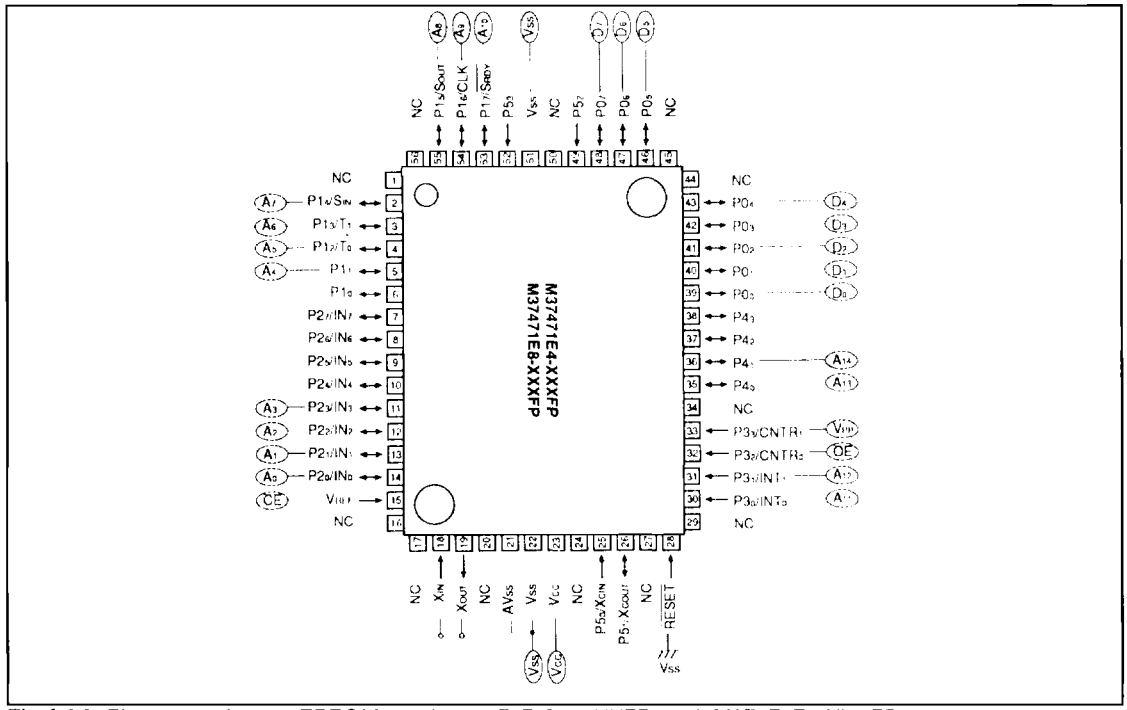

Fig.4.4.3 Pin connection at EPROM mode (M37471E4-XXXFP and M37471E8-XXXFP)

4.4.2 Pin description

Table 4.4.2 shows the pin description at ordinary operating mode and EPROM mode.

Table 4.4.2 Pin description

Pin	Name	Mode	Function
V_{CC}, V_{SS}	Supply voltage	Ordinary operation/ EPROM	Supply 2.7 to 5.5V to V_{CC}, and 0V to V_{SS}.
AVss	Analog power supply	Ordinary operation/ EPROM	Acts as ground level input pin for A-D converter. Same voltage as Vss is applied. (Note 1)
VREF	Reference voltage input	Ordinary operation	Acts as reference voltage input pin for the A–D converter.
	Mode input	EPROM	Becomes CE input.
RESET	Reset input	Ordinary operation	Specifies reset when held at "L" for at least 2μs.
		EPROM	Connect to Vss.
XIN	Clock input	Ordinary operation/ EPROM	Acts as input and output pins interfacing with the internal clock generating circuit. Connect a ceramic resonator or crystal oscillator between the XIN and XOUT pins to set the oscillator frequency. An internal feedback resistor is connected between the XIN and XOUT pins. If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.
XOUT	Clock output	Ordinary operation/ EPROM	
$P0_0$–$P0_7$	I/O port P0	Ordinary operation	Acts as 8–bit I/O port with CMOS output format. When input port is selected, these pins can be connected individually to pull-up transistors. A key on wakeup function is also provided.
	Data I/O D_0–D_7	EPROM	Becomes data(D_0–D_7) I/O.
$P1_0$–$P1_7$	I/O port P1	Ordinary operation	Acts as 8–bit I/O port with CMOS output format. When input port is selected, these pins can be connected in groups of four to pull-up transistors. $P1_2$ and $P1_3$ can also be used as timer outputs T_0 and T_1, and $P1_4$, $P1_5$, $P1_6$, and $P1_7$ can also be used as SIN, SOUT, CLK, and SRDY of the serial I/O function. SOUT and SRDY outputs can be set to N–channel open drain output.
	Address input A_4–A_{10}	EPROM	Pins $P1_1$ to $P1_7$ are address(A_4–A_{10}) input pins. Leave $P1_0$ pin open.
$P2_0$–$P2_7$ (Note 2)	I/O port P2	Ordinary operation	Acts as 8–bit I/O port with CMOS output format. When input port is selected, these pins can be connected in groups of four to pull-up transistors. These pins can also be used as analog inputs IN_0 to IN_7.
	Address input A_0–A_3	EPROM	Pins $P2_0$ to $P2_3$ are address(A_0–A_3) input pins. Leave $P2_4$ to $P2_7$ open.

Note 1: For 56-pin QFP type only.
2: At M37470E4-XXXSP and M37470E8-XXXSP, there are 4-bit as $P2_0$–$P2_3$(IN_0–IN_3) only.

Table 4.4.2 Pin description

Pin	Name	Mode	Function
$P3_0$-$P3_3$	Input port P3	Ordinary operation	Acts as 4-bit input port. $P3_0$ and $P3_1$ can also be used as external interrupt input pins INT_0 and INT_1, and $P3_2$ and $P3_3$ can also be used as timer input pins $CNTR_0$ and $CNTR_1$.
	Address input A_{11}, A_{12} Mode input V_{PP} input	EPROM	Pins $P3_0$ and $P3_1$ are address(A_{11}, A_{12}) input pins. $P3_2$ becomes $\overline{OE}$ input pin. $P3_3$ becomes V_{PP} input pin. At programming and program verifing, supply V_{PP} level into this pin.
$P4_0$-$P4_3$ (Note 2)	I/O port P4	Ordinary operation	Acts as 4-bit I/O port with CMOS output format. When input port is selected, these pins can be connected in groups of four to pull-up transistors.
	Address input A_{13}, A_{14}	EPROM	Pins $P4_0$ and $P4_1$ are address(A_{13}, A_{14}) input pins. Leave pins $P4_2$ and $P4_3$ open.
$P5_0$-$P5_3$ (Note 3)	Input port P5	Ordinary operation	Acts as 4-bit input port that can be connected as a group of four pins to pull-up transistors. $P5_0$ and $P5_1$ can also be used as the X_{CIN} and X_{COUT} pins for the clock-function clock generating circuit. When using these pins as X_{CIN} and X_{COUT} pins, an internal feedback resistor is connected between them. To enable external clock input, connect the clock source to the X_{CIN} pin and leave the X_{COUT} pin open.
		EPROM	Setting to open.

Note 2: At M37470E4-XXXSP and M37470E8-XXXSP, there are 2-bit as $P4_0$ and $P4_1$ only.
3: At M37470E4-XXXSP and M37470E8-XXXSP, there are nothing.

4.4.3 Reading, writing, and erasure of built-in PROM

Activate EPROM mode in the built-in PROM versions by forcing the RESET pin to "L". In EPROM mode, the built-in PROM can be read from, written to, and erased, as described below.

(1) Reading

Apply 0V to the $\overline{\text{RESET}}$ pin and 5V to the V_{CC} pin.

Input the address signal (A_0 to A_{14}) and set the CE and OE pins to "L"—the PROM contents will appear at the data I/O pins (D_0 to D_7). If the CE pin or the OE pin is set to "H", the data I/O pins will float.

(2) Writing

Apply 0V to the $\overline{\text{RESET}}$ pin and 6V to the V_{CC} pin.

Set the $\overline{\text{OE}}$ pin to "H" and apply V_{PP} to the V_{PP} pin to activate program mode. Set the address to be written to by the address input pins (A_0 to A_{14}) and input the data in parallel through the data I/O pins (D_0 to D_7). When the $\overline{\text{CE}}$ pin is set to "L" in this status, the data is written to PROM.

(3) Erasure

Only the built-in EPROM version that has an erasure window on the package's top surface (M37471E8SS) can be erased. To erase the EPROM, shine an ultraviolet light source of wavelength 2537Å onto the window for a minimum dose of 15W·s/cm^2.

Note the following points when writing data with a PROM writer:

- M37470E4-XXXSP, and M37471E4-XXXSP/FP

  When using a PROM writer, the address range should be between 6000_{16} and $7FFF_{16}$. Read/write operations on addresses 0000_{16} to $5FFF_{16}$ cannot be performed correctly.

- M37470E8-XXXSP, M37471E8-XXXSP/FP and M37471E8SS

  When using a PROM writer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16}.

Table 4.4.3 Input/Output signal at each mode

Mode \ Pin name	CE	OE	V_{PP}	V_{CC}	RESET	D_0~D_7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	0V	Output
Output disable	V_{IL}	V_{IH}	V_{CC}			Floating
Write	V_{IL}	V_{IH}	12.5V			Input
Verify	V_{IH}	V_{IL}	12.5V			Output
Write disable	V_{IH}	V_{IH}	12.5V			Floating

Note : V_{IL} means "L" input voltage, V_{IH} means "H" input voltage.

4.4.4 Notes on handling

(1) Sunlight and fluorescent light include wavelengths that will erase written data. When using the window version of the 7470 Series in read mode, always cover the transparent glass window with a light-proof seal.
(2) Mitsubishi provides light-proof seals designed to cover the transparent glass window of the window version. Make sure that the seal does not touch the lead pins of the microcomputer.
(3) Before erasing the window version, clean the transparent glass of the window. Dirt such as grease from hands and glue may hinder the passage of ultraviolet light and affect the erasure characteristics.
(4) Writing involves the use of high voltages, so make sure that excessive voltages are not used. Pay particular attention when turning on the power source.
(5) Mitsubishi does not test or screen any writing to PROM in blank one-time programmable microcomputers*1 after they have left the factory. To improve reliability after writing, we recommend that these microcomputers are written to and tested in the sequence shown in the flow diagram of Figure 4.4.4.

(*1: Blank microcomputers have nothing written in PROM when they leave the factory.)

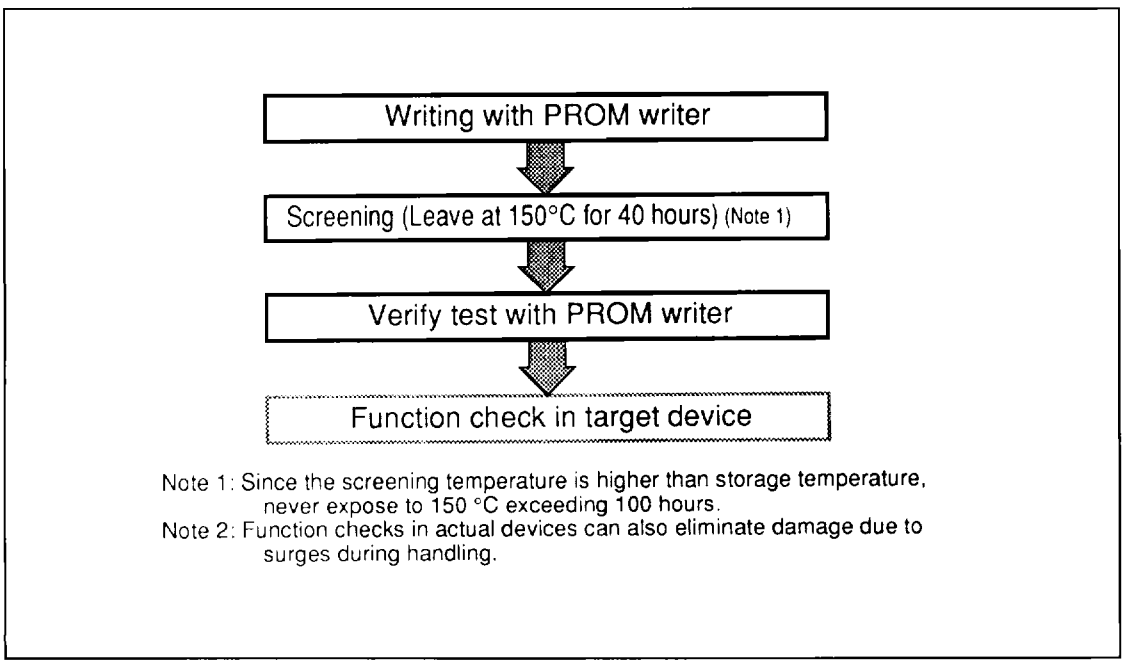

Fig.4.4.4 Writing and test for blank one-time programmable type

4.5 Electric Characteristics

4.5.1 Electric characteristics of M37470E4-XXXSP and M37470E8-XXXSP

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3 to 7	V
V_I	Input voltage X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_3$, $P4_0$–$P4_1$, V_{REF}, $\overline{RESET}$		−0.3 to V_{CC}+0.3 (Note 1)	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$–$P4_1$, X_{OUT}		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	T_a=25°C	1000	mW
Topr	Operating temperature		−20 to 85	°C
Tstg	Storage temperature		−40 to 150	°C

Note 1: At writing to PROM, the value for $P3_3$ is 13V.

Recommended operating conditions (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$–$P2_3$, $P4_0$–$P4_1$	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$–$P2_3$, $P4_0$–$P4_1$	0		0.25V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
I_{OH}(sum)	"H" sum output current $P0_0$–$P0_7$, $P4_0$–$P4_1$			−30	mA
I_{OH}(sum)	"H" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_3$			−30	mA
I_{OL}(sum)	"L" sum output current $P0_0$–$P0_7$, $P4_0$–$P4_1$			60	mA
I_{OL}(sum)	"L" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_3$			60	mA
I_{OH}(peak)	"H" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$–$P4_1$			−10	mA
I_{OL}(peak)	"L" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$–$P4_1$			20	mA
I_{OH}(avg)	"H" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$–$P4_1$ (Note 3)			−5	mA
I_{OL}(avg)	"L" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$–$P4_1$ (Note 3)			10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 2)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK($P1_6$) (Note 2)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 2)			4	MHz

Note 2: Oscillation frequency is at 50% duty cycle.

3: The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms.

Electrical characteristics (V_{CC}=2.7 to 5.5V, V_{SS}=0V, Ta=−20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{T+}–V_{T-}	Hysteresis $P0_0$–$P0_7$, $P3_0$–$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}–V_{T-}	Hysteresis RESET	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}–V_{T-}	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_2$, $P4_0$, $P4_1$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$–$P2_3$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current RESET, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_2$, $P4_0$, $P4_1$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$–$P2_3$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current RESET, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed f(X_{IN})=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed f(X_{IN})=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At wait mode, f(X_{IN})=4MHz	V_{CC}=5V		1	2	
			V_{CC}=3V		0.5	1	
		Stop all oscillation V_{CC}=5V	Ta=25°C		0.1	1	µA
			Ta=85°C		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D converter characteristics

(V_{CC}=2.7 to 5.5V, V_{SS}=0V, Ta=−20 to 85°C, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, I_{OL}(sum)=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, I_{OL}(sum)=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

4.5.2 Electric characteristics of M37471E4-XXXSP/FP, M37471E8-XXXSP/FP and M37471E8SS

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss Output transistors are at "OFF" state.	−0.3 to 7	V
V_I	Input voltage X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_3$, V_{REF}, $\overline{RESET}$		−0.3 to V_{CC}+0.3 (Note 1)	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$, X_{OUT}		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	Ta=25°C	1000(Note 2)	mW
Topr	Operating temperature		−20 to 85	°C
Tstg	Storage temperature		−40 to 150	°C

Note 1: At writing to PROM, the value for $P3_3$ is 13V.
2: 500mW for M37471E4-XXXFP and M37471E8-XXXFP.

Recommended operating conditions (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=−20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$–$P2_7$, $P4_0$–$P4_3$, $P5_0$–$P5_3$ (Note 3)	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$–$P2_7$, $P4_0$–$P4_3$, $P5_0$–$P5_3$ (Note 3)	0		0.25V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
I_{OH}(sum)	"H" sum output current $P0_0$–$P0_7$, $P4_0$–$P4_3$			−30	mA
I_{OH}(sum)	"H" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_7$			−30	mA
I_{OL}(sum)	"L" sum output current $P0_0$–$P0_7$, $P4_0$–$P4_3$			60	mA
I_{OL}(sum)	"L" sum output current $P1_0$–$P1_7$, $P2_0$–$P2_7$			60	mA
I_{OH}(peak)	"H" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$			−10	mA
I_{OL}(peak)	"L" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$			20	mA
I_{OH}(avg)	"H" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$ (Note 6)			−5	mA
I_{OL}(avg)	"L" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$ (Note 6)			10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 4)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK($P1_6$) (Note 4)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 4)			4	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 4, 5)		32	50	kHz

Note 3: It is except to use $P5_0$ as X_{CIN}.
4: Oscillation frequency is at 50% duty cycle.
5: When used in the low-speed mode, the clock oscillating frequency for clock function should be $f(X_{CIN}) < f(X_{IN})/3$.
6: The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms.

Electrical characteristics (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=−20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_3$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{T+}–V_{T-}	Hysteresis $P0_0$–$P0_7$, $P3_0$–$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}–V_{T-}	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_2$, $P4_0$–$P4_3$, $P5_0$–$P5_3$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$–$P2_7$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_2$, $P4_0$–$P4_3$, $P5_0$–$P5_3$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$–$P2_7$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed f(X_{IN})=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed f(X_{IN})=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At low- speed mode, X_{COUT} is low-power mode, A-D conversion is not executed f(X_{IN})=0Hz, f(X_{CIN})=32kHz, Ta=25°C	V_{CC}=5V		30	80	μA
			V_{CC}=3V		15	40	
		At wait mode, f(X_{IN})=4MHz	V_{CC}=5V		1	2	mA
			V_{CC}=3V		0.5	1	
		At wait mode, f(X_{IN})=0Hz, f(X_{CIN})=32kHz, X_{COUT} is low-power mode, Ta=25°C	V_{CC}=5V		3	12	μA
			V_{CC}=3V		2	8	
		Stop all oscillation V_{CC}=5V	Ta=25°C		0.1	1	
			Ta=85°C		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D converter characteristics

(V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=−20 to 85°C, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, I_{OL}(sum)=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, I_{OL}(sum)=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V