User's Manual

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R8C/LAPS Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/Lx Series

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/LAPS Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview	—	—
User's Manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/LAPS Group User's Manual: Hardware	This User's Manual
User's Manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from the Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2

*3

*1

R/W: Read and write.
R: Read only.
W: Write only.
–: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input / Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver / Transmitter
VCO	Voltage Controlled Oscillator

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0000h			
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0002h			
0003h			
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0005h	Processor Mode Register 1	PM1	153
0006h	System Clock Control Register 0	CM0	82, 93
0007h	System Clock Control Register 1	CM1	83, 94
0008h	Module Standby Control Register 0	MSTCR0	186, 261, 293
0009h	System Clock Control Register 3	CM3	84, 95
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000Bh	Reset Source Determination Register	RSTFR	24
000Ch	Oscillation Stop Detection Register	OCD	85, 96
000Dh	Watchdog Timer Reset Register	WDTR	153
000Eh	Watchdog Timer Start Register	WDTS	153
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0038h	Voltage Monitor 0 Circuit Control Register	VW0C	41
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	42
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Address	Register	Symbol	Page
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0044h			
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004Ah			
004Bh			
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004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register	SSUIC/IICIC	119
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0051h			
0052h			
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0058h	Timer RB0 Interrupt Control Register	TRB0IC	118
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Note:
1. Blank spaces are reserved. No access is allowed.

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Address	Register	Symbol	Page
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
:			
FFDBh	Option Function Select Register 2	OFS2	26, 149, 156
:			
FFFFh	Option Function Select Register	OFS	25, 44, 148, 155, 332

1. Overview

1.1 Features

The R8C/LAPS Group of single-chip MCUs incorporates the R8C CPU core, which implements a powerful instruction set for a high level of efficiency and supports a 1 Mbyte address space, allowing execution of instructions at high speed. In addition, the CPU core integrates a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and synchronous serial communication unit (SSU), helps reduce the number of system components.
The R8C/LAPS Group has data flash (2 KB × 2 blocks).

1.1.1 Applications

Remote control, etc.

1.1.2 Specifications

Table 1.1 lists the Specifications.

Table 1.1 Specifications

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.0 V to 5.5 V) 125 ns (f(XIN) = 8 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash	Refer to **Table 1.2 Product List**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 25, CMOS input port: 1, selectable pull-up resistor (1) • High current drive ports: 8
Clock	Clock generation circuits	• 2 circuits: XIN clock oscillation circuit Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 • Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 13 ($\overline{\text{INT}}$ × 5, key input × 8) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for watchdog timer
Timer	Timer RB0, Timer RB1	8 bits × 2 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timer RJ0	16 bits × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
Synchronous Serial Communication Unit (SSU)		1 (shared with I²C-bus)
I²C bus		1 (shared with SSU)
Flash Memory		• Programming and erasure voltage: VCC = 1.8 V to 5.5 V (data flash VCC = 1.8 V to 5.5 V) • Programming and erasure endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ROM code protect, ID code check • On-chip debug function • On-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 10 MHz (VCC = 2.0 V to 5.5 V) f(XIN) = 8 MHz (VCC = 1.8 V to 5.5 V)
Current Consumption		Typ. 4.7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 2.3 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 0.5 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		–20 to 85°C (N version)

Note:
1. No pull-up resistor is provided in the pins P5_4 to P5_6.

1.2 Product Lists

Table 1.2 lists product information for R8C/LAPS Group. Figure 1.1 shows the Correspondence of Part No., with Memory Size and Package for R8C/LAPS Group.

Table 1.2 Product List for R8C/LAPS Group **Current of Sep 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LAP6SNSP	32 Kbytes	2 Kbyte × 2	3 Kbytes	PLSP0030JB-A	N Version
R5F2LAP7SNSP	48 Kbytes	2 Kbyte × 2	3 Kbytes	PLSP0030JB-A	
R5F2LAP8SNSP	64 Kbytes	2 Kbyte × 2	3 Kbytes	PLSP0030JB-A	
R5F2LAPASNSP	96 Kbytes	2 Kbyte × 2	3.5 Kbytes	PLSP0030JB-A	
R5F2LAPCSNSP	128 Kbytes	2 Kbyte × 2	3.5 Kbytes	PLSP0030JB-A	

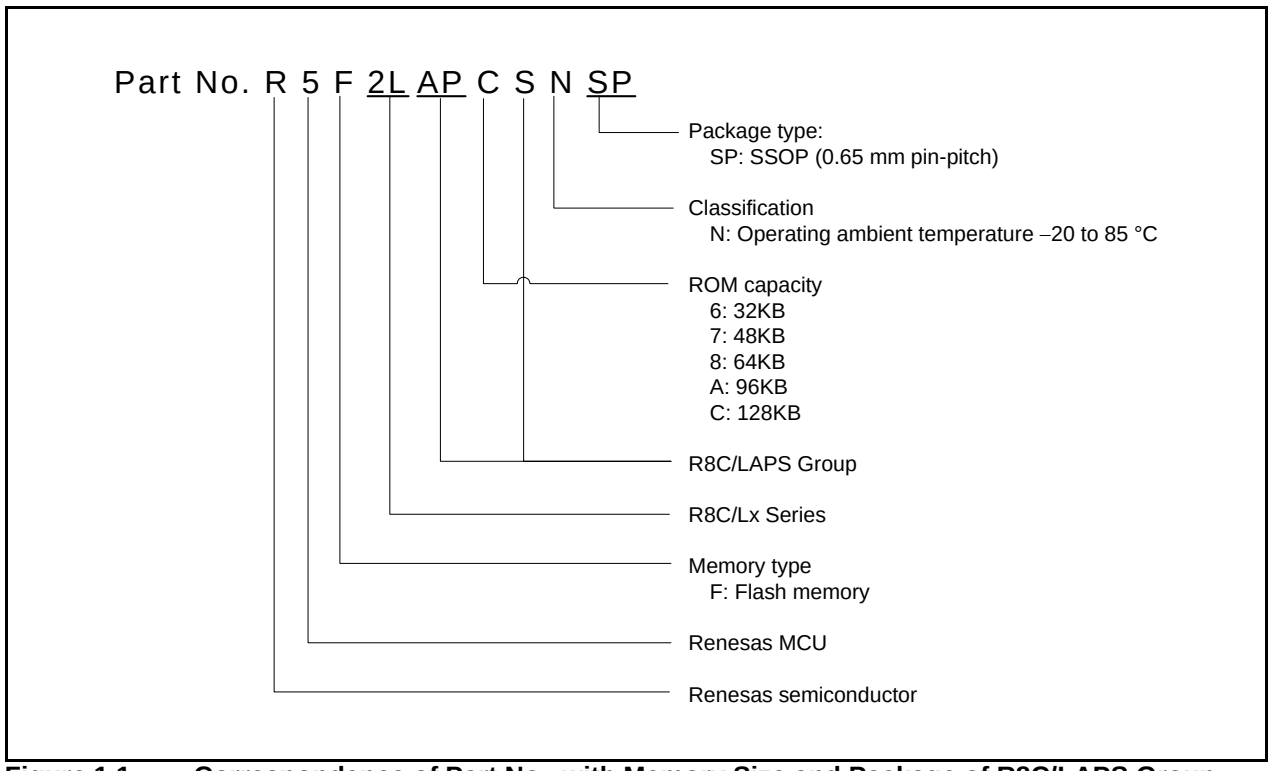


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LAPS Group

1.3 Block Diagrams

Figure 1.2 shows a Block Diagram of R8C/LAPS Group.

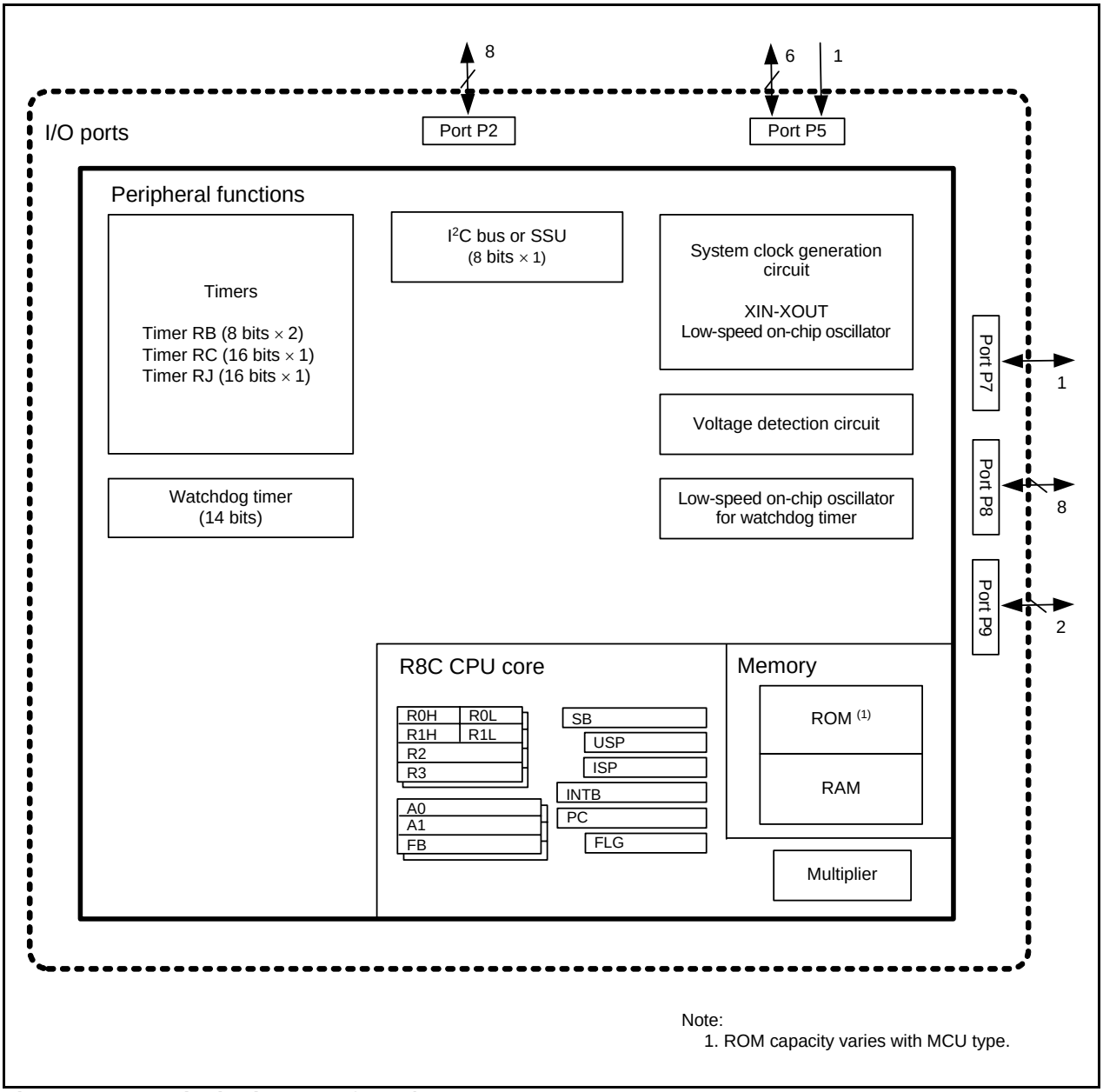
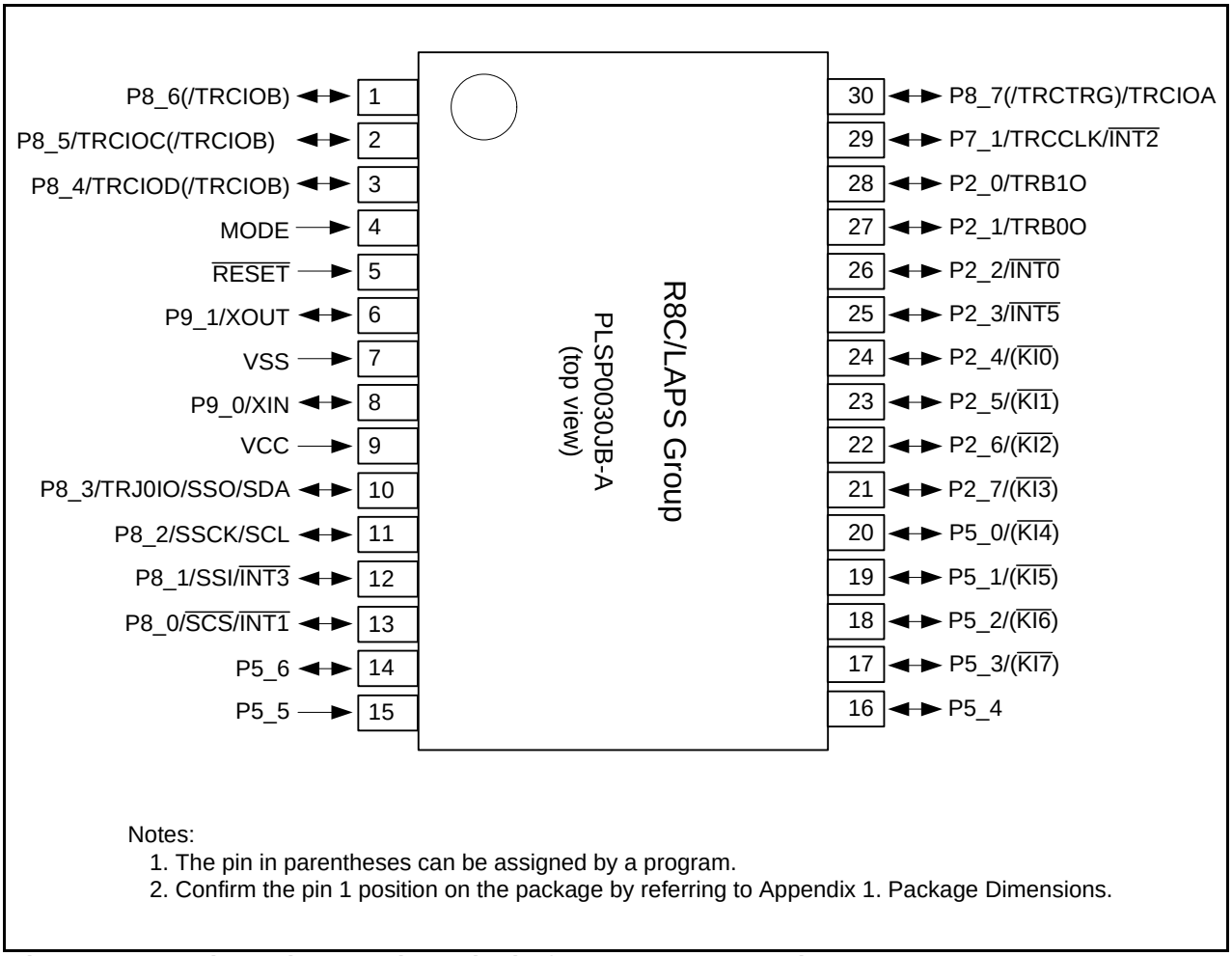


Figure 1.2 Block Diagram of R8C/LAPS Group

1.4 Pin Assignments

Figure 1.3 shows pin assignments (top view). Table 1.3 lists the pin name information by pin number.



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to Appendix 1. Package Dimensions.

Figure 1.3 Pin Assignment (Top View) of PLSP0030JB-A Package

Table 1.3 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules			
			Interrupt	Timer	SSU	I²C bus
1		P8_6		(TRCIOB)		
2		P8_5		TRCIOC(/TRCIOB)		
3		P8_4		TRCIOD(/TRCIOB)		
4	MODE					
5	$\overline{\text{RESET}}$					
6	XOUT	P9_1				
7	VSS					
8	XIN	P9_0				
9	VCC					
10		P8_3		TRJ0IO	SSO	SDA
11		P8_2			SSCK	SCL
12		P8_1	$\overline{\text{INT3}}$		SSI	
13		P8_0	$\overline{\text{INT1}}$		$\overline{\text{SCS}}$	
14		P5_6				
15		P5_5				
16		P5_4				
17		P5_3	($\overline{\text{KI7}}$)			
18		P5_2	($\overline{\text{KI6}}$)			
19		P5_1	($\overline{\text{KI5}}$)			
20		P5_0	($\overline{\text{KI4}}$)			
21		P2_7	($\overline{\text{KI3}}$)			
22		P2_6	($\overline{\text{KI2}}$)			
23		P2_5	($\overline{\text{KI1}}$)			
24		P2_4	($\overline{\text{KI0}}$)			
25		P2_3	$\overline{\text{INT5}}$			
26		P2_2	$\overline{\text{INT0}}$			
27		P2_1		TRB0O		
28		P2_0		TRB1O		
29		P7_1	$\overline{\text{INT2}}$	TRCCLK		
30		P8_7		(TRCTRG/)TRCIOA		

Note:
1. The pin in parentheses can be assigned by a program.

1.5 Pin Functions

Table 1.4 lists Pin Functions for R8C/LAPS Group.

Table 1.4 Pin Functions for R8C/LAPS Group

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins
Timer RB	TRB0O, TRB1O	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RJ	TRJ0IO	I/O	Timer RJ I/O pins
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
I/O ports	P2_0 to P2_7, P5_0 to P5_4, P5_6, P7_1, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Port P8 can be used as LED drive ports.
Input port	P5_5	I	Input-only port

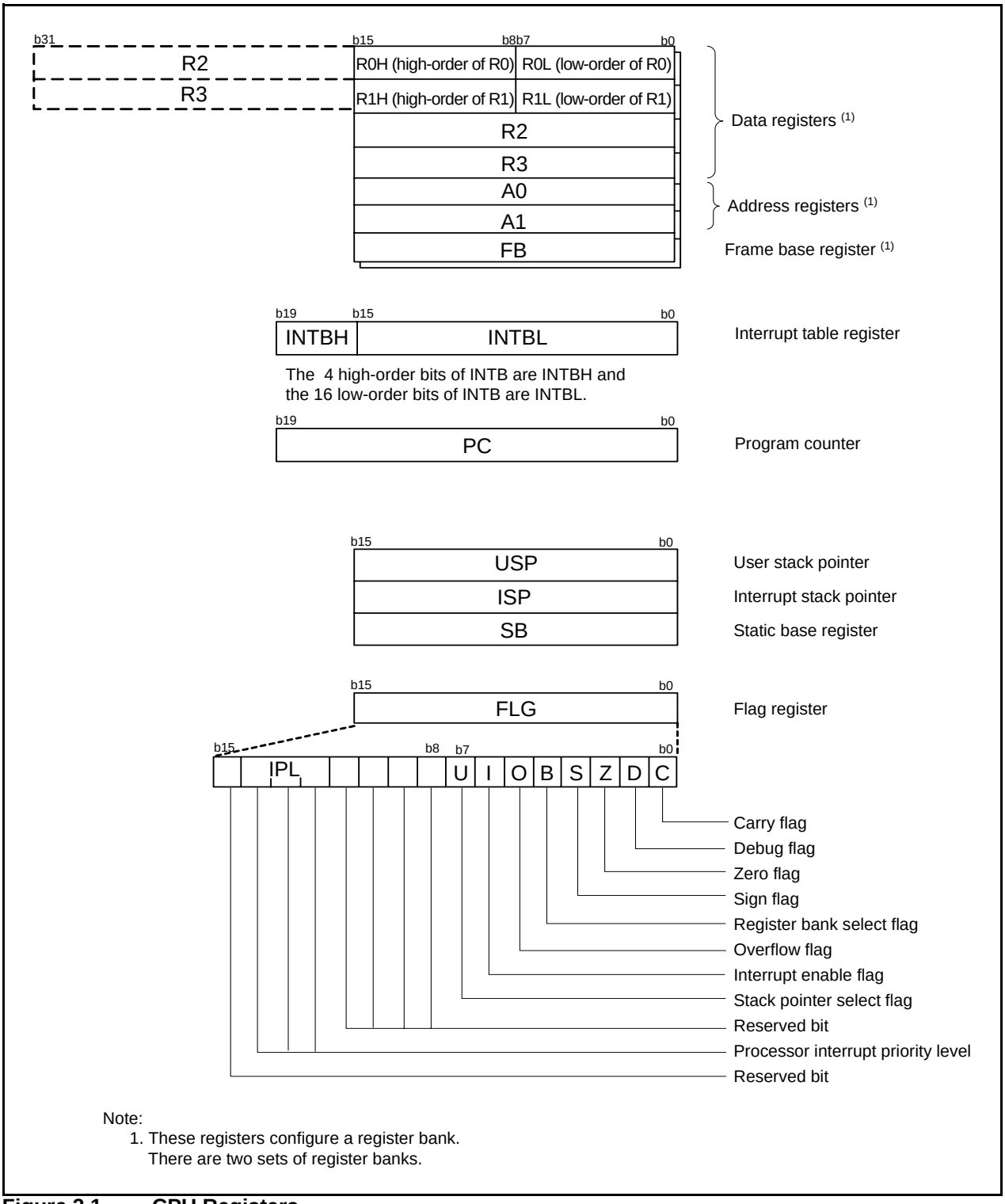
I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.



Note:
1. These registers configure a register bank.
There are two sets of register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

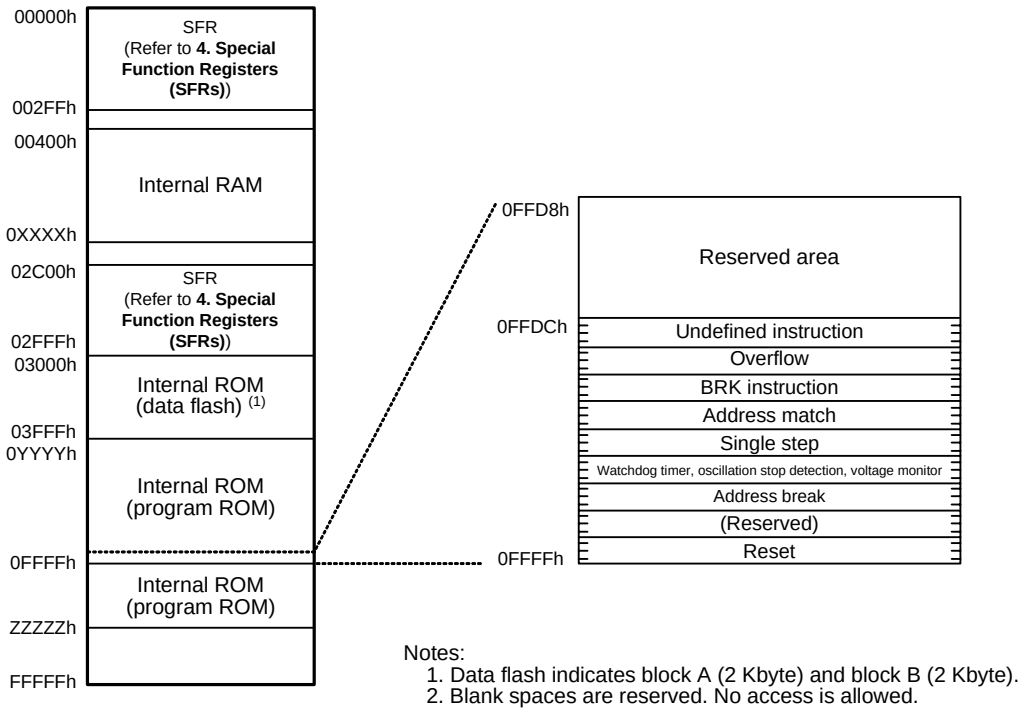
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

Figure 3.1 is a Memory Map of R8C/LAPS Group. The R8C/LAPS Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh. The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3-Kbyte internal RAM area is allocated addresses 00400h to 00FFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (2 Kbyte) and block B (2 Kbyte).
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM		Data Flash
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh	
R5F2LAP6SNSP	32 Kbytes	08000h	0FFFFh	3 Kbytes	00FFFh	Available
R5F2LAP7SNSP	48 Kbytes	04000h	0FFFFh	3 Kbytes	00FFFh	
R5F2LAP8SNSP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	
R5F2LAPASNSP	96 Kbytes	04000h	1BFFFh	3.5 Kbytes	011FFh	
R5F2LAPCSNSP	128 Kbytes	04000h	23FFFh	3.5 Kbytes	011FFh	

Figure 3.1 Memory Map of R8C/LAPS Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.9 list SFR information and Table 4.10 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h 00000100b (2)
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register 0	MSTCR0	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh (3)
000Ch	Oscillation Stop Detection Register	OCD	00000100b (4) 00h (4)
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Module Standby Control Register 1	MSTCR1	00h
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (5)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (6) 00100000b (7)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (6) 1100X011b (7)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. The CSPRO bit in the CSPR register is set to 1.
3. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
4. The reset value differs depending on the mode.
5. The CSPROINI bit in the OFS register is set to 0.
6. The LVDAS bit in the OFS register is set to 1.
7. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h			
0052h			
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h			
00A1h			
00A2h			
00A3h			
00A4h			
00A5h			
00A6h			
00A7h			
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h			
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h			
00E2h			
00E3h			
00E4h	Port P2 Register	P2	XXh
00E5h			
00E6h	Port P2 Direction Register	PD2	00h
00E7h			
00E8h			
00E9h	Port P5 Register	P5	XXh
00EAh			
00EBh	Port P5 Direction Register	PD5	00h
00ECh			
00EDh	Port P7 Register	P7	XXh
00EEh			
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h	Port P9 Register	P9	XXh
00F2h	Port P8 Direction Register	PD8	00h
00F3h	Port P9 Direction Register	PD9	00h
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h			
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh			
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h	Timer Carrier Wave I/O Control Register	TRCRIO	00h
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h			
01E4h			
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h			
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h	Port P8 Pull-Up Control Register	P8PUR	00h
01E9h	Port P9 Pull-Up Control Register	P9PUR	00h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h	Port P8 Drive Capacity Control Register	P8DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
:			
2FFFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.10 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

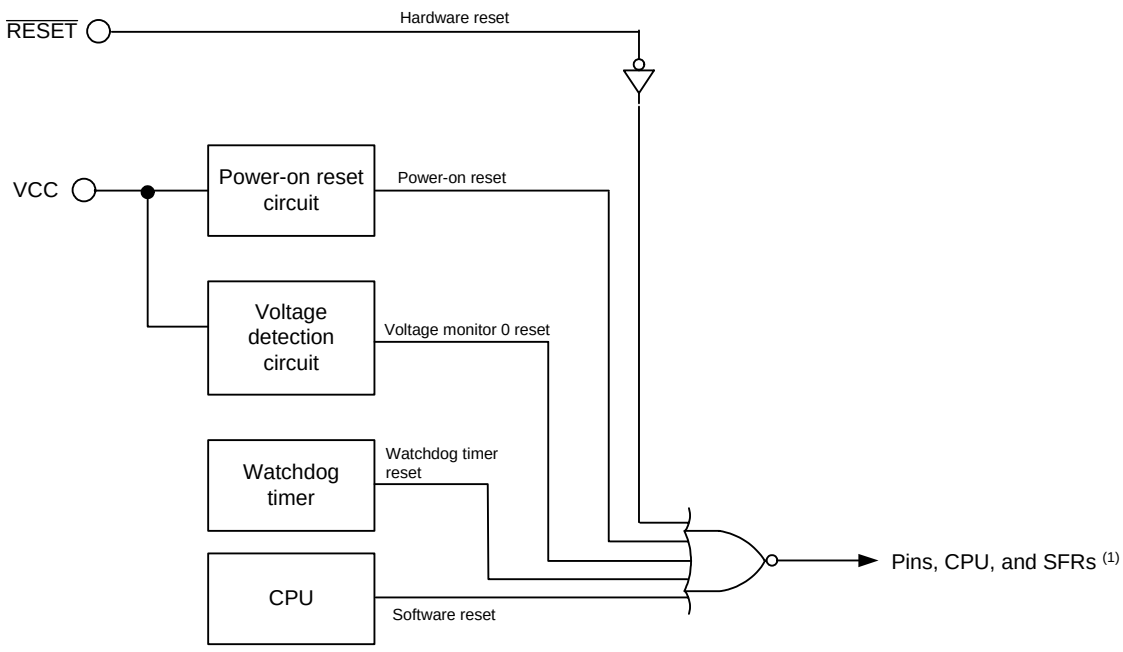
Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Resets

The following resets are available: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources and Figure 5.1 shows the Reset Circuit Block Diagram.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	The input voltage to the $\overline{\text{RESET}}$ pin is held low.
Power-on reset	VCC rises.
Voltage monitor 0 reset	VCC falls. (Monitor voltage: Vdet0)
Watchdog timer reset	Underflow of the watchdog timer
Software reset	Write 1 to the PM03 bit in the PM0 register.



Note:
1. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.

Figure 5.1 Reset Circuit Block Diagram

Table 5.2 shows the Pin Status while $\overline{\text{RESET}}$ Pin Level is Low. Figure 5.2 shows the CPU Register Status after Reset and Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Status while $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Pin Status
P2, P5_0 to P5_6, P7_1, P8, P9_0 to P9_1	High impedance

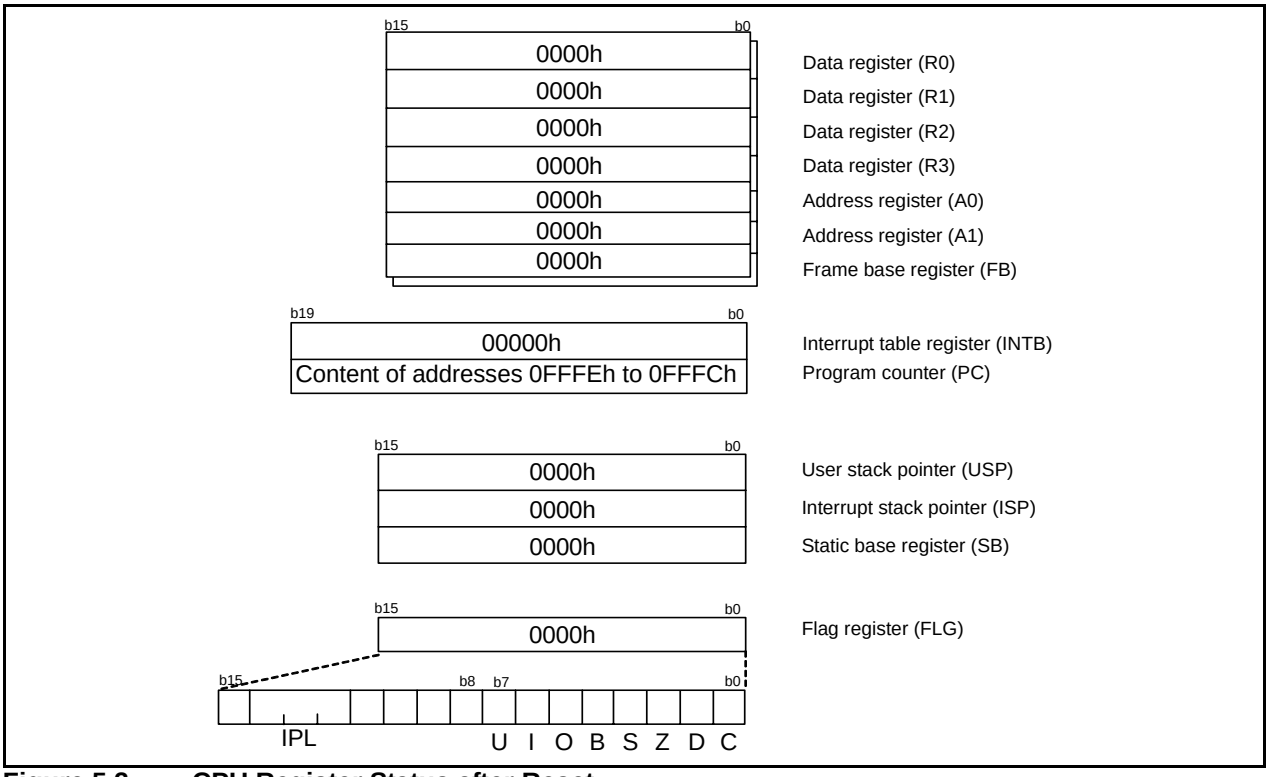
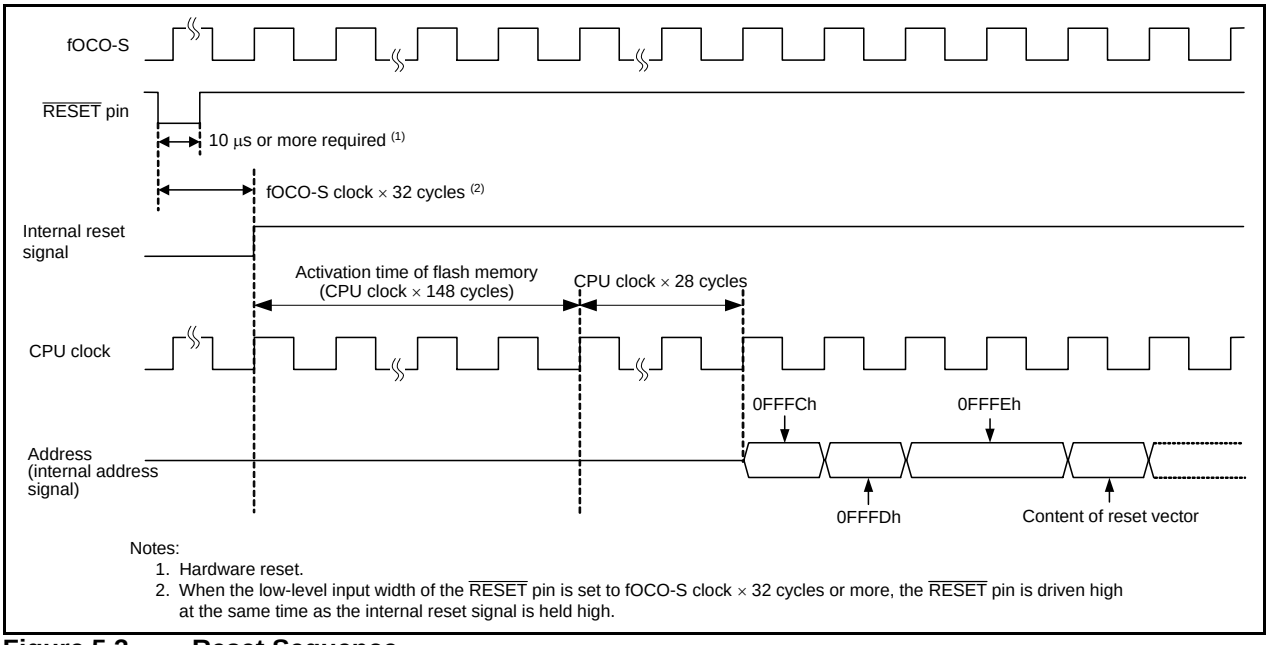


Figure 5.2 CPU Register Status after Reset



Notes:
1. Hardware reset.
2. When the low-level input width of the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 32 cycles or more, the $\overline{\text{RESET}}$ pin is driven high at the same time as the internal reset signal is held high.

Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	Setting this bit to 1 resets the MCU. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	X	X	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag (4)	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—			

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. When 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.
4. A hardware reset is detected.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **14.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

A reset is applied using the $\overline{\text{RESET}}$ pin. When a low-level signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, the pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Status while RESET Pin Level is Low**, **Figure 5.2 CPU Register Status after Reset**, and **Table 4.1** to **Table 4.9 SFR Information**).

When the input level applied to the $\overline{\text{RESET}}$ pin changes from low to high, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after reset.

The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled low while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.

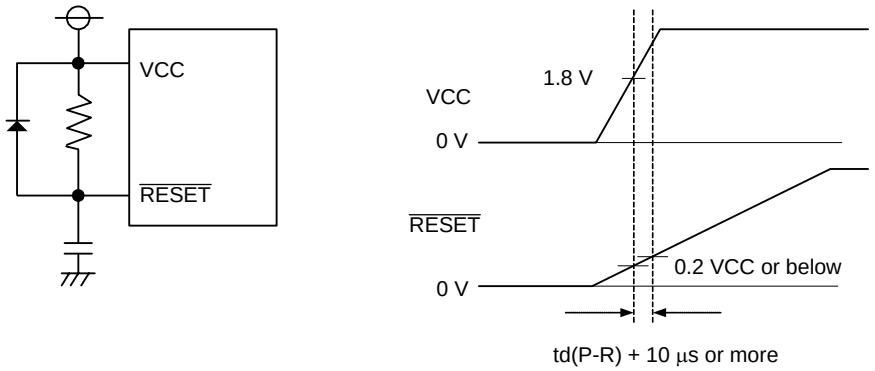
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

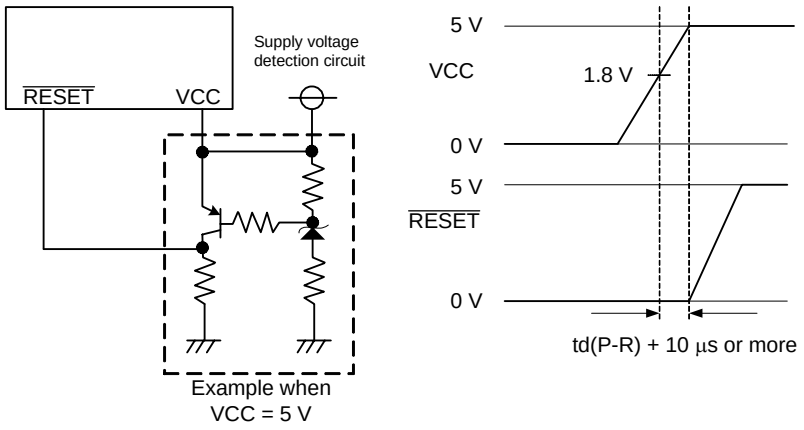
5.2.2 Power On

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **25. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **25. Electrical Characteristics**.

Figure 5.4 Example of Hardware Reset Circuit and Operation



Note:
1. Refer to **25. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

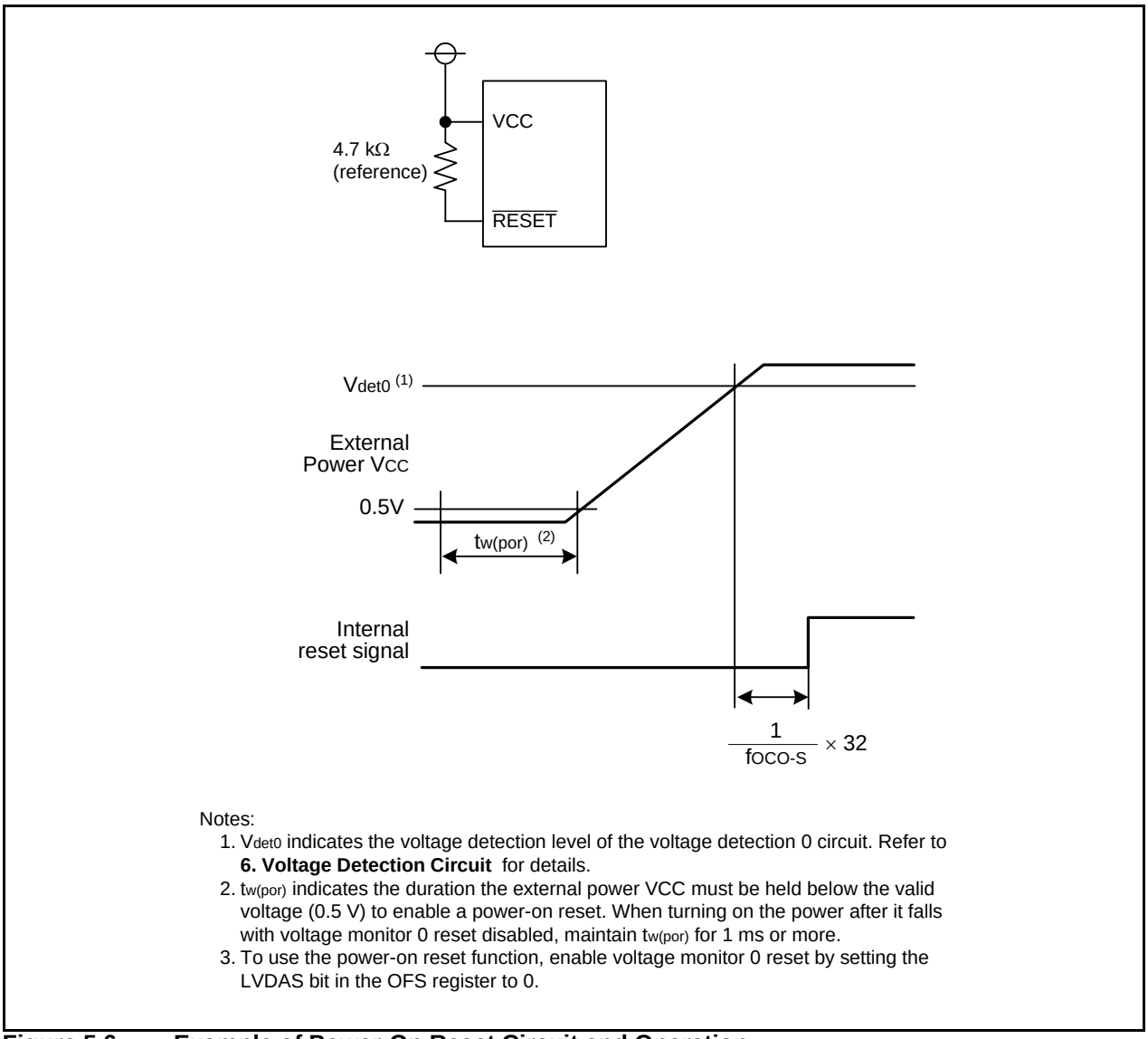
When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the pins, CPU, and SFRs are reset. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8 VCC or above.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after power-on reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset). The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 and VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFRs are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

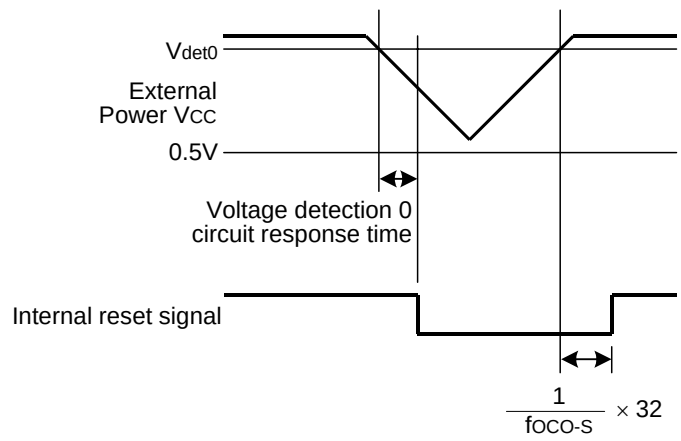
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Example of Voltage Monitor 0 Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFRs when the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows while writing to the internal RAM is in progress, the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 and WDTUFS1 and bits WDTRCS0 and WDTRCS1 in the OFS2 register, respectively.
Refer to **15. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFRs. The program beginning with the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset. When 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm start-up determination function uses voltage monitor 0 reset.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

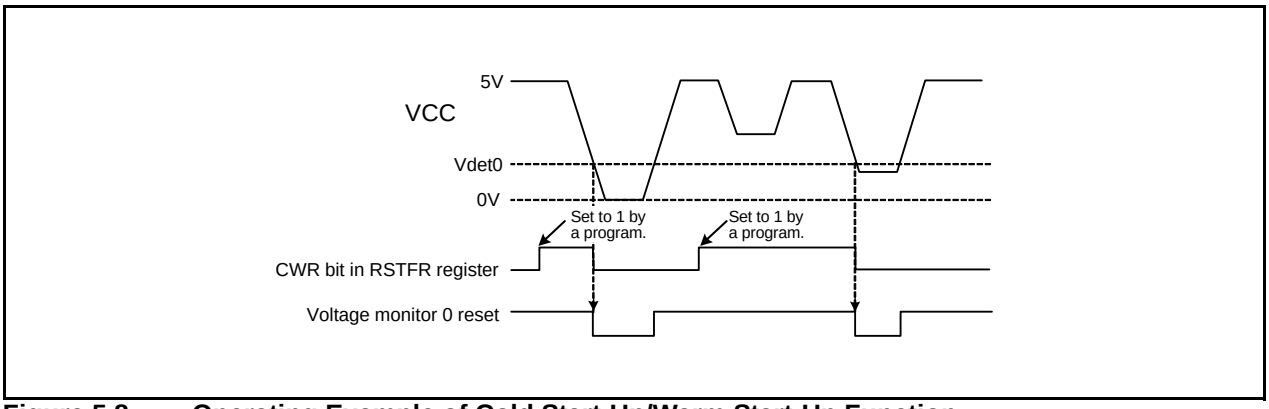


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected).
If a software reset occurs, the SWR bit is set to 1 (detected).
If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Introduction

The detection voltage of voltage detection 0 can be selected among four levels using the OFS register.
The detection voltage of voltage detection 1 can be selected among 16 levels using the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by rising or falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	Selectable among 4 levels using the OFS register.	Selectable among 16 levels using the VD1LS register.	VCC
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC or LVCMP2 input voltage is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at: Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enable/ disable	No digital filter function	Supported	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

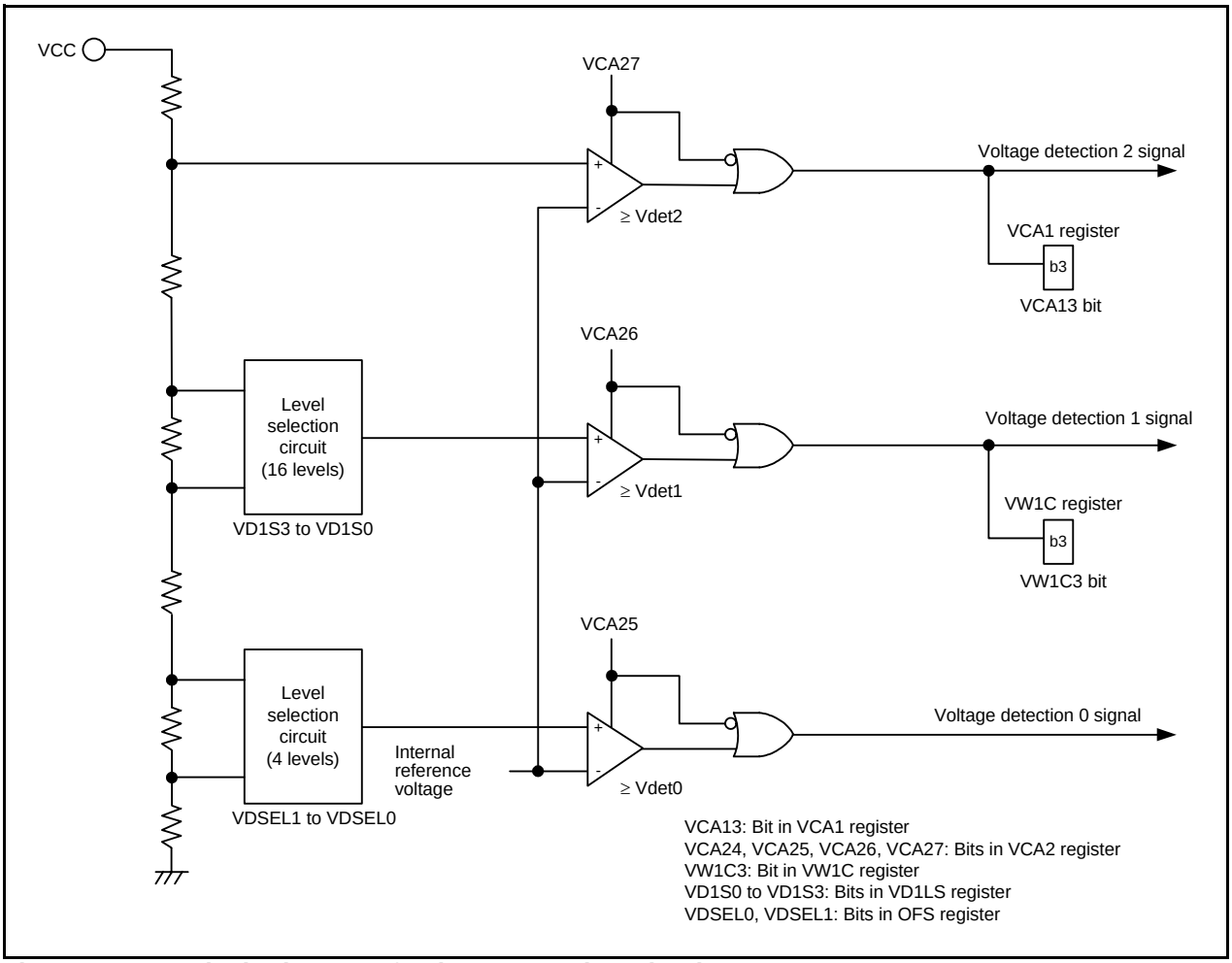


Figure 6.1 Block Diagram of Voltage Detection Circuit

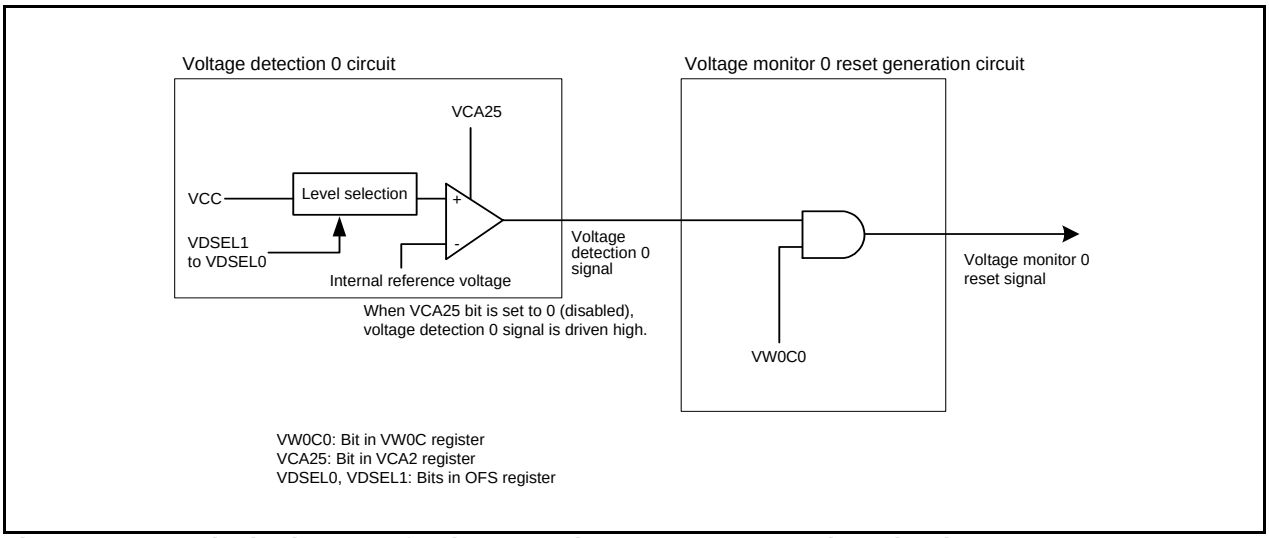


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

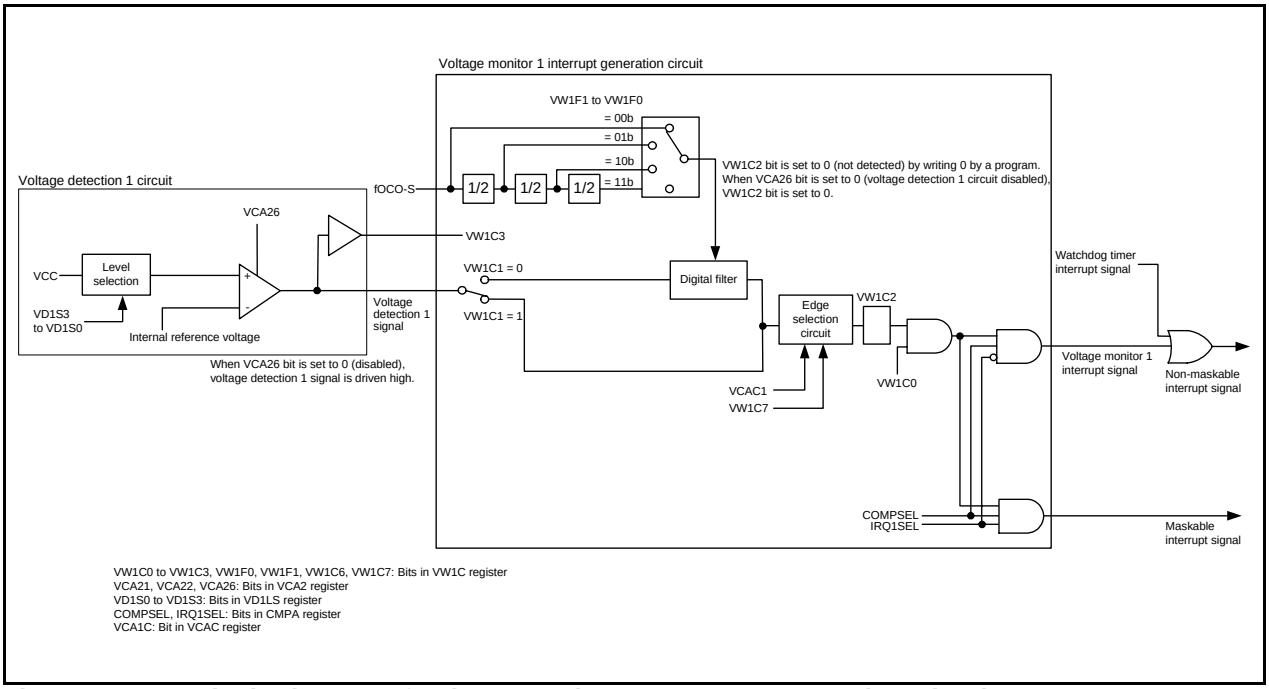


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

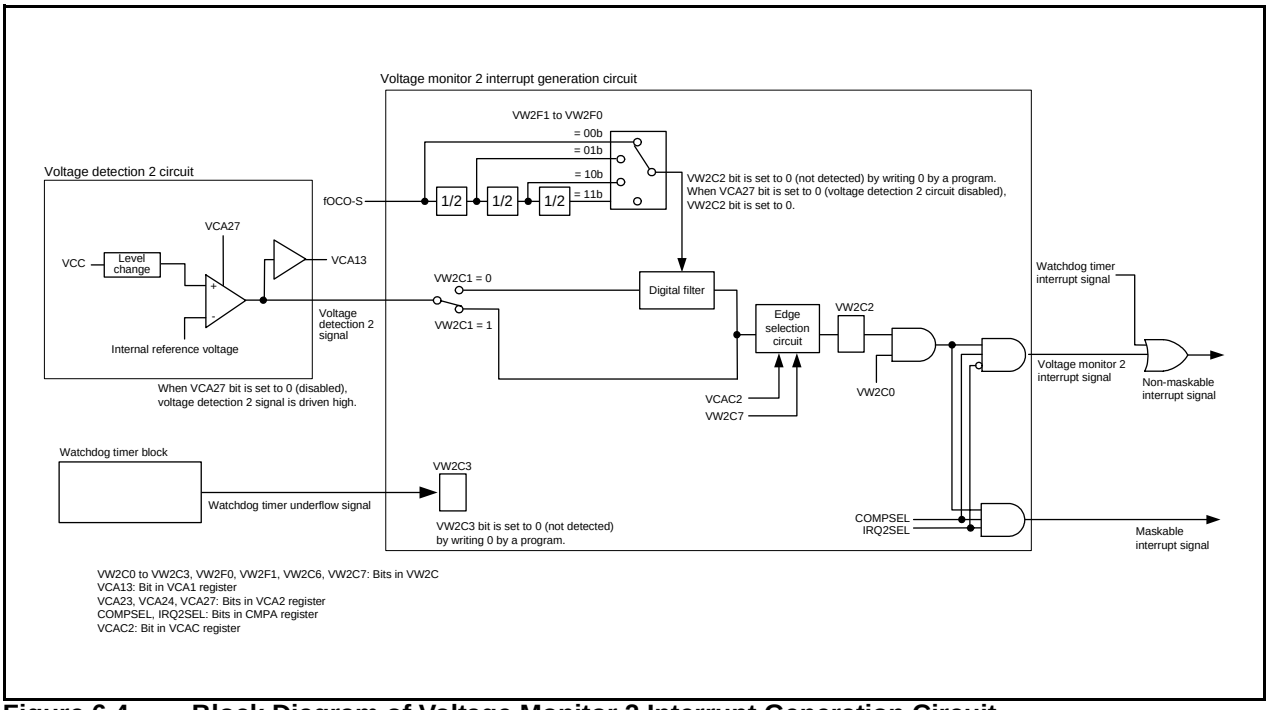


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit (1)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2 interrupt type select bit (2)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor interrupt type selection enable bit (1, 2)	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

Notes:
1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).
2. When the VW2C0 bit in the VW2C register is set to 1 (enabled), do not set bits IRQ2SEL and COMPSEL simultaneously (with one instruction).

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCAC1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCAC2 bit is set to 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

6.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Voltage detection 2 signal monitor flag (1)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.
   When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **10.6.8 Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (all clocks stop).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1 (voltage detection 1 circuit enabled).
   After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1 (voltage detection 2 circuit enabled).
   After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 0 0: 2.20 V (Vdet1_0) 0 0 0 1: 2.35 V (Vdet1_1) 0 0 1 0: 2.50 V (Vdet1_2) 0 0 1 1: 2.65 V (Vdet1_3) 0 1 0 0: 2.80 V (Vdet1_4) 0 1 0 1: 2.95 V (Vdet1_5) 0 1 1 0: 3.10 V (Vdet1_6) 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: 4.45 V (Vdet1_F)	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	0	1	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	1	1	0	0	X	0	1	1

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	Set to 1.	R/W
b7	—			

Note:
1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter disable mode select bit (2, 6)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (5)	0: When VCC reaches Vdet1 or above. 1: When VCC reaches Vdet1 or below.	R/W

Notes:

1. The VW1C0 bit is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled). To set the VW1C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
6. When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter disable mode select bit (2, 6)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet2 passing detected	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW2F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit (5)	0: When VCC reaches Vdet2 or above. 1: When VCC reaches Vdet2 or below.	R/W

Notes:

1. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled). To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. When using the digital filter (while the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.
6. When the VW2C0 bit is set to 1 (enabled), do not set the VW2C1 bit and bits VW2F1 and VW2F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **25. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.3.3 Monitoring Vdet2

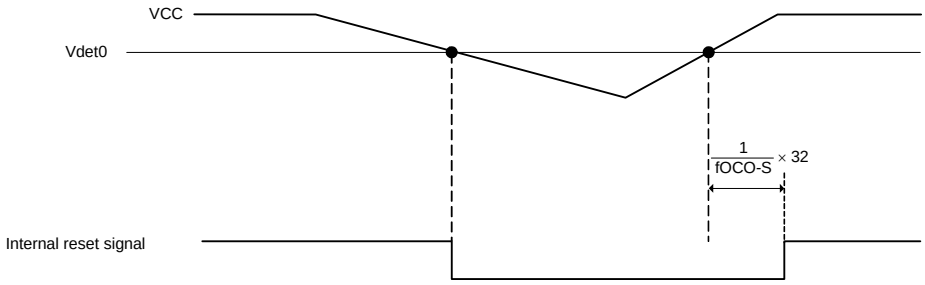
Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **25. Electrical Characteristics**).

- Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.



When the internal reset signal is driven low, the pins, CPU, and SFRs are initialized.
When the internal reset signal level changes from low to high, a program is executed beginning with the address indicated by the reset vector.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.

Figure 6.5 Operating Example of Voltage Monitor 0 Reset

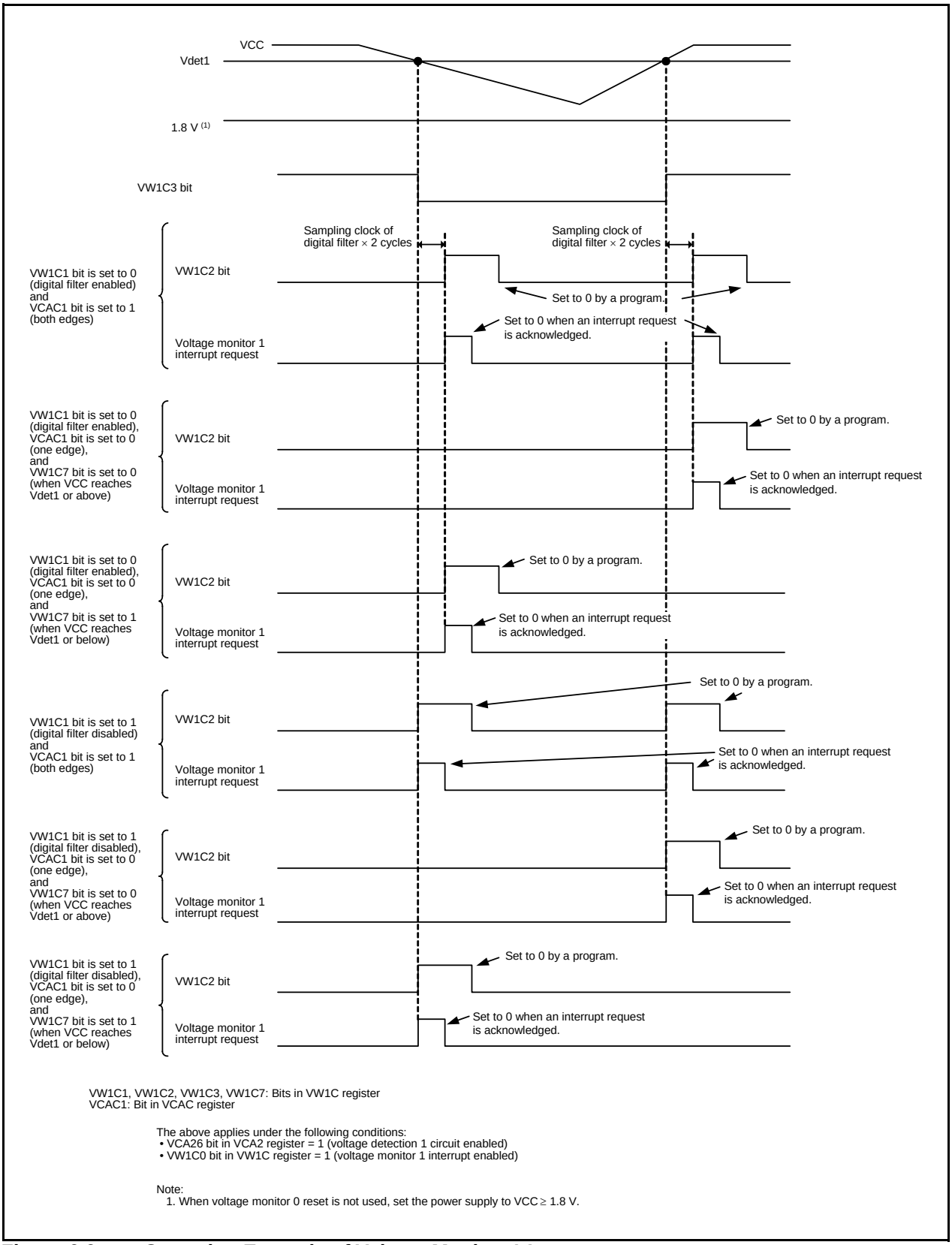
6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td (E-A).	
4	Set the COMPSEL bit in the CMPA register to 1.	
5 (1)	Select the interrupt type by the IRQ1SEL bit in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F1 to VW1F0 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	—
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	—
11	Wait for 2 cycles of the sampling clock of the digital filter	— (No wait time required)
12 (3)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the voltage detection 1 circuit is enabled while the voltage monitor 1 interrupt is disabled, low voltage is detected and the VW1C2 bit becomes 1.
   When low voltage is detected after the voltage detection 1 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 1 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW1C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies under the following conditions:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

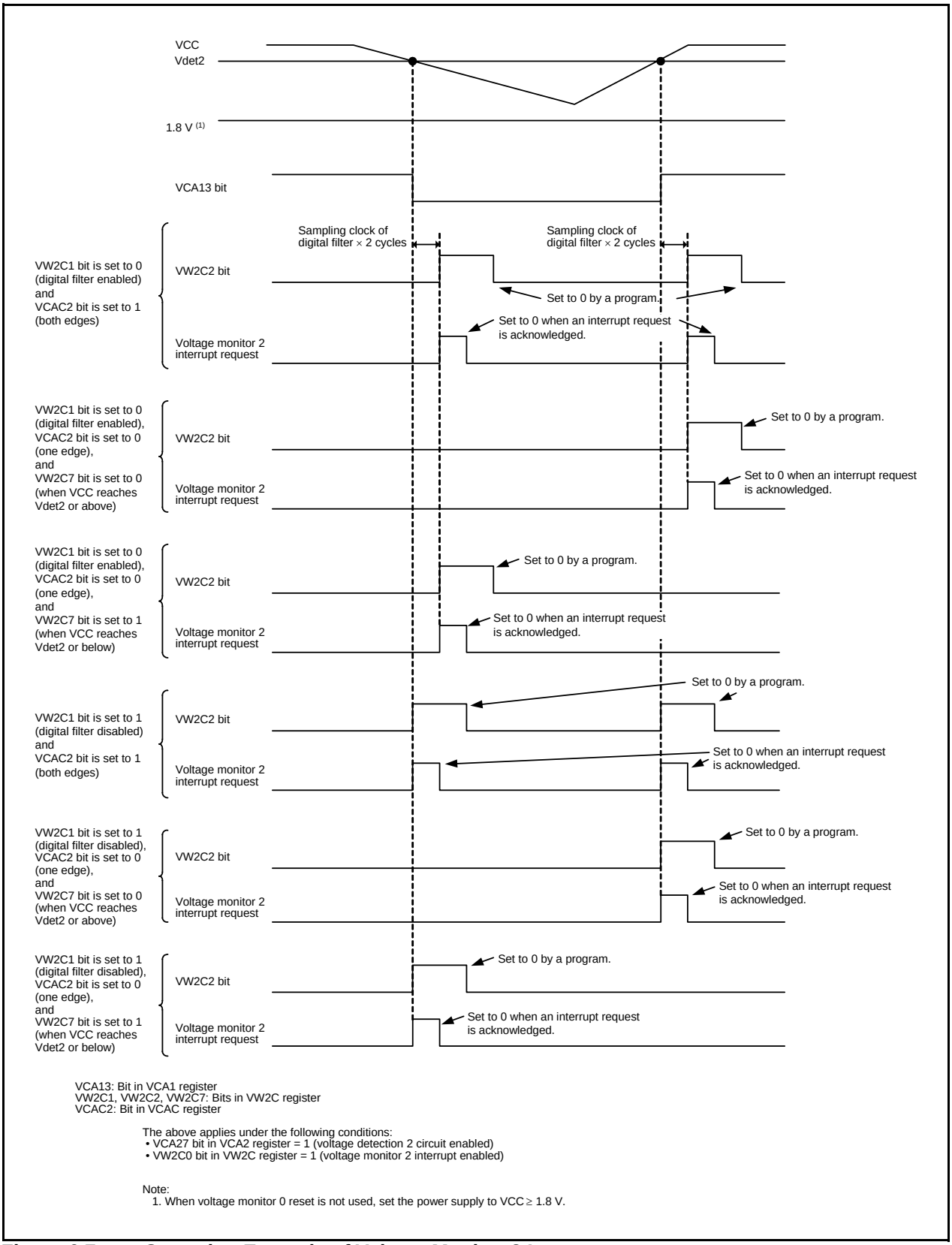
6.6 Voltage Monitor 2 Interrupt

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.
To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td(E-A).	
3	Set the COMPSEL bit in the CMPA register to 1.	
4 (1)	Select the interrupt type by the IRQ2SEL bit in the CMPA register.	
5	Select the sampling clock of the digital filter by bits VW2F0 to VW2F1 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
6 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	—
7	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
8	Set the VW2C2 bit in the VW2C register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	—
10	Wait for 2 cycles of the sampling clock of the digital filter.	— (No wait time required)
11 (3)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).
2. When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
3. When the voltage detection 2 circuit is enabled while the voltage monitor 2 interrupt is disabled, low voltage is detected and the VW2C2 bit becomes 1.
   When low voltage is detected after the voltage detection 2 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 2 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW2C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies under the following conditions:
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt enabled)

Note:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

7. I/O Ports

7.1 Introduction

I/O ports are shared with the I/O functions for the oscillation circuits and timers. When these functions are not used, pins can be used as I/O ports.
Table 7.1 lists the Overview of I/O Ports.

Table 7.1 Overview of I/O Ports

Port	I/O Format	I/O Setting	Internal Pull-Up Resister (1)	Drive Capacity Switch (2)	Input Level Switch (3)
P2	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 8-bit units.
P5_0 to P5_3	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 7-bit units.
P5_4, P5_6	I/O CMOS3 state	Set in 1-bit units.	None	None	
P5_5	CMOS input level	—	None	None	
P7_1	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 1-bit units.
P8	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	Set in 1-bit units.	Set in 8-bit units.
P9_0 to P9_1	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 2-bit units.

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers P2PUR, P5PUR, P7PUR, P8PUR, and P9PUR.
2. Whether the drive capacity of the output transistor is set to low or high can be selected by P8DRR register.
3. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 and VLT1.

7.2 I/O Port Functions

The PDi_j (j = 0 to 7) bit in the PDi (i = 2, 5, 7 to 9) register controls the input/output of ports P2, P5, P7 to P9. The Pi register consists of a port latch to retain output data and a circuit to read the pin status.
Figures 7.1 to 7.4 show the I/O Port Configurations, and Table 7.2 lists the I/O Port Functions.

Table 7.2 I/O Port Functions

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register (1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

Note:
1. i = 2, 5, 7 to 9; j = 0 to 7

7.3 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Table 1.3 Pin Name Information by Pin Number**).
Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 2, 5, 7 to 9; j = 0 to 7). Refer to the description of each function for information on how to set peripheral functions.

Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 2, 5, 7 to 9; j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

7.4 Pins Other than I/O Ports

Figure 7.5 shows the Pin Configuration.

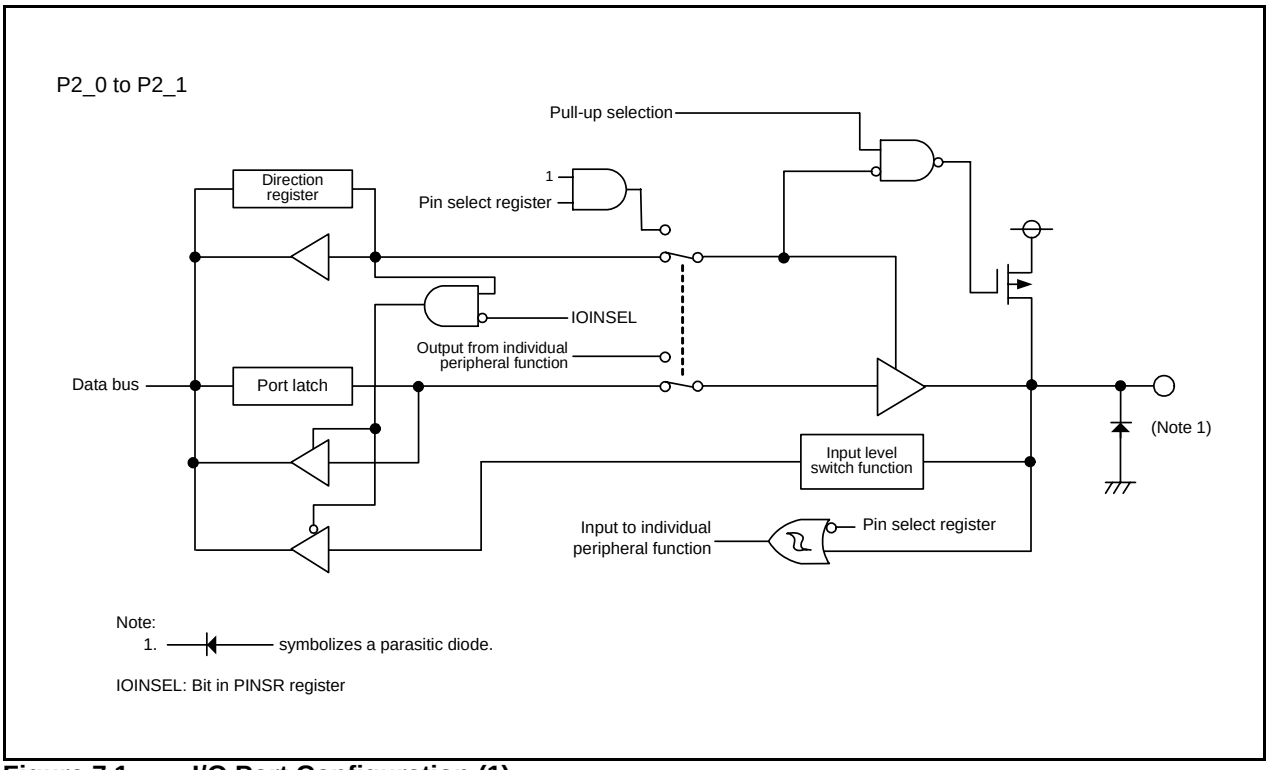


Figure 7.1 I/O Port Configuration (1)

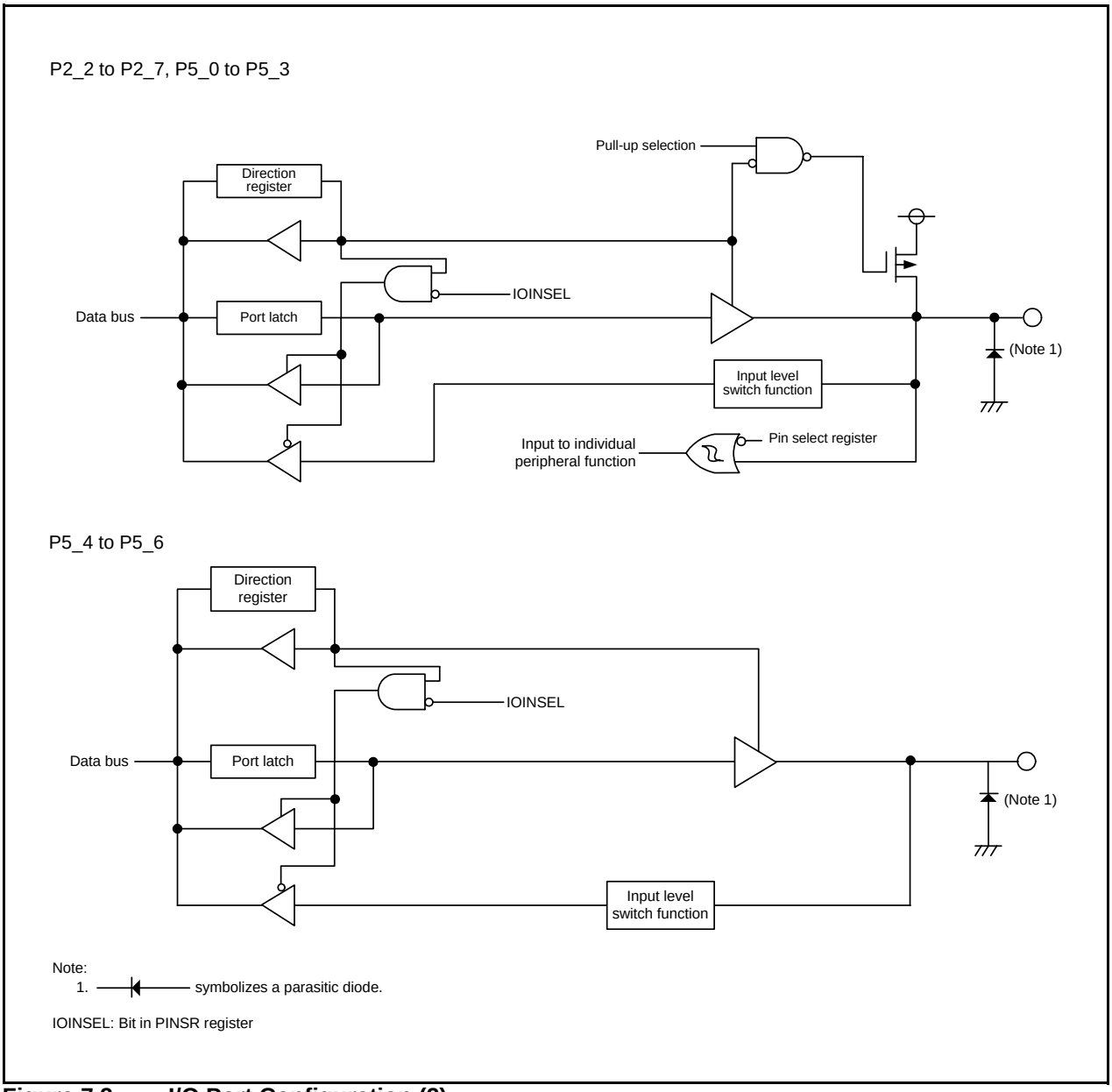


Figure 7.2 I/O Port Configuration (2)

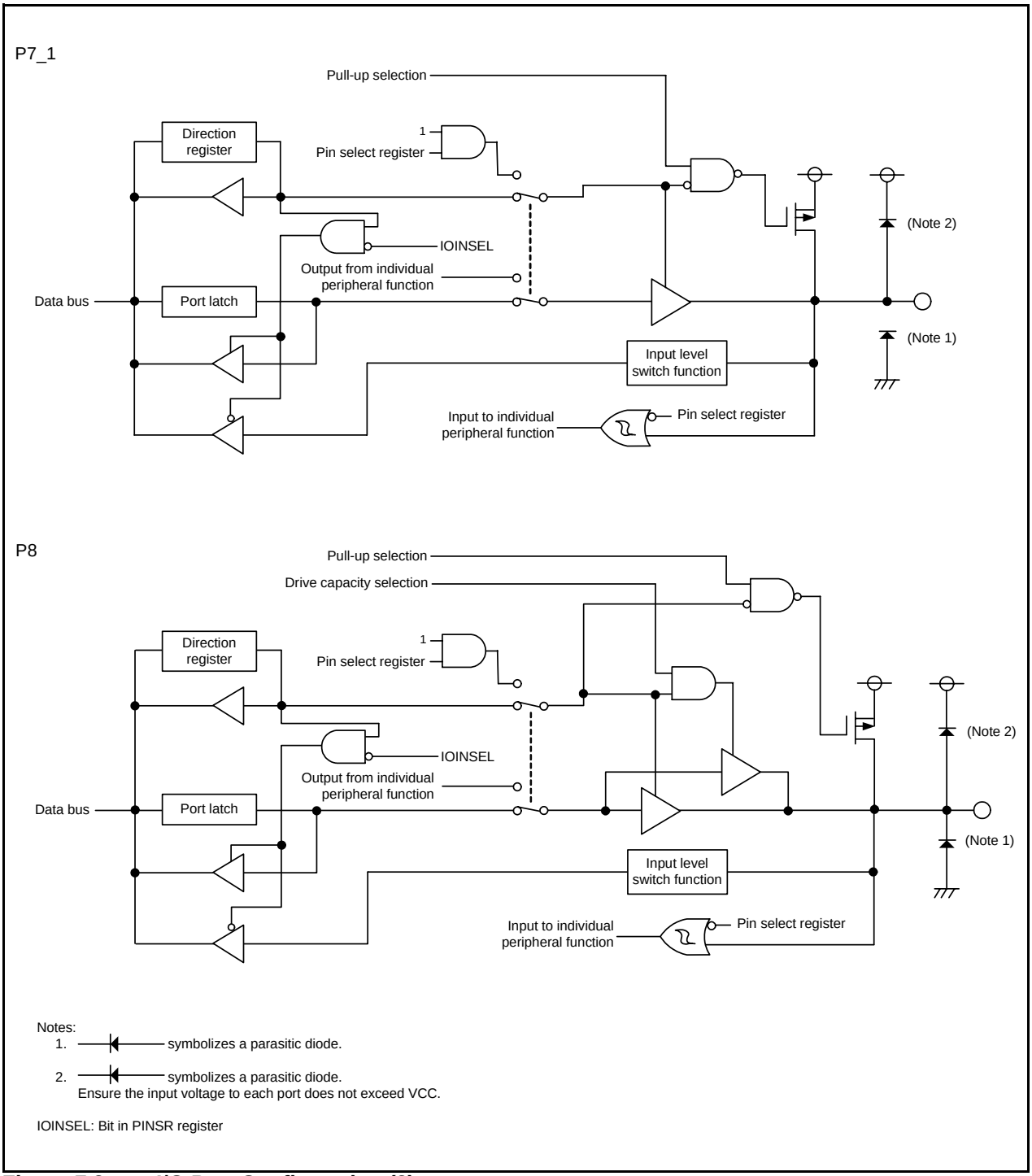


Figure 7.3 I/O Port Configuration (3)

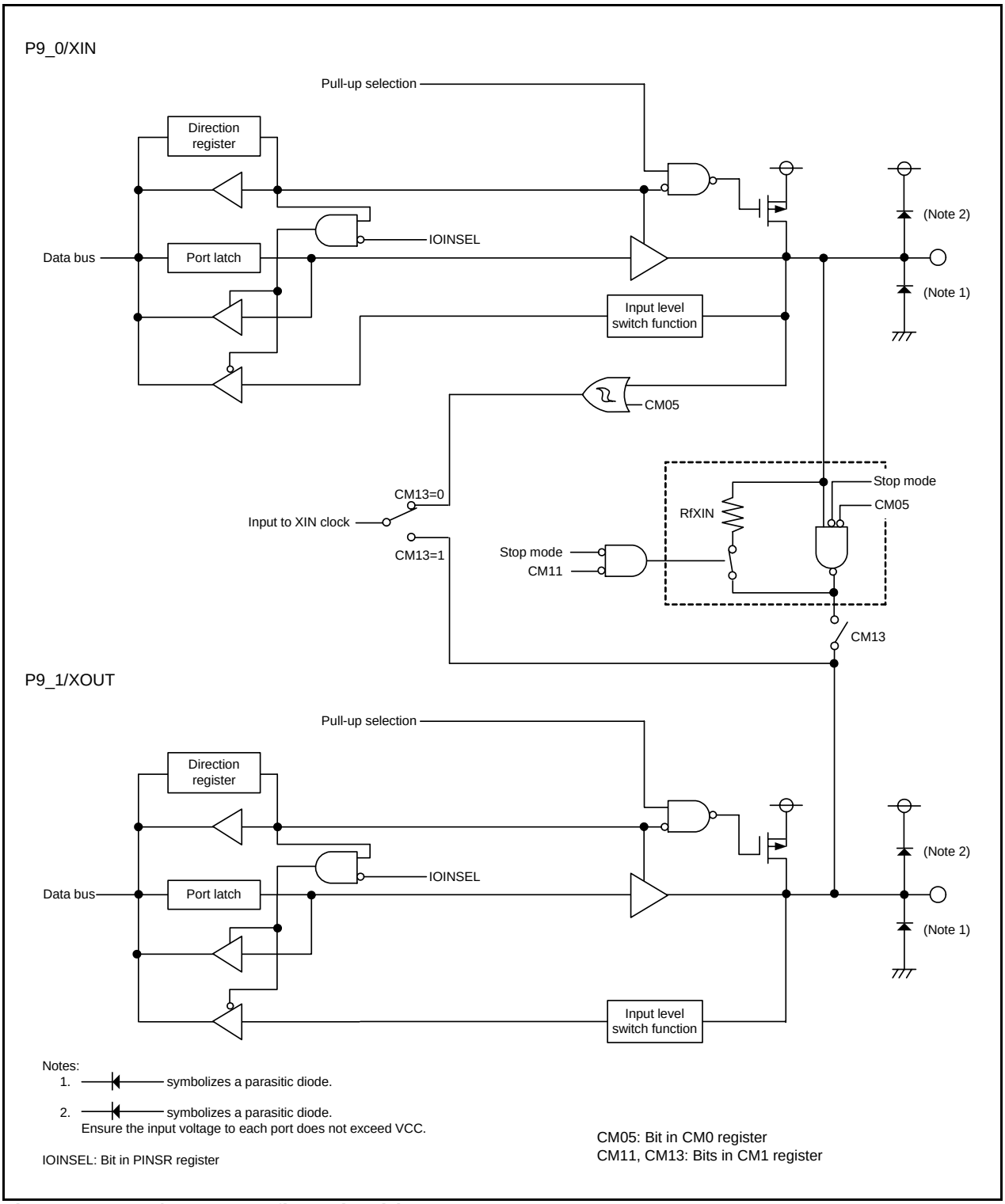


Figure 7.4 I/O Port Configuration (4)

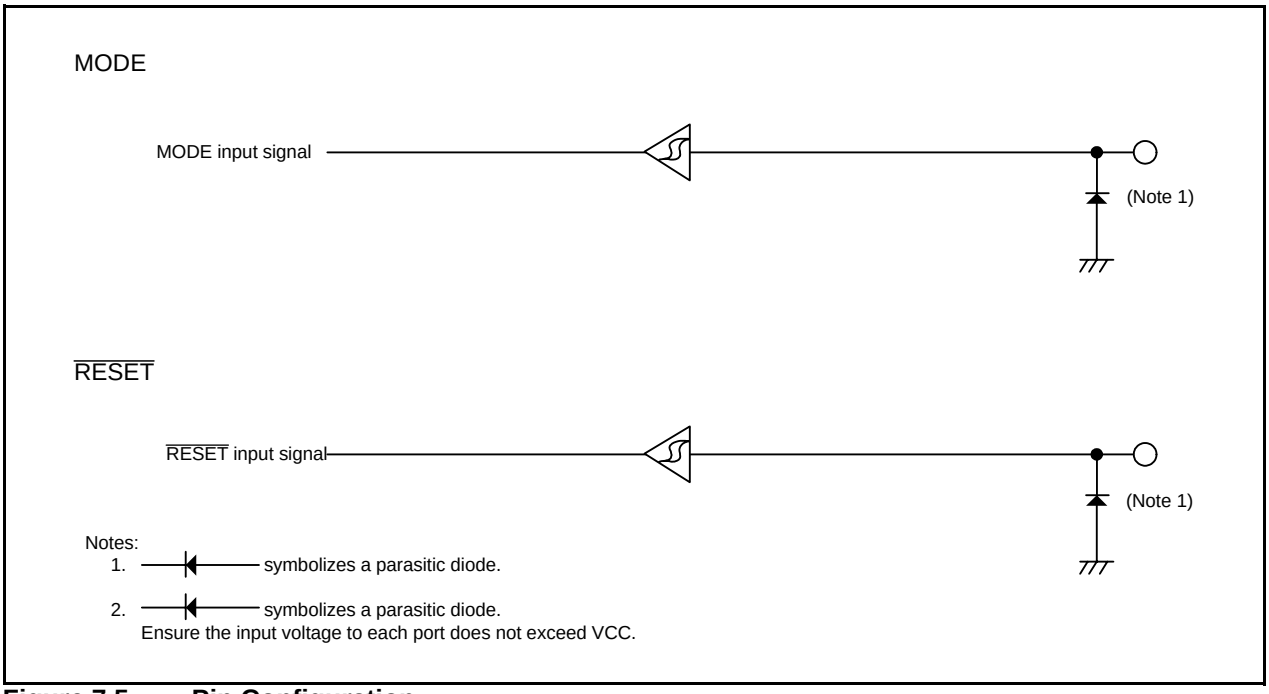


Figure 7.5 Pin Configuration

7.5 Registers

7.5.1 Port Pi Direction Register (PDi) (i = 2, 5, 7 to 9)

Address 00E6h (PD2), 00EBh (PD5 (1, 2)), 00EFh (PD7(3)), 00F2h (PD8), 00F3h (PD9(4))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (function as an input port) 1: Output mode (function as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. PD5_7 bit in the PD5 register is reserved bit. When writing to the PD5_7 bit, set to 0. When read, the content is 0.
2. Port P5_5 is the input port. When writing to the PD5_5 bit, set to 0. When read, the content is 0.
3. Bits PD7_0, PD7_2 to PD7_7 in the PD7 register are reserved bits. When writing to bits PD7_0, PD7_2 to PD7_7, set to 0. When read, the content is 0.
4. Bits PD9_2 and PD9_3 in the PD9 register are reserved bits. When writing to bits PD9_2 and PD9_3, set to 0. When read, the content is 0.
   Bits PD9_4 to PD9_7 in the PD9 register are unavailable on this MCU. When writing to bits PD9_4 to PD9_7, set to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.
To use the peripheral function as output, set the direction register to 1 (output mode).

7.5.2 Port Pi Register (Pi) (i = 2, 5, 7 to 9)

Address 00E4h (P2), 00E9h (P5 (1)), 00EDh (P7(2)), 00F0h (P8), 00F1h (P9(3))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: Low level 1: High level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Notes:
1. P5_7 bit in the P5 register is reserved bit. When writing to the P5_7 bit, set to 0. When read, the content is 0.
2. Bits P7_0, PD7_2 to P7_7 in the P7 register are reserved bits. When writing to bits P7_0, P7_2 to P7_7, set to 0. When read, the content is 0.
3. Bits P9_2 and P9_3 in the PD9 register are reserved bits. When writing to bits P9_2 and P9_3, set to 0. When read, the content is 0.
   Bits P9_4 to P9_7 in the PD9 register are unavailable on this MCU. When writing to bits P9_4 to P9_7, set to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 2, 5, 7 to 9, j = 0 to 7) (Port Pi_j Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.5.3 Timer RJ Pin Select Register (TRJSR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	TRJ0IOSEL1	TRJ0IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ0IOSEL0	TRJ0IO pin select bit	b1 b0 0 0: TRJ0IO pin not used 0 1: P8_3 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TRJ0IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

To use the I/O pins for timer RJ0, set the TRJSR register.
Set this register before setting the timer RJ0 associated registers. Also, do not change the setting value of this register during timer RJ0 operation.

7.5.4 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	TRCIOASEL1	TRCIOASEL0	—	TRCCLKSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCCLKSEL0	TRCCLK pin select bit	0: TRCCLK pin not used 1: P7_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b3 b2 0 0: TRCIOA/TRCTRG pin not used 0 1: TRCIOA/TRCTRG pin assigned to P8_7 1 0: Do not set. 1 1: Do not set.	R/W
b3	TRCIOASEL1			R/W
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P8_6 assigned 1 0: P8_5 assigned (1) 1 1: P8_4 assigned (2)	R/W
b5	TRCIOBSEL1			R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. When the TRCIOCSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOC pin assigned to P8_5), P8_5 functions as the TRCIOC pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.
2. When the TRCIODSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOD pin assigned to P8_4), P8_4 functions as the TRCIOD pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.

The TRCPSR0 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation. If the assignment of the timer RC pins is changed, an edge may occur depending on the changed pin level, causing the TRC register to be set to 0000h.

7.5.5 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TRCIODSEL0	—	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	0: TRCIOC pin not used 1: P8_5 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	TRCIODSEL0	TRCIOD pin select bit	0: TRCIOD pin not used 1: P8_4 assigned	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

The TRCPSR1 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

7.5.6 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I^{2}C bus switch bit	0: SSU function selected 1: I^{2}C bus function selected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

7.5.7 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 2, 5, 7 to 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register.	R/W
b4	IICTCTWI	I^2C double transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I^2C half transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Note:
1. Do not set both the IICTCTWI and IICTCHALF bits to 1 when the I2C bus function is used. Set these bits to 0 when the SSU function is used.

7.5.8 Port Pi Pull-Up Control Register (PiPUR) (i = 2, 5, 7 to 9)

Address 01E2h (P2PUR), 01E5h (P5PUR(2)), 01E7h (P7PUR(3)), 01E8h (P8PUR), 01E9h (P9PUR(4))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PUi7	PUi6	PUi5	PUi4	PUi3	PUi2	PUi1	PUi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PUi0	Port Pi_0 pull-up	0: Not pulled up	R/W
b1	PUi1	Port Pi_1 pull-up	1: Pulled up (1)	R/W
b2	PUi2	Port Pi_2 pull-up		R/W
b3	PUi3	Port Pi_3 pull-up		R/W
b4	PUi4	Port Pi_4 pull-up		R/W
b5	PUi5	Port Pi_5 pull-up		R/W
b6	PUi6	Port Pi_6 pull-up		R/W
b7	PUi7	Port Pi_7 pull-up		R/W

Notes:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.
2. Bits PU54 to PU57 in the P5PUR register are reserved bits. When writing to bits PU54 to PU57, set to 0. When read, the content is 0.
3. Bits PU70, PU72 to PU77 in the P7PUR register are reserved bits. When writing to bits PU70, PU72 to PU77, set to 0. When read, the content is 0.
4. Bits PU92 and PU93 in the P9PUR are reserved bits. When writing to bits PU92 and PU93, set to 0. When read, the content is 0.
   Bits PU94 to PU97 in the P9PUR register are unavailable on this MCU. When writing to bits PU94 to PU97, set to 0. When read, the content is 0.

For pins used as input, the setting values in the PiPUR register are valid.

7.5.9 Port P8 Drive Capacity Control Register (P8DRR)

Address 01F1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P8DRR7	P8DRR6	P8DRR5	P8DRR4	P8DRR3	P8DRR2	P8DRR1	P8DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P8DRR0	P8_0 drive capacity	0: Low	R/W
b1	P8DRR1	P8_1 drive capacity	1: High (1)	R/W
b2	P8DRR2	P8_2 drive capacity		R/W
b3	P8DRR3	P8_3 drive capacity		R/W
b4	P8DRR4	P8_4 drive capacity		R/W
b5	P8DRR5	P8_5 drive capacity		R/W
b6	P8DRR6	P8_6 drive capacity		R/W
b7	P8DRR7	P8_7 drive capacity		R/W

Note:
1. Both high-level output and low-level output are set to high drive capacity.

The P8DRR register selects whether the drive capacity of the P8 output transistor is set to low or high. The P8DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
For pins used as output, the setting values in the P8DRR register are valid.

7.5.10 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	VLT05	VLT04	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	VLT04	P2 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT05			R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

The VLT0 register selects the voltage level of the input threshold values for port P2. The corresponding bits are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5.11 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT17	VLT16	—	—	VLT13	VLT12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	VLT12	P5 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT13			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	VLT16	P7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT17			R/W

The VLT1 register selects the voltage level of the input threshold values for ports P5 and P7. The corresponding bits are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5.12 Input Threshold Control Register 2 (VLT2)

Address 01F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VLT23	VLT22	VLT21	VLT20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT20	P8 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT21			R/W
b2	VLT22	P9 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT23			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

The VLT2 register selects the voltage level of the input threshold values for ports P8 and P9. Bits VLT20 to VLT23 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.6 Port Settings

Tables 7.4 to 7.29 list the port settings.

Table 7.4 P2_0/TRB1O

Register		PD2	TRB1IOC	TRB1MR		Function
Bit		PD2_0	TOCNT	TMOD		
				1	0	
Pin	P2_0	0	X	0	0	Input port (1)
		1	X	0	0	Output port
		X	1			
	TRB1O	X	0	0	1	Programmable waveform generation mode (pulse output)
		X	0	1	0	Programmable one-shot waveform generation mode
		X	0	1	1	Programmable wait one-shot waveform generation mode

X: 0 or 1
Note:
1. Pulled up by setting the PU20 bit in the P2PUR register to 1.

Table 7.5 P2_1/TRB0O

Register		PD2	TRB0IOC	TRB0MR		Function
Bit		PD2_1	TOCNT	TMOD		
				1	0	
Pin	P2_1	0	X	0	0	Input port (1)
		1	X	0	0	Output port
		X	1			
	TRB0O	X	0	0	1	Programmable waveform generation mode (pulse output)
		X	0	1	0	Programmable one-shot waveform generation mode
		X	0	1	1	Programmable wait one-shot waveform generation mode

X: 0 or 1
Note:
1. Pulled up by setting the PU21 bit in the P2PUR register to 1.

Table 7.6 P2_2/$\overline{\text{INT0}}$

Register		PD2	INTEN	Function
Bit		PD2_2	INT0EN	
Pin	P2_2	0	X	Input port (1)
		1	X	Output port
	$\overline{\text{INT0}}$	0	1	$\overline{\text{INT0}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU22 bit in the P2PUR register to 1.

Table 7.7 P2_3/$\overline{\text{INT5}}$

Register		PD2	INTEN1	Function
Bit		PD2_3	INT5EN	
Pin	P2_3	0	X	Input port (1)
		1	X	Output port
	$\overline{\text{INT5}}$	0	1	$\overline{\text{INT5}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU23 bit in the P2PUR register to 1.

Table 7.8 P2_4/$\overline{KI0}$

Register		PD2	KIEN	Function
Bit		PD2_4	KI0EN	
Pin	P2_4	0	X	Input port (1)
		1	X	Output port
	$\overline{KI0}$	0	1	$\overline{KI0}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU24 bit in the P2PUR register to 1.

Table 7.9 P2_5/$\overline{KI1}$

Register		PD2	KIEN	Function
Bit		PD2_5	KI1EN	
Pin	P2_5	0	X	Input port (1)
		1	X	Output port
	$\overline{KI1}$	0	1	$\overline{KI1}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU25 bit in the P2PUR register to 1.

Table 7.10 P2_6/$\overline{KI2}$

Register		PD2	KIEN	Function
Bit		PD2_6	KI2EN	
Pin	P2_6	0	X	Input port (1)
		1	X	Output port
	$\overline{KI2}$	0	1	$\overline{KI2}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU26 bit in the P2PUR register to 1.

Table 7.11 P2_7/$\overline{KI3}$

Register		PD2	KIEN	Function
Bit		PD2_7	KI3EN	
Pin	P2_7	0	X	Input port (1)
		1	X	Output port
	$\overline{KI3}$	0	1	$\overline{KI3}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU27 bit in the P2PUR register to 1.

Table 7.12 P5_0/$\overline{KI4}$

Register		PD5	KIEN1	Function
Bit		PD5_0	KI4EN	
Pin	P5_0	0	X	Input port (1)
		1	X	Output port
	$\overline{KI4}$	0	1	$\overline{KI4}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU50 bit in the P5PUR register to 1.

Table 7.13 P5_1/$\overline{KI5}$

Register		PD5	KIEN1	Function
Bit		PD5_1	KI5EN	
Pin	P5_1	0	X	Input port (1)
		1	X	Output port
	$\overline{KI5}$	0	1	$\overline{KI5}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU51 bit in the P5PUR register to 1.

Table 7.14 P5_2/$\overline{KI6}$

Register		PD5	KIEN1	Function
Bit		PD5_2	KI6EN	
Pin	P5_2	0	X	Input port (1)
		1	X	Output port
	$\overline{KI6}$	0	1	$\overline{KI6}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU52 bit in the P5PUR register to 1.

Table 7.15 P5_3/$\overline{KI7}$

Register		PD5	KIEN1	Function
Bit		PD5_3	KI7EN	
Pin	P5_3	0	X	Input port (1)
		1	X	Output port
	$\overline{KI7}$	0	1	$\overline{KI7}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU53 bit in the P5PUR register to 1.

Table 7.16 P5_4

Register		PD5	Function
Bit		PD5_4	
Pin	P5_4	0	Input port
		1	Output port

Table 7.17 P5_5

Register		PD5	Function
Bit		PD5_5	
Pin	P5_5	0	Input port
		1	Do not set.

Table 7.18 P5_6

Register		PD5	Function
Bit		PD5_6	
Pin	P5_6	0	Input port
		1	Output port

Table 7.19 P7_1/TRCCLK/$\overline{INT2}$

Register		PD7	TRCPSR0	TRCCR1			INTEN	Function
Bit		PD7_1	TRCCLKSEL0	TCK			INT2EN1	
				2	1	0		
Pin	P7_1	0	0	X	X	X	X	Input port (1)
		1	0	X	X	X	X	Output port
	TRCCLK	0	1	1	0	1	X	TRCCLK input (1)
	$\overline{INT2}$	0	0	X	X	X	1	$\overline{INT2}$ input (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU71 bit in the P7PUR register to 1.

Table 7.20 P8_0/$\overline{SCS}$/$\overline{INT1}$

Register		PD8	INTEN	SSMR2		Function
Bit		PD8_0	INT1EN	CSS		
				1	0	
Pin	P8_0	0	X	0	0	Input port (1)
		1	X	0	0	Output port (2)
	$\overline{SCS}$	0	X	0	1	$\overline{SCS}$ input (1)
		0	X	1	X	$\overline{SCS}$ output (1, 2, 3)
	$\overline{INT1}$	0	1	0	0	$\overline{INT1}$ input (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU80 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR0 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1.

Table 7.21 P8_1/SSI/$\overline{INT3}$

Register Bit		PD8	INTEN	SSUIICSR	SSU Associated Register	Function
		PD8_1	INT3EN	IICSEL		
Pin	P8_1	0	X	X	Synchronous serial communication unit (refer to **Table 22.4 Association between Communication Modes and I/O Pins**).	Input port (1)
		1	X	X		Output port (2)
	SSI	0	X	0		SSI input (1)
		X	X	0		SSI output (1, 2, 3)
	$\overline{INT3}$	0	1	X		$\overline{INT3}$ input (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU81 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR1 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).

Table 7.22 P8_2/SSCK/SCL

Register		PD8	SSUIICSR	ICCR1	SSMR2	SSU Associated Register	Function
Bit		PD8_2	IICSEL	ICE	SCKS		
Pin	P8_2	0	0	X	0	Synchronous serial communication unit (refer to **Table 22.4 Association between Communication Modes and I/O Pins**).	Input port (1)
			1	0			
		1	0	X	0		Output port (2)
			1	0			
	SCL	0	1	1	0		SCL input/output (1, 2)
	SSCK	0	0	X	1		SSCK input (1)
		0	0	X	1		SSCK output (1, 2, 3)

X: 0 or 1

Notes:

1. Pulled up by setting the PU82 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR2 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1. At this time, set the PD8_2 bit in the PD8 register to 0.

Table 7.23 P8_3/TRJ0IO/SSO/SDA

Register		PD8	TRJSR		TRJ0IOC	TRJ0MR			SSUIICSR	ICCR1	SSU Associated Register	Function
Bit		PD8_3	TRJ0IOSEL		TOPCR	TMOD			IICSEL	ICE		
			1	0		2	1	0				
Pin	P8_3	0	Other than 01b		1	X	X	X	1	0	Synchronous serial communication unit (refer to **Table 22.4 Association between Communication Modes and I/O Pins**).	Input port (1)
									0	X		
		1	Other than 01b		1	X	X	X	1	0		Output port (2)
									0	X		
	SDA	0	Other than 01b		1	X	X	X	1	1		SDA input/output (1, 2)
	SSO	0	Other than 01b		1	X	X	X	0	X		SSO input (1)
		0	Other than 01b						0	X		SSO output (1, 2, 3)
	TRJ0IO	X	0	1	0	0	0	1	0	X		Pulse output mode (1, 2)
									1	0		
		X	0	1	0	0	1	0	0	X		Event counter mode
									1	0		
		X	0	1	0	0	1	1	0	X		Pulse width measurement mode
									1	0		
		X	0	1	0	1	0	0	0	X		Pulse period measurement mode
									1	0		

X: 0 or 1

Notes:

1. Pulled up by setting the PU83 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR3 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).

Table 7.24 P8_4/TRCIOD(/TRCIOB)

Register		PD8	TRCPSR0		TRCPSR1	TRCOER		TRCMR			TRCIOR0			TRCIOR1			Function
Bit		PD8_4	TRCIOBSEL		TRCIOD SEL0	EB	ED	PWM			IOB			IOD			
			1	0				2	B	D	2	1	0	2	1	0	
Pin	P8_4	0	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	Input port (1)
		1	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	Output port (2)
		X															
	(TRCIOB)	X	1	1	0	0	X	0	X	X	X	X	X	X	X	X	PWM2 mode waveform output (2)
		X	1	1	0	0	X	1	1	X	X	X	X	X	X	X	PWM mode waveform output (2)
		X	1	1	0	0	X	1	0	X	0	0	1	X	X	X	Timer waveform output (output compare function) (2)
											0	1	X				
		0	1	1	0	X	X	1	0	X	1	0	X	X	X	X	Timer mode (input capture function) (1)
												1	0				
	TRCIOD	X	Other than 11b		1	X	0	1	X	1	X	X	X	X	X	X	PWM mode waveform output (2)
		X	Other than 11b		1	X	0	1	X	0	X	X	X	0	0	1	Timer waveform output (output compare function) (2)
														0	1	X	
		0	Other than 11b		1	X	X	1	X	0	X	X	X	1	X	X	Timer mode (input capture function) (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU84 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR4 bit in the P8DRR register to 1.

Table 7.25 P8_5/TRCIOC(/TRCIOB)

Register		PD8	TRCPSR0		TRCPSR1	TRCOER		TRCMR			TRCIOR0			TRCIOR1			Function
Bit		PD8_5	TRCIOBSEL		TRCIOC SEL0	EB	EC	PWM			IOB			IOC			
			1	0				2	B	C	2	1	0	2	1	0	
Pin	P8_5	0	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	Input port (1)
		1	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	Output port (2)
		X															
	(TRCIOB)	X	1	0	X	0	X	0	X	X	X	X	X	X	X	X	PWM2 mode waveform output (2)
		X	1	0	X	0	X	1	1	X	X	X	X	X	X	X	PWM mode waveform output (2)
		X	1	0	X	0	X	1	0	X	0	0	1	X	X	X	Timer waveform output (output compare function) (2)
											0	1	X				
		0	1	0	0	X	X	1	0	X	1	0	X	X	X	X	Timer mode (input capture function) (1)
												1	0				
	TRCIOC	X	Other than 10b		1	X	0	1	X	1	X	X	X	X	X	X	PWM mode waveform output (2)
		X	Other than 10b		1	X	0	1	X	0	X	X	X	0	0	1	Timer waveform output (output compare function) (2)
														0	1	X	
		0	Other than 10b		1	X	X	1	X	0	X	X	X	1	X	X	Timer mode (input capture function) (1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU85 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR5 bit in the P8DRR register to 1.

Table 7.26 P8_6(/TRCIOB)

Register		PD8	TRCPSR0		TRCOER	TRCMR			TRCIOR0			Function
Bit		PD8_6	TRCIOB SEL		EB	PWM			IOB			
			1	0		2	B	D	2	1	0	
Pin	P8_6	0	Other than 01b		X	X	X	X	X	X	X	Input port (1)
		1	Other than 01b		X	X	X	X	X	X	X	Output port (2)
	(TRCIOB)	X	0	1	0	0	X	X	X	X	X	PWM2 mode waveform output (2)
		X	0	1	0	1	1	X	X	X	X	PWM mode waveform output (2)
		X	0	1	0	1	0	X	0	0	1	Timer waveform output (output compare function) (2)
									0	1	X	
		0	0	1	X	1	0	X	1	0	X	Timer mode (input capture function) (1)
										1	0	

X: 0 or 1

Notes:
1. Pulled up by setting the PU86 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR6 bit in the P8DRR register to 1.

Table 7.27 P8_7/TRCIOA(/TRCTRG)

Register		PD8	TRCPSR0		TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit		PD8_7	TRCIOASEL		EA	PWM2	IOA			TCEG		
			1	0			2	1	0	1	0	
Pin	P8_7	0	0	0	X	X	X	X	X	X	X	Input port (1)
		1	0	0	X	X	X	X	X	X	X	Output port (2)
	TRCIOA	X	0	1	0	1	0	0	1	X	X	Timer waveform output (output compare function) (2)
								1	X			
		0	0	1	X	1	1	0	X	X	X	Timer mode (input capture function) (1)
								1	0			
	(TRCTRG)	0	0	1	X	0	X	X	X	0	1	PWM2 mode (TRCTRG input) (1)
										1	X	

X: 0 or 1

Notes:
1. Pulled up by setting the PU87 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR7 bit in the P8DRR register to 1.

Table 7.28 P9_0/XIN

Register		PD9	CM0	CM1			Function		
Bit		PD9_0	CM05	CM					
				10	11	13		Oscillation buffer	Feedback resistor
Pin	P9_0	0	1	0	1	0	Input port (1)	OFF	OFF
		1	1	0	1	0	Output port	OFF	OFF
	XIN	0	0	0	1	0	XIN clock input (1)	ON	ON
		0	0	1	1	0	XIN clock input stop (STOP mode) (1)	ON	ON
		0	0	0	0	1	XIN-XOUT oscillation (on-chip feedback resistor enabled)	ON	ON
		0	0	0	1	1	XIN-XOUT oscillation (on-chip feedback resistor disabled)	ON	OFF
		0	1	0	0	1	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)	OFF	ON
		0	1	0	1	1	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)	OFF	OFF
		0	0	1	X	1	XIN-XOUT oscillation stop (STOP mode)	OFF	OFF

X: 0 or 1

Note:
1. Pulled up by setting the PU90 bit in the P9PUR register to 1.

Table 7.29 P9_1/XOUT

Register		PD9	CM0	CM1			Function		
Bit		PD9_1	CM05	CM					
				10	11	13		Oscillation buffer	Feedback resistor
Pin	P9_1	0	X	0	1	0	Input port (1)	OFF	OFF
		1	X	0	1	0	Output port	OFF	OFF
	XOUT	0	0	0	0	1	XIN-XOUT oscillation (on-chip feedback resistor enabled)	ON	ON
		0	0	0	1	1	XIN-XOUT oscillation (on-chip feedback resistor disabled)	ON	OFF
		0	1	0	0	1	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)	OFF	ON
		0	1	0	1	1	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)	OFF	OFF
		0	0	1	X	1	XIN-XOUT oscillation stop (STOP mode)	OFF	OFF

X: 0 or 1

Note:
1. Pulled up by setting the PU91 bit in the P9PUR register to 1.

7.7 Unassigned Pin Handling

Table 7.30 lists Unassigned Pin Handling.

Table 7.30 Unassigned Pin Handling

Pin Name	Connection
Ports P2, P5_0 to P5_4, P5_6, P7_1, P8, P9_0, P9_1	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
P5_5	Connect to VCC.
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor. (3)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is used.

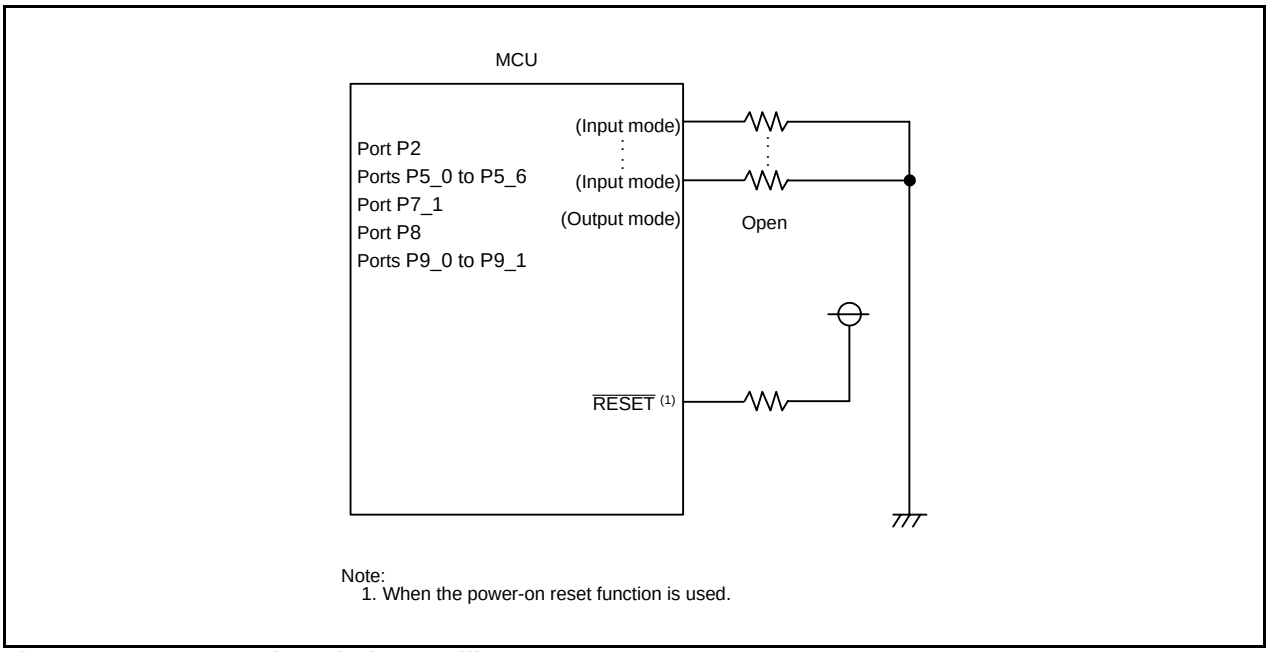


Figure 7.6 Unassigned Pin Handling

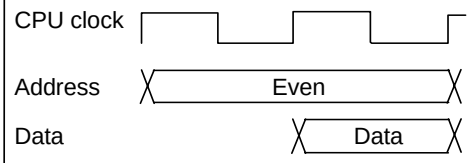
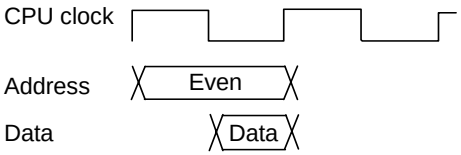
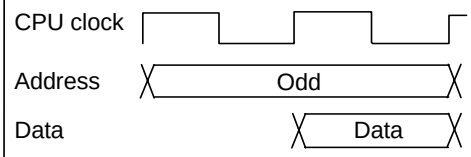
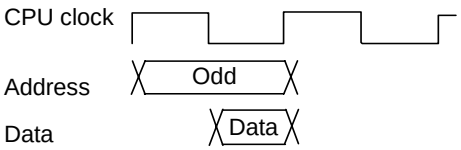
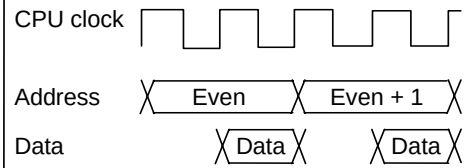
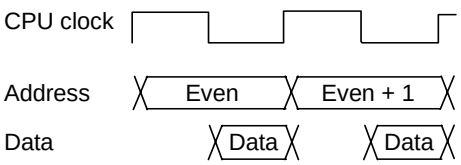
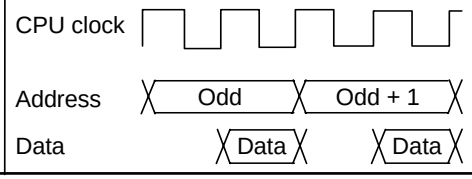
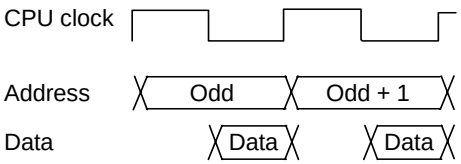
8. Bus

The bus cycles differ when accessing ROM/RAM and when accessing SFR.
Table 8.1 lists the Bus Cycles by Access Area.
ROM/RAM and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 shows Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area

Access Area	Bus Cycle
SFR/Data flash	2 cycles of CPU clock
Program ROM/RAM	1 cycle of CPU clock

Table 8.2 Access Units and Bus Operations

Area	SFR, Data flash	ROM (program ROM), RAM
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only the following SFRs are connected with the 16-bit bus:
Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
Timer RJ: TRJ0 Registers (i = 0 to 1)
SSU: Registers SSTDR, SSTDRH, SSRDR, and SSRDRH
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1

Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

9.1 Introduction

The following three circuits are incorporated in the clock generation circuit:
- XIN clock oscillation circuit
- Low-speed on-chip oscillator
- Low-speed on-chip oscillator for the watchdog timer

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows the Clock Generation Circuit and Figure 9.2 shows the Peripheral Function Clock.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	Low-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator for Watchdog Timer
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• Watchdog timer clock source
Clock frequency	0 to 20 MHz	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	—	—
Oscillator connect pins	XIN, XOUT (1)	— (1)	—
Oscillation stop, restart function	Usable	Usable	Usable
Oscillator status after reset	Stop	Oscillate	Stop (2) Oscillate (3)
Others	Externally generated clock can be input	—	—

Notes:
1. These pins can be used as P9_0 and P9_1 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit is not used.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
2. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
3. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).

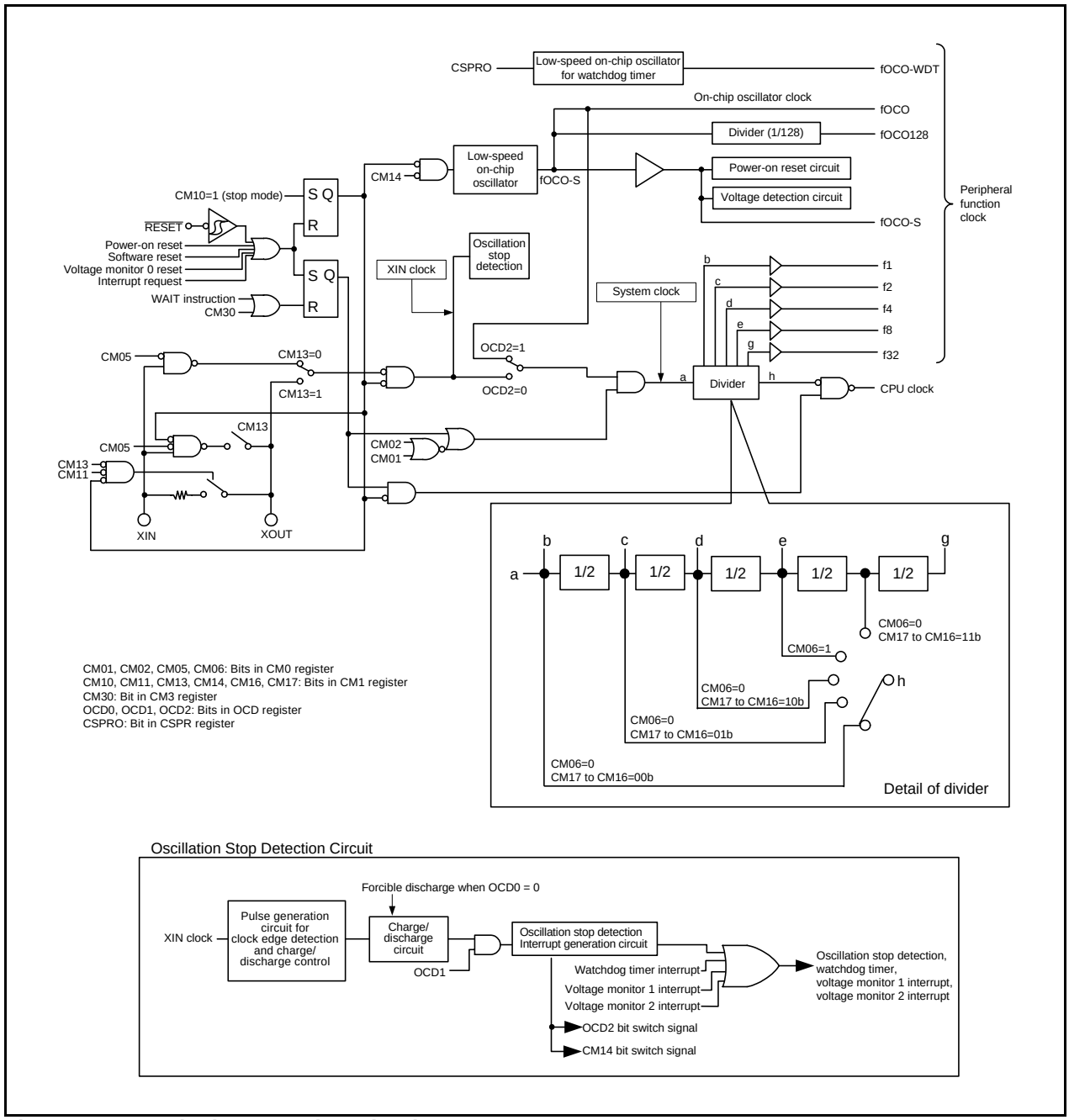


Figure 9.1 Clock Generation Circuit

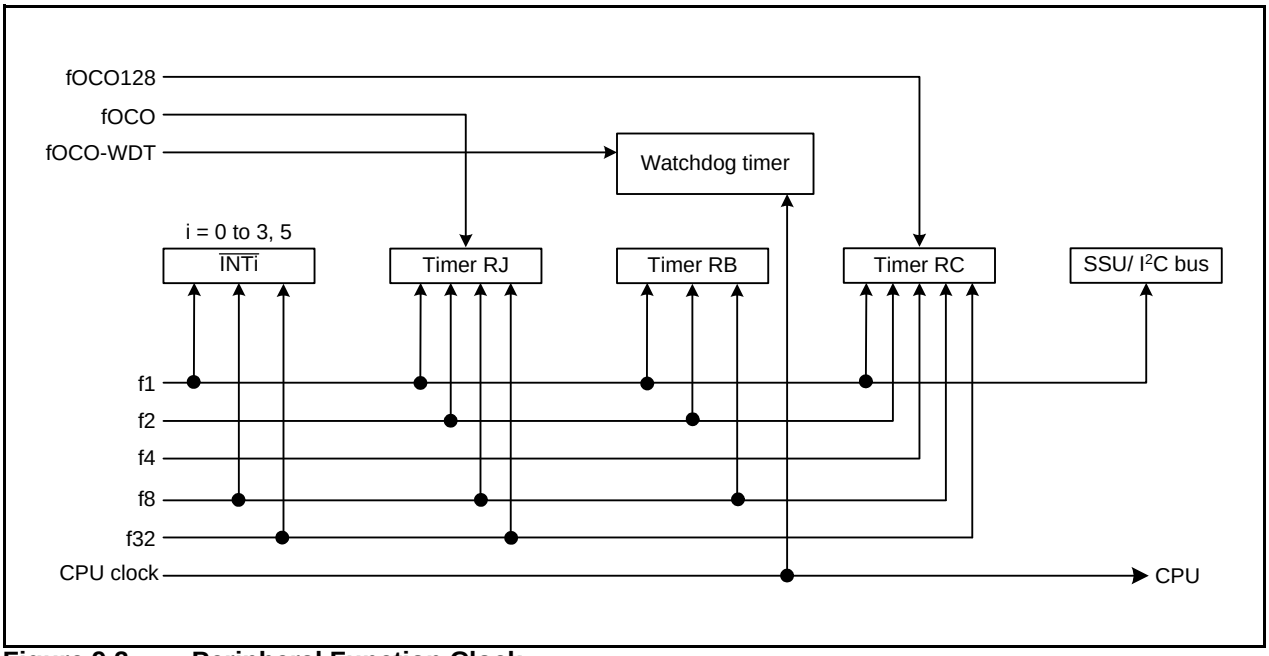


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CM06	CM05	—	CM03	CM02	CM01	—
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	CM01	Peripheral function clock stop bit in wait mode	b1 b0 0 0: Peripheral function clock does not stop in wait mode 0 1: Clocks f1 to f32 stop in wait mode 1 0: Clocks f1 to f32 stop in wait mode 1 1: Clocks f1 to f32 stop in wait mode	R/W
b2	CM02			R/W
b3	CM03	Reserved bit	Set to 1.	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 2)	0: XIN clock oscillates 1: XIN clock stops	R/W
b6	CM06	CPU clock division select bit 0 (3)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:

1. The CM05 bit can be used to stop the XIN clock when the system clock is other than the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. Only when the CM05 bit to 1 (XIN clock stops) and the CM13 bit is set to 0 (I/O ports), P9_0 and P9_1 can be used as I/O ports.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
3. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 7)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	Reserved bit	Set to 1.	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6)	0: I/O ports P9_0 and P9_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1 (all clocks stop), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P9_0 and P9_1 as input ports, set the CM13 bit to 0 (I/O ports) and the CM05 bit in the CM0 register to 1 (XIN clock stops).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 0 (XIN clock oscillates), and the CM11 bit to 1 (on-chip feedback resistor disabled). When the PD9_0 bit in the PD9 register is further set to 0 (input mode), an external clock can be input. Set XOUT as the I/O port P9_1 at this time. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
6. Once the CM13 bit is set to 1 (XIN-XOUT pin) by a program, it cannot be set to 0 (I/O ports P9_0 and P9_1).
7. Do not set the CM10 bit to 1 when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division (2)	R/W
b6	CM36	System clock select bit when exiting wait or stop mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait or stop mode 0 1: Do not set. 1 0: Do not set. 1 1: XIN clock selected (3)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • CM05 bit in CM0 register = 0 (XIN clock oscillates)
   • CM13 bit in CM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0. However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	On-chip oscillator clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode or low-speed on-chip oscillator mode (XIN clock stops).
2. When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) when the XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. When the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even if 0 (XIN clock selected) is written to it.
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled). In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.
5. The OCD3 bit remains 0 (XIN clock oscillates) when bits OCD1 to OCD0 are set to 00b.
6. Refer to **9.6.1 How to Use Oscillation Stop Detection Function** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a oscillator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XIN pin.

Figure 9.3 shows Examples of XIN Clock Connection Circuit.

During and after reset, the XIN clock stops.

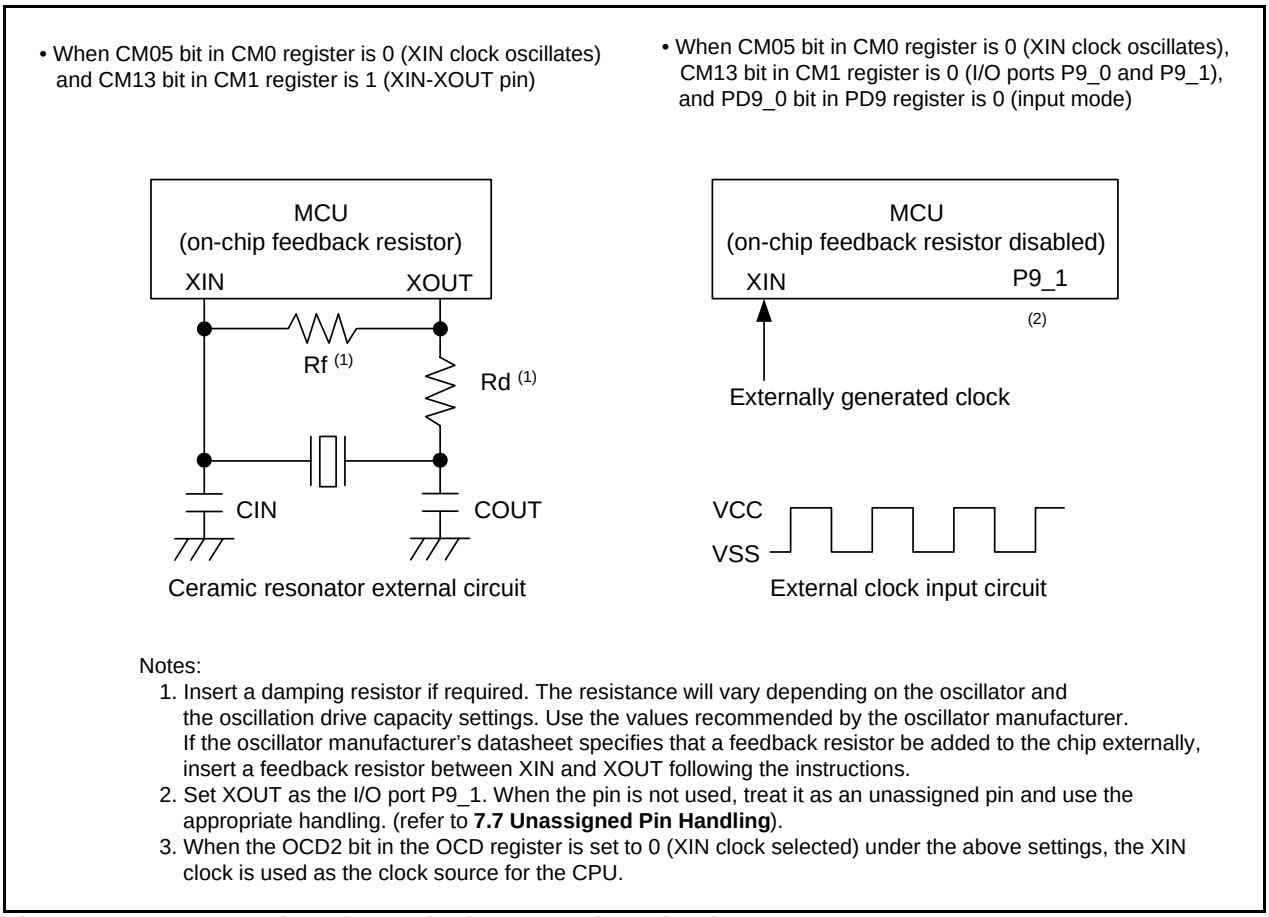
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates).

After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source by setting the OCD2 bit in the OCD register to 0 (XIN clock selected).

The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) by setting the OCD2 bit is to 1 (on-chip oscillator clock selected).

When switching the XIN clock to an externally generated clock, or an externally generated clock to the XIN clock, set the CM05 bit to 1 (XIN clock stops).

In stop mode, all clocks including the XIN clock stop. Refer to **10. Power Control** for details.



Notes:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the values recommended by the oscillator manufacturer. If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
2. Set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling. (refer to **7.7 Unassigned Pin Handling**).
3. When the OCD2 bit in the OCD register is set to 0 (XIN clock selected) under the above settings, the XIN clock is used as the clock source for the CPU.

Figure 9.3 Examples of XIN Clock Connection Circuit

9.4 Low-Speed On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the low-speed on-chip oscillator.
The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, and peripheral function clock (fOCO, fOCO-S, and fOCO128).
After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.5 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. (Refer to **Figure 9.1 Clock Generation Circuit**.)

9.5.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock or on-chip oscillator clock can be selected.

9.5.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. The division ratio can be selected by the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.5.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, and 32) clock is generated by the system clock divided by i. It is used for timers RJ, RB, and RC.
When the MCU enters wait mode after bits CM02 to CM01 in the CM0 register are set to 01, 10, or 11, the fi clock stops.

9.5.4 fOCO

fOCO is an operating clock for the peripheral functions.
This clock runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RJ.
In wait mode, the fOCO clock does not stop.

9.5.5 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.5.6 fOCO128

fOCO128 clock is generated by fOCO-S divided by 128.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC.

9.5.7 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protection mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.6 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.2 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following states if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
- Oscillation stop detection interrupt request is generated

Table 9.2 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Condition for enabling the oscillation stop detection function	Bits OCD1 to OCD0 are set to 11b.
Operation at oscillation stop detection	Oscillation stop detection interrupt generation

9.6.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 9.3 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.5 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.4 shows the Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected.
- To enter wait mode while the oscillation stop detection function is used, set bits CM02 to CM1 to 00 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set bits OCD1 to OCD0 to 11b.

Table 9.3 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection (when (a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) Bits OCD1 to OCD0 in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

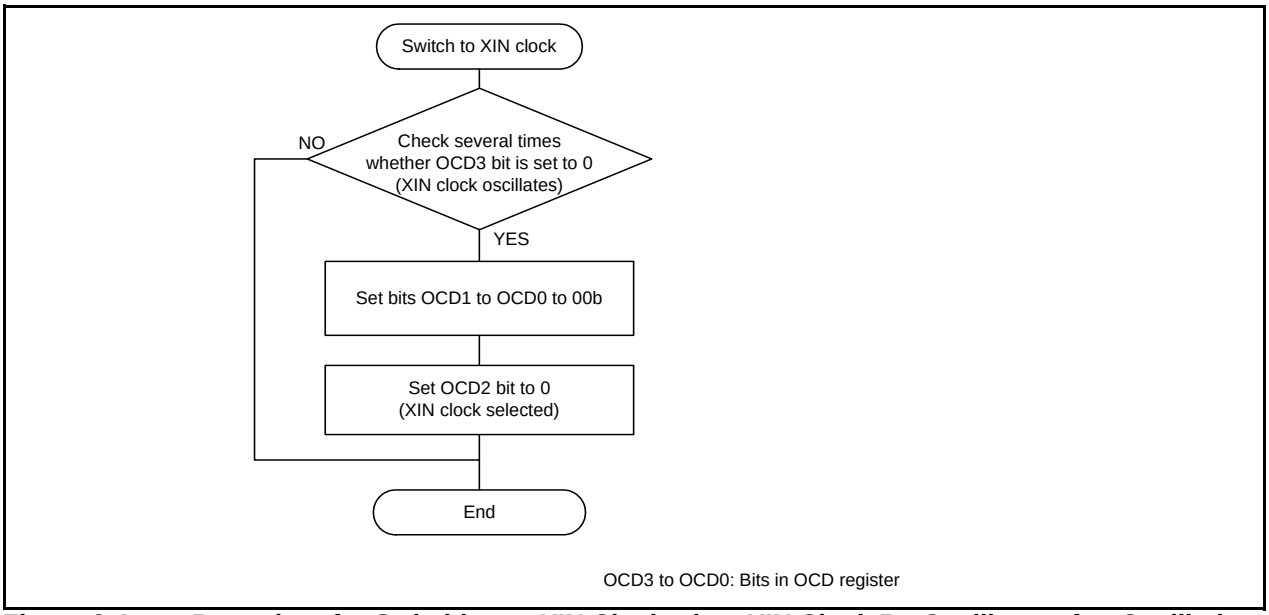


Figure 9.4 Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected

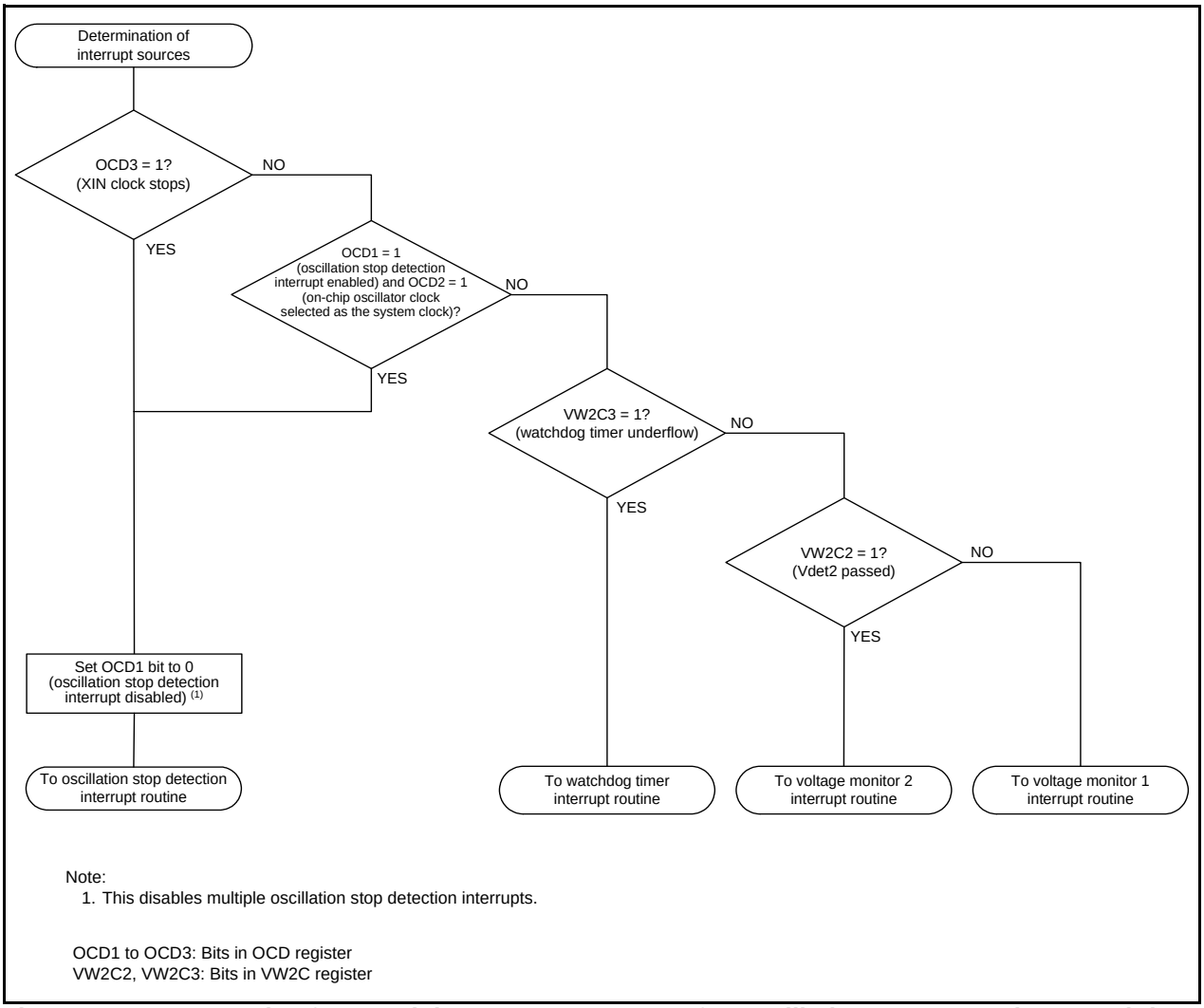


Figure 9.5 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

9.7 Notes on Clock Generation Circuit

9.7.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

9.7.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Power Control

10.1 Introduction

There are three power control modes. The states other than wait mode and stop mode are referred to as standard operating mode here.
Table 10.1 lists each mode. Figure 10.1 shows the State Transitions in Power Control Mode.

Table 10.1 Power Control

Mode		Operation
Standard operating mode	High-speed clock	The CPU and peripheral functions operate.
	Low-speed on-chip oscillator	
Wait mode		The CPU stops and peripheral functions operate.
Stop mode		The CPU stops and peripheral functions other than the watchdog timer stop (oscillation off).

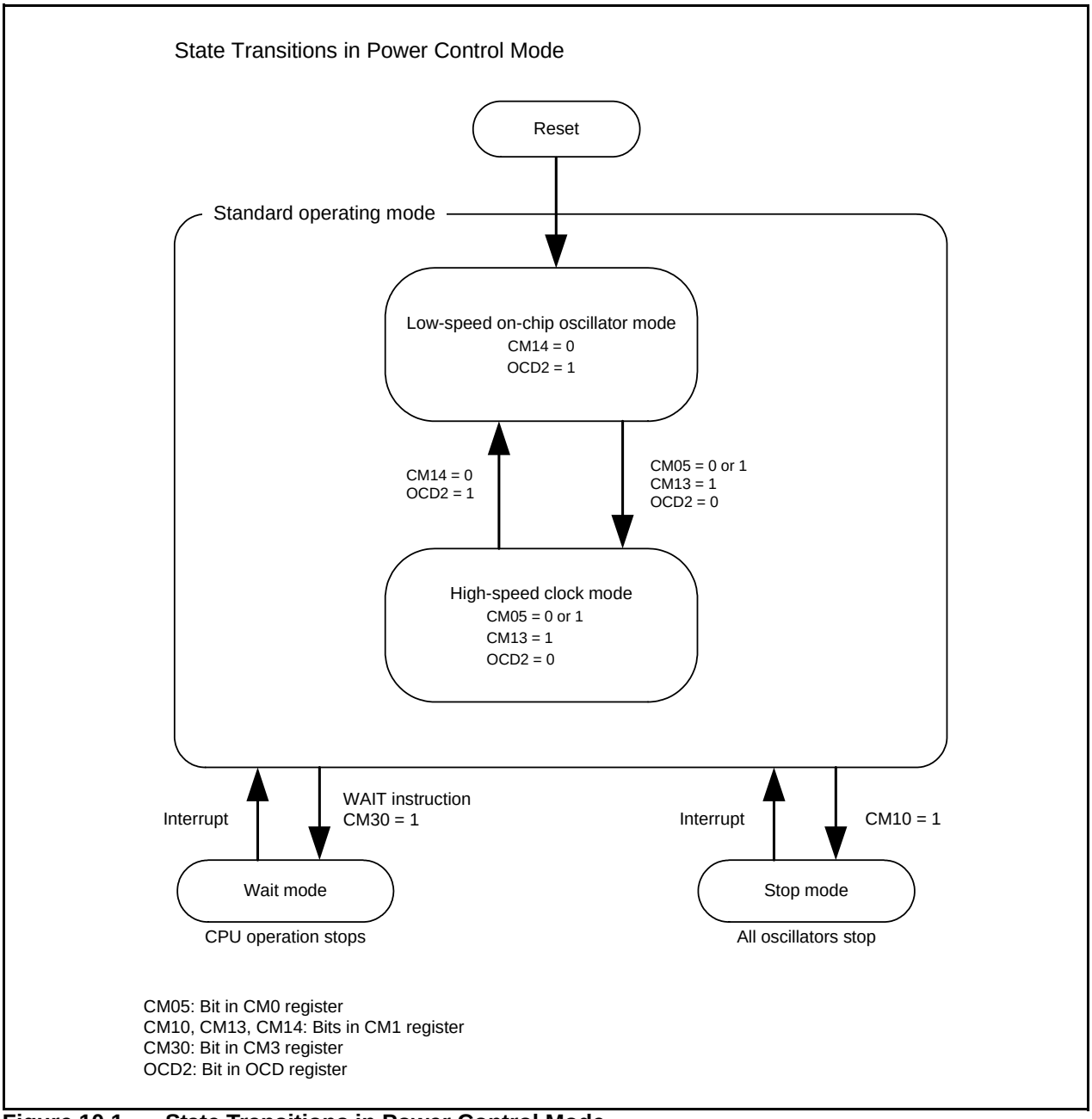


Figure 10.1 State Transitions in Power Control Mode

10.2 Registers

10.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CM06	CM05	—	CM03	CM02	CM01	—
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	CM01	Peripheral function clock stop bit in wait mode	b1 b0 0 0: Peripheral function clock does not stop in wait mode 0 1: Clocks f1 to f32 stop in wait mode 1 0: Clocks f1 to f32 stop in wait mode 1 1: Clocks f1 to f32 stop in wait mode	R/W
b2	CM02			R/W
b3	CM03	Reserved bit	Set to 1.	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 2)	0: XIN clock oscillates 1: XIN clock stops	R/W
b6	CM06	CPU clock division select bit 0 (3)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:

1. The CM05 bit can be used to stop the XIN clock when the system clock is other than the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. Only when the CM05 bit to 1 (XIN clock stops) and the CM13 bit is set to 0 (I/O ports), P9_0 and P9_1 can be used as I/O ports.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
3. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

10.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 7)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	Reserved bit	Set to 1.	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6)	0: I/O ports P9_0 and P9_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1 (all clocks stop), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P9_0 and P9_1 as input ports, set the CM13 bit to 0 (I/O ports) and the CM05 bit in the CM0 register to 1 (XIN clock stops).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 0 (XIN clock oscillates), and the CM11 bit to 1 (on-chip feedback resistor disabled). When the PD9_0 bit in the PD9 register is further set to 0 (input mode), an external clock can be input. Set XOUT as the I/O port P9_1 at this time. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
6. Once the CM13 bit is set to 1 (XIN-XOUT pin) by a program, it cannot be set to 0 (I/O ports P9_0 and P9_1).
7. Do not set the CM10 bit to 1 when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

10.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division (2)	R/W
b6	CM36	System clock select bit when exiting wait or stop mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait or stop mode 0 1: Do not set. 1 0: Do not set. 1 1: XIN clock selected (3)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • CM05 bit in CM0 register = 0 (XIN clock oscillates)
   • CM13 bit in CM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0. However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

10.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	On-chip oscillator clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode or low-speed on-chip oscillator mode (XIN clock stops).
2. When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) when the XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. When the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even if 0 (XIN clock selected) is written to it.
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled). In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.
5. The OCD3 bit remains 0 (XIN clock oscillates) when bits OCD1 to OCD0 are set to 00b.
6. Refer to **9.6.1 How to Use Oscillation Stop Detection Function** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

10.2.5 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **10.6.8 Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (all clocks stop).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1 (voltage detection 1 circuit enabled).
   After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1 (voltage detection 2 circuit enabled).
   After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

10.3 Standard Operating Mode

Table 10.2 lists the Clock Selection in Standard Operating Mode.
In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

Table 10.2 Clock Selection in Standard Operating Mode

Modes		OCD Register	CM1 Register				CM0 Register	
		OCD2	CM17	CM16	CM14	CM13	CM06	CM05
High-speed clock mode	No division	0	0	0	—	0 or 1 (1)	0	0
	Divide-by-2	0	0	1	—	0 or 1 (1)	0	0
	Divide-by-4	0	1	0	—	0 or 1 (1)	0	0
	Divide-by-8	0	—	—	—	0 or 1 (1)	1	0
	Divide-by-16	0	1	1	—	0 or 1 (1)	0	0
Low-speed on-chip oscillator mode	No division	1	0	0	0	—	0	—
	Divide-by-2	1	0	1	0	—	0	—
	Divide-by-4	1	1	0	0	—	0	—
	Divide-by-8	1	—	—	0	—	1	—
	Divide-by-16	1	1	1	0	—	0	—

—: Indicates that either 0 or 1 can be set.
Note:
1. Set the CM13 bit to 0 to select the external clock input and set the CM13 bit to 1 to select the on-chip oscillation circuit.

10.3.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO can be used for timer RJ.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

10.3.2 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on), the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks.
Also, When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To enter wait mode from this mode, lower consumption current in wait mode can be further reduced by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **10.6 Reducing Power Consumption**.

10.4 Wait Mode

Since the CPU clock stops in wait mode, CPU operation using the CPU clock and watchdog timer operation with count source protection mode disabled are halted. However, the XIN clock and on-chip oscillator clock do not stop, so peripheral functions using these clocks continue operating.

10.4.1 Peripheral Function Clock Stop Function

The peripheral function clock to stop in wait mode can be selected by setting bits CM01 and CM02 in the CM0 register (peripheral function clock stop bits in wait mode). This controls power consumption according to applications.

10.4.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).

When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).

If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode.

Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (lowcurrent-consumption read mode enabled).

To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled). To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled).

When setting bits CM37 and CM36 to values other than 00b to enter wait mode from high-speed clock mode, set the XIN clock frequency to 28 kHz or more.

10.4.3 Reducing Internal Power Using VCA20 Bit

When the MCU enters wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced using the VCA20 bit in the VCA2 register. To enable internal power consumption using the VCA20 bit, follow the procedure shown in 10.8.9 Reducing Internal Power Consumption Using VCA20 Bit.

10.4.4 Pin Status in Wait Mode

Each I/O port retains its states immediately before the MCU enters wait mode.

10.4.5 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt. The peripheral function interrupts are affected by bits CM01 and CM02.
Table 10.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 10.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 to CM01 = 00b	CM02 to CM01 = 01b	CM02 to CM01 = 10b	CM02 to CM01 = 11b
Synchronous serial communication unit interrupt/I^2C bus interface interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
Key input interrupt	Usable	Usable	Usable	Usable
Timer RJ interrupt	Usable in all modes.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.
Timer RB interrupt	Usable in all modes.	(Do not use.)	Usable by selecting fOCO as timer RJ count source and timer RJ underflow as timer RB count source	Usable by selecting fOCO as timer RJ count source and timer RJ underflow as timer RB count source
Timer RC interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
$\overline{INT}$ interrupt	Usable	Usable if there is no filter.	Usable if there is no filter.	Usable if there is no filter.
Voltage monitor 1 interrupt	Usable	Usable	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use.)	(Do not use.)	(Do not use.)

The following interrupts can be used to exit wait mode:

- When bits CM02 to CM01 are set to 00b (peripheral function clock does not stop in wait mode), peripheral function interrupts.
- When bits CM02 to CM01 are set to 01b (clocks f1 to f32 stop in wait mode), the interrupts of the peripheral functions operating with external signals or the on-chip oscillator clock.
- When bits CM02 to CM01 are set to 10b (clocks f1 to f32 stop in wait mode), the interrupts of the peripheral functions operating with external signals or the on-chip oscillator clock.
- When bits CM02 to CM01 are set to 11b (clocks f1 to f32 stop in wait mode), the same applies when bits CM02 to CM01 are set to 10b.

10.4.6 Exiting Wait Mode after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 10.2 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).

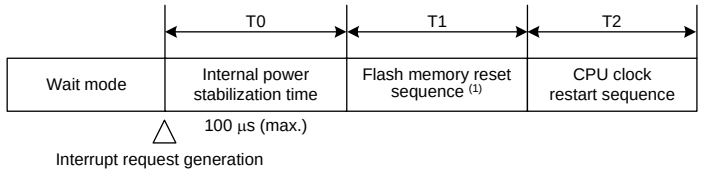
To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.

(1) Set the I flag to 0 (maskable interrupt disabled)
(2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 10.2.

The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Flash Memory Reset Time (T1)	Time until CPU Clock Supply (T2)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	100 μs (max.) (2)	Period of system clock × 1 cycle (1)	Period of CPU clock × 2 cycles	The total of T0 to T2 is the time from wait mode to first instruction execution following exit.
	1 (internal power low consumption enabled)	100 μs (max.) (2)			
1 (flash memory stops) (RAM operates)	0 (internal power low consumption disabled	0 μs			
	1 (internal power low consumption enabled)	100 μs (max.)			



Notes:
1. This time is also required when the flash memory stops (the FMSTP bit in the FMR0 register is set to 1).
2. The activation of the flash memory is also completed within the internal power stabilization time.

Figure 10.2 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

10.4.7 Exiting Wait Mode after WAIT Instruction is Executed

Figure 10.3 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed.

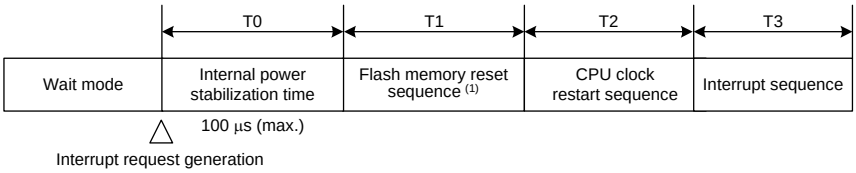
To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1 (maskable interrupts enabled).
(3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 10.3.

The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Flash Memory Reset Time (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	100 μs (max.) (2)	Period of system clock × 1 cycle (1)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode until an interrupt routine is executed.
	1 (internal power low consumption enabled)	100 μs (max.) (2)				
1 (flash memory stops) (RAM operates)	0 (internal power low consumption disabled	0 μs				
	1 (internal power low consumption enabled)	100 μs (max.)				



Notes:
1. This time is also required when the flash memory stops (the FMSTP bit in the FMR0 register is set to 1).
2. The activation of the flash memory is also completed within the internal power stabilization time.

Figure 10.3 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

10.5 Stop Mode

All oscillator circuits except fOCO-WDT stop in stop mode. Since the CPU clock and the peripheral function clock stop, CPU operation and peripheral function operation using these clocks are halted. If the voltage applied to the VCC pin is VRAM or more, the content of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 10.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 10.4 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$ interrupt	Usable if there is no filter.
Timer RJ interrupt	Usable if there is no filter when an external pulse is counted in event counter mode.
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (the VW1C1 bit in the VW1C register is set to 1).
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (the VW2C1 bit in the VW2C register is set to 1).

10.5.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1. At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

10.5.2 Pin Status in Stop Mode

Each I/O port retains its state before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT (P9_1) pin is held high.

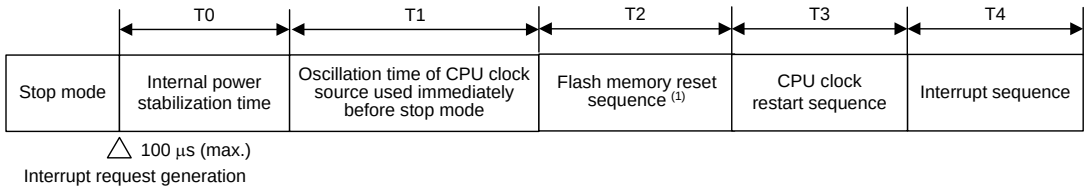
10.5.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 10.4 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1 (maskable interrupts enabled).
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).

FMR0 Register FMSTP Bit	Internal Power Stabilization Time (T0)	Flash Memory Reset Time (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 µs (max.) (2)	Period of system clock × 1 cycle (1)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from stop mode until an interrupt routine is executed.
1 (flash memory stops) (RAM operates)	100 µs (max.)				



Notes:
1. This time is also required when the flash memory stops (the FMSTP bit in the FMR0 register is set to 1).
2. The activation of the flash memory is also completed within the internal power stabilization time.

Figure 10.4 Time from Stop Mode to Interrupt Routine Execution

10.6 Reducing Power Consumption

This section describes key points and processing methods for reducing power consumption. They should be referred to when designing a system or creating a program.

10.6.1 Voltage Detection Circuit

When voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). When voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
When power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

10.6.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to output. When setting them to input, fix to a stable electric potential before the MCU enters wait mode or stop mode.

10.6.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases.
Unnecessary clocks should be stopped accordingly.

Stopping the low-speed on-chip oscillator oscillation: Set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off) and the OCD2 bit in the OCD register to 0 (XIN clock selected).

10.6.4 Wait Mode and Stop Mode

Power consumption can be reduced in wait mode and stop mode.

10.6.5 Stopping Peripheral Function Clocks

When peripheral function clocks are not necessary in wait mode, set bits CM01 and CM02 bit in the CM0 register to stop the clock.

10.6.6 Timers

When timer RJ is not used, set the TCKCUT bit in the TRJ0MR register to 1 (count source cutoff).
When timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
When timer RC is not used, set the MSTTRC bit in the MSTCR0 register to 1 (standby).

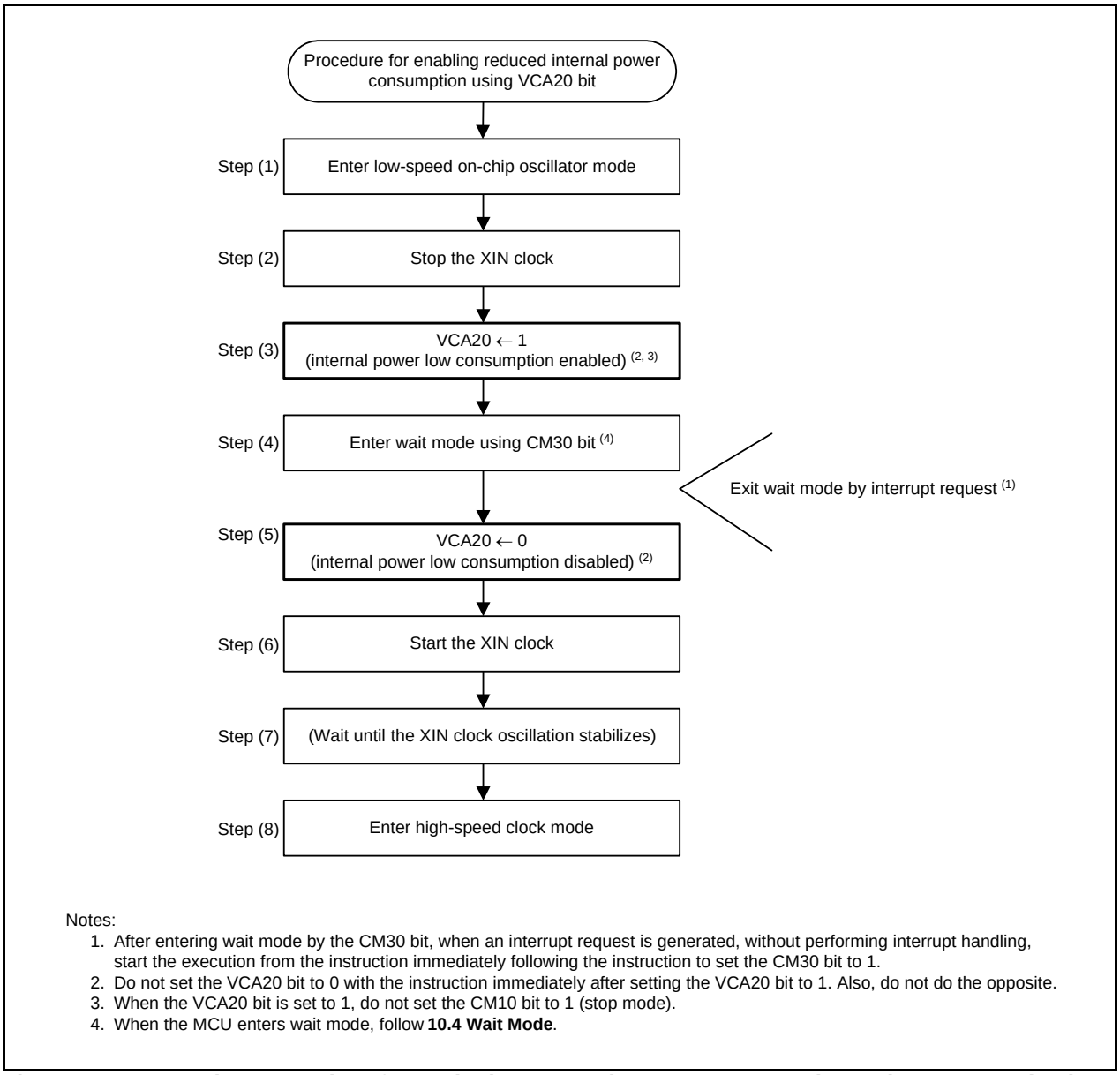
10.6.7 Clock Synchronous Serial Interface

When the SSU or I^2C bus is not used, set the MSTIIC bit in the MSTCR0 register to 1 (standby).

10.6.8 Reducing Internal Power Consumption Using VCA20 Bit

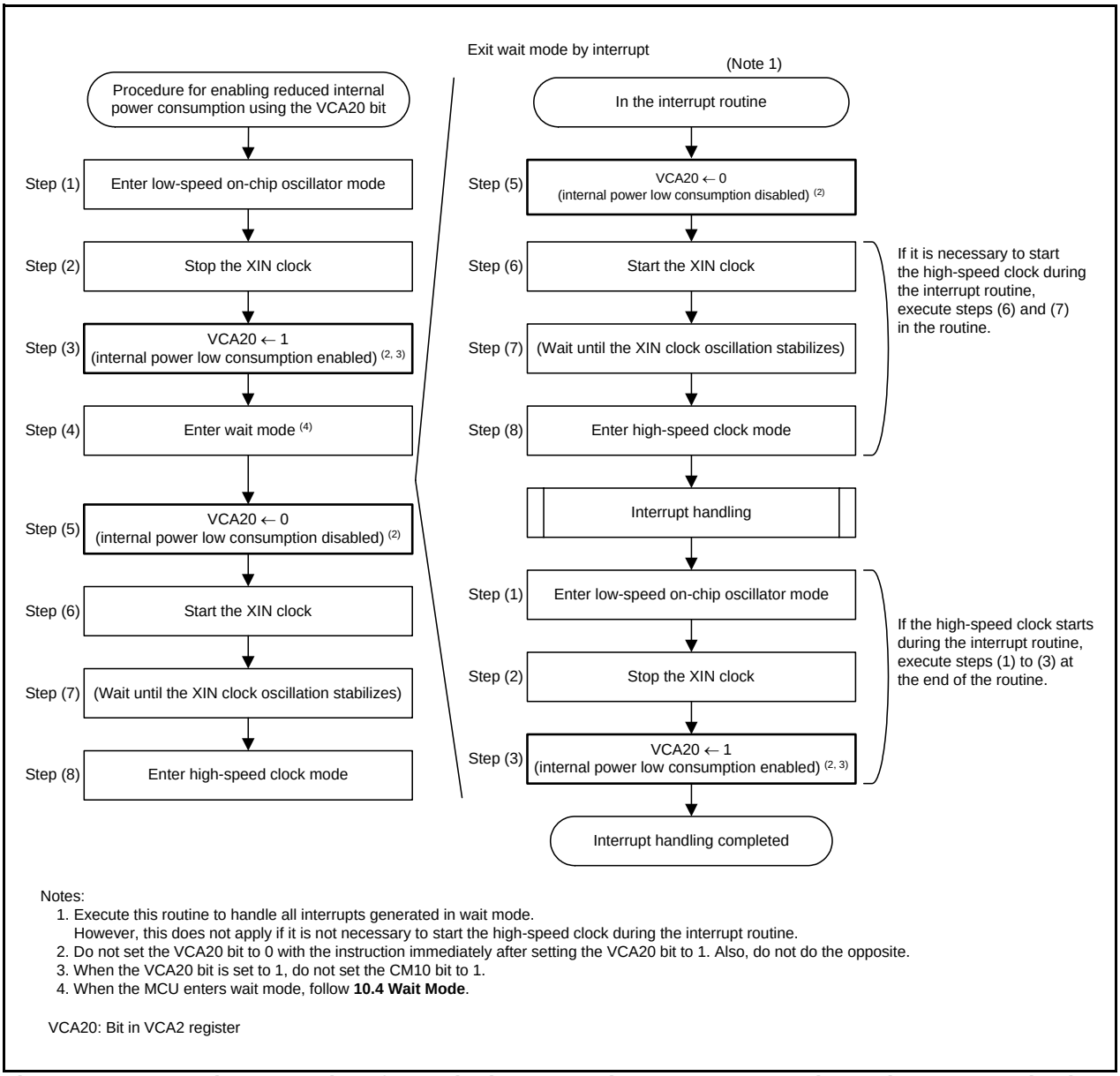
The electric current in wait mode can be further reduced by setting the VCA20 bit in the VCA2 register to 1 (low consumption enabled). Set the VCA20 bit to 1 in low-speed on-chip oscillator mode before entering wait mode.

The setting procedure for reducing internal power consumption using the VCA20 bit differs when the CM30 bit in the CM3 register is set to 1 (MCU enters wait mode) to enter wait mode and when the WAIT instruction is executed to enter wait mode. Figure 10.5 shows the Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode) to Enter Wait Mode. Figure 10.6 shows the Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when WAIT Instruction is Executed to Enter Wait Mode.



Notes:
1. After entering wait mode by the CM30 bit, when an interrupt request is generated, without performing interrupt handling, start the execution from the instruction immediately following the instruction to set the CM30 bit to 1.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **10.4 Wait Mode**.

Figure 10.5 Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode) to Enter Wait Mode



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1.
4. When the MCU enters wait mode, follow **10.4 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 10.6 Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when WAIT Instruction is Executed to Enter Wait Mode

10.6.9 Stopping Flash Memory

In low-speed on-chip oscillator mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.

Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.

When the MUC enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.

Do not use the settings of FMR27 = 1 (low-current-consumption read mode enabled) and FMSTP = 1 (flash memory stops) at the same time.

Figure 10.7 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

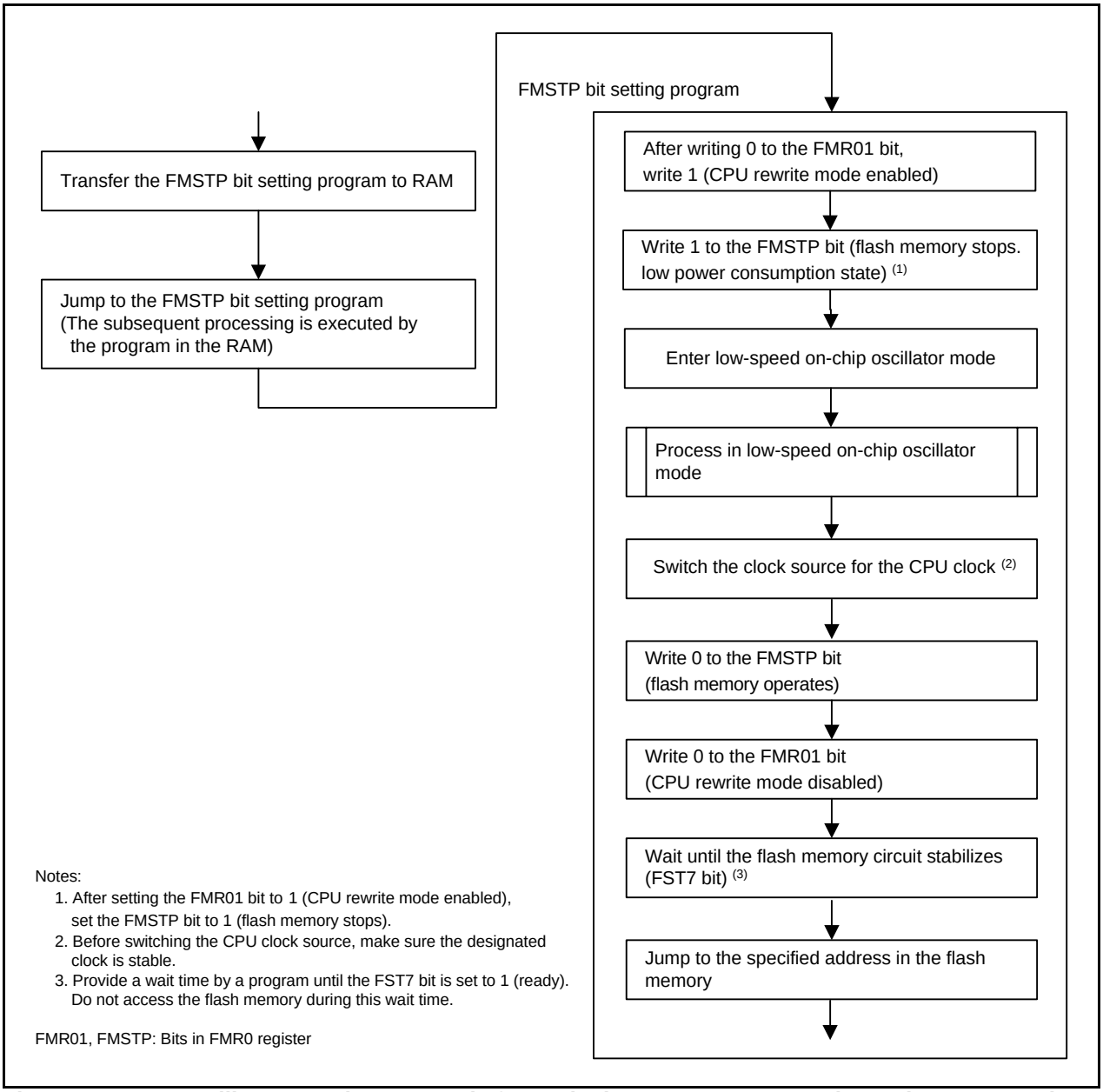
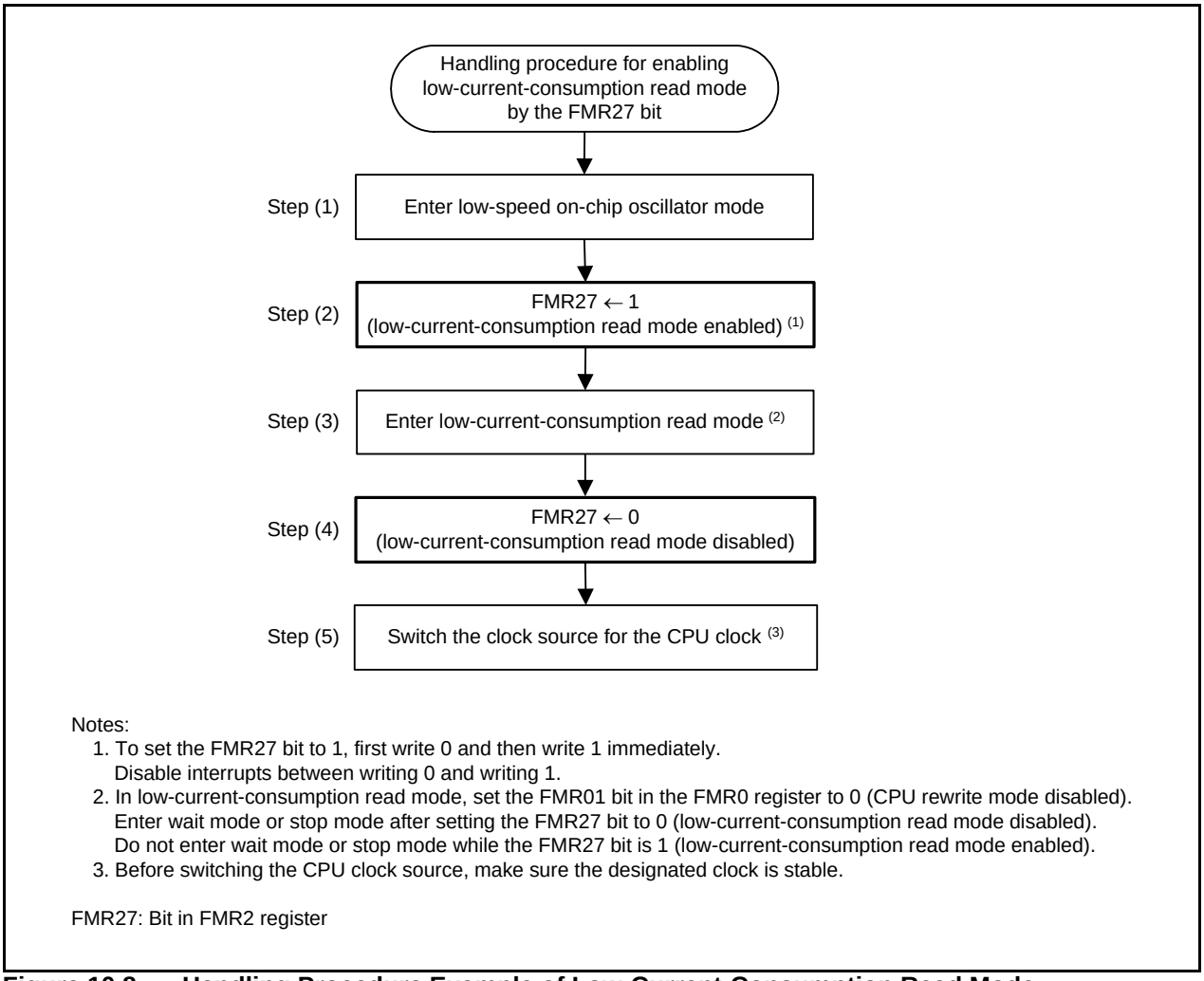


Figure 10.7 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

10.6.10 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
• The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
Do not use the settings of FMR27 = 1 (low-current-consumption read mode enabled) and FMSTP = 1 (flash memory stops) at the same time.
Figure 10.8 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately.
   Disable interrupts between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
3. Before switching the CPU clock source, make sure the designated clock is stable.

FMR27: Bit in FMR2 register

Figure 10.8 Handling Procedure Example of Low-Current-Consumption Read Mode

10.7 Notes on Power Control

10.7.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) first and then set the CM10 bit in the CM1 register to 1. An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to registers CM0 and CM1 enabled
        FSET    I           ; Interrupt enabled
        BSET    0,CM1       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

10.7.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode. Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).
To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled). An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        FSET    I           ; Interrupt enabled
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register disabled
        FSET    I           ; Interrupt enabled
```

10.7.3 Reducing Internal Power Using VCA20 Bit

Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode.

To enter wait mode by setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode), follow the procedure shown in Figure 10.5 to set the procedure for reducing internal power consumption using the VCA20 bit.

To enter wait mode by executing WAIT instruction, follow the procedure shown in Figure 10.6 to set the procedure for reducing internal power consumption using the VCA20 bit.

11. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, and OCD
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC3 bit: Registers VCA2, VD1LS, VW0C, VW1C, and VW2C

11.1 Register

11.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	—	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD 0: Write disabled 1: Write enabled (1)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (1)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	PRC3	Protect bit 3	Enables writing to registers VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (1)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:

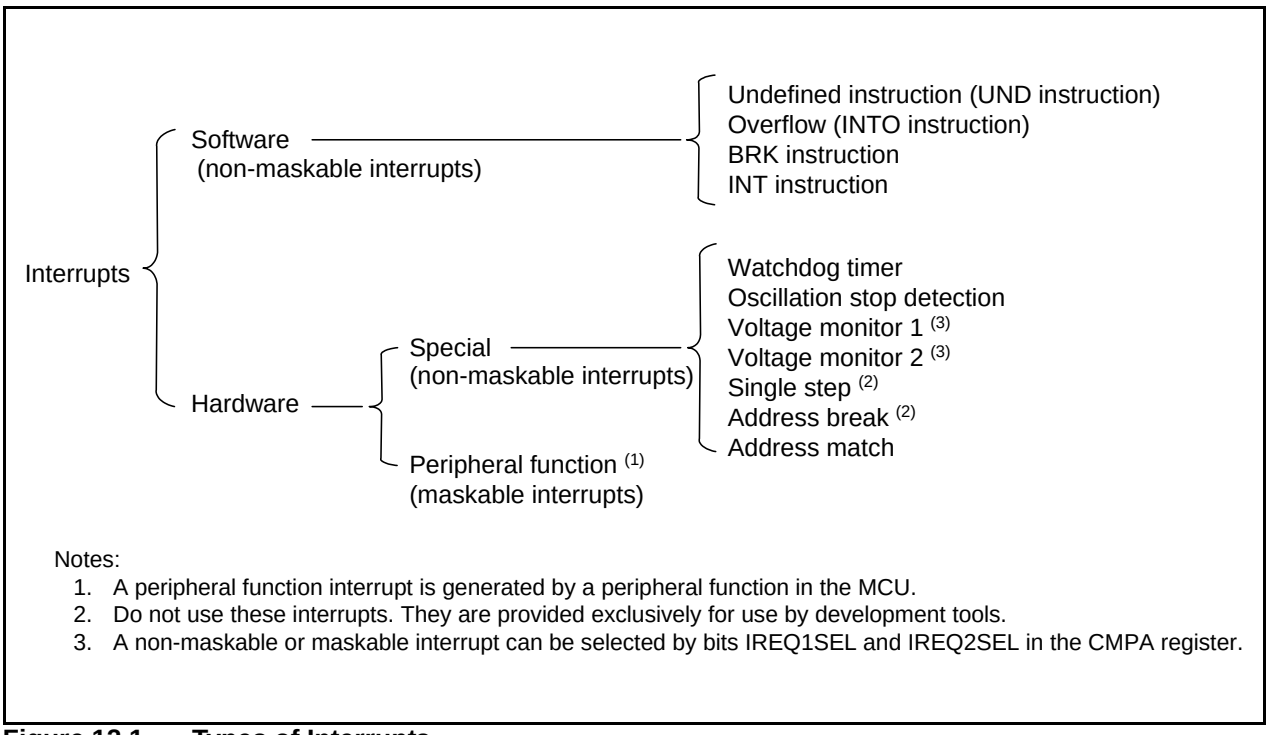
1. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

12. Interrupts

12.1 Introduction

12.1.1 Types of Interrupts

Figure 12.1 shows the Types of Interrupts.



Notes:
1. A peripheral function interrupt is generated by a peripheral function in the MCU.
2. Do not use these interrupts. They are provided exclusively for use by development tools.
3. A non-maskable or maskable interrupt can be selected by bits IREQ1SEL and IREQ2SEL in the CMPA register.

Figure 12.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

12.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

12.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

12.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

12.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

12.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

12.1.3 Special Interrupts

Special interrupts are non-maskable.

12.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **15. Watchdog Timer**.

12.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

12.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.4 Voltage Monitor 2 Interrupt

A voltage monitor 2 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.5 Single-Step Interrupt, Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

12.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER00 bit in the AIER0 register or AIER10 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **12.6 Address Match Interrupt**.

12.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Table 12.2 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

12.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows an Interrupt Vector.

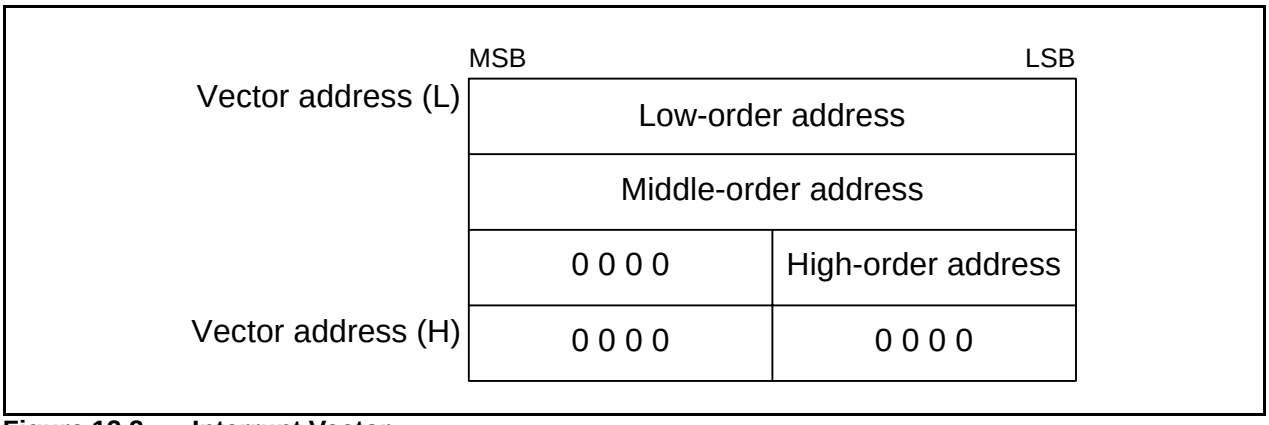


Figure 12.2 Interrupt Vector

12.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 12.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **24.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 12.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		12.6 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1 (2), Voltage monitor 2 (3)	0FFF0h to 0FFF3h		15. Watchdog Timer, 9. Clock Generation Circuit, 6. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Notes:
1. Do not use these interrupts. They are provided exclusively for use by development tools.
2. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (nonmaskable interrupt).
3. Voltage monitor 2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 0 (nonmaskable interrupt).

12.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 12.2 lists the Relocatable Vector Tables.

Table 12.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (3)	+0 to +3 (0000h to 0003h)	0	—	R8C/Tiny Series Software Manual
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	24. Flash Memory
(Reserved)		2	—	—
(Reserved)		3	—	—
(Reserved)		4	—	—
$\overline{\text{INT5}}$	+20 to +23 (0014h to 0017h)	5	INT5IC	12.4 $\overline{\text{INT}}$ Interrupt
(Reserved)		6	—	—
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	18. Timer RC
(Reserved)		8	—	—
(Reserved)		9	—	—
(Reserved)		10	—	—
(Reserved)		11	—	—
(Reserved)		12	—	—
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	12.5 Key Input Interrupt
(Reserved)		14	—	—
Synchronous serial communication unit/ I^2C bus interface (2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/ IICIC	22. Synchronous Serial Communication Unit (SSU), 23. I^2C bus Interface
(Reserved)		16	—	—
(Reserved)		17	—	—
(Reserved)		18	—	—
(Reserved)		19	—	—
(Reserved)		20	—	—
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	12.4 $\overline{\text{INT}}$ Interrupt
Timer RJ0	+88 to +91 (0058h to 005Bh)	22	TRJ0IC	19. Timer RJ
Timer RB1	+92 to +95 (005Ch to 005Fh)	23	TRB1IC	17. Timer RB
Timer RB0	+96 to +99 (0060h to 0063h)	24	TRB0IC	17. Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
(Reserved)		27	—	—
(Reserved)	+112 to +115 (0070h to 0073h)	28	—	—
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	12.4 $\overline{\text{INT}}$ Interrupt
(Reserved)	+120 to +123 (0078h to 007Bh)	30	—	—
(Reserved)		31	—	—
Software (3)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	—	R8C/Tiny Series Software Manual
(Reserved)		42	—	—
(Reserved)		43	—	—
(Reserved)		44 to 49	—	—
Voltage monitor 1 (4)	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit
Voltage monitor 2 (5)	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC	
(Reserved)		52 to 55	—	—
Software (3)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63	—	R8C/Tiny Series Software Manual

Notes:
1. These addresses are relative to those in the INTB register.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. These interrupts are not disabled by the I flag.
4. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 1 (maskable interrupt).
5. Voltage monitor 2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 1 (maskable interrupt).

12.2 Registers

12.2.1 Interrupt Control Register (KUPIC, TRJ0IC, TRB1IC, TRB0IC, VCMP1IC, VCMP2IC)

Address 004Dh (KUPIC), 0056h (TRJ0IC), 0057h (TRB1IC), 0058h (TRB0IC), 0072h (VCMP1IC), 0073h (VCMP2IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.2.2 Interrupt Control Register (FMRDYIC, TRCIC, SSUIC/IICIC)

Address 0041h (FMRDYIC), 0047h (TRCIC), 004Fh (SSUIC/IICIC (1))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Selectable by the IICSEL bit in the SSUIICSR register.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.2.3 INTi Interrupt Control Register (INTiIC) (i = 0 to 3, 5)

Address 0045h (INT5IC), 0055h (INT2IC), 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.
2. When the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

12.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

12.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the synchronous serial communication unit interrupt the I^2C bus interface interrupt, and the flash memory interrupt are different. Refer to **12.7 Interrupts of Timer RC, Synchronous Serial Communication Unit, I^2C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)**.

12.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 12.3 lists the Settings of Interrupt Priority Levels and Table 12.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are the conditions when an interrupt is acknowledged:

- I flag = 1 (maskable interrupts enabled)
- IR bit = 1 (interrupt requested)
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 12.3 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	—
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 12.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts disabled

12.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 12.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **12.7 Interrupts of Timer RC, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the above interrupts.

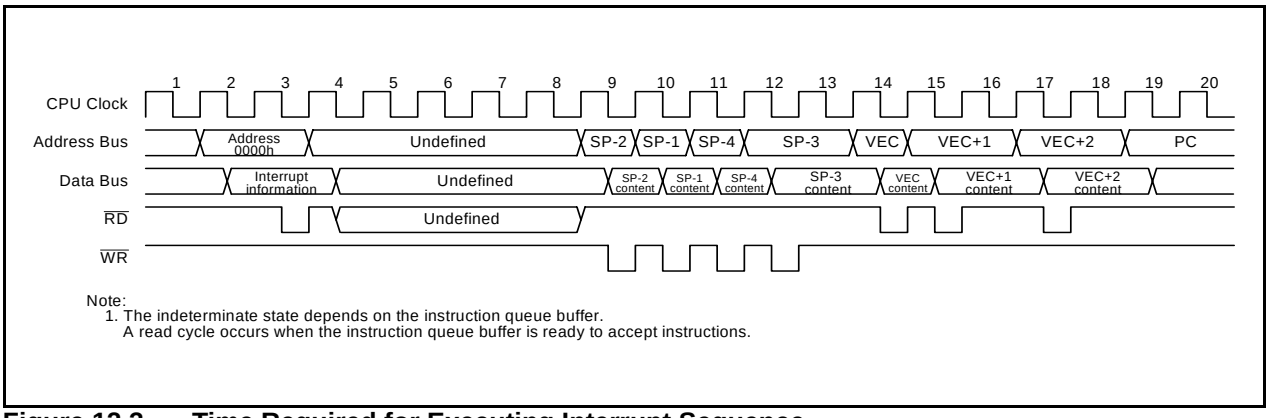
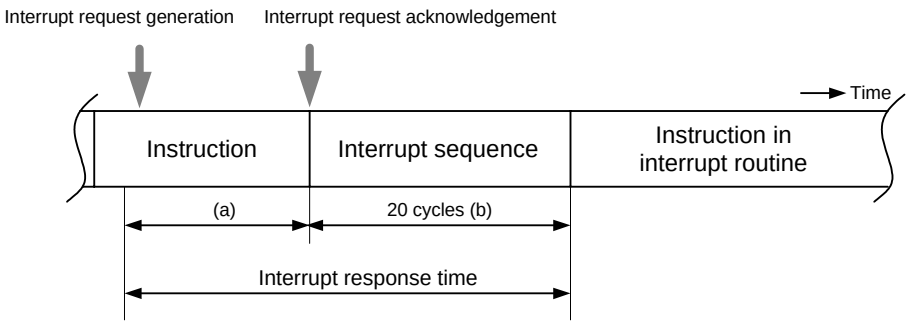


Figure 12.3 Time Required for Executing Interrupt Sequence

12.3.5 Interrupt Response Time

Figure 12.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 12.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 12.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 12.4 Interrupt Response Time

12.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 12.5 is set in the IPL.
Table 12.5 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 12.5 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break	7
Software, address match, single-step	No change

12.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 12.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

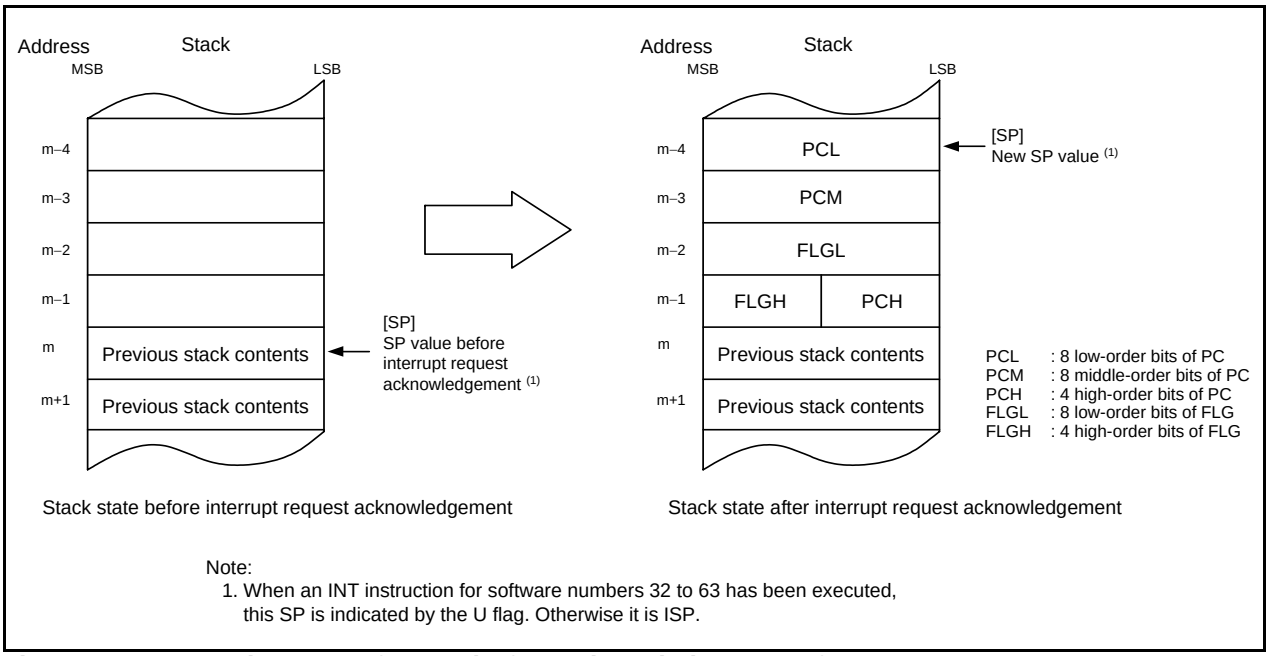
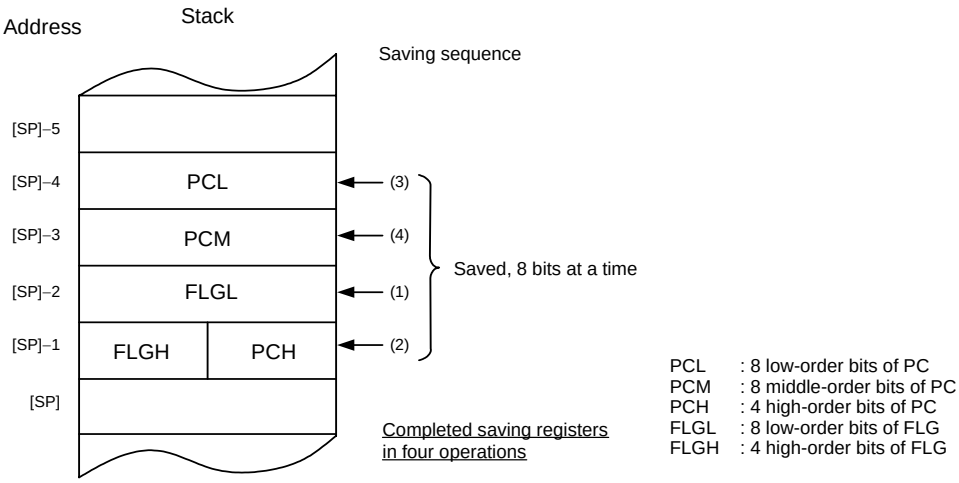


Figure 12.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 12.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed,
this SP is indicated by the U flag. Otherwise it is ISP.

Figure 12.6 Register Saving Operation

12.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

12.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of the watchdog timer and other special interrupts is set by hardware.

Figure 12.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. When an instruction is executed, the MCU executes the interrupt routine.

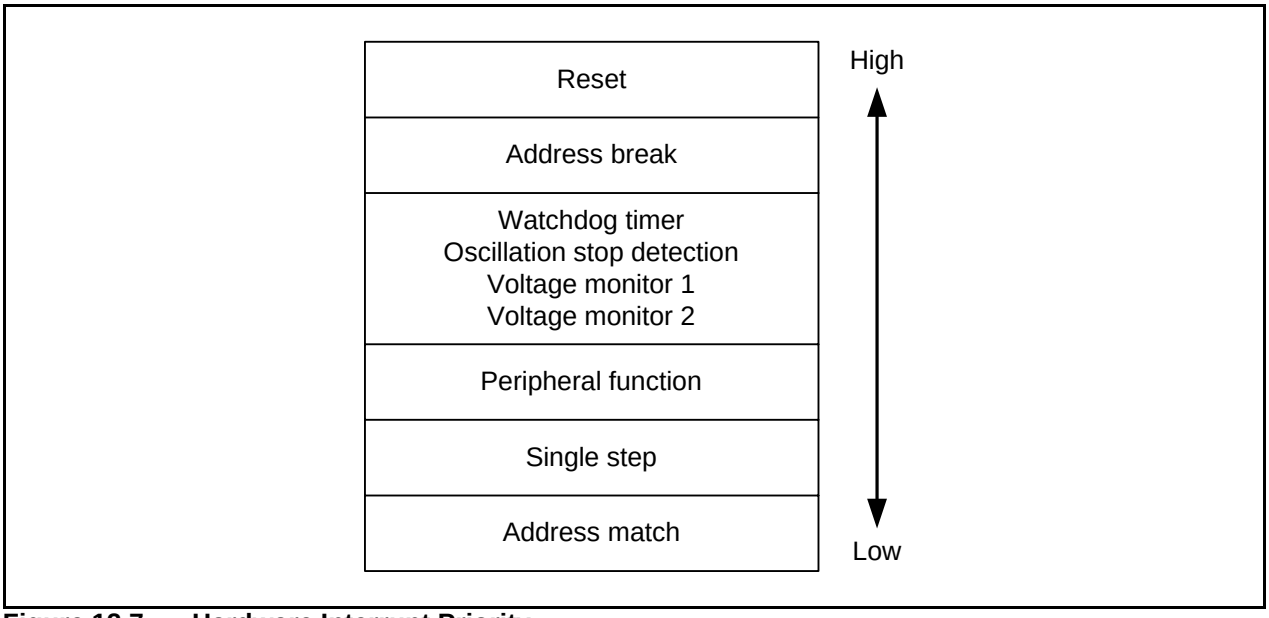


Figure 12.7 Hardware Interrupt Priority

12.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt. Figure 12.8 shows the Interrupt Priority Level Selection Circuit.

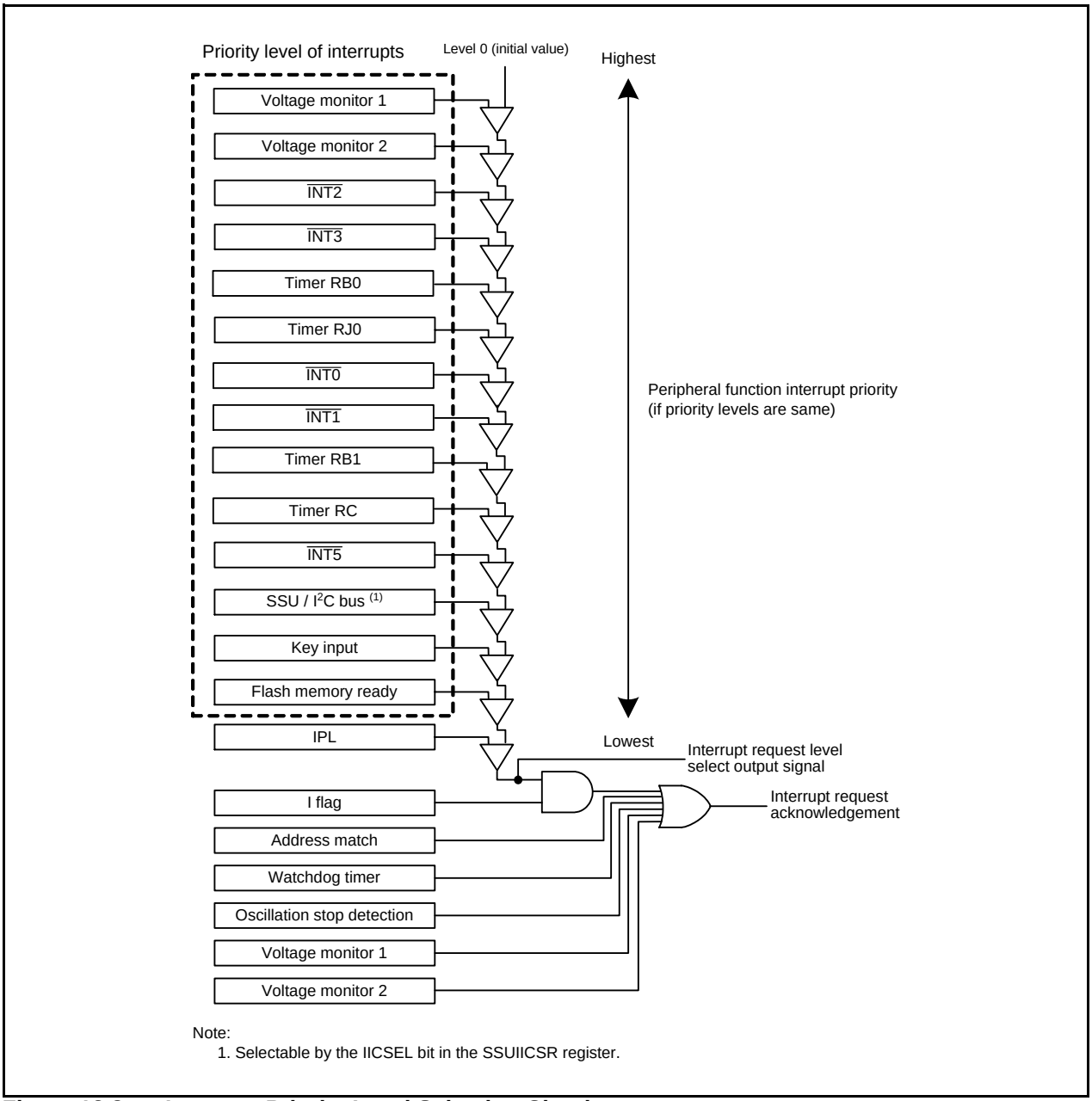


Figure 12.8 Interrupt Priority Level Selection Circuit

12.4 $\overline{\text{INT}}$ Interrupt

12.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3, 5)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pin used as the $\overline{\text{INTi}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC, and the external trigger input of timer RB0.
The $\overline{\text{INT2}}$ pin is shared with the event input of timer RJ.
The $\overline{\text{INT5}}$ pin is shared with the external trigger input of timer RB1.
Table 12.6 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 12.6 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P2_2	Input	$\overline{\text{INT0}}$ interrupt input, timer RB0 external trigger input, timer RC pulse output forced cutoff input
$\overline{\text{INT1}}$	P8_0	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P7_1	Input	$\overline{\text{INT2}}$ interrupt input, timer RJ event control
$\overline{\text{INT3}}$	P8_1	Input	$\overline{\text{INT3}}$ interrupt input
$\overline{\text{INT5}}$	P2_3	Input	$\overline{\text{INT5}}$ interrupt input, timer RB1 external trigger input

12.4.2 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.4.3 External Input Enable Register 1 (INTEN1)

Address 01FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INT5PL	INT5EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	INT5EN	$\overline{\text{INT5}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT5PL	$\overline{\text{INT5}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. To set the INT5PL bit to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN1 register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.4.4 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

12.4.5 INT Input Filter Select Register 1 (INTF1)

Address 01FDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INT5F1	INT5F0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	INT5F0	$\overline{\text{INT5}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT5F1			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

12.4.6 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3, 5)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF0 and INTiF1 in registers INTF and INTF1. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).
Figure 12.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 12.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

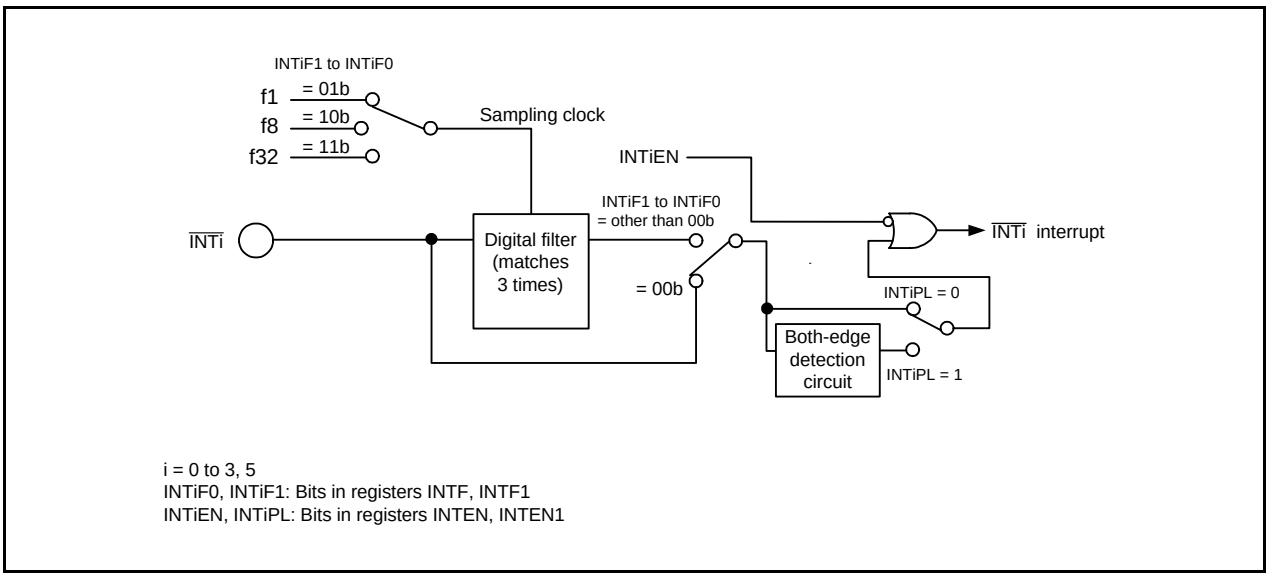


Figure 12.9 $\overline{\text{INTi}}$ Input Filter Configuration

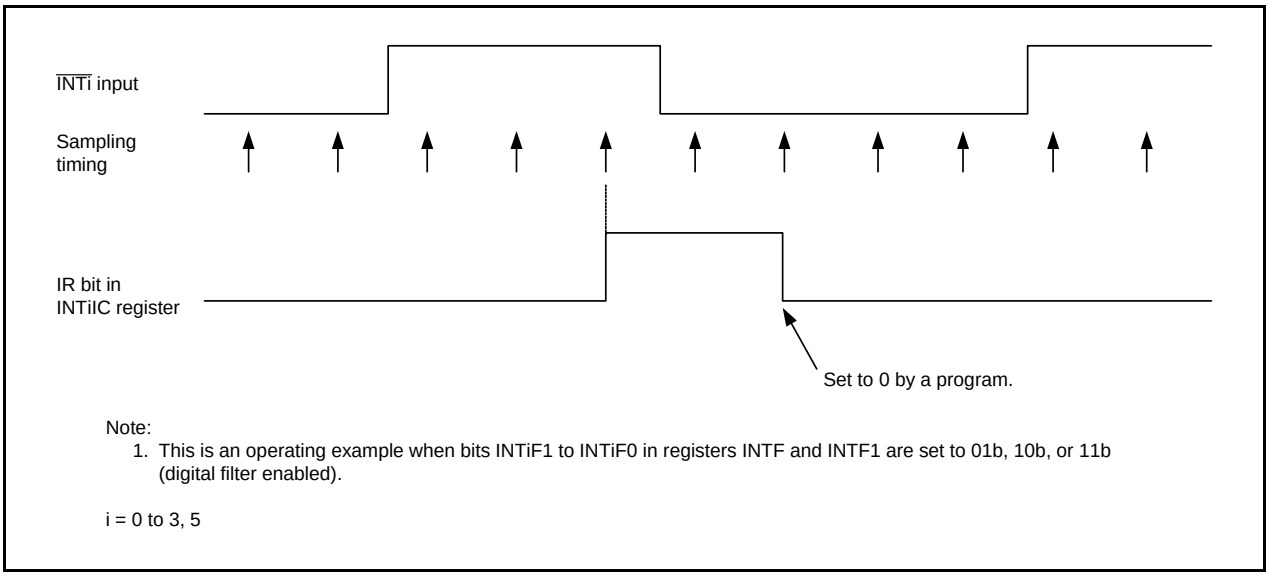


Figure 12.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

12.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K17}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN bit (i = 0 to 7) in the KIEN register is be used to select whether or not the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is also be used to select the input polarity.

When inputting a low signal to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{K10}$ to $\overline{K17}$ is not detected as interrupts. When inputting a high signal to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{K10}$ to $\overline{K17}$ is also not detected as interrupts.

Figure 12.11 shows a Block Diagram of Key Input Interrupt. Table 12.7 lists the Key Input Interrupt Pin Configuration.

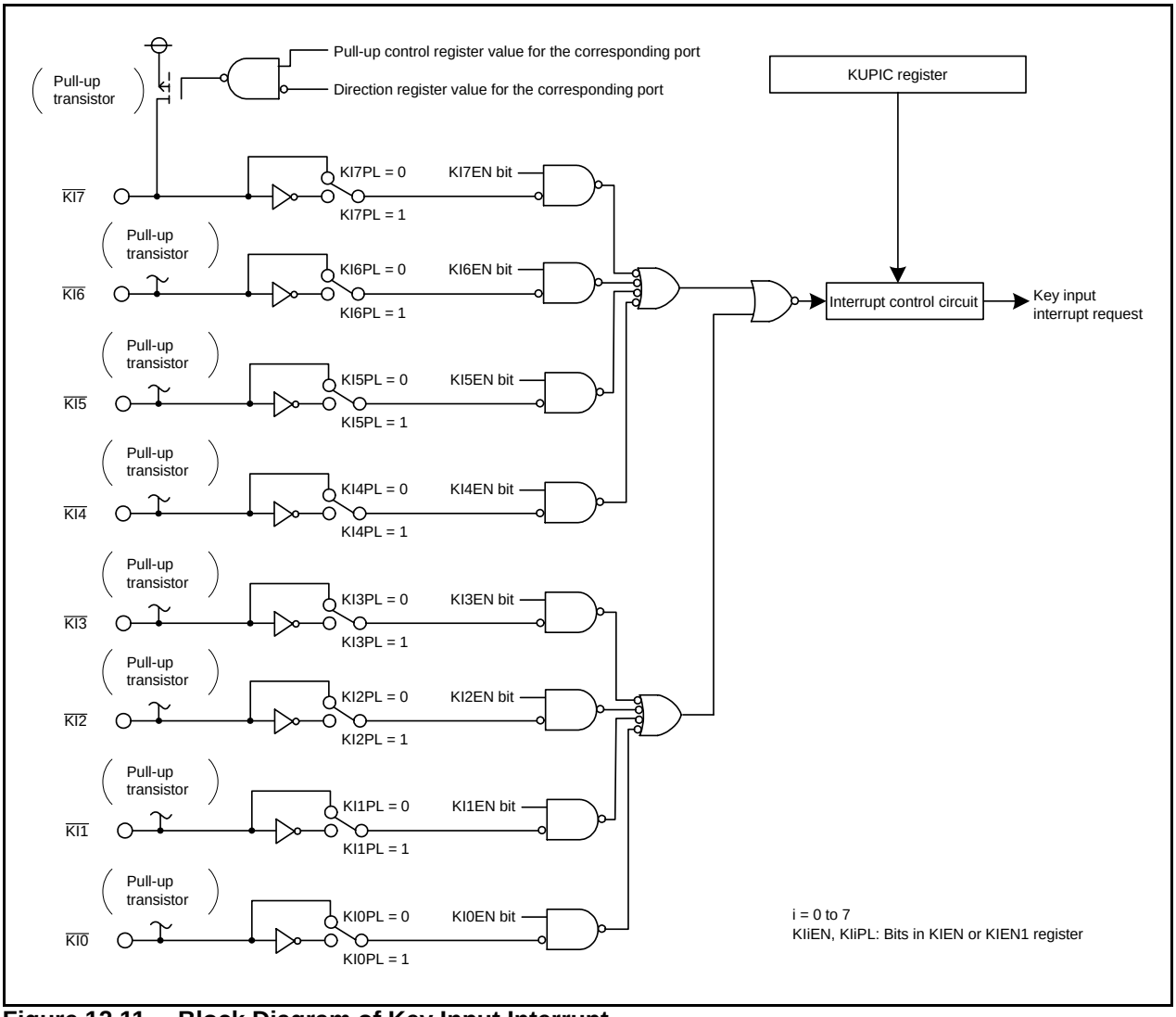


Figure 12.11 Block Diagram of Key Input Interrupt

Table 12.7 Key Input Interrupt Pin Configuration

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input
$\overline{KI4}$	Input	$\overline{KI4}$ interrupt input
$\overline{KI5}$	Input	$\overline{KI5}$ interrupt input
$\overline{KI6}$	Input	$\overline{KI6}$ interrupt input
$\overline{KI7}$	Input	$\overline{KI7}$ interrupt input

12.5.1 Key Input Enable Register 0 (KIEN)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.5.2 Key Input Enable Register 1 (KIEN1)

Address 01FFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI7PL	KI7EN	KI6PL	KI6EN	KI5PL	KI5EN	KI4PL	KI4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI4EN	KI4 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI4PL	KI4 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI5EN	KI5 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI5PL	KI5 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI6EN	KI6 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI6PL	KI6 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI7EN	KI7 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI7PL	KI7 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN1 register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi (i = 0 or 1) register. This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi (i = 0 or 1) register. The AIERi bit in the AIERi register can be used to select the interrupt enabled or disabled. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **12.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 12.8 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged.

Table 12.8 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than listed above	Address indicated by RMADi register + 1

Notes:
1. Refer to the **12.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001).
   Chapter 4. Instruction Code/Number of Cycles contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 12.9 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

12.6.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER00	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER10	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi0	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

12.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

12.7 Interrupts of Timer RC, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)

The interrupts of timer RC, the synchronous serial communication unit, the I²C bus interface, and the flash memory each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 12.10 lists the Registers Associated with Interrupts of Timer RC, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory.

Table 12.10 Registers Associated with Interrupts of Timer RC, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory

Peripheral Function Name	Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC	TRCSR	TRCIER	TRCIC
Synchronous serial communication unit	SSSR	SSER	SSUIC
I²C bus interface	ICSR	ICIER	IICIC
Flash memory	RDYSTI (bit 0 of FST)	RDYSTIE (bit 7 of FMR0)	FMRDYIC
	BSYAEI (bit 1 of FST)	BSYAEIE (bit 6 of FMR0)	
		CMDERIE (bit 5 of FMR0)	

As with other maskable interrupts, the interrupts of timer RC, the synchronous serial communication unit, the I²C bus interface, and the flash memory are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**18. Timer RC**, **22. Synchronous Serial Communication Unit (SSU), 23. I²C bus Interface,** and **24. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **12.3 Interrupt Control**.

12.8 Notes on Interrupts

12.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0 (no interrupt requested).
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

12.8.2 SP Setting

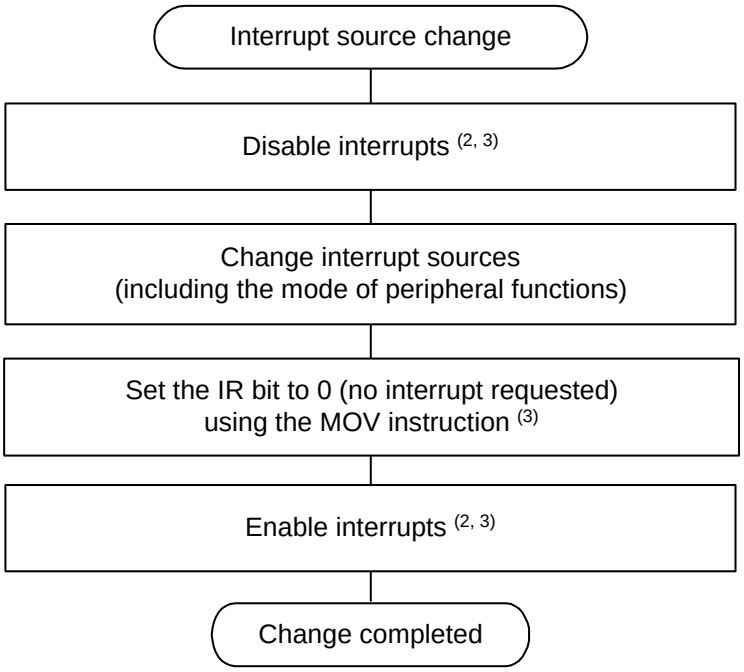
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

12.8.3 External Interrupt, Key Input Interrupt

Either the low-level width or high-level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$, and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to **Table 25.21 Timing Requirements of External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3, 5) and Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 7)**.

12.8.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 12.12 shows a Procedure Example for Changing Interrupt Sources.



IR bit: Bit in the interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt requested). Refer to **12.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 12.12 Procedure Example for Changing Interrupt Sources

12.8.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:
AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.
Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    POPC    FLG             ; Enable interrupts
```

13. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

13.1 Introduction

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 13.1 shows the ID Code Areas.

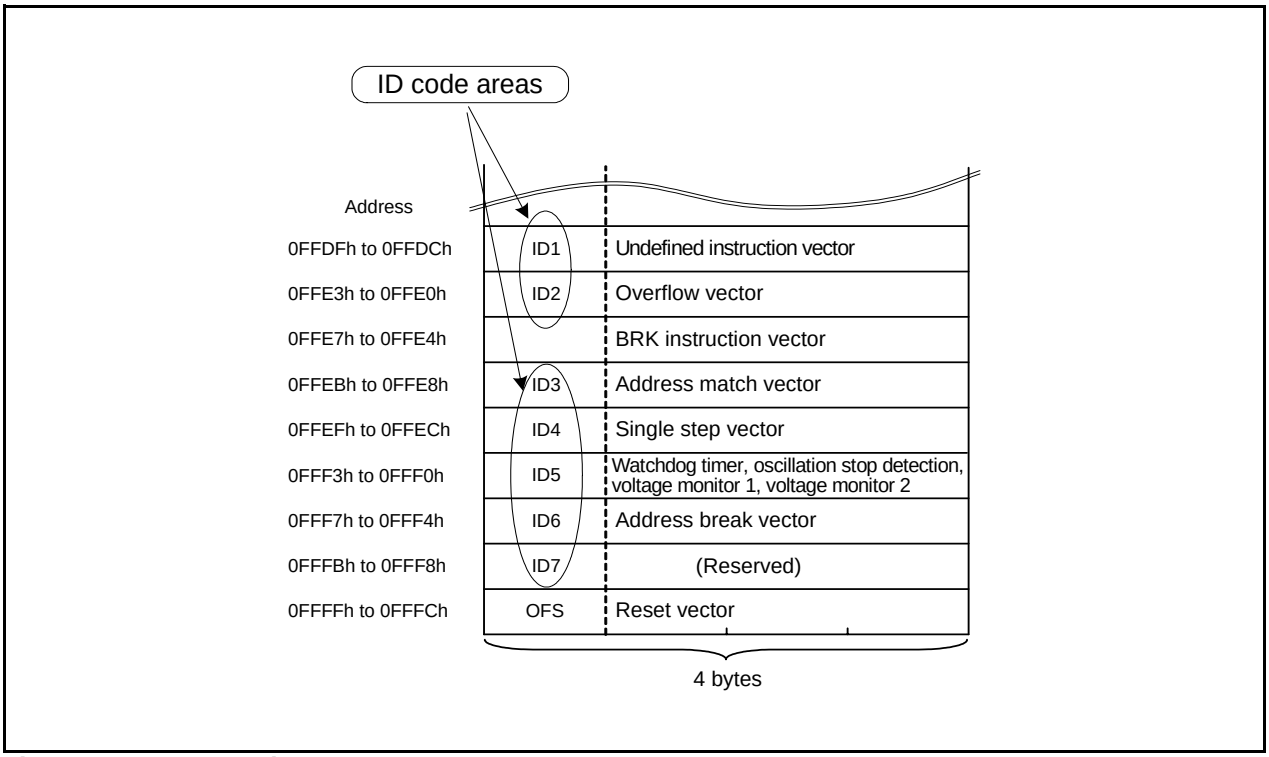


Figure 13.1 ID Code Areas

13.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 13.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 13.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 13.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. Reserve word:
   A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 13.1.

13.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 13.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 13.2 lists the Conditions and Operations of Forced Erase Function.
When the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 13.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	–	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID code match)
	Other than ALeRASE (1)	–	ID code check (ID code check function)

Note:
1. For “Protect”, refer to **13.4 Standard Serial I/O Mode Disabled Function**.

13.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 13.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.
Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or the parallel programmer.

13.5 Notes on ID Code Areas

13.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Option Function Select Area

14.1 Introduction

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-addresses, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 14.1 shows the Option Function Select Area.

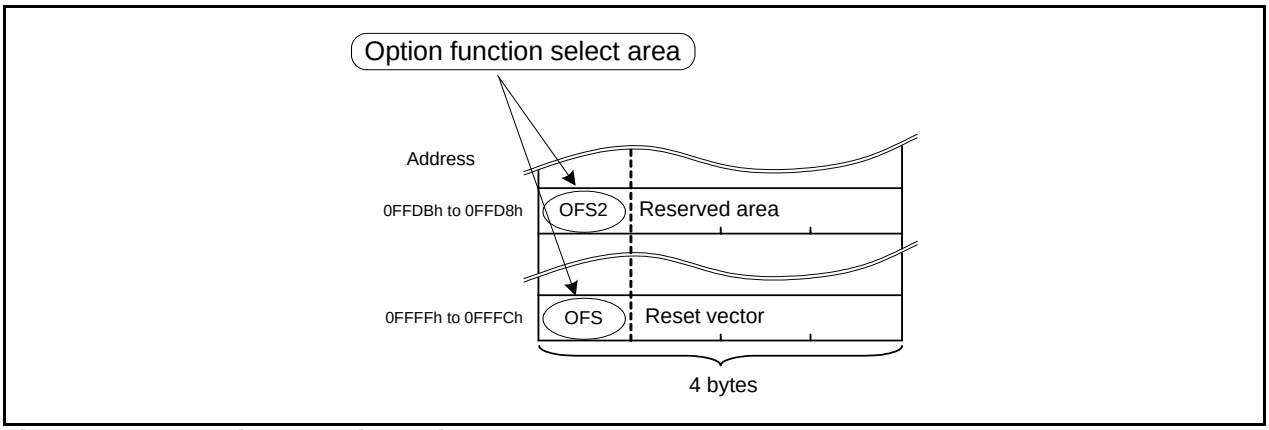


Figure 14.1 Option Function Select Area

14.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

14.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

14.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **14.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

14.3 Notes on Option Function Select Area

14.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h) ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

15. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

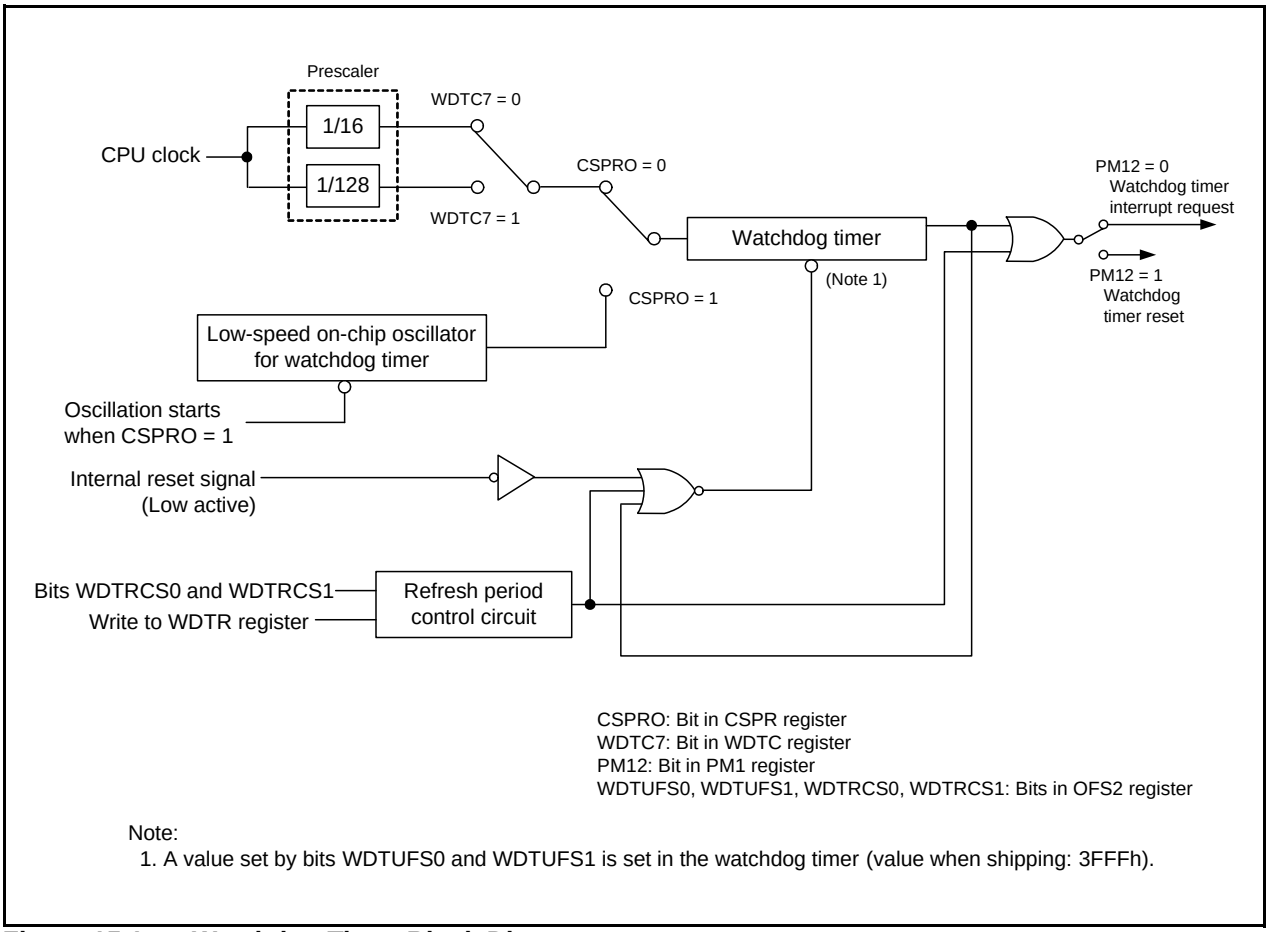
15.1 Introduction

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 15.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 15.1 shows the Watchdog Timer Block Diagram.

Table 15.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selectable by the WDTC7 bit in the WDTC register • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selectable by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.



Note:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).

Figure 15.1 Watchdog Timer Block Diagram

15.2 Registers

15.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

15.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh into this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

15.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

15.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
After Reset	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are 00b (03FFh): b5 to b0 01b (0FFFh): b7 to b2 10b (1FFFh): b8 to b3 11b (3FFFh): b9 to b4		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divide-by-16 1: Divide-by-128	R/W

15.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 1.

After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode selected	R/W

Note:
1. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts between writing 0 and writing 1.

15.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4	R/W
b5	VDSEL1		0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

15.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **14.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

15.3 Functional Description

15.3.1 Common Items for Multiple Modes

15.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 15.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

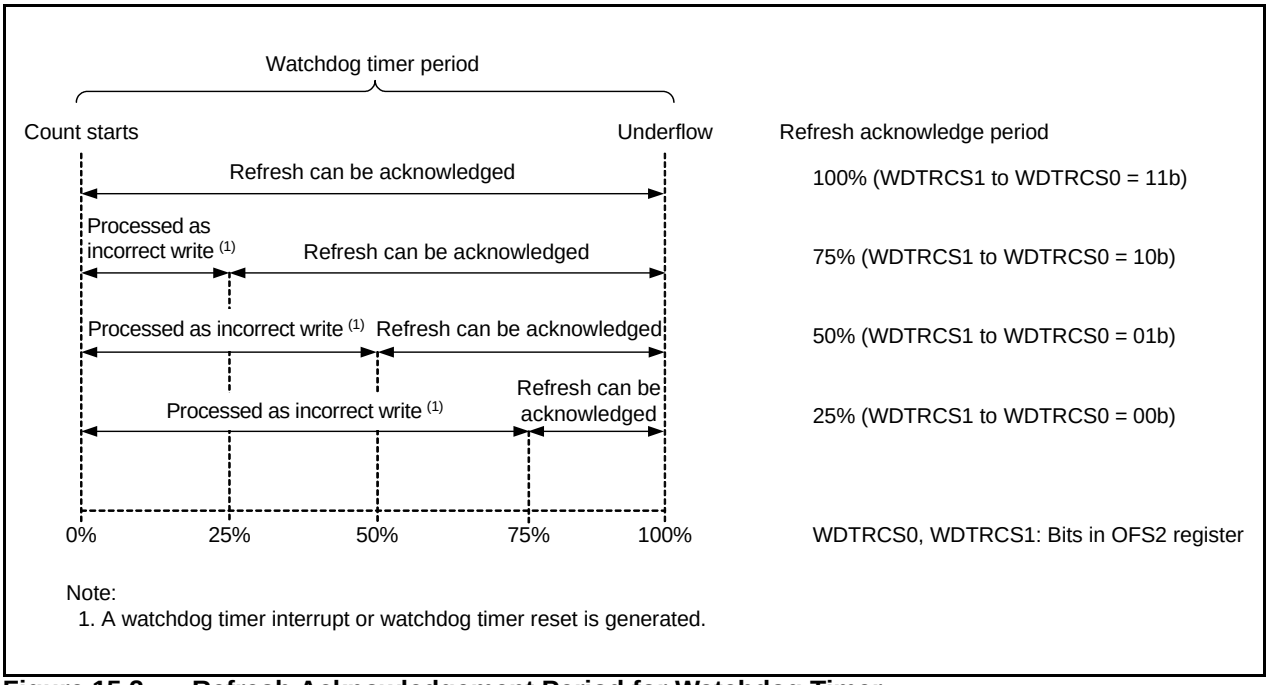


Figure 15.2 Refresh Acknowledgement Period for Watchdog Timer

15.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 15.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 15.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 13.1 ms when: - The CPU clock frequency is set to 20 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0. Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1. Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit in the OFS register cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 15.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 15.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode and stop mode once it starts.)
Operation at underflow	Watchdog timer reset (Refer to **5.5 Watchdog Timer Reset.**)
Registers, bits	• When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit in the OFS register cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

16. Timers

The following three types of four timers are available:

- Timer RB: Two 8-bit timer with an 8-bit prescalers
- Timer RC: 16-bit timer
- Timer RJ: A 16-bit timer

All these timers operate independently.

Table 16.1 Functional Comparison of Timers

Item		Timer RJ (0)	Timer RB (0)	Timer RB (1)	Timer RC
Configuration		16-bit timer (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)
Count		Decrement	Decrement	Decrement	Increment/Decrement
Count sources		• f1 • f2 • f8 • fOCO	• f1 • f2 • f8 • Timer RJ (0) underflow	• f1 • f2 • f8	• f1 • f2 • f4 • f8 • f32 • TRCCLK
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode	Timer mode (output compare function)
	Count of the external count source	Event counter mode	—	—	Timer mode (output compare function)
	External pulse width/period measurement	Pulse width measurement mode, pulse period measurement mode	—	—	Timer mode (input capture function; 4 pins)
	PWM output	Pulse output mode (1) Event counter mode (1)	Programmable waveform generation mode	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1) PWM mode (3 pins) PWM2 mode (1 pin)
	One-shot waveform output	—	Programmable one-shot generation mode Programmable wait one-shot generation mode	Programmable one-shot generation mode Programmable wait one-shot generation mode	PWM mode (3 pins)
Input pin		TRJ0IO	$\overline{\text{INT0}}$	$\overline{\text{INT5}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD
Output pin		TRJ0IO	TRB0O	TRB1O	TRCIOA, TRCIOB, TRCIOC, TRCIOD
Related interrupt		Timer RJ0 interrupt	Timer RB0 interrupt, $\overline{\text{INT0}}$ interrupt	Timer RB1 interrupt, $\overline{\text{INT5}}$ interrupt	Compare match/input capture A to D interrupt, Overflow interrupt, $\overline{\text{INT0}}$ interrupt
Timer stop		Provided	Provided	Provided	Provided

Note:

1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

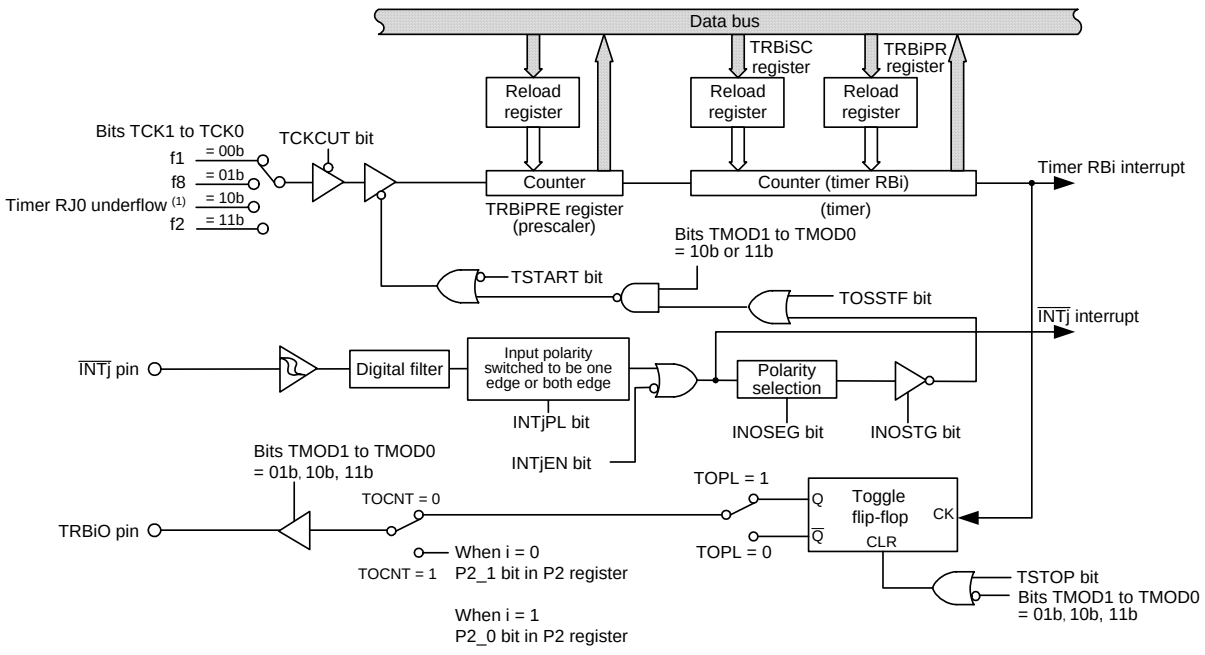
17. Timer RB

17.1 Introduction

Timer RB has two timers (RB0 and RB1).
Timer RB0 and timer RB1 are 8-bit timers with an 8-bit prescaler.
Timer RB has two 8-bit timers (timer RB0 and timer RB1) with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter (refer to **Tables 17.3 to 17.6 for the Specifications of Each Mode** for accessing the reload register and counter). Timer RBi (i = 0 or 1) has timer RBi primary and timer RBi secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 17.1 shows the Timer RBi Block Diagram. Table 17.1 lists the Timer RBi Pin Configuration.

Timer RB supports the four operating modes:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RJ0 underflows).
  Underflow of timer RJ0 cannot be selected as the count source for timer RB1.
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.



TSTART, TCSTF: Bits in TRBiCR register
TOSSTF: Bit in TRBiOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBiIOC register
TMOD0, TMOD1, TCK0, TCK1, TCKCUT: Bits in TRBiMR register

i = 0 or 1
j = 0 or 5

Note:
1. Underflow of timer RJ0 cannot be selected as the count source for timer RB1.

Figure 17.1 Timer RBi Block Diagram

Table 17.1 Timer RBi Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRBO	P2_1	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)
TRB1O	P2_0		

Table 17.2 Assigned $\overline{\text{INTj}}$ Pin and Internal Count Source for Each Timer RBi Channel (i = 0 or 1, j = 0 or 5)

Channel	$\overline{\text{INTj}}$ pin	Internal count source (Underflow)
Timer RB0	$\overline{\text{INT0}}$ pin	Timer RJ0
Timer RB1	$\overline{\text{INT5}}$ pin	—

17.2 Registers

17.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Reserved bit	Set to 1.	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (3)	R/W
b4	MSTTRJ1	Reserved bit	Set to 1.	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

17.2.2 Timer RBi Control Register (TRBiCR) (i = 0 or 1)

Address 0108h (TRB0CR), 0098h (TRB1CR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RBi count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RBi count status flag (1)	0: Count stops 1: During count operation (3)	R
b2	TSTOP	Timer RBi count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **17.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When 1 is written to the TSTOP bit, registers TRBiPRE, TRBiSC, TRBiPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBiOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, it indicates that a one-shot pulse trigger has been acknowledged.

17.2.3 Timer RBi One-Shot Control Register (TRBiOCR) (i = 0 or 1)

Address 0109h (TRB0OCR), 0099h (TRB1OCR),

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RBi one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, the content is 0.	R/W
b1	TOSSP	Timer RBi one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RBi one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is written to the TSTOP bit in the TRBiCR register, the TOSSTF bit is set to 0.

The TRBiOCR register is enabled when bits TMOD1 to TMOD0 in the TRBiMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

17.2.4 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1)

Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RBi output enable bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

17.2.5 Timer RBi Mode Register (TRBiMR) (i = 0 or 1)

Address 010Bh (TRB0MR), 009Bh (TRB1MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RBi operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RBi write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RBi count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RJ0 underflow (3) 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RBi count source cutoff bit (1)	0: Count source provided 1: Count source cut off	R/W

Notes:
1. Change bits TMOD0 and TMOD1, TCK0 and TCK1, and TCKCUT when both the TSTART and TCSTF bits in the TRBiCR register are set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
3. To use the underflow signal of timer RJ0 as the count source for timer RB0, set timer RJ0 in timer mode, pulse output mode, or event counter mode. Underflow of timer RJ0 cannot be selected as the count source for timer RB1.

17.2.6 Timer RBi Prescaler Register (TRBiPRE) (i = 0 or 1)

Address 010Ch (TRB0PRE), 009Ch (TRB1PRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RJ0 underflows. (1)	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

Note:
1. Underflow of timer RJ0 cannot be selected as the count source for timer RB1.

When 1 is written to the TSTOP bit in the TRBiCR register, the TRBiPRE register is set to FFh.

17.2.7 Timer RBi Secondary Register (TRBiSC) (i = 0 or 1)

Address 010Dh (TRB0SC), 009Dh (TRB1SC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RBi prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RBi prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBiPR and TRBiSC are reloaded to the counter alternately and counted.
2. The count value can be read by reading the TRBiPR register even when the secondary period is being counted.

When 1 is written to the TSTOP bit in the TRBiCR register, the TRBiSC register is set to FFh.
To write to the TRBiSC register, perform the following steps.
(1) Write the value into the TRBiSC register.
(2) Write the value into the TRBiPR register. (If the value does not change, write the same value second time.)

17.2.8 Timer RBi Primary Register (TRBiPR) (i = 0 or 1)

Address 010Eh (TRB0PR), 009Eh (TRB1PR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RBi prescaler underflows.	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RBi prescaler underflows. (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RBi prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RBi prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBiPR and TRBiSC are reloaded to the counter alternately and counted.

When 1 is written to the TSTOP bit in the TRBiCR register, the TRBiPR register is set to FFh.

17.3 Timer Mode

In timer mode, a internally generated count source or timer RJ0 underflows are counted (refer to **Table 17.3**). Registers TRBiOCR and TRBiSC are not used in this mode.
Underflow of timer RJ0 cannot be selected as the count source for timer RB1.

Table 17.3 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJ0 underflow (1)
Count operations	• Decrement • When the timer underflows, it reloads the reload register content before the count continues (when timer RBi underflows, the content of timer RBi primary reload register is reloaded).
Division ratio	1/(n+1)(m+1) n: Value set in TRBiPRE register, m: Value set in TRBiPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	When timer RBi underflows [timer RBi interrupt].
TRBiO pin function	Programmable I/O port
$\overline{\text{INTi}}$ pin function	Programmable I/O port or $\overline{\text{INTi}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE.
Write to timer	• When registers TRBiPRE and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE and TRBiPR are written during count operation: If the TWRC bit in the TRBiMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **17.3.2 Timer Write Control during Count Operation**.)

Note:
1. Underflow of timer RJ0 cannot be selected for timer RB1.

i = 0 or 1, j = 0 or 5

17.3.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Timer Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

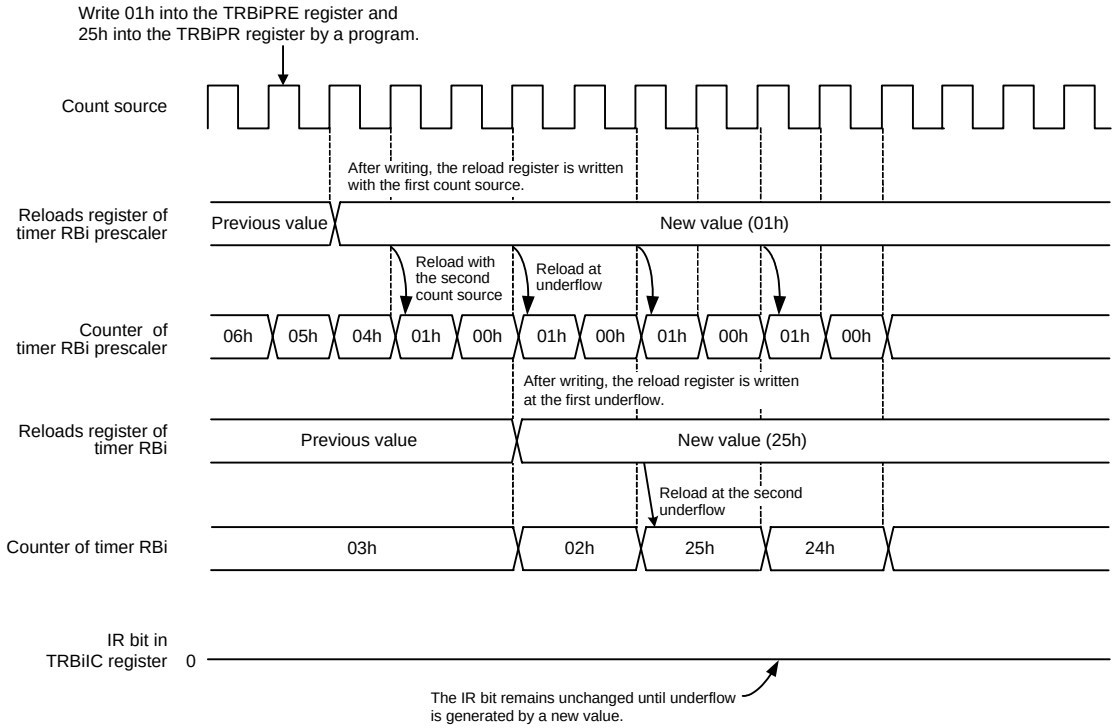
Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RBi output enable bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

17.3.2 Timer Write Control during Count Operation

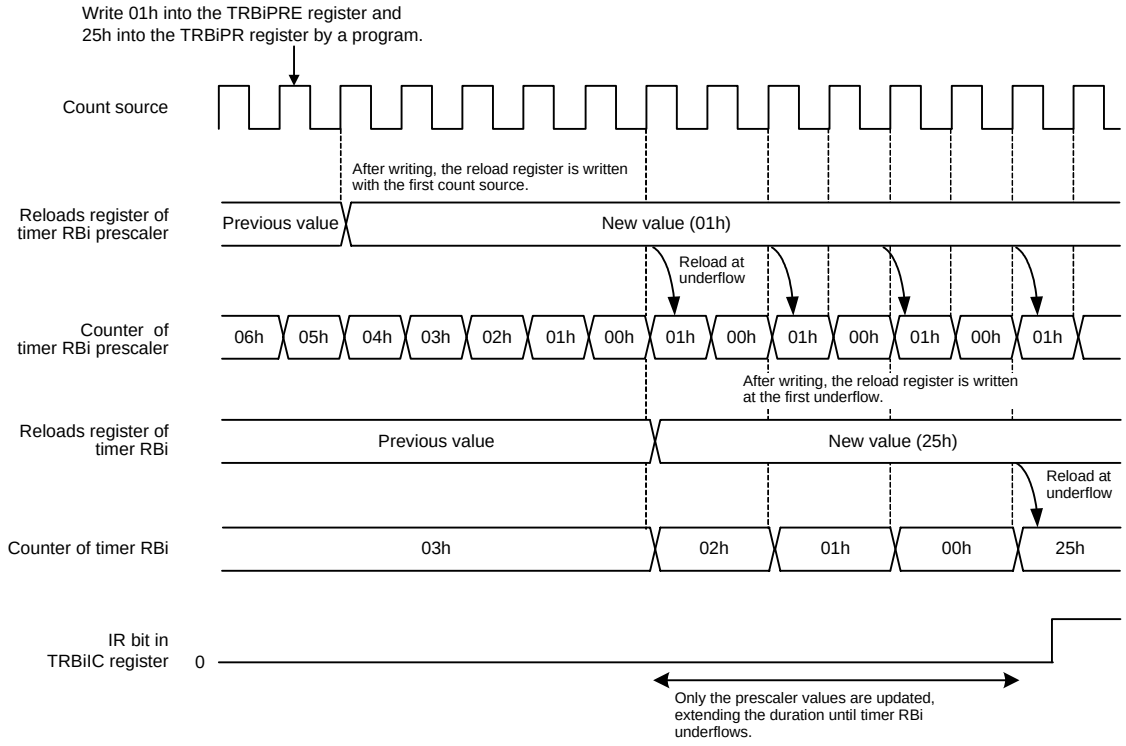
Timer RBi (i = 0 or 1) has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBiMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. If the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted when the prescaler value changes. Figure 17.2 shows an Operating Example of Timer RBi when Counter Value is Rewritten during Count Operation.

When the TWRC bit in the TRBiMR register is set to 0 (write to reload register and counter)



When the TWRC bit in the TRBiMR register is set to 1 (write to reload register only)



The above applies under the following condition:
Both the TSTART and TCSTF bits in the TRBiCR register are set to 1 (during count operation).

i = 0 or 1

Figure 17.2 Operating Example of Timer RBi when Counter Value is Rewritten during Count Operation

17.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBiO pin is inverted each time the counter underflows, while the values in registers TRBiPR (i = 0 or 1) and TRBiSC are counted alternately (refer to **Table 17.4**). Counting starts by counting the setting value of the TRBiPR register. The TRBiOCR register is unused in this mode.
Figure 17.3 shows an Operating Example in Timer RBi in Programmable Waveform Generation Mode.

Table 17.4 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJ0 underflow (1)
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Frequency of count source n: Value set in TRBiPRE register m: Value set in TRBiPR register p: Value set in TRBiSC register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RBi underflows during the secondary period (at the same time as the TRBiO output change) [timer RBi interrupt]
TRBiO pin function	Programmable output port or pulse output
$\overline{\text{INTj}}$ pin function	Programmable I/O port or $\overline{\text{INTj}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE (2).
Write to timer	• When registers TRBiPRE, TRBiSC, and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE, TRBiSC, and TRBiPR are written to during count operation, values are written to the reload registers only. (3)
Selectable function	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBiIOC register. • Waveform output enable function The timer RB waveform output enabled is selected by the TOCNT bit in the TRBiIOC register. (4)

Notes:
1. Underflow of timer RJ0 cannot be selected for timer RB1.
2. Even when the secondary period is being counted, the TRBiPR register may be read.
3. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBiPR register.
4. The value written to the TOCNT bit is enabled by the following.
   • When count starts.
   • When a timer RBi interrupt request is generated.
   The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

i = 0 or 1, j = 0 or 5

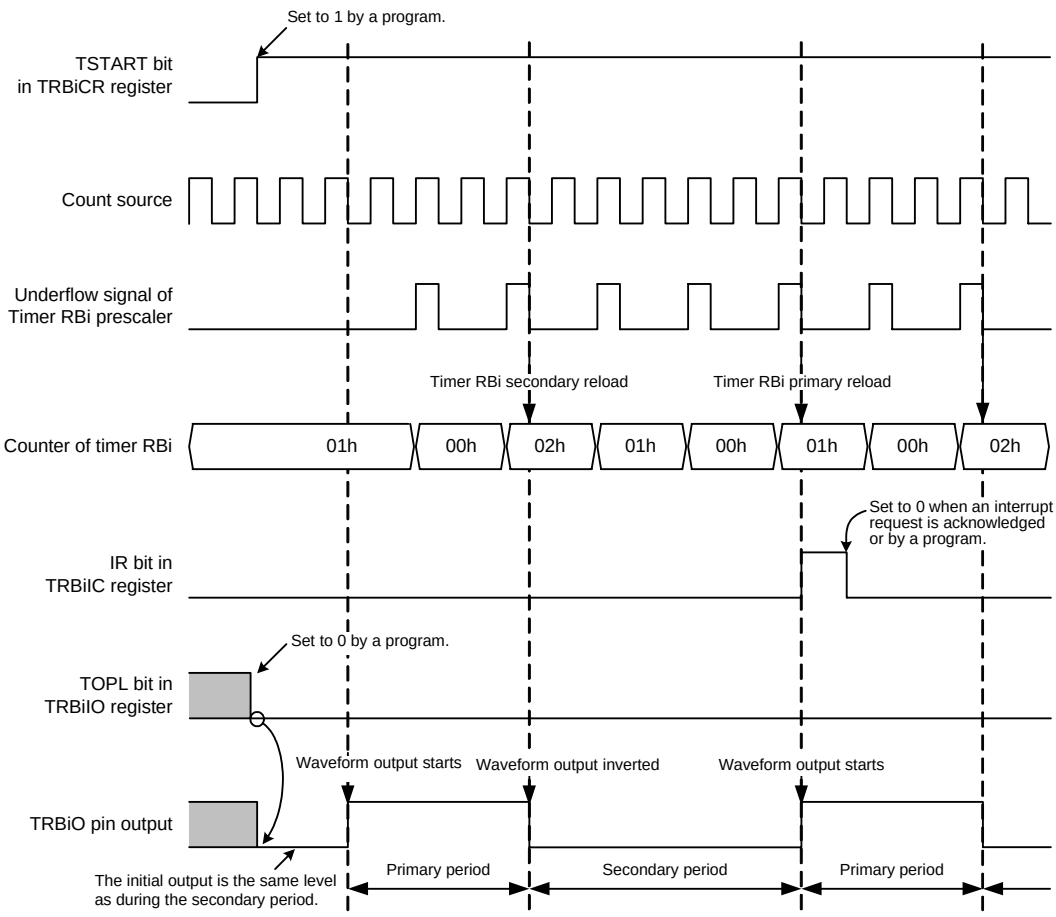
17.4.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Programmable Waveform Generation Mode

Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	0: High-level output for the primary period, low-level output for the secondary period Low-level output when the timer is stopped 1: Low-level output for the primary period, high-level output for the secondary period High-level output when the timer is stopped	R/W
b1	TOCNT	Timer RBi output enable bit	0: Timer RB waveform output enabled 1: Timer RB waveform output disabled	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

17.4.2 Operating Example



The above applies under the following conditions:

TRBiPRE = 01h, TRBiPR = 01h, TRBiSC = 02h
TOCNT in TRBiIOC register = 0 (timer RBi waveform output from the TRBiO pin)

i = 0 or 1

Figure 17.3 Operating Example in Timer RBi in Programmable Waveform Generation Mode

17.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBiO (i = 0 or 1) pin by a program or an external trigger input (input to the $\overline{\text{INTj}}$ (j = 0 or 5) pin) (refer to **Table 17.5**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBiPR register. The TRBiSC register is not used in this mode.
Figure 17.4 shows an Operating Example in Programmable One-Shot Generation Mode.

Table 17.5 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJ0 underflow (1)
Count operations	• The setting value of the TRBiPR register is decremented. • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the content of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Frequency of count source n: Value set in TRBiPRE register, m: Value set in TRBiPR register
Count start conditions	• The TSTART bit in the TRBiCR register is set to 1 (count starts) and the next trigger is generated. • 1 (one-shot starts) is written to the TOSST bit in the TRBiOCR register. • Trigger input to the $\overline{\text{INTj}}$ pin
Count stop conditions	• When reloading completes after timer RBi underflows during the primary period • 1 (one-shot stops) is written to the TOSSP bit in the TRBiOCR register. • 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the waveform output from the TRBiO pin ends) [timer RBi interrupt]
TRBiO pin function	Pulse output
$\overline{\text{INTj}}$ pin functions	• When the INOSTG bit in the TRBiIOC register is set to 0 ($\overline{\text{INTj}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INTj}}$ (j = 0 or 5) interrupt input • When the INOSTG bit in the TRBiIOC register is set to 1 ($\overline{\text{INTj}}$ one-shot trigger enabled): external trigger ($\overline{\text{INTj}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE.
Write to timer	• When registers TRBiPRE and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE and TRBiPR are written during count operation, values are written to the reload register only (2).
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBiIOC register. • One-shot trigger select function Refer to **17.5.3 One-Shot Trigger Selection**.

Notes:
1. Underflow of timer RJ0 cannot be selected for timer RB1.
2. The set value is reflected at the following one-shot pulse after writing to the TRBiPR register.

i = 0 or 1, j = 0 or 5

17.5.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Programmable One-Shot Generation Mode

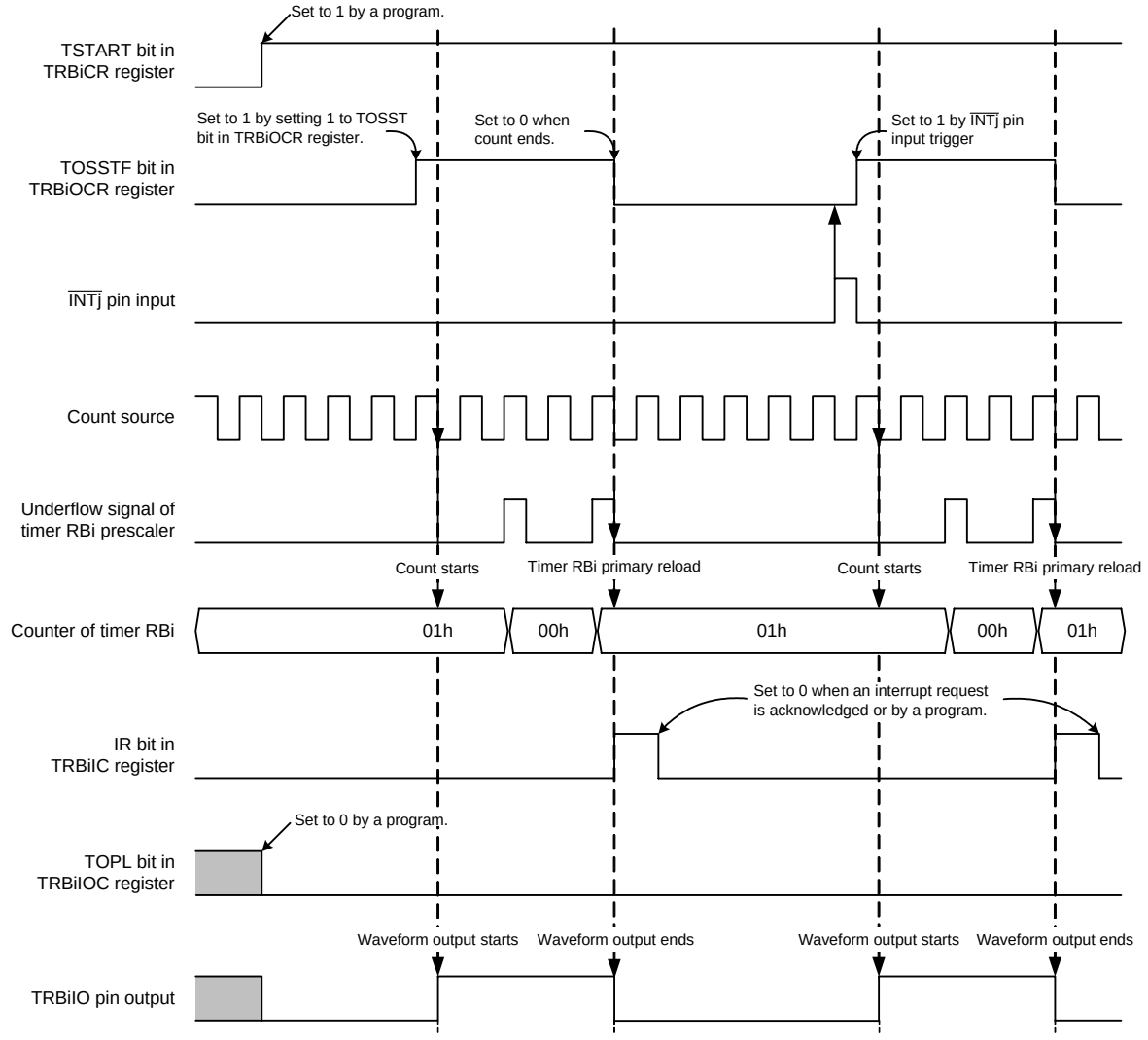
Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	0: High-level output of a one-shot pulse, low-level output when the timer is stopped 1: Low-level output of a one-shot pulse, high-level output when the timer is stopped	R/W
b1	TOCNT	Timer RBi output enable bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger disabled (2) 1: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger enabled (2)	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **17.5.3 One-Shot Trigger Selection**.
2. A one-shot trigger is input from the $\overline{\text{INT0}}$ pin for timer RB0 and the $\overline{\text{INT5}}$ pin for timer RB1.

17.5.2 Operating Example



The above applies under the following conditions:

TRBiPRE = 01h, TRBiPR = 01h
TOPL in TRBiIOC register = 0, TOCNT = 0
INOSTG = 1 (INTj one-shot trigger enabled)
INOSEG = 1 (edge trigger at the rising edge)

i = 0 or 1
j = 0 or 5

Figure 17.4 Operating Example in Programmable One-Shot Generation Mode

17.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBiCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:
- 1 is written to the TOSST bit in the TRBiOCR register by a program.
- Trigger input from the $\overline{\text{INTj}}$ (j = 0 or 5) pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBiOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INTj}}$ pin, input the trigger after making the following settings:

(1) When i = $\overline{\text{INT0}}$
- Set the port direction bit in the port direction register corresponding to the $\overline{\text{INT0}}$ pin to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F0 and INT0F1 in the INTF register.
- Set the INT0PL bit in the INTEN register to 0 (one edge) and set the POL bit in the INT0IC register to 0 (falling edge). Furthermore, set the INOSEG bit in the TRB0IOC register to select a falling or rising edge.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRB0IOC register to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled).

(2) When i = $\overline{\text{INT5}}$
- Set the port direction bit in the port direction register corresponding to the $\overline{\text{INT5}}$ pin to 0 (input mode).
- Select the $\overline{\text{INT5}}$ digital filter with bits INT5F0 and INT5F1 in the INTF1 register.
- Set the INT5PL bit in the INTEN1 register to 0 (one edge) and set in the POL bit in the INT5IC register to 0 (falling edge). Furthermore, set the INOSEG bit in the TRB1IOC register to select a falling or rising edge.
- Set the INT5EN bit in the INTEN1 register to 0 (enabled).
- After completing the above, set the INOSTG bit in the TRB1IOC register to 1 ($\overline{\text{INT5}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INTj}}$ pin.
- Processing to handle the interrupts is required. Refer to **12. Interrupts**, for details.
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INTjIC register changes.

17.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBiO (i = 0 or 1) pin by a program or an external trigger input (input to the $\overline{\text{INTj}}$ (j = 0 or 5) pin) (refer to **Table 17.6**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value of the TRBiSC register after waiting for a given length of time equal to the setting value of the TRBiPR register. Figure 17.5 shows an Operating Example in Programmable Wait One-Shot Generation Mode.

Table 17.6 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJ0 underflow (1)
Count operations	• The setting value of the timer RBi primary is decremented. • When a count of the timer RBi primary underflows, the timer reloads the contents of timer RBi secondary before the count continues. • When a count of the timer RBi secondary underflows, the timer reloads the contents of timer RBi primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the content of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Frequency of count source n: Value set in TRBiPRE register, m: Value set in TRBiPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Frequency of count source n: Value set in TRBiPRE register, p: Value set in TRBiSC register
Count start conditions	• The TSTART bit in the TRBiCR register is set to 1 (count starts) and the next trigger is generated. • 1 (one-shot starts) is written to the TOSST bit in the TRBiOCR register. • Trigger input to the $\overline{\text{INTj}}$ pin
Count stop conditions	• When reloading completes after timer RBi underflows during the secondary period. • 1 (one-shot stops) is written to the TOSSP bit in the TRBiOCR register. • 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	In half a cycle of the count source after timer RBi underflows during secondary period (at the same time as the waveform output from the TRBiO pin ends) [timer RBi interrupt].
TRBiO pin function	Pulse output
$\overline{\text{INTj}}$ pin functions	• When the INOSTG bit in the TRBiIOC register is set to 0 ($\overline{\text{INTj}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INTj}}$ interrupt input • When the INOSTG bit in the TRBiIOC register is set to 1 ($\overline{\text{INTj}}$ one-shot trigger enabled): external trigger ($\overline{\text{INTj}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE.
Write to timer	• When registers TRBiPRE, TRBiSC, and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE, TRBiSC, and TRBiPR are written during count operation, values are written to the reload registers only. (2)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBiIOC register. • One-shot trigger select function Refer to **17.5.3 One-Shot Trigger Selection**.

Notes:
1. Underflow of timer RJ0 cannot be selected for timer RB1.
2. The set value is reflected at the following one-shot pulse after writing to registers TRBiSC and TRBiPR.

i = 0 or 1, j = 0 or 5

17.6.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Programmable Wait One-Shot Generation Mode

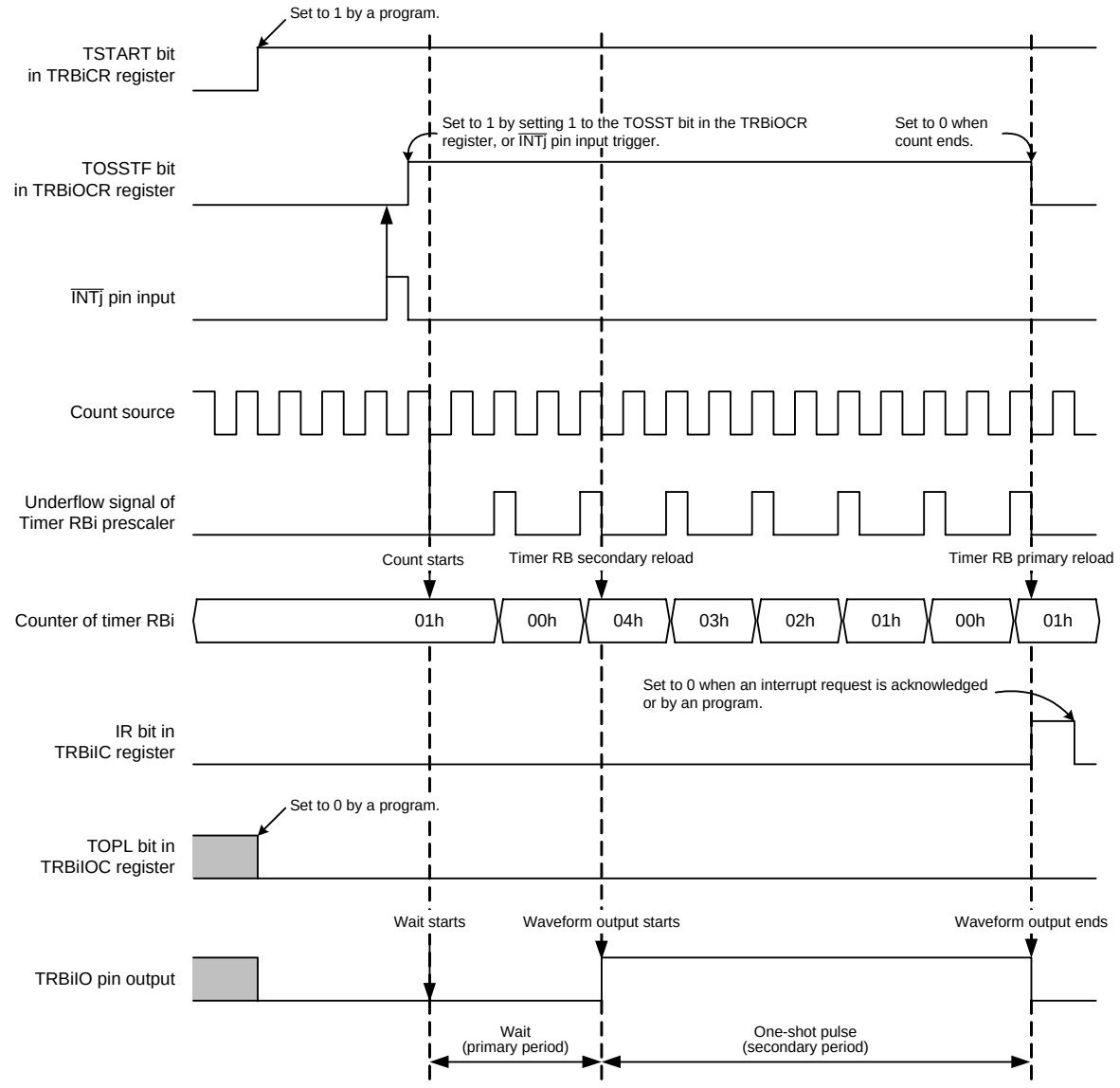
Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	0: High-level output of a one-shot pulse, low-level output when the timer stops or during wait 1: Low-level output of a one-shot pulse, low-level output when the timer stops or during wait	R/W
b1	TOCNT	Timer RBi output enable bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger disabled (2) 1: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger enabled (2)	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **17.5.3 One-Shot Trigger Selection**.
2. A one-shot trigger is input from the $\overline{\text{INT0}}$ pin for timer RB0 and the $\overline{\text{INT5}}$ pin for timer RB1.

17.6.2 Operating Example



The above applies under the following conditions:

TRBiPRE = 01h, TRBiPR = 01h, TRBiSC = 04h
INOSTG = 1 (INTj one-shot trigger enabled)
INOSEG = 1 (edge trigger at the rising edge)

i = 0 or 1
j = 0 or 5

Figure 17.5 Operating Example in Programmable Wait One-Shot Generation Mode

17.7 Notes on Timer RB

- Timer RBi stops counting after a reset. Set the values in the timer RBi and timer RBi prescalers before the count starts.
- Even if the prescaler and timer RBi is read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBiCR register to 0 (count stops) or setting the TOSSP bit in the TRBiOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for one or two cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit. Timer RB starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 (during count operation) for one or two cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RBi counting is stopped when the TCSTF bit is set to 0 (count stops).
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RBi:
     TRBiCR, TRBiOCR, TRBiIOC, TRBiMR, TRBiPRE, TRBiSC, and TRBiPR

- When the TSTOP bit in the TRBiCR register is set to 1 during timer operation, timer RBi stops immediately.
- When 1 is written to the TOSST or TOSSP bit in the TRBiOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. When 1 is written to the TOSSP bit during the period between when 1 is written to the TOSST bit and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, when 1 is written to the TOSST bit during the period between when 1 is written to the TOSSP bit and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RJ0 as the count source for timer RB0, set timer RJ0 in timer mode, pulse output mode, or event counter mode. Underflow of timer RJ0 cannot be selected as the count source for timer RB1.

17.7.1 Timer Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR register (i = 0 or 1) is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

17.7.2 Programmable Waveform Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

17.7.3 Programmable One-Shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

17.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

18.1 Introduction

Timer RC uses f1 as its operating clock. Table 18.1 lists the Timer RC Operating Clocks.

Table 18.1 Timer RC Operating Clocks

Condition	Timer RC Operating Clock
The count source is f1, f2, f4, f8, f32, or TRCCLK input. (Bits TCK2 to TCK0 in the TRCCR1 register are set to 000b to 101b.)	f1

Table 18.2 lists the Timer RC Pin Configuration. Figure 18.1 shows the Timer RC Block Diagram.

Timer RC supports the following three modes:

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — A match between the values of a counter and a register is detected. (Pin output can be changed at detection.)

The following two modes use the output compare function:

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

For the input capture function, the output compare function, and in PWM mode, settings may be selected independently for each pin.
In PWM2 mode, waveforms are output based on a combination of the counter or the register.

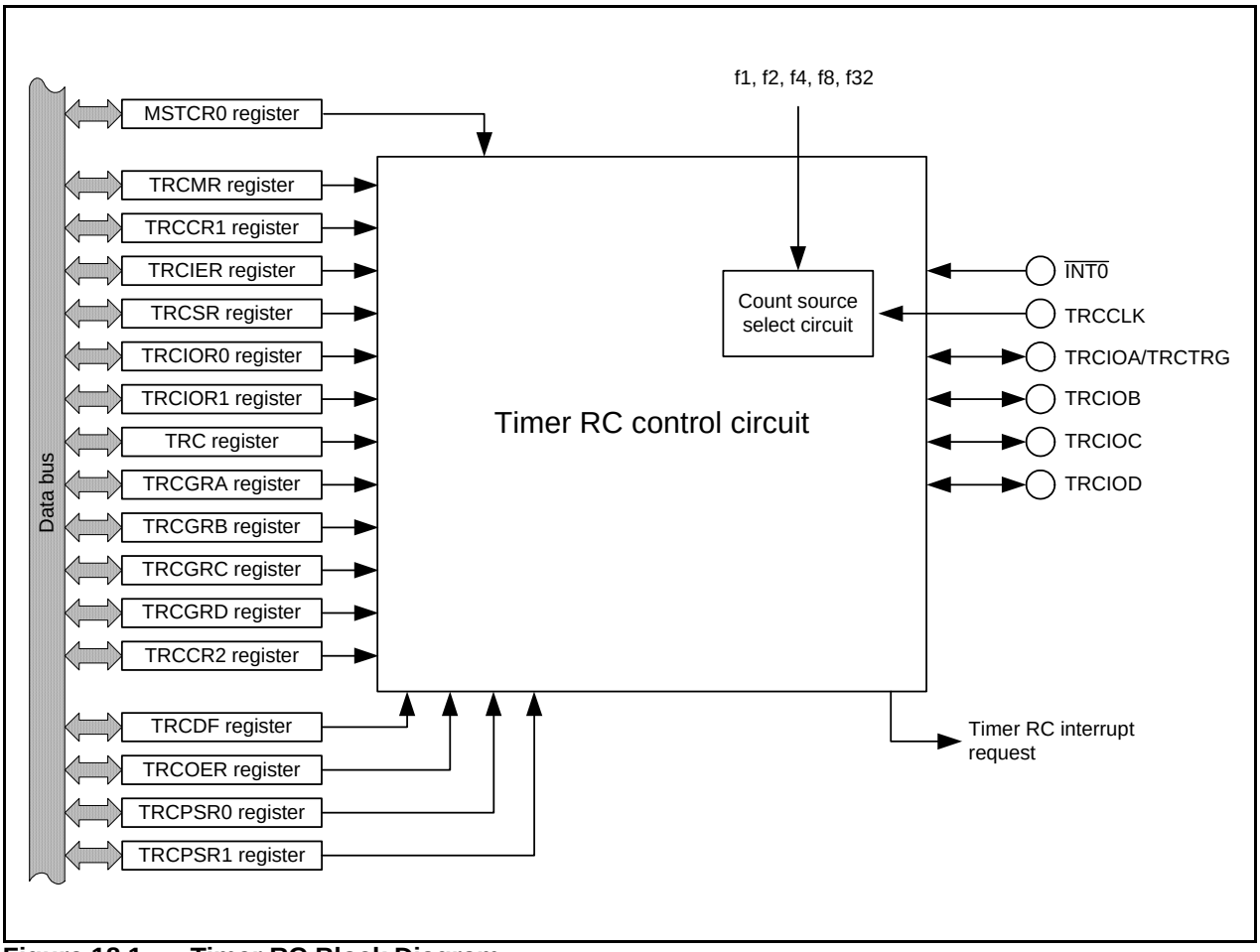


Figure 18.1 Timer RC Block Diagram

Table 18.2 Timer RC Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P8_7	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCIOB	P8_6, P8_5, or P8_4		
TRCIOC	P8_5		
TRCIOD	P8_4		
TRCCLK	P7_1	Input	External clock input
TRCTRG	P8_7	Input	PWM2 mode external trigger input

18.2 Registers

Table 18.3 lists the Registers Associated with Timer RC.

Table 18.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR0	Valid	Valid	Valid	Valid	18.2.1 Module Standby Control Register 0 (MSTCR0)
0120h	TRCMR	Valid	Valid	Valid	Valid	18.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 18.2.3 Timer RC Control Register 1 (TRCCR1) 18.5.1 Timer RC Control Register 1 (TRCCR1) in Timer Mode (Output Compare Function) 18.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 18.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	18.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	18.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	–	–	Timer RC I/O control register 0, timer RC I/O control register 1 18.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 18.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 18.4.1 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Input Capture Function) 18.4.2 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Input Capture Function) 18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Output Compare Function) 18.5.3 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Output Compare Function)
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	18.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	18.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	–	Valid	Valid	Valid	18.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	–	–	Valid	18.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	–	Valid	Valid	Valid	18.2.12 Timer RC Output Master Enable Register (TRCOER)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	18.2.13 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	18.2.14 Timer RC Pin Select Register 1 (TRCPSR1)

–: Invalid

18.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	—	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	Reseved bit	Set to 1.	R/W
b2	—	Reseved bit	Set to 0.	R/W
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTLCD	Reseved bit	Set to 1.	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	Reseved bit	Set to 1.	R/W

Notes:

1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

18.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on the TRCMR register in PWM2 mode, refer to **18.9.5 TRCMR Register in PWM2 Mode**.

18.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: TRC counter cleared by input capture or by compare match with the TRCGRA register	R/W

Note:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).

18.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by IMFD bit enabled	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W

18.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading. (1) [Condition for setting to 1] Refer to **Table 18.4 Conditions for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input-capture/compare-match flag B		R/W
b2	IMFC	Input-capture/compare-match flag C		R/W
b3	IMFD	Input-capture/compare-match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Condition for setting to 0] Write 0 after reading. (1) [Condition for setting to 1] Refer to **Table 18.4 Conditions for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it.)
   - The bit's value remains unchanged if 1 is written to it.

Table 18.4 Conditions for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input Capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in registers TRCIOR0 and TRCIOR1.
2. Includes the condition that bits BFC and BFD in the TRCMR register are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

18.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA input pin	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in PWM mode and PWM2 mode.

18.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in PWM mode and PWM2 mode.

18.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Counts a count source. Count operation is increment. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

18.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB),
012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

18.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

18.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)	0: Function is not used 1: Function is used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Digital filter function clock select bit (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

18.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOA pin functions as a programmable I/O port)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOB pin functions as a programmable I/O port)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOC pin functions as a programmable I/O port)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOD pin functions as a programmable I/O port)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (output disabled) when a low or high-level signal is applied to the $\overline{\text{INT0}}$ pin depending on POL bit in INT0IC register.)	R/W

Note:
1. These bits are disabled for pins set as input-capture input.

18.2.13 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	TRCIOASEL1	TRCIOASEL0	—	TRCCLKSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCCLKSEL0	TRCCLK pin select bit	0: TRCCLK pin not used 1: P7_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b3 b2 0 0: TRCIOA/TRCTRG pin not used 0 1: TRCIOA/TRCTRG pin assigned to P8_7 1 0: Do not set. 1 1: Do not set.	R/W
b3	TRCIOASEL1			R/W
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P8_6 assigned 1 0: P8_5 assigned (1) 1 1: P8_4 assigned (2)	R/W
b5	TRCIOBSEL1			R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. When the TRCIOCSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOC pin assigned to P8_5), P8_5 functions as the TRCIOC pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.
2. When the TRCIODSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOD pin assigned to P8_4), P8_4 functions as the TRCIOD pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.

The TRCPSR0 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation. If the assignment of the timer RC pins is changed, an edge may occur depending on the changed pin level, causing the TRC register to be set to 0000h.

18.2.14 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TRCIODSEL0	—	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	0: TRCIOC pin not used 1: P8_5 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	TRCIODSEL0	TRCIOD pin select bit	0: TRCIOD pin not used 1: P8_4 assigned	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

The TRCPSR1 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

18.3 Common Items for Multiple Modes

18.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 18.5 lists the Count Source Selection, and Figure 18.2 shows the Count Source Block Diagram.

Table 18.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in TRCCR1 register
External signal input to TRCCLK pin	• Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) • The corresponding direction bit in the direction register is set is set to 0 (input mode)

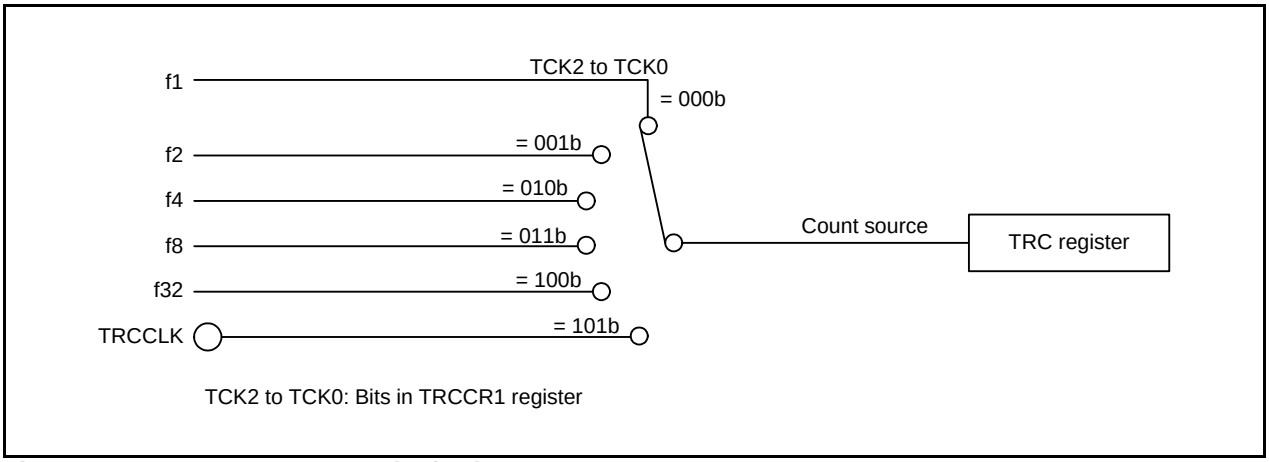


Figure 18.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be set to three cycles or more of the timer RC operation clock. (See **Table 18.1 Timer RC Operating Clocks.**)

18.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register of the TRCGRA or TRCGRB register.

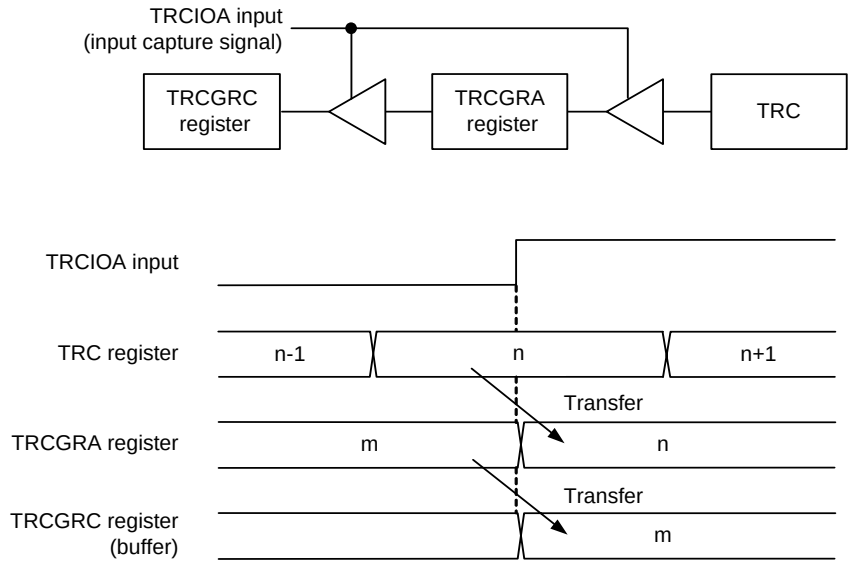
- Buffer register of TRCGRA register: TRCGRC register
- Buffer register of TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 18.6 lists the Buffer Operation in Each Mode, Figure 18.3 shows the Buffer Operation of Input Capture Function, and Figure 18.4 shows the Buffer Operation of Output Compare Function.

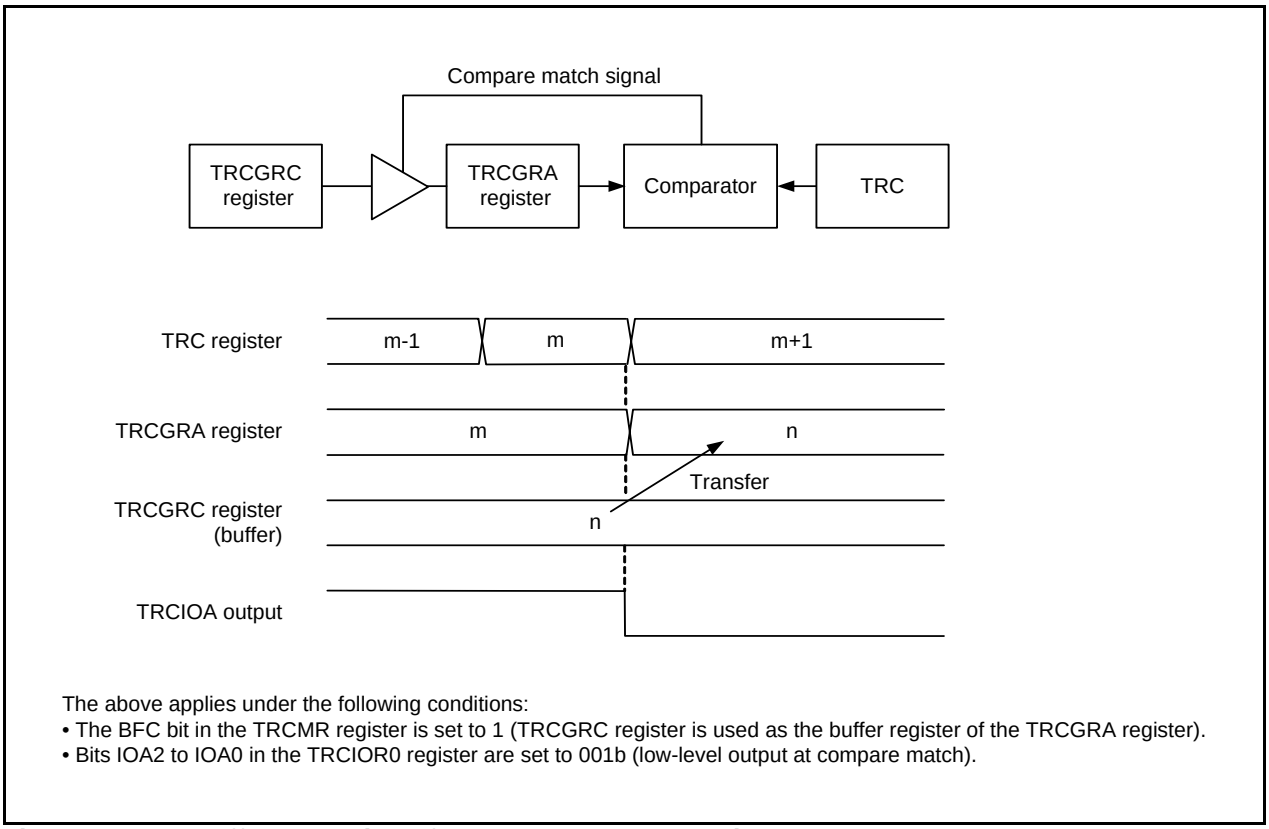
Table 18.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	The content of the TRCGRA (TRCGRB) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRC register and the TRCGRA (TRCGRB) register	The content of the buffer register is transferred to the TRCGRA (TRCGRB) register.
PWM2 mode	• Compare match between the TRC register and the TRCGRA register • TRCTRG pin trigger input	The content of the buffer register (TRCGRD) is transferred to the TRCGRB register.



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 100b (input capture at the rising edge).

Figure 18.3 Buffer Operation of Input Capture Function



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 001b (low-level output at compare match).

Figure 18.4 Buffer Operation of Output Compare Function

Make the following settings in timer mode.
- To use the TRCGRC register as the buffer register of the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register of the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

When the TRCGRC or TRCGRD register is also used as the buffer register for the output compare function, in PWM mode, or PWM2 mode, the IMFC or IMFD bit in the TRCSR register is set to 1 by a compare match with the TRC register.
When the TRCGRC register or TRCGRD register is also used as the buffer register for the input capture function, the IMFC or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC or TRCIOD pin.

18.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is determined when three matches occur. The digital filter function and sampling clock can be selected using the TRCDF register. Figure 18.5 shows a Block Diagram of Digital Filter.

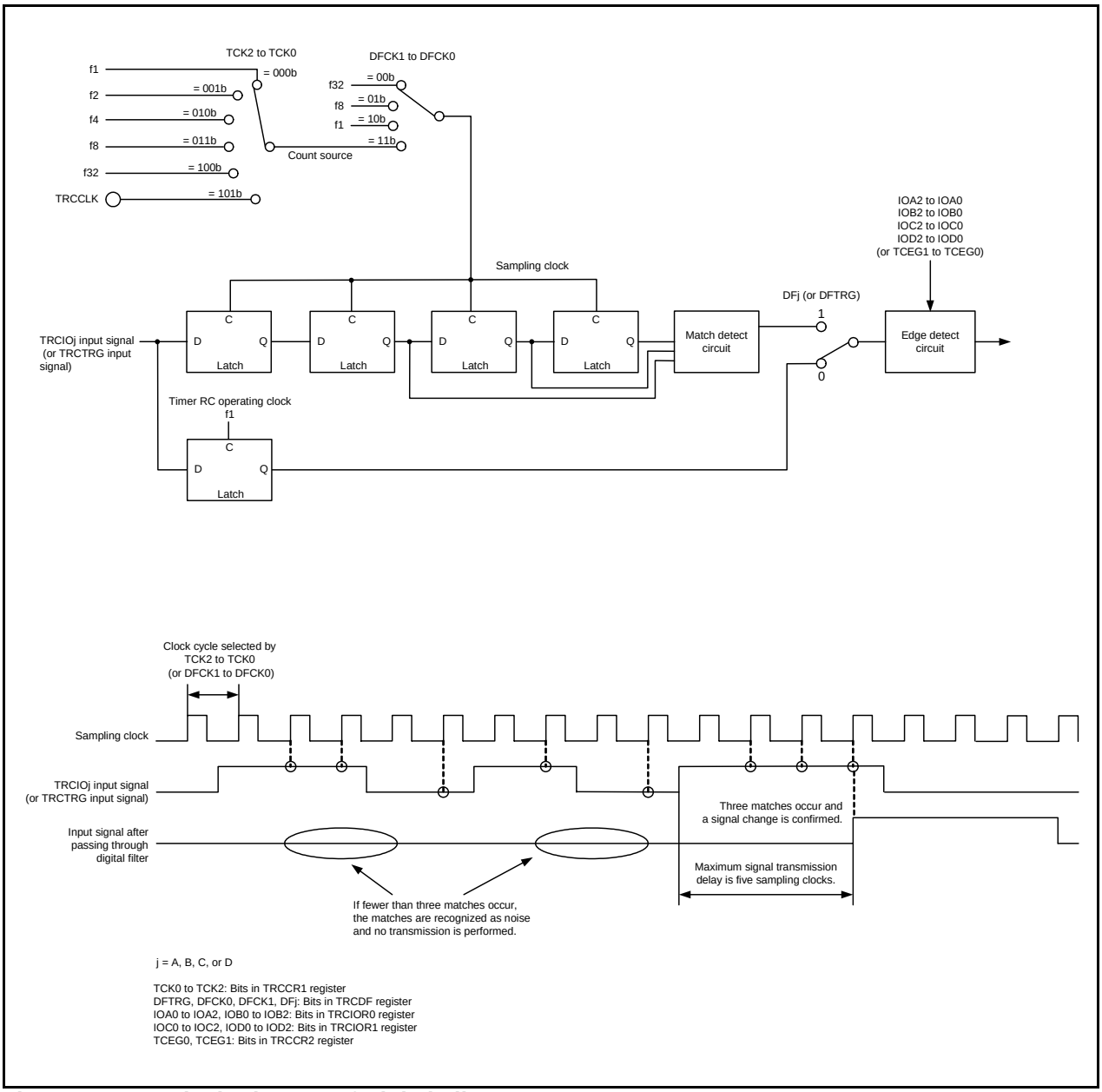


Figure 18.5 Block Diagram of Digital Filter

18.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, PWM mode, or PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, PWM mode, or PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled).
When the PTO bit in the TRCOER register is 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), if a low-level (or high-level) signal is input to the $\overline{\text{INT0}}$ pin, bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as a programmable I/O port) after one or two cycles of the timer RC operating clock. For details of the timer RC operating clock, refer to **Table 18.1 Timer RC Operating Clocks**.

Make the following settings to use this function.

- Set the pin state following forced cutoff of pulse output (high impedance (input), low-level output, or high-level output). (Refer to **7. I/O Ports**.)
- Set the INT0EN bit to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge) in the INTEN register.
- Set the POL bit in the INT0IC register to select a rising or falling edge.
  When the POL bit is set to 0 (falling edge), the pulse output is forcibly cut off at the falling edge of the $\overline{\text{INT0}}$ pin.
  When the POL bit is set to 1 (rising edge), the pulse output is forcibly cut off at the rising edge of the $\overline{\text{INT0}}$ pin.
- Set the direction registers for the I/O ports selected as $\overline{\text{INT0}}$ to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F0 and INT0F1 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit and a change in the $\overline{\text{INT0}}$ pin input (refer to **12.8 Notes on Interrupts**).
For details on interrupts, refer to **12. Interrupts**.

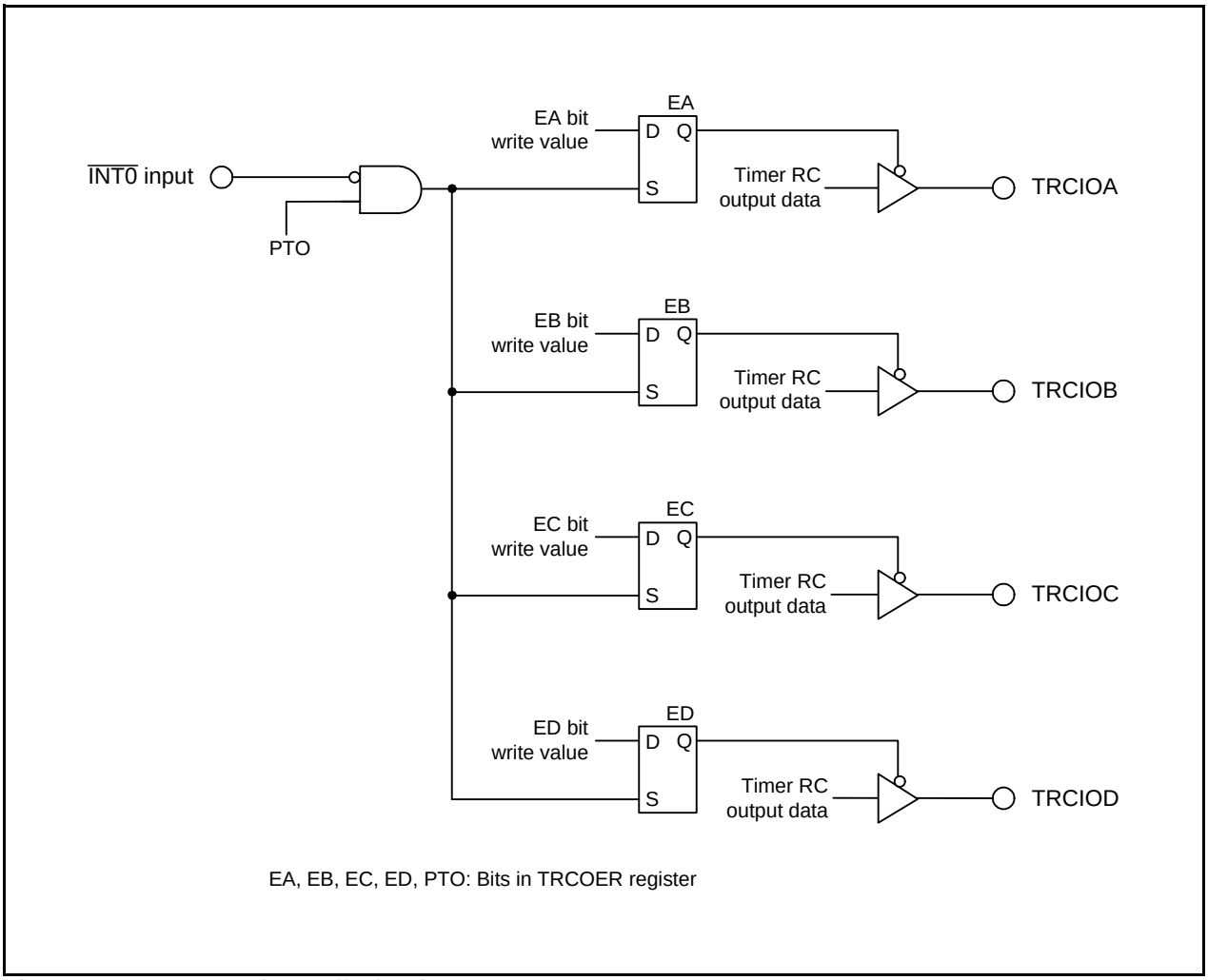


Figure 18.6 Forced Cutoff of Pulse Output

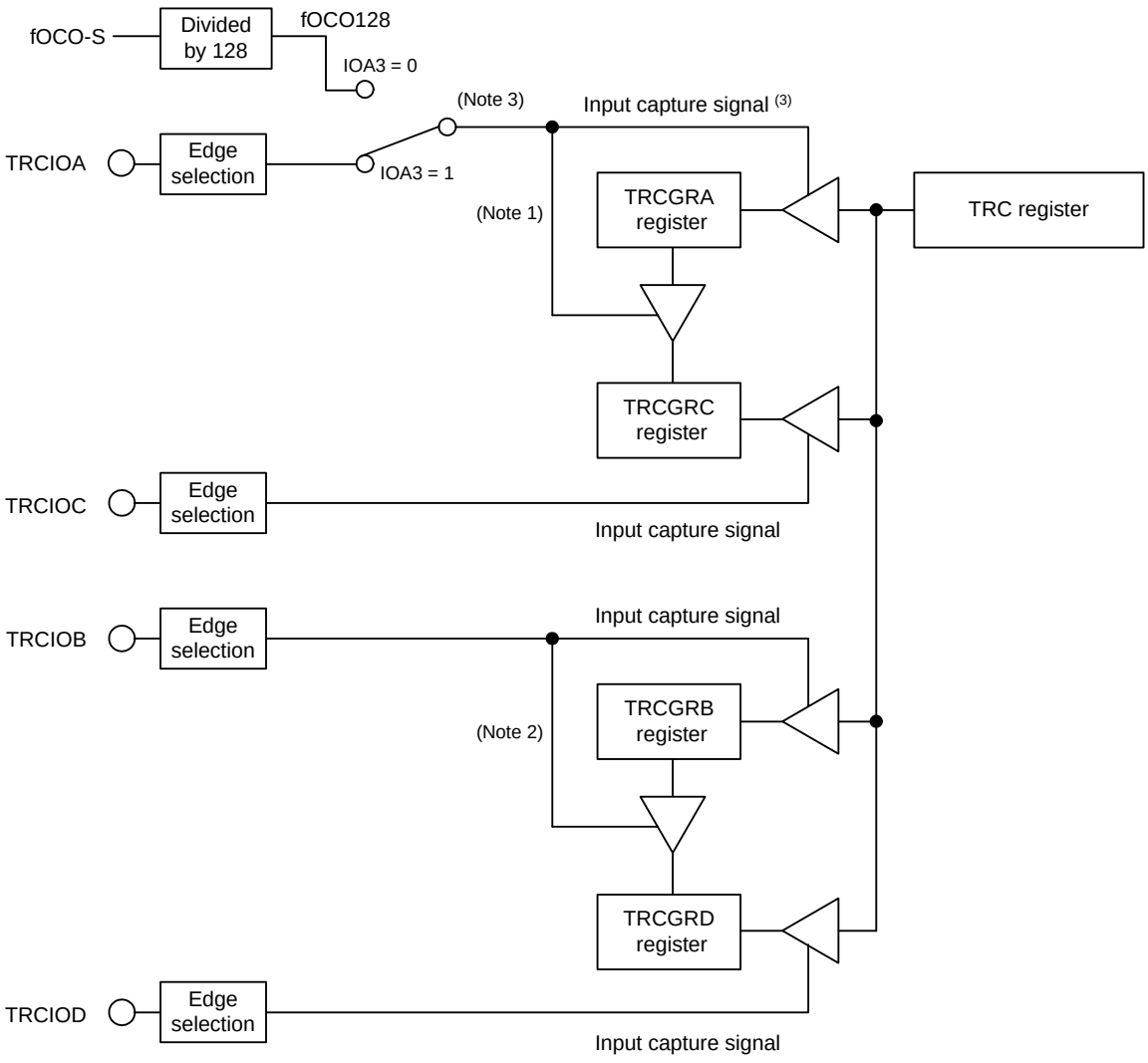
18.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the content of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. Table 18.7 lists the Input Capture Function Specifications, Figure 18.7 shows a Block Diagram of Input Capture Function, Table 18.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 18.8 shows an Operating Example of Input Capture Function.

Table 18.7 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, or external signal (rising edge) input to the TRCCLK pin
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free-running operation): 1/fk × 65,536 fk: Frequency of count source • The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by TRCGRA input capture): 1/fk × (n + 1) n: Value set in TRCGRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before the count stops.
Interrupt request generation timing	• Input capture (active edge of the TRCIOj input) • TRC register overflows
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or input capture input (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Input-capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input-capture input active edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Digital filter (Refer to **18.3.3 Digital Filter**.) • Timing for setting the TRC register to 0000h Overflow or input capture

j = A, B, C, or D



IOA3: Bit in TRCIOR0 register

Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 18.7 Block Diagram of Input Capture Function

18.4.1 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Input Capture Function)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 for the input capture function.	R/W
b3	IOA3	TRCGRA input-capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 for the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

18.4.2 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Input Capture Function)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 for the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 for the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

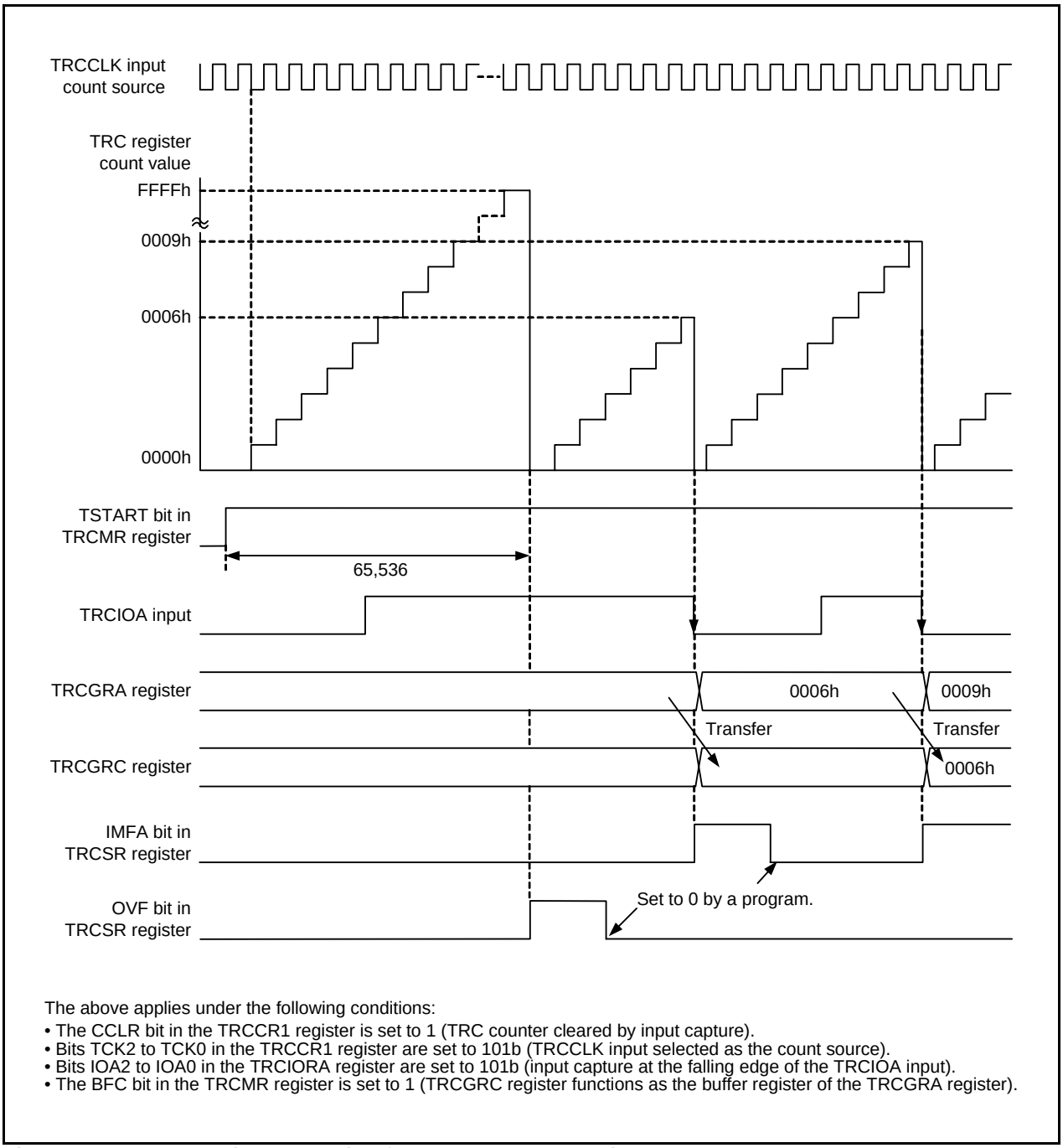
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 18.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	–	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to retain the transferred value from the general register. (Refer to **18.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

18.4.3 Operating Example



The above applies under the following conditions:
- The CCLR bit in the TRCCR1 register is set to 1 (TRC counter cleared by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (TRCCLK input selected as the count source).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register of the TRCGRA register).

Figure 18.8 Operating Example of Input Capture Function

18.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs, a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 18.9 lists the Output Compare Function Specifications, Figure 18.9 shows a Block Diagram of Output Compare Function, Table 18.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 18.10 shows an Operating Example of Output Compare Function.

Table 18.9 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, or external signal input to the TRCCLK pin (rising edge)
Count operation	Increment
Count periods	• The CCLR bit in the TRCCR1 register is set to 0 (free-running operation): 1/fk × 65,536 fk: Frequency of count source • The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by TRCGRA compare match): 1/fk × (n + 1) n: Value set in TRCGRA register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with the TRCGRA register). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains the output level before the count stops, the TRC register retains a value before the count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register). The count stops at a compare match with the TRCGRA register. The output-compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match.) • TRC register overflow
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or output compare output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Output-compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Output level selection at the compare match Low-level output, High-level output, or toggle output • Initial output level selection Selectable output level for the period from the count start to the compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **18.3.4 Forced Cutoff of Pulse Output**.) • Timer RC can be used as an internal timer by disabling the timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin.

j = A, B, C, or D

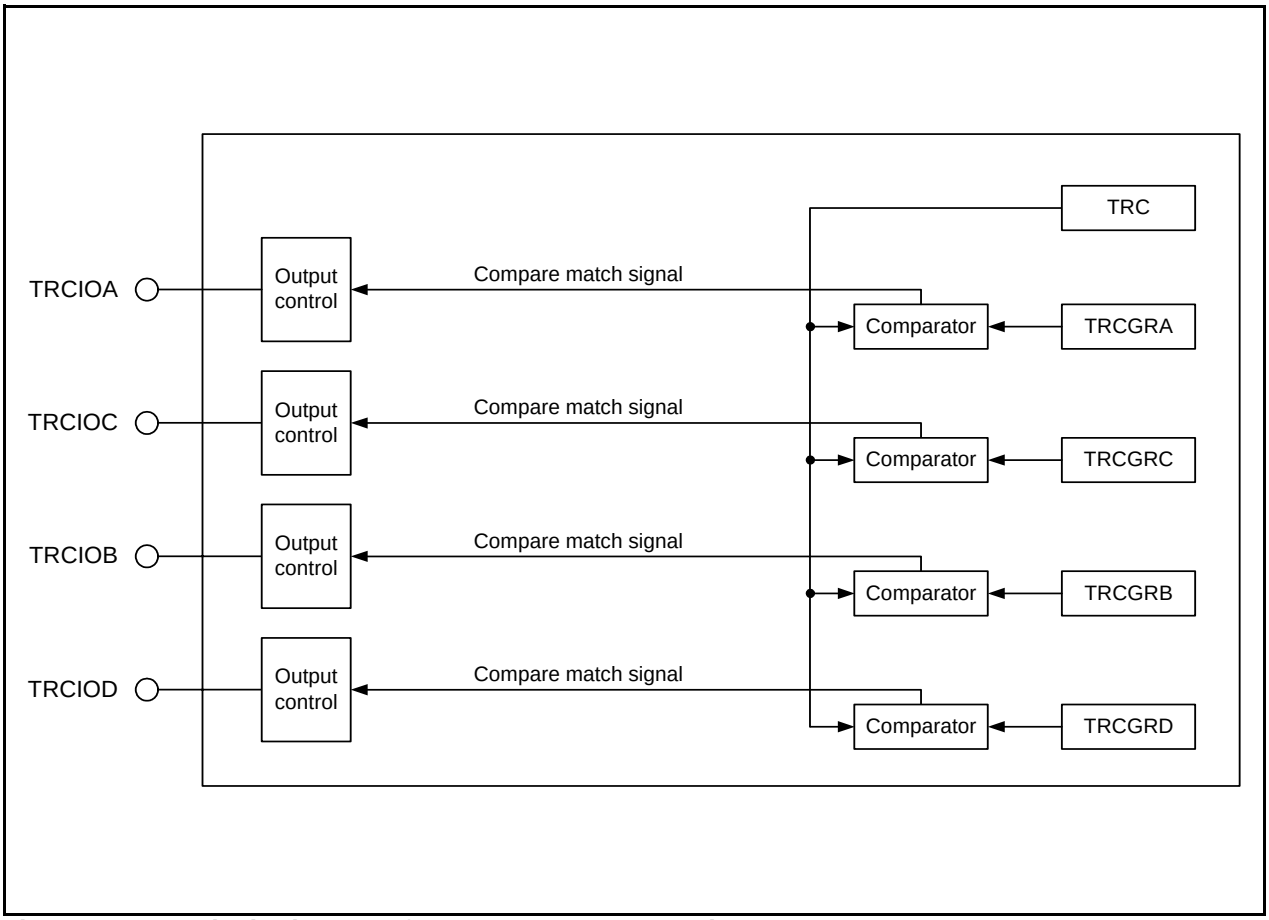


Figure 18.9 Block Diagram of Output Compare Function

18.5.1 Timer RC Control Register 1 (TRCCR1) in Timer Mode (Output Compare Function)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output at low 1: Initial output at high	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.6 Port Settings**), the initial output level is output when the TRCCR1 register is set.

Table 18.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	–	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **18.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Output Compare Function)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Pin output by compare match is disabled (TRCIOA pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRCGRA register 1 0: High-level output at compare match with the TRCGRA register 1 1: Toggle output at compare match with the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 for the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Pin output by compare match is disabled (TRCIOB pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRCGRB register 1 0: High-level output at compare match with the TRCGRB register 1 1: Toggle output at compare match with the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 for the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

18.5.3 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Output Compare Function)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRCGRC register 1 0: High-level output at compare match with the TRCGRC register 1 1: Toggle output at compare match with the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 for the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRCGRD register 1 0: High-level output at compare match with the TRCGRD register 1 1: Toggle output at compare match with the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 for the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

18.5.4 Timer RC Control Register 2 (TRCCR2) in Timer Mode (Output Compare Function)

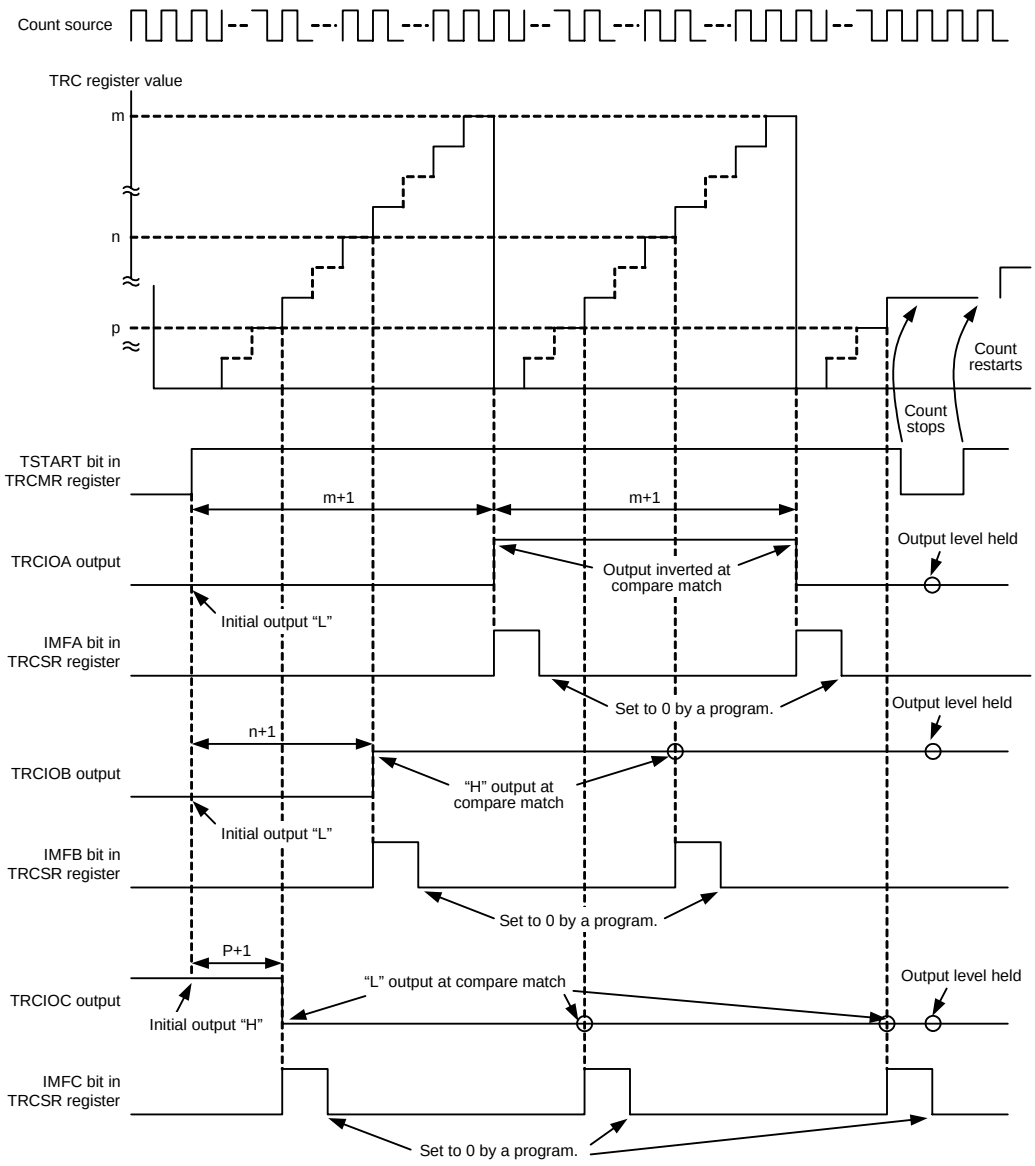
Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

18.5.5 Operating Example



The above applies under the following conditions:

- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (TRCIOA, TRCIOB, and TRCIOC pin output enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by compare match with TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are are set to 0 (initial output at low until compare match) and the TOC bit is set to 1 (initial output at high until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted by TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b (TRCIOB high-level output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b (TRCIOC low-level output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 18.10 Operating Example of Output Compare Function

18.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Each pin output can be controlled as follows:

- TRCIOA output is controlled by the values of registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values of registers TRCGRB and TRCGRD.

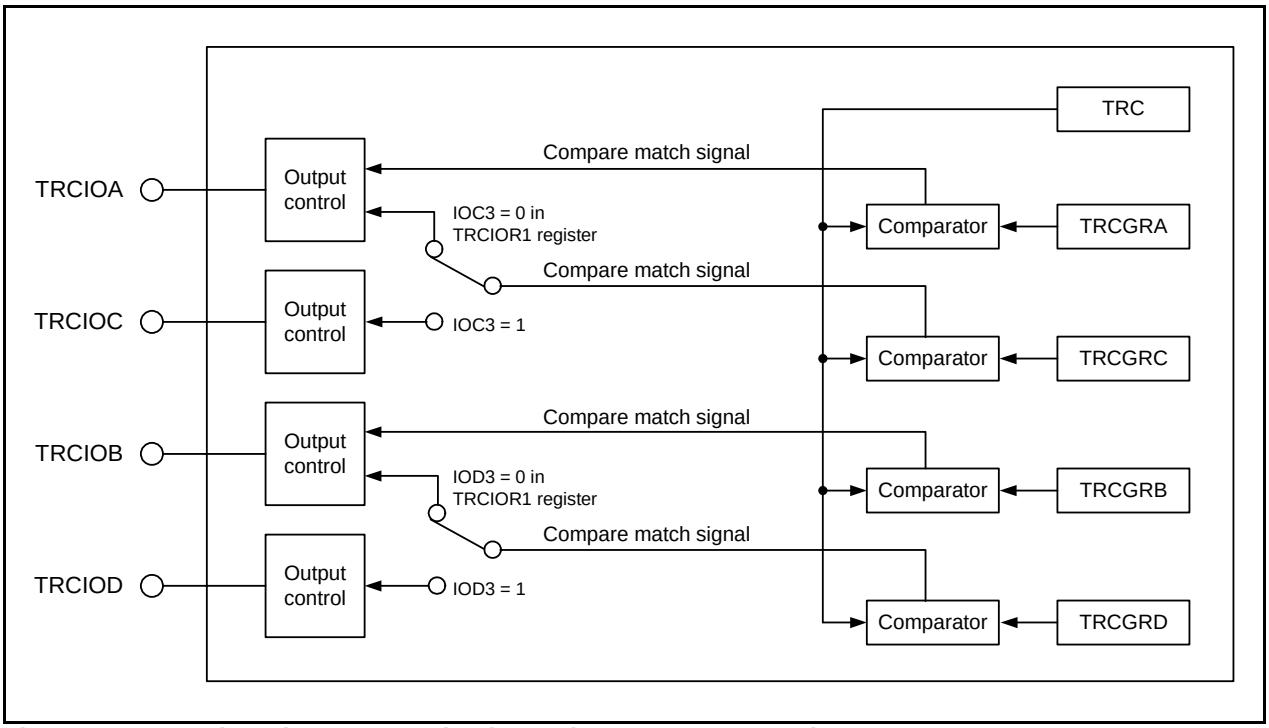
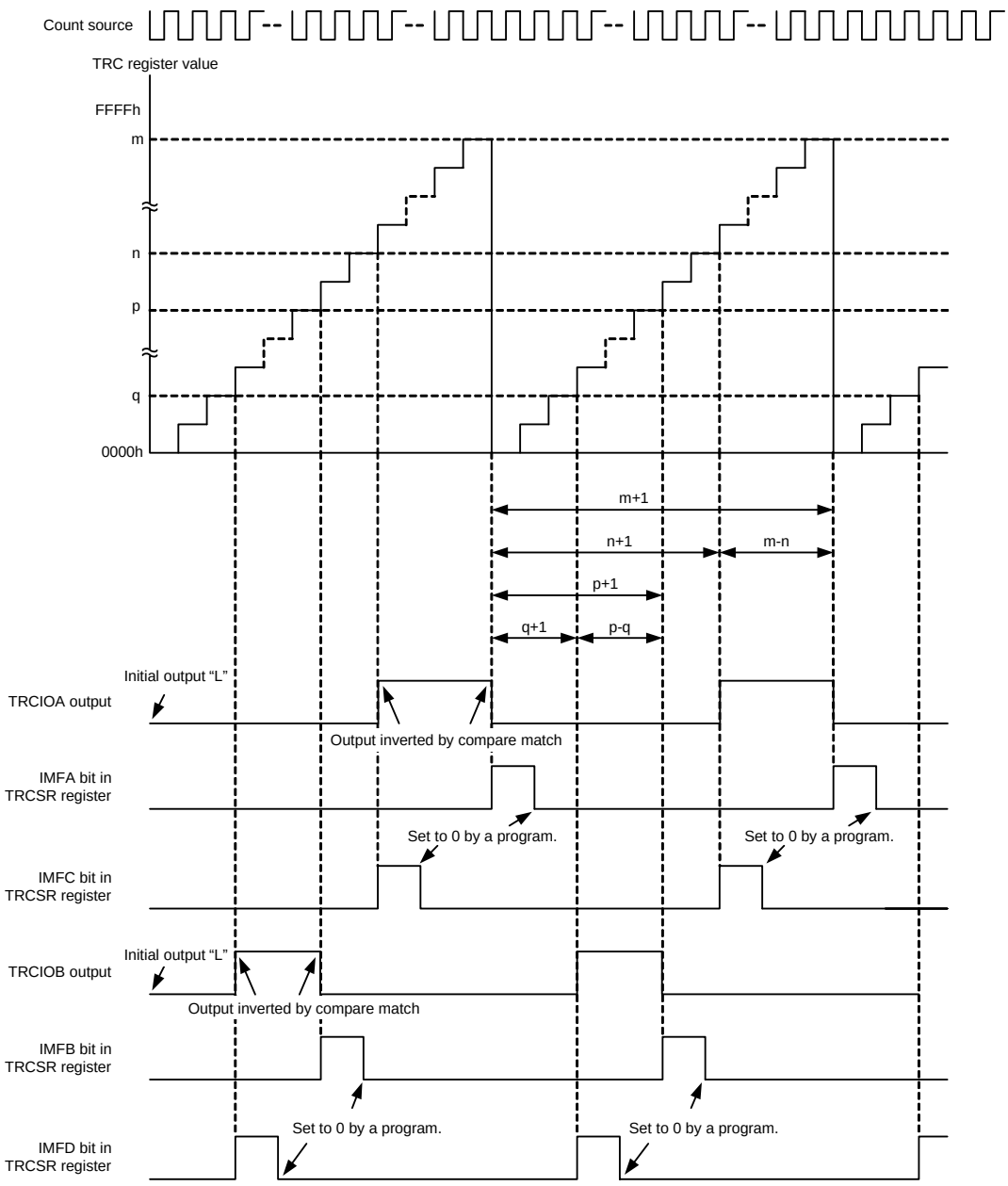


Figure 18.11 Changing Output Pins in Registers TRCGRC and TRCGRD

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 18.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.



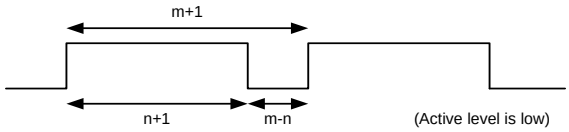
The above applies under the following conditions:
Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
Bits EA and EB in the TRCOER register are set to 0 (TRCIOA and TRCIOB pin output enabled).
The CCLR bit in the TRCCR1 register are set to 1 (TRC register is set to 0000h by compare match with the TRCGRA register).
Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output at low until compare match).
Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted by TRCGRA register compare match).
Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted by TRCGRB register compare match).
Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted by TRCGRC register compare match).
The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted by TRCGRD register compare match).
The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
The CSEL bit in the TRCCR2 register are set to 0 (TRC count continues after compare match).

Figure 18.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

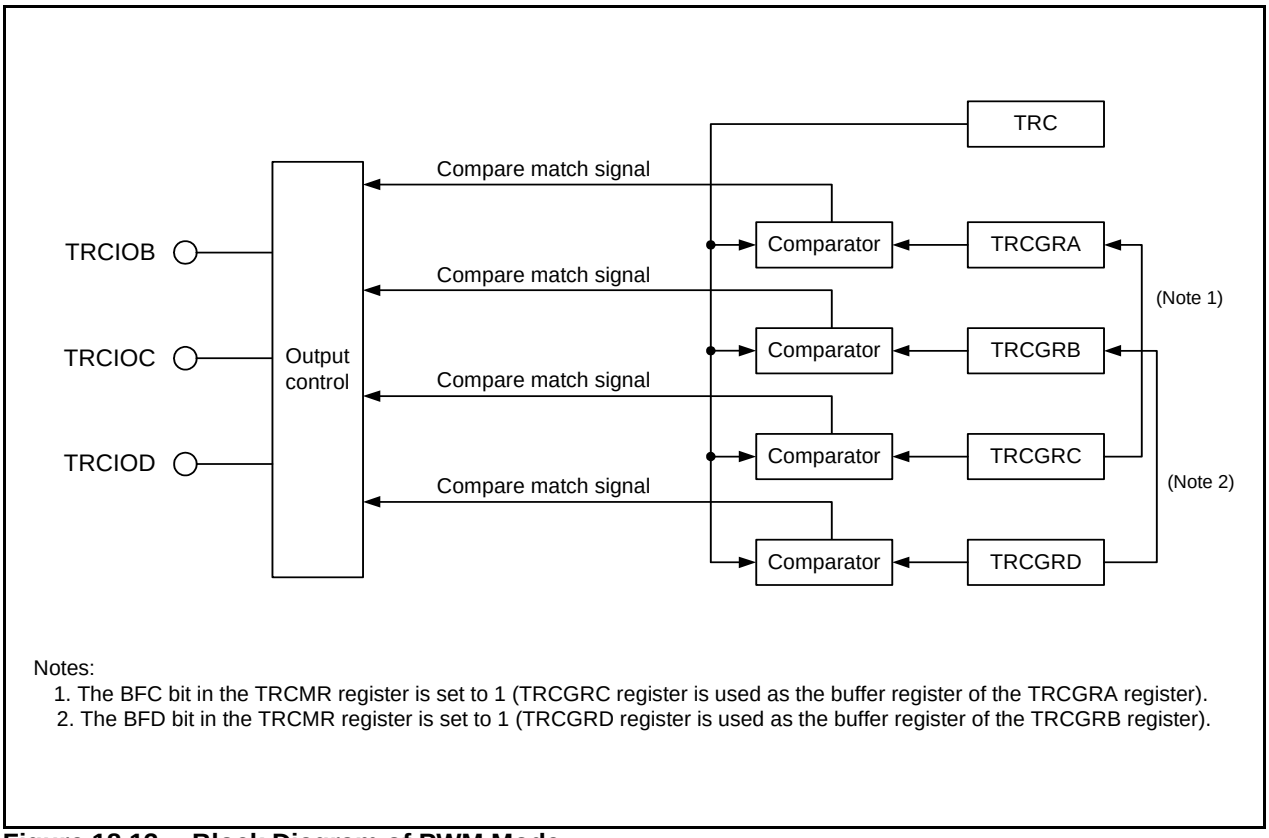
18.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. PWM mode or timer mode can be selected for each individual pin. (However, the TRCGRA register cannot be used for timer mode since the register is used when using any pin for PWM mode.)
Table 18.11 lists the PWM Mode Specifications, Figure 18.13 shows a Block Diagram of PWM Mode, Table 18.12 lists the Functions of TRCGRj Register in PWM Mode, and Figures 18.14 and 18.15 show Operating Examples in PWM Mode.

Table 18.11 PWM Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, or external signal (rising edge) input to the TRCCLK pin
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive level width: 1/fk × (n + 1) fk: Frequency of count source m: Value set in TRCGRA register n: Value set in TRCGRh register 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with the TRCGRA register). 0 (count stops) is written to the TSTART bit in the TRCMR register. The PWM output pin retains the output level before the count stops, The TRC register retains a value before the count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register). The count stops at a compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match) • TRC register overflow
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or PWM output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• One to three pins selectable as PWM pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each individual pin • Initial level selectable for each individual pin • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **18.3.4 Forced Cutoff of Pulse Output**.)

j = A, B, C, or D
h = B, C, or D



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register is used as the buffer register of the TRCGRB register).

Figure 18.13 Block Diagram of PWM Mode

18.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode.	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.6 Port Settings**), the initial output level is output when the TRCCR1 register is set.

18.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

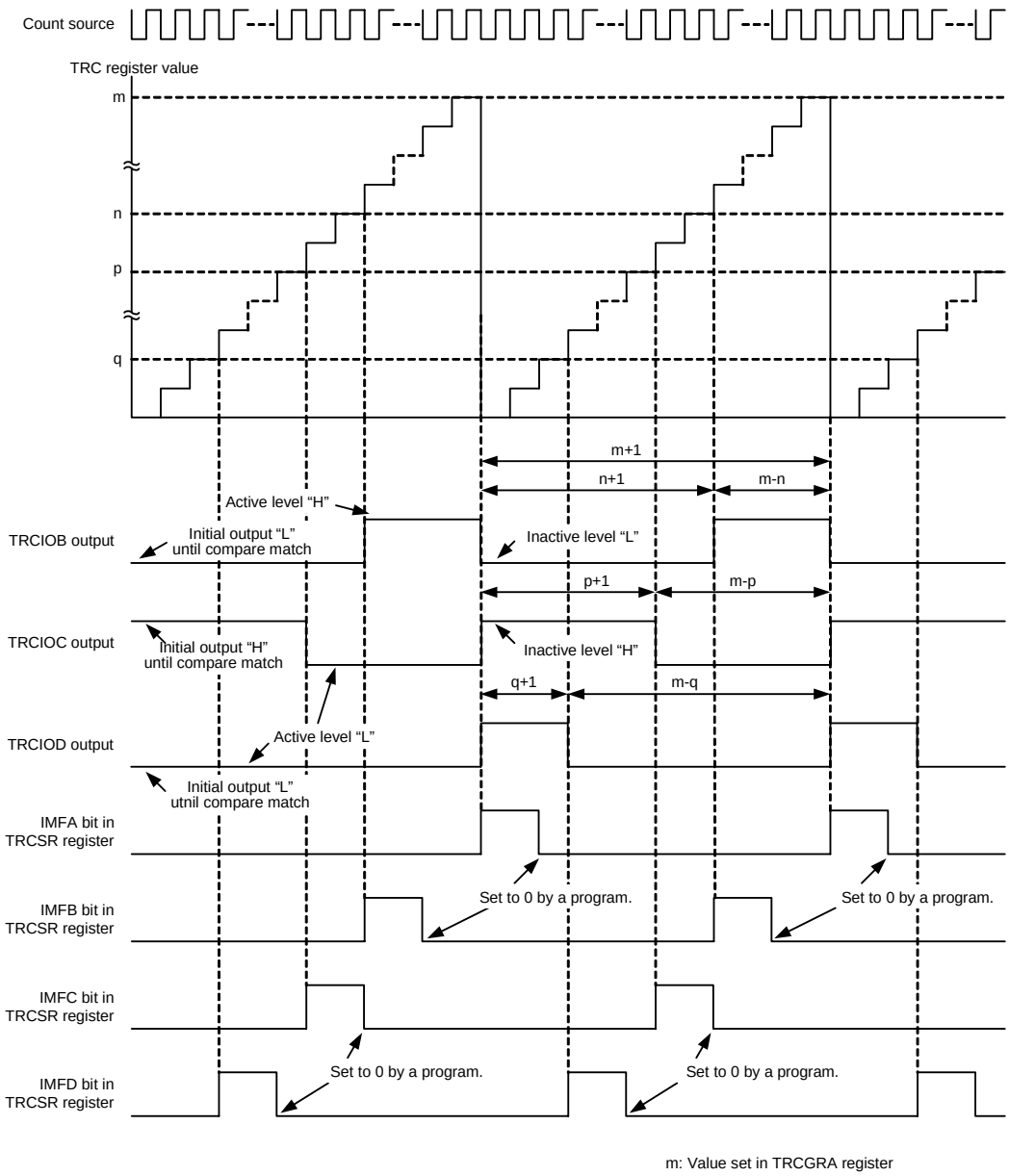
Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

Table 18.12 Functions of TRCGRj Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	–	General register. Set the PWM period.	–
TRCGRB	–	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period. (Refer to **18.3.2 Buffer Operation**.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **18.3.2 Buffer Operation**.)	TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even if a compare match occurs when the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

18.6.3 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (TRCIOB, TRCIOC, and TRCIOD pin output enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level) and the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 (high active), bits POLC and POLD are set to 0 (low active).

Figure 18.14 Operating Example in PWM Mode

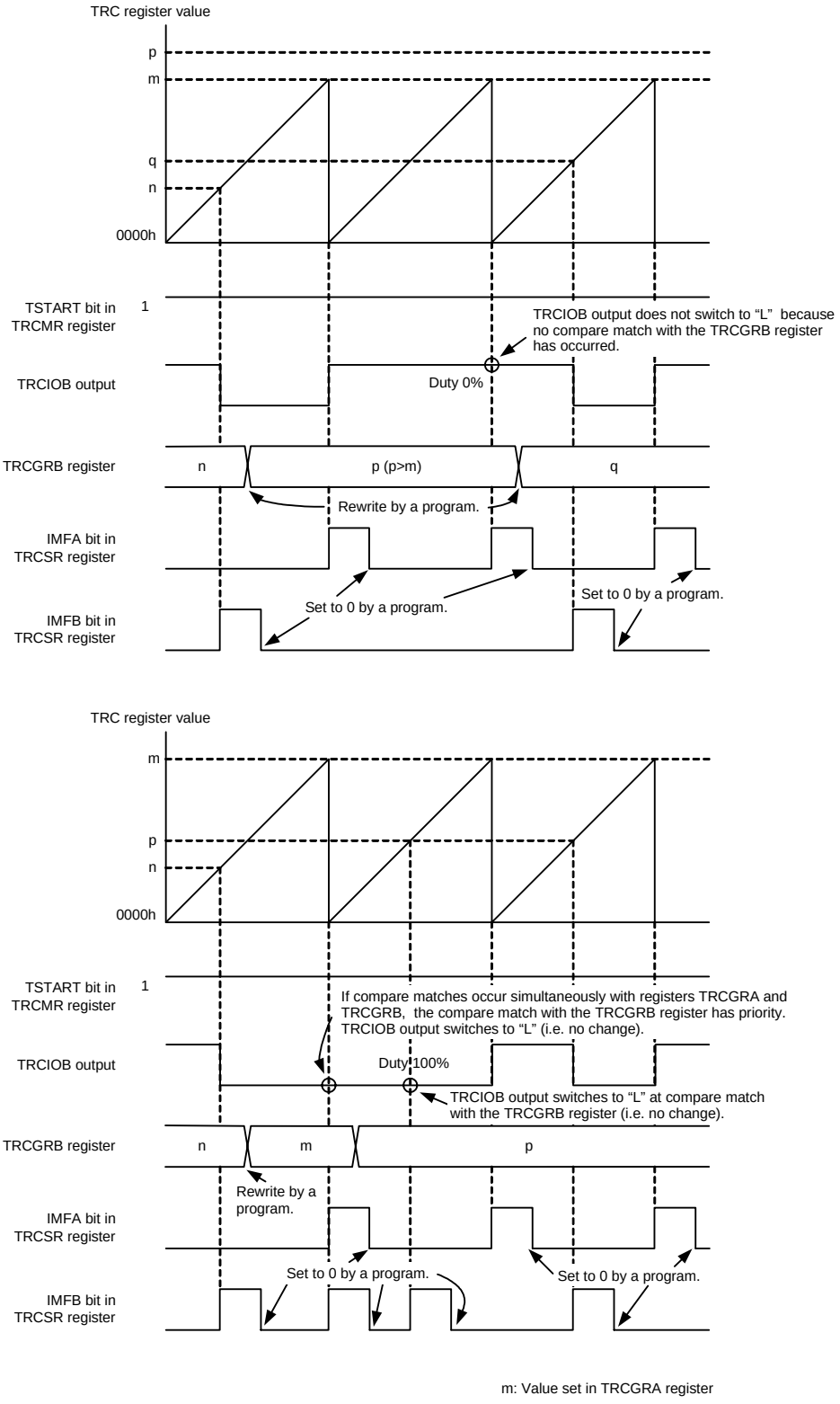
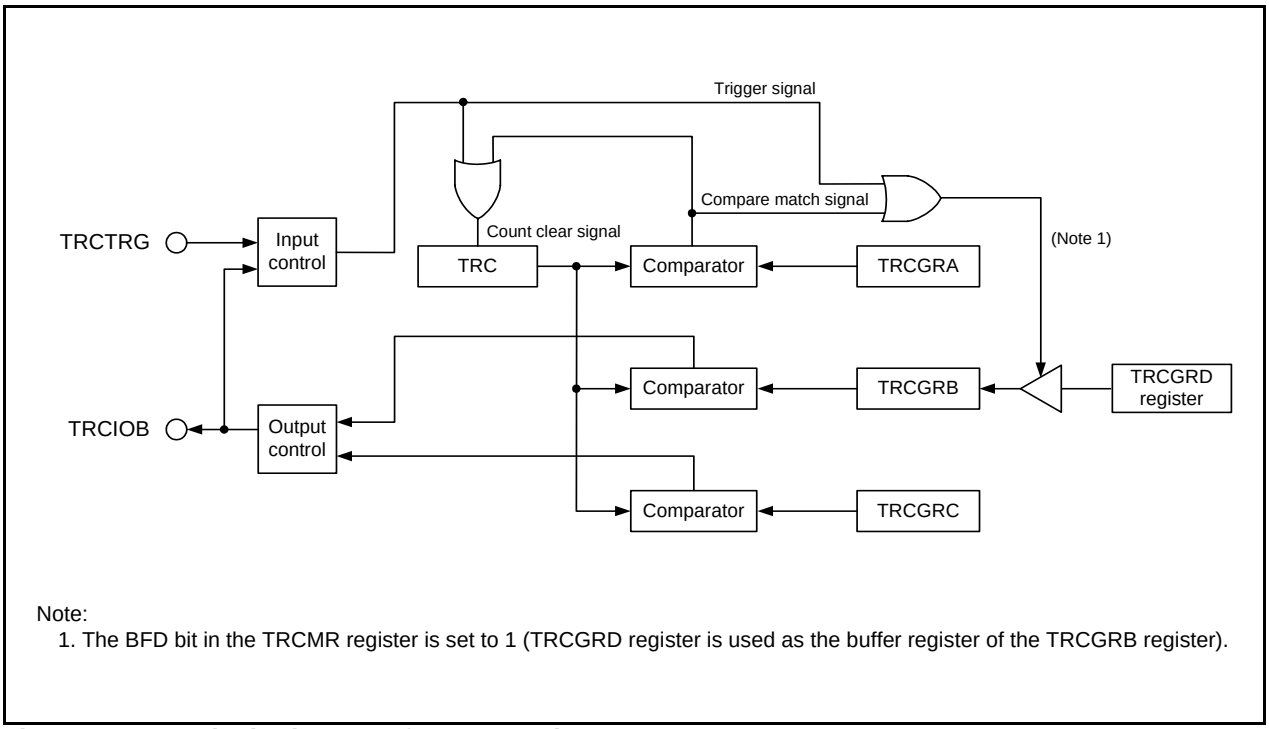


Figure 18.15 Operating Example in PWM Mode (Duty 0% and Duty 100%)

18.7 PWM2 Mode

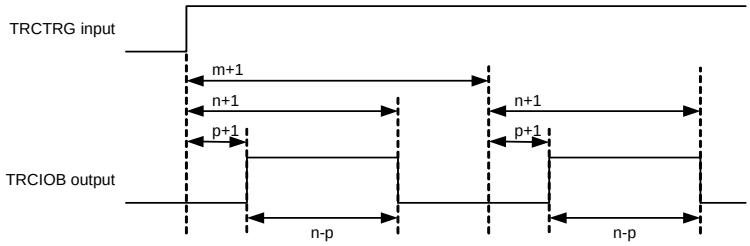
This mode outputs a single PWM waveform. After a given wait time has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 18.16 shows a Block Diagram of PWM2 Mode, Table 18.13 lists the PWM2 Mode Specifications, Table 18.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 18.17 to 18.19 show Operating Examples in PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (TRCGRD register is used as the buffer register of the TRCGRB register).

Figure 18.16 Block Diagram of PWM2 Mode

Table 18.13 PWM2 Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, or external signal input to TRCCLK pin (rising edge)
Count operation	TRC register increment
PWM waveform	PWM period: 1/fk × (m + 1) (no TRCTRG input) Active level width: 1/fk × (n - p) Wait time from count start or trigger: 1/fk × (p + 1) fk: Frequency of count source m: Value set in TRCGRA register n: Value set in TRCGRB register p: Value set in TRCGRC register  (TRCTRG: Rising edge, active level is high)
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before the count stops. • The count stops at a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1 The TRCIOB pin outputs the initial level. The TRC register retains the value before the count stops when the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h when the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match.) • TRC register overflow
TRCIOA/TRCTRG pins function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC/TRCIOD pins function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• External trigger and active edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **18.3.4 Forced Cutoff of Pulse Output**.) • Digital filter (Refer to **18.3.3 Digital Filter**.)

j = A, B, C, or D

18.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode.	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level is high (Initial output at low High-level output at compare match with the TRCGRC register Low-level output at compare match with the TRCGRB register) 1: Active level is low (Initial output at high Low-level output at compare match with the TRCGRC register High-level output at compare match with the TRCGRB register)	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode.	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4	R/W
b5	TCK1		0 0 0: f1	R/W
b6	TCK2		0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.6 Port Settings**), the initial output level is output when the TRCCR1 register is set.

18.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

18.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)	0: Function is not used 1: Function is used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Digital filter function clock select bit (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

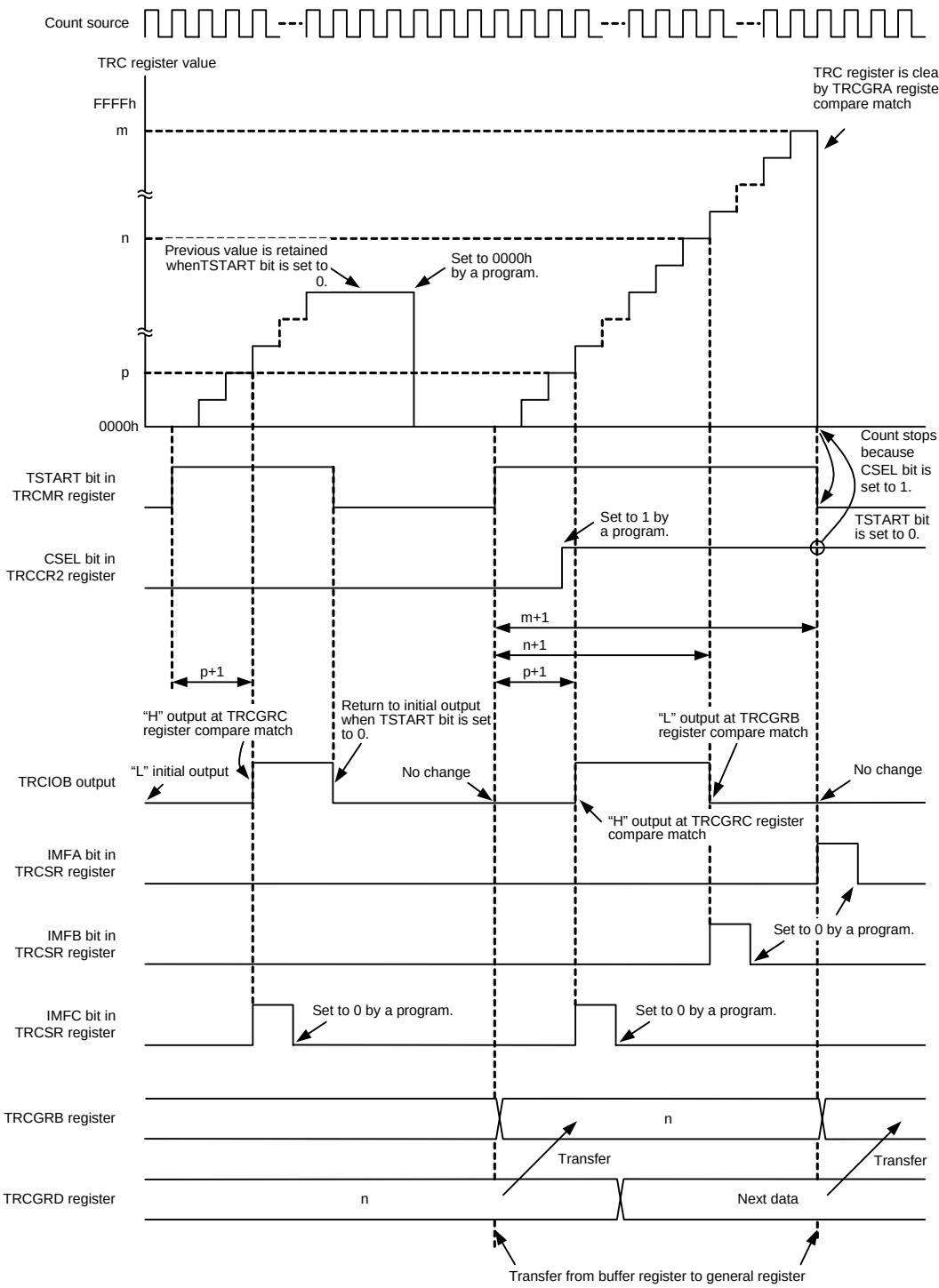
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Table 18.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	–	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	–	General register. Set the PWM output change point.	
TRCGRC (1)	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **18.3.2 Buffer Operation**.)	TRCIOB pin

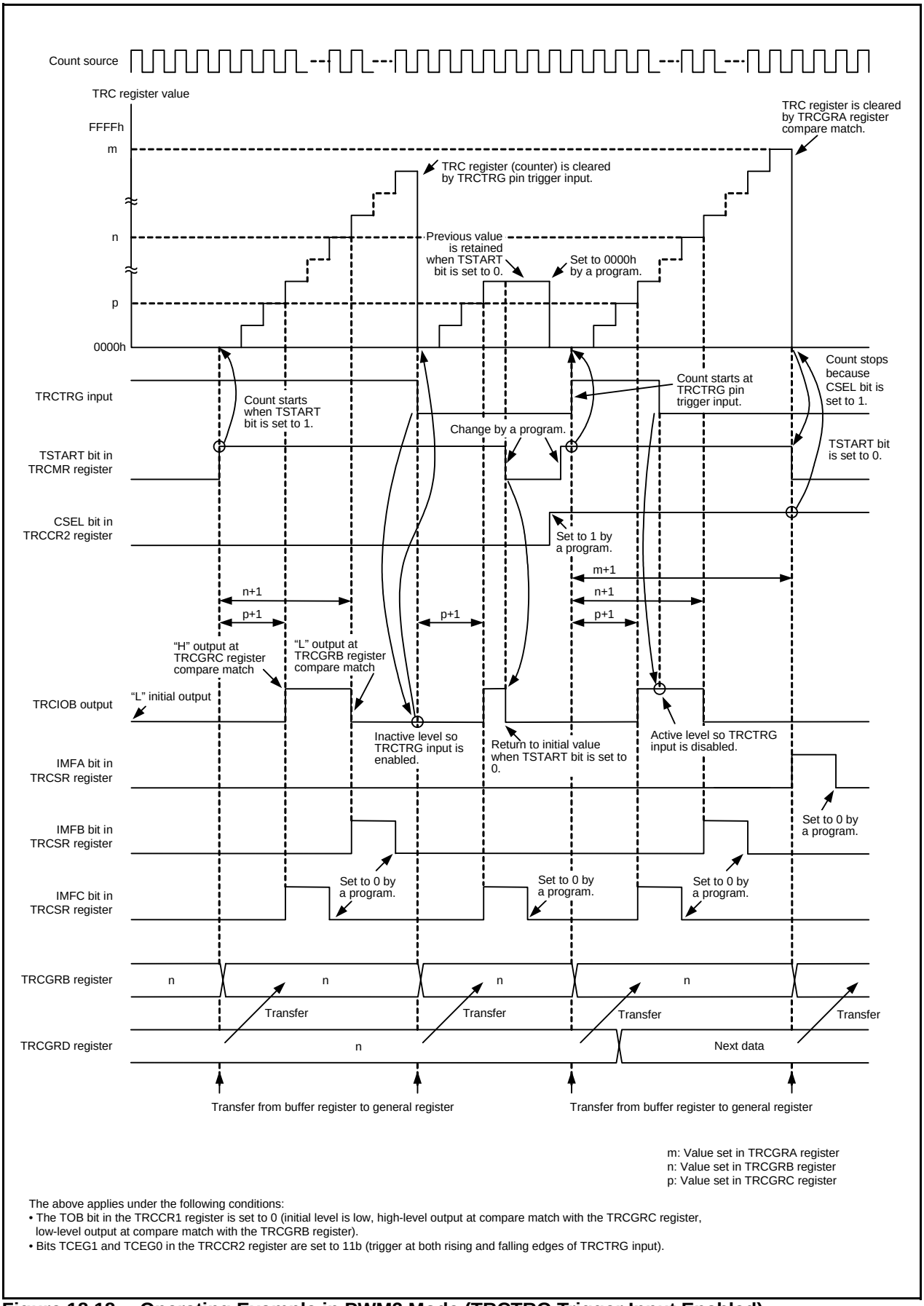
j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set registers TRCGRB and TRCGRC to the same value.

18.7.4 Operating Example



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 18.17 Operating Example in PWM2 Mode (TRCTRG Trigger Input Disabled)



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 18.18 Operating Example in PWM2 Mode (TRCTRG Trigger Input Enabled)

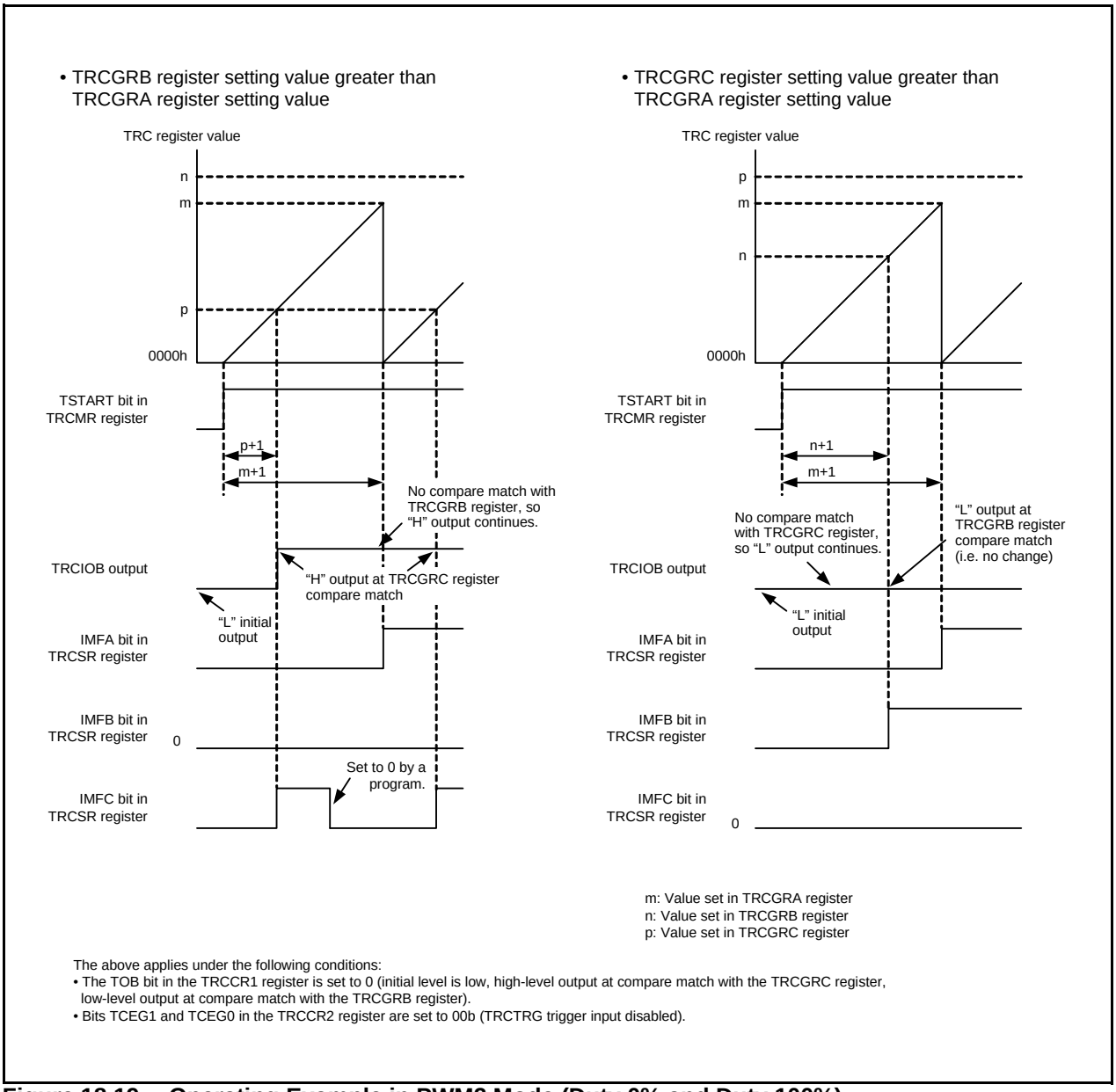


Figure 18.19 Operating Example in PWM2 Mode (Duty 0% and Duty 100%)

18.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 18.15 lists the Registers Associated with Timer RC Interrupt and Figure 18.20 shows a Block Diagram of Timer RC Interrupt.

Table 18.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

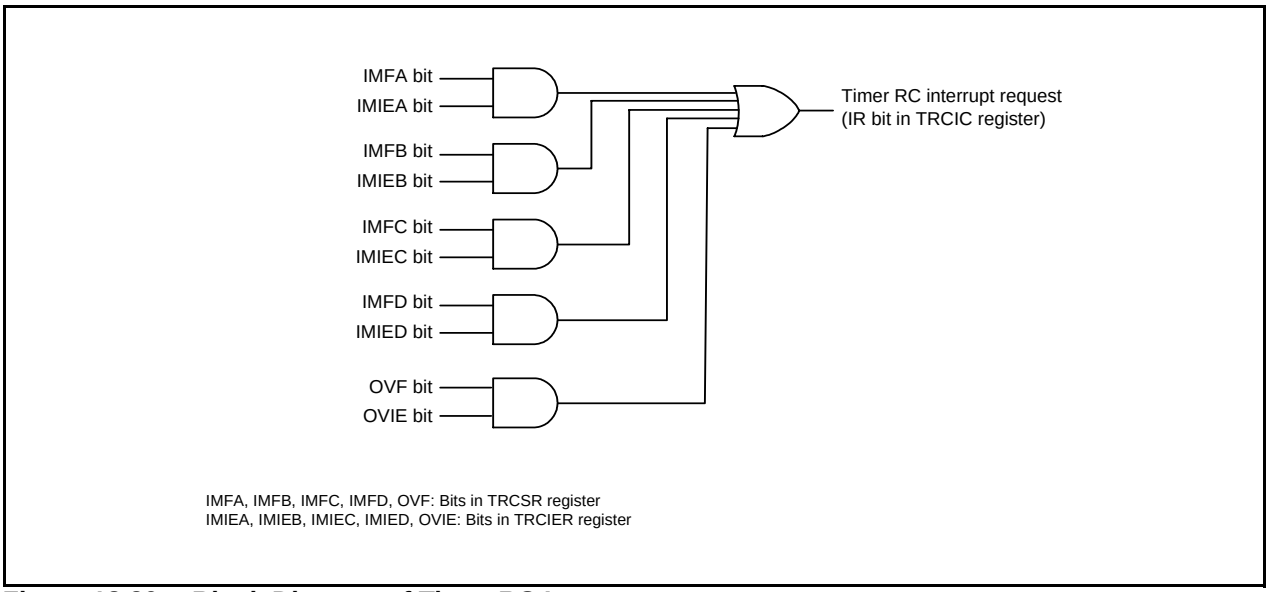


Figure 18.20 Block Diagram of Timer RC Interrupt

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **18.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **18.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **12.3 Interrupt Control**, for details of the TRCIC register and **12.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

18.9 Notes on Timer RC

18.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRC register cleared by compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.W   TRC,DATA        ;Read
```

18.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA      ;Read
```

18.9.3 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

18.9.4 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 18.1 Timer RC Operating Clocks**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 18.5 Block Diagram of Digital Filter**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).
- When the input capture function is used, if an edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in the TRCIOR0 or TRCIOR1 register is input to the TRCIOj pin, the IMFj bit in the TRCSR register is set to 1 even when the TSTART bit in the TRCMR register is 0 (count stops).

18.9.5 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

19. Timer RJ

19.1 Introduction

Timer RJ0 is a 16-bit timer.
Timer RJ0 has an input and output pin.
The timers each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing the TRJ0 register (refer to **Tables 19.2 to 19.6** for details of the specifications of each mode).
The count source for timer RJ is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 19.1 shows the Timer RJ0 Block Diagram. Table 19.1 lists the Timer RJ0 Pin Configuration.

Timer RJ0 supports the following five operating modes:

- Timer mode: The timer counts an internal count source.
- Pulse output mode: The timer counts an internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

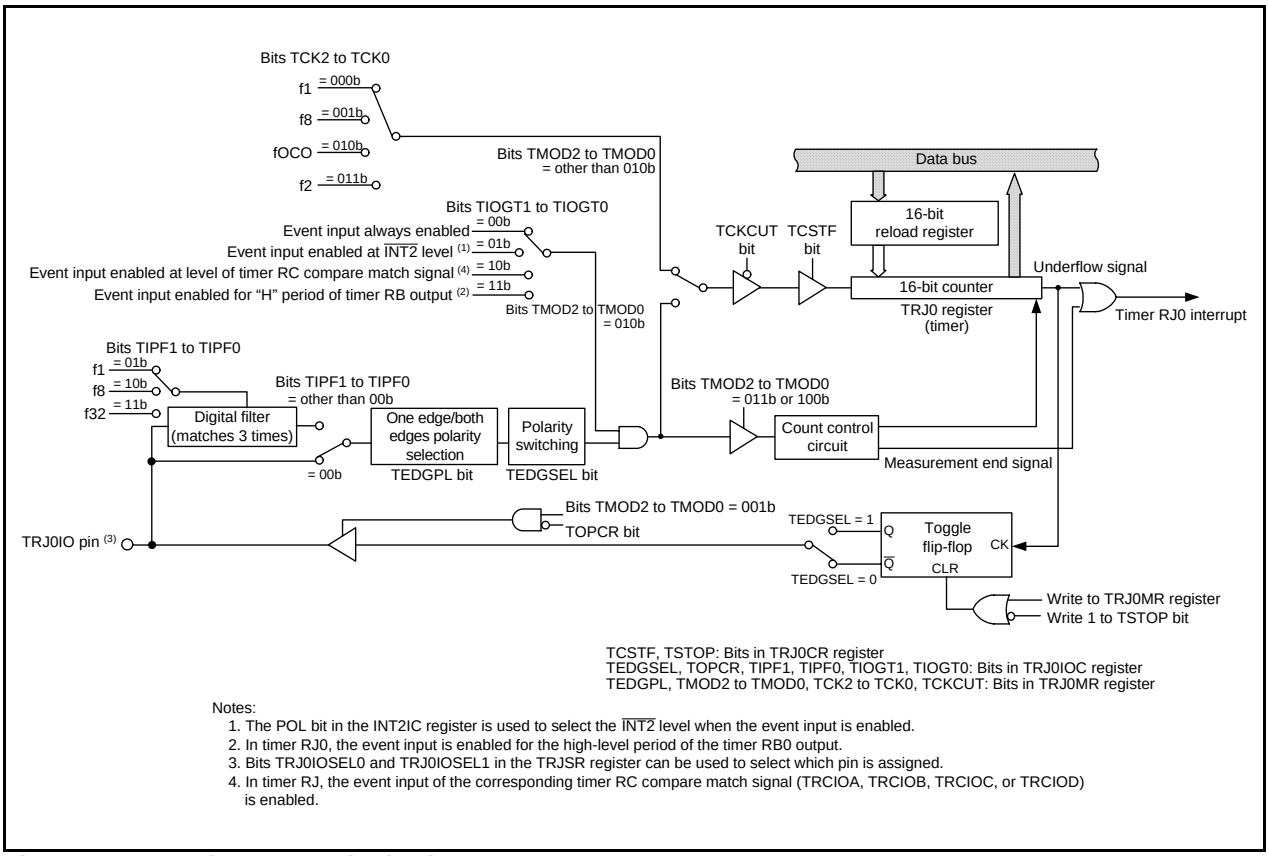


Figure 19.1 Timer RJ0 Block Diagram

Table 19.1 Timer RJ0 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRJ0IO	P8_3	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.

19.2 Registers

19.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Reserved bit	Set to 1.	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (3)	R/W
b4	MSTTRJ1	Reserved bit	Set to 1.	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

19.2.2 Timer RJ0 Control Register (TRJ0CR)

Address 0080h (TRJ0CR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RJ0 count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RJ0 count status flag (1)	0: Count stops 1: During count operation	R
b2	TSTOP	Timer RJ0 count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RJ0 underflow flag (3, 5)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **19.8 Notes on Timer RJ** for notes regarding bits TSTART and TCSTF.
2. When 1 is written to the TSTOP bit, bits TSTART and TCSTF and the TRJ0 register are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. The TEDGF bit is not used in timer mode, pulse output mode, and event counter mode.
5. Set to 0 in timer mode, pulse output mode, and event counter mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRJ0CR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

19.2.3 Timer RJ0 I/O Control Register (TRJ0IOC)

Address 0081h (TRJ0IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJ0IO polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRJ0IO output control bit		R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJ0IO input filter select bit	Function varies according to the operating mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJ0IO event input control bit		R/W
b7	TIOGT1			R/W

19.2.4 Timer RJ0 Mode Register (TRJ0MR)

Address 0082h (TRJ0MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RJ0 operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	TEDGPL	TRJ0IO input polarity select bit	0: One edge 1: Both edges (1)	R/W
b4	TCK0	Timer RJ0 count source select bit	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: Do not set. 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RJ0 count source cut off bit	0: Count source provided 1: Count source cut off	R/W

Note:

1. When setting the TEDGPL bit to 1 (both edges), set the TEDGSEL bit in the TRJ0IOC register to 0 (count on rising edge). The setting of both edges can be used only in event counter mode.

   When both the TSTART and TCSTF bits in the TRJ0CR register are set to 0 (count stops), rewrite the TRJ0MR register.

19.2.5 Timer RJ0 Event Pin Select Register (TRJ0ISR)

Address 0083h (TRJ0ISR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	RCCPSEL2	RCCPSEL1	RCCPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCCPSEL0	Timer RC compare input event select bit (1)	b1 b0 0 0: TRCIOD output used 0 1: TRCIOC output used 1 0: TRCIOB output used 1 1: TRCIOA output used	R/W
b1	RCCPSEL1			R/W
b2	RCCPSEL2	Timer RC compare event invert bit	0: Low-level period of the compare match signal is counted 1: High-level period of the compare match signal is counted	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Bits RCCPSEL0 and RCCPSEL1 in the TRJ0ISR register are used to select the compare output from timer RC.

19.2.6 Timer RJ0 Register (TRJ0)

Address 0084h to 0085h (TRJ0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	b15	b14	b13	b12	b11	b10	b9	b8	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b15 to b0	Timer mode	Counts an internal count source.	0000h to FFFFh	R/W
	Pulse output mode		0000h to FFFFh	R/W
	Event counter mode	Counts an external count source.	0000h to FFFFh	R/W
	Pulse width measurement mode	Measures the pulse width of input pulses from external (counts an internal count source).	0001h to FFFFh (3)	R/W
	Pulse period measurement mode	Measures the pulse period of input pulses from external (counts an internal count source).	0001h to FFFFh (3)	R/W

Notes:
1. When 1 is written to the TSTOP bit in the TRJ0CR register, the TRJ0 register is set to FFFFh.
2. Access the TRJ0 register in 16-bit units. Do not access this register in 8-bit units.
3. Do not set 0000h to the TRJ0 register in pulse width measurement mode and pulse period measurement mode.

19.2.7 Timer RJ Pin Select Register (TRJSR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	TRJ0IOSEL1	TRJ0IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ0IOSEL0	TRJ0IO pin select bit	b1 b0 0 0: TRJ0IO pin not used 0 1: P8_3 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TRJ0IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

To use the I/O pins for timer RJ0, set the TRJSR register.
Set this register before setting the timer RJ0 associated registers. Also, do not change the setting value of this register during timer RJ0 operation.

19.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 19.2**).

Table 19.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(m+1) m: Value set in TRJ0 register
Count start condition	1 (count starts) is written to the TSTART bit in the TRJ0CR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJ0CR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJ0CR register.
Interrupt request generation timing	When timer RJ0 underflows [timer RJ0 interrupt].
TRJ0IO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading the TRJ0 register.
Write to timer	• When the TRJ0 register is written while the count is stopped, values written to both the reload register and counter. • When the TRJ0 register is written during count operation, values are written to the reload register and counter (refer to **19.3.2 Timer Write Control during Count Operation**).

19.3.1 Timer RJ0 I/O Control Register (TRJ0IOC) in Timer Mode

Address 0081h (TRJ0IOC)

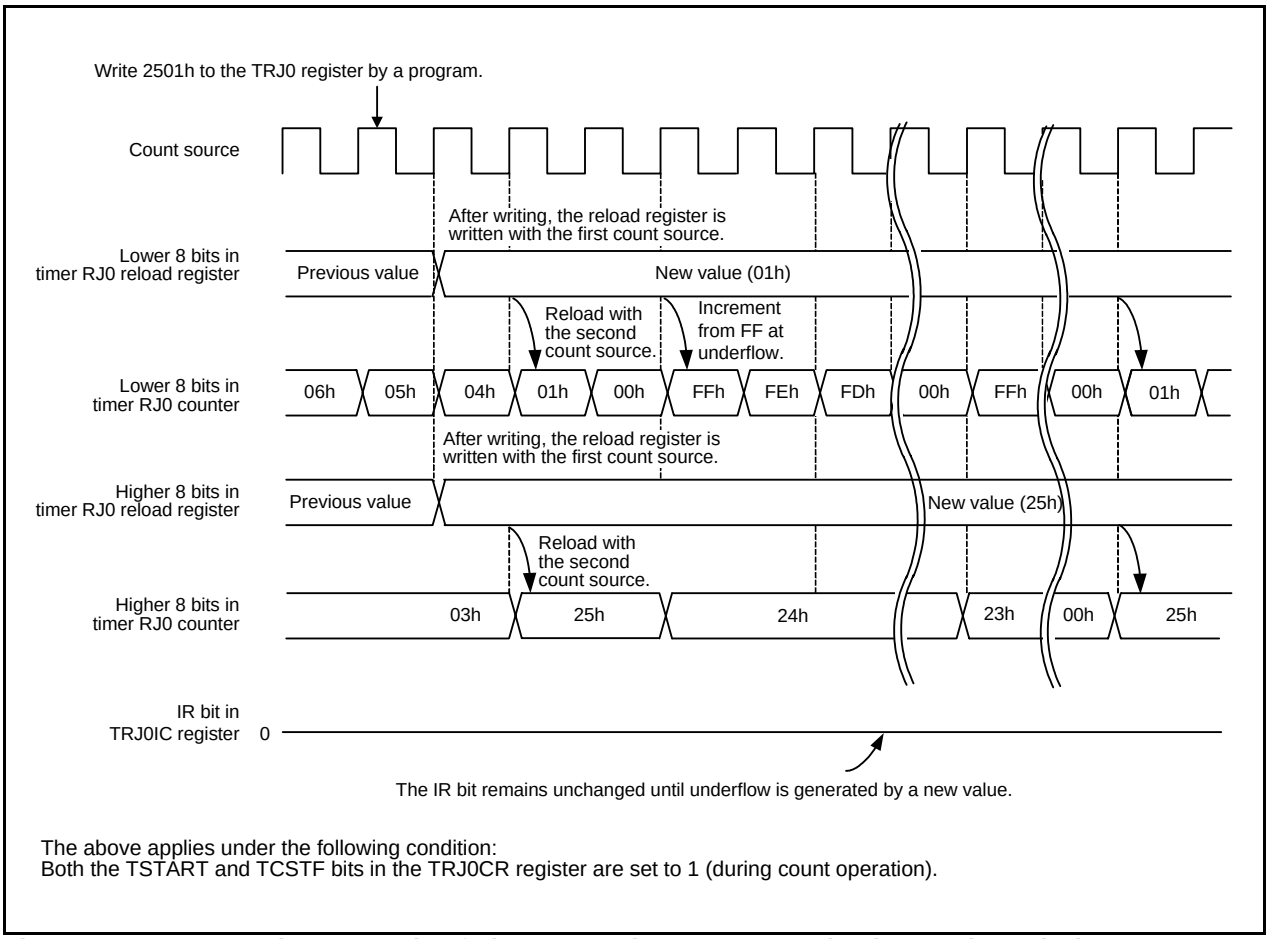
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJ0IO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRJ0IO output control bit		R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJ0IO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJ0IO event input control bit		R/W
b7	TIOGT1			R/W

19.3.2 Timer Write Control during Count Operation

Timer RJ0 has a reload register and a counter. When writing to the timer, values are written to both the reload register and counter.

Figure 19.2 shows an Operating Example of Timer RJ0 when Counter Value is Rewritten during Count Operation.



The above applies under the following condition:
Both the TSTART and TCSTF bits in the TRJ0CR register are set to 1 (during count operation).

Figure 19.2 Operating Example of Timer RJ0 when Counter Value is Rewritten during Count Operation

19.4 Pulse Output Mode

In pulse output mode, an internally generated count source is counted, and a pulse with inverted polarity is output from the TRJ0IO pin each time the timer underflows (refer to **Table 19.3**).

Table 19.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(m+1) m: Value set in TRJ0 register
Count start condition	1 (count starts) is written to the TSTART bit in the TRJ0CR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJ0CR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJ0CR register.
Interrupt request generation timing	When timer RJ0 underflows [timer RJ0 interrupt].
TRJ0IO pin function	Pulse output or programmable output port
Read from timer	The count value can be read out by reading the TRJ0 register.
Write to timer	• When the TRJ0 register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJ0 register is written during count operation, values are written to the reload register and counter (refer to **19.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRJ0IO output polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRJ0IOC register. (1) • Pulse output stop function Output from the TRJ0IO pin is stopped by the TOPCR bit in the TRJ0IOC register. • TRJ0IO pin select function Use of the TRJ0IO pin is selected by bits TRJ0IOSEL0 and TRJ0IOSEL1 in the TRJSR register.

Note:
1. By writing to the TRJ0MR register, the output pulse is set to the level when the pulse output starts.

19.4.1 Timer RJ0 I/O Control Register (TRJ0IOC) in Pulse Output Mode

Address 0081h (TRJ0IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJ0IO polarity switch bit	0: TRJ0IO output starts at high 1: TRJ0IO output starts at low	R/W
b1	TOPCR	TRJ0IO output control bit	0: TRJ0IO output 1: I/O port	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJ0IO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJ0IO event input control bit		R/W
b7	TIOGT1			R/W

19.5 Event Counter Mode

In event counter mode, external signal inputs to the TRJ0IO pin are counted (refer to **Table 19.4**).

Table 19.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal input to the TRJ0IO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(m+1) m: Value set in TRJ0 register
Count start condition	1 (count starts) is written to the TSTART bit in the TRJ0CR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJ0CR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJ0CR register.
Interrupt request generation timing	When timer RJ0 underflows [timer RJ0 interrupt].
TRJ0IO pin function	Count source input
Read from timer	The count value can be read out by reading the TRJ0 register.
Write to timer	• When the TRJ0 register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJ0 register is written during count operation, values are written to the reload register and counter (refer to **19.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRJ0IO input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRJ0IOC register. • Count source input pin select function Use of the TRJ0IO pin is selected by bits TRJ0IOSEL0 and TRJ0IOSEL1 in the TRJSR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRJ0IOC register. • Event input control function The enabled period for the event input to the TRJ0IO pin is selected by bits TIOGT0 and TIOGT1 in the TRJ0IOC register.

19.5.1 Timer RJ0 I/O Control Register (TRJ0IOC) in Event Counter Mode

Address 0081h (TRJ0IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJ0IO polarity switch bit (1)	0: Count at the rising edge of TRJ0IO input 1: Count at the falling edge of TRJ0IO input	R/W
b1	TOPCR	TRJ0IO output control bit	Set to 0 in event counter mode.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJ0IO input filter select bit (2)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJ0IO event input control bit	b7 b6 0 0: Event input always enabled 0 1: Event input enabled at $\overline{\text{INT2}}$ level (3) 1 0: Event input enabled at level of timer RC compare match signal (5) 1 1: Event input enabled for high-level period of timer RB output (4)	R/W
b7	TIOGT1			R/W

Notes:
1. Do not change the setting value of the TEDGSEL bit during count operation.
2. When the same value from the TRJ0IO pin is sampled three times continuously, the input is determined.
3. Set the INT2PL bit in the INTEN register to 0 (one edge).
   When the POL bit in the INT2IC register is set to 0 (falling edge selected), the event input for the $\overline{\text{INT2}}$ high-level period is enabled. When the POL bit is set to 1 (rising edge selected), the event input for the $\overline{\text{INT2}}$ low-level period is enabled.
4. In timer RJ0, the event input is enabled for the high-level period of the timer RB0 output.
5. In timer RJ, the event input of the corresponding timer RC compare match signal (TRCIOA, TRCIOB, TRCIOC, or TRCIOD) is enabled. Bits RCCPSEL0 and RCCPSEL1 in the TRJ0ISR register can be used to select the compare output from timer RC, and the RCCPSEL2 bit can be used to select the level of the timer RC compare match signal.

19.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRJ0IO pin is measured (refer to **Table 19.5**).
Figure 19.3 shows an Operating Example in Pulse Width Measurement Mode.

Table 19.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • The count is continued only while the measured pulse is high or low level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRJ0CR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJ0CR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJ0CR register.
Interrupt request generation timing	• When timer RJ0 underflows [timer RJ0 interrupt]. • Rising or falling of the TRJ0IO input (end of measurement period) [timer RJ0 interrupt]
TRJ0IO pin function	Measured pulse input
Read from timer	The count value can be read out by reading the TRJ0 register.
Write to timer	• When the TRJ0 register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJ0 register is written during count operation, values are written to the reload register and counter (refer to **19.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting A high-level or low-level period is selected by the TEDGSEL bit in the TRJ0IOC register. • Measured pulse input pin select function Use of the TRJ0IO pin is selected by bits TRJ0IOSEL0 and TRJ0IOSEL1 in the TRJSR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRJ0IOC register.

19.6.1 Timer RJ0 I/O Control Register (TRJ0IOC) in Pulse Width Measurement Mode

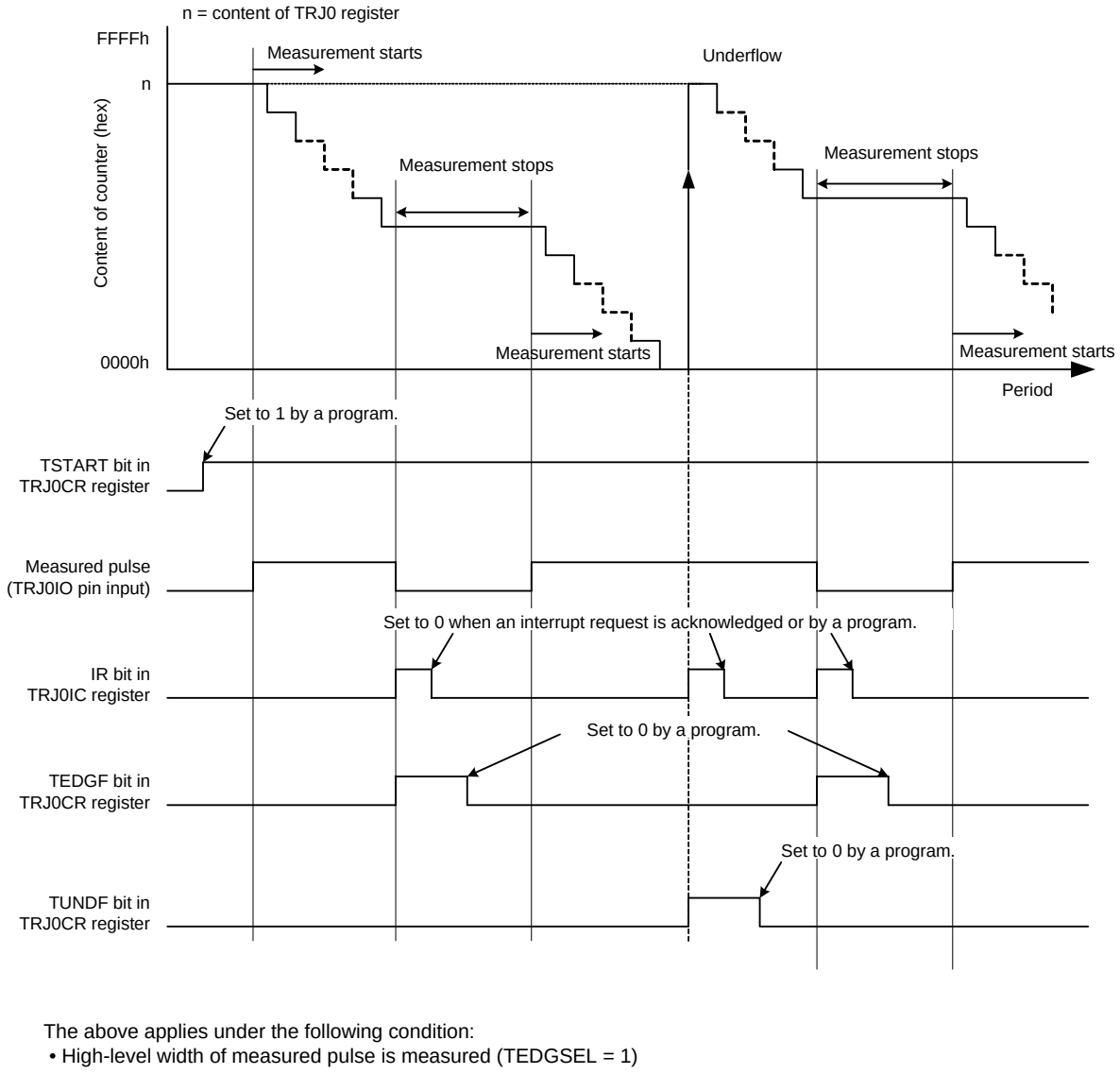
Address 0081h (TRJ0IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJ0IO polarity switch bit	0: Low-level width of TRJ0IO input is measured 1: High-level width of TRJ0IO input is measured	R/W
b1	TOPCR	TRJ0IO output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJ0IO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJ0IO event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRJ0IO pin is sampled three times continuously, the input is determined.

19.6.2 Operating Example



The above applies under the following condition:
- High-level width of measured pulse is measured (TEDGSEL = 1)

Figure 19.3 Operating Example in Pulse Width Measurement Mode

19.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRJ0IO pin is measured (refer to **Table 19.6**).
Figure 19.4 shows an Operating Example in Pulse Period Measurement Mode.

Table 19.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RJ0. Then timer RJ0 reloads the contents of the reload register at the second underflow and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRJ0CR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRJ0CR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJ0CR register.
Interrupt request generation timing	• When timer RJ0 underflows or reloads [timer RJ0 interrupt]. • Rising or falling of the TRJ0IO input (end of measurement period) [timer RJ0 interrupt]
TRJ0IO pin function	Measured pulse input
Read from timer	The count value can be read out by reading the TRJ0 register.
Write to timer	• When the TRJ0 register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJ0 register is written during count operation, values are written to the reload register and counter (refer to **19.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL bit in the TRJ0IOC register. • Measured pulse input pin select function Use of the TRJ0IO pin is selected by bits TRJ0IOSEL0 and TRJ0IOSEL1 in the TRJSR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRJ0IOC register.

19.7.1 Timer RJ0 I/O Control Register (TRJ0IOC) in Pulse Period Measurement Mode

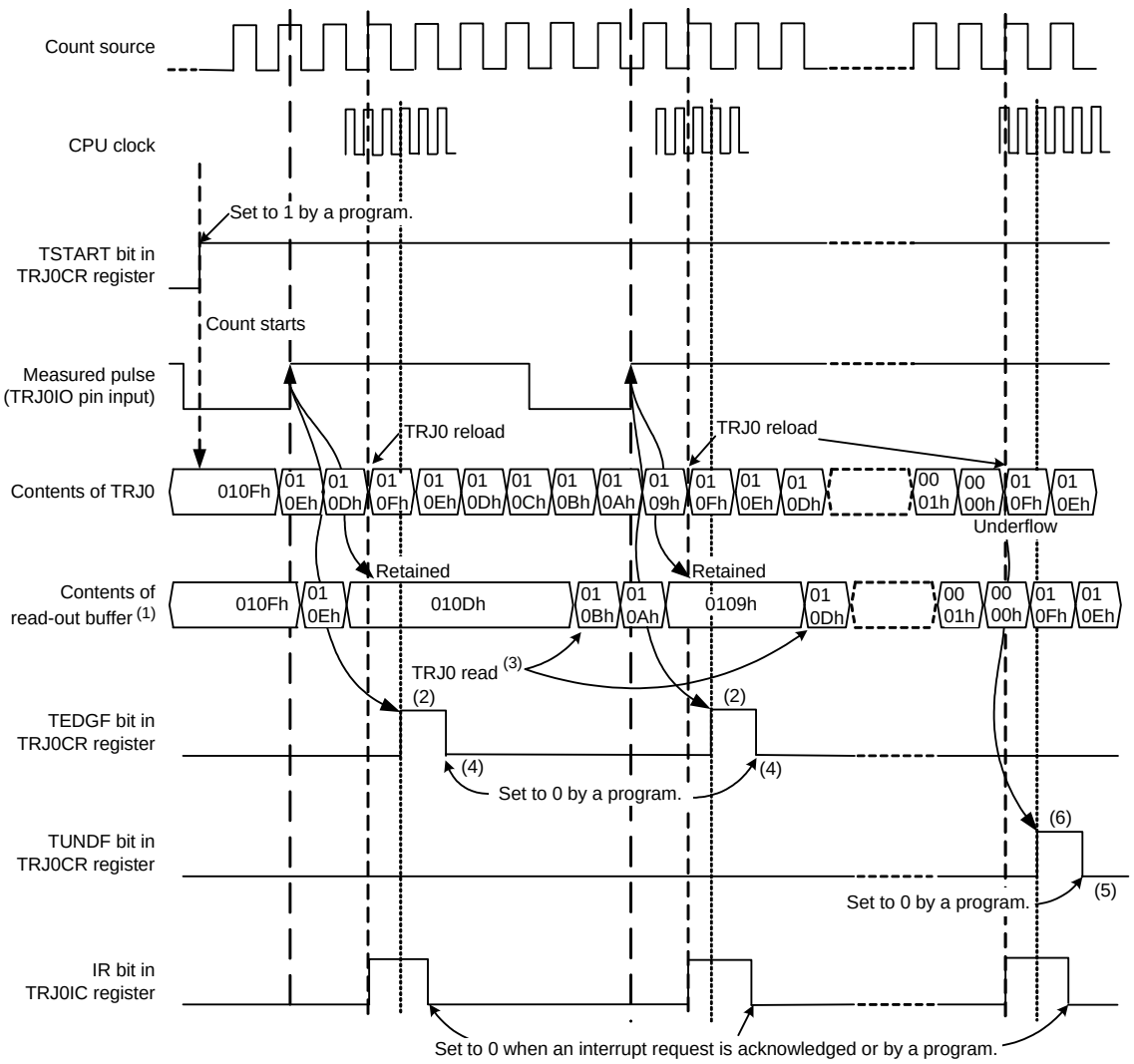
Address 0081h (TRJ0IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJ0IO polarity switch bit	0: Period from one rising edge to next rising edge of measured pulse is measured 1: Period from one falling edge to next falling edge of measured pulse is measured	R/W
b1	TOPCR	TRJ0IO output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJ0IO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJ0IO event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRJ0IO pin is sampled three times continuously, the input is determined.

19.7.2 Operating Example



The above applies when the initial value in the TRJ0 register is set to 010Fh and the period from one rising edge to the next rising edge of the measurement pulse is measured (TEDGSEL = 0).

Notes:
1. The content of the read-out buffer can be read by reading the TRJ0 register in pulse period measurement mode.
2. After the active edge of the measurement pulse is input, a TRJ0 reload occurs at the second rising edge of the count source. Then the TEDGF bit in the TRJ0CR register is set to 1 (active edge received) at the second rising edge of the CPU clock.
3. The TRJ0 register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents of the read-out buffer are retained until the TRJ0 register is read. If the TRJ0 register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRJ0CR register. At the same time, write 1 to the TUNDF bit.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit in the TRJ0CR register. At the same time, write 1 to the TEDGF bit.
6. When timer RJ0 underflows and reloads at the input of an active edge simultaneously, bits TUNDF and TEDGF are set to 1 at the second rising edge of the CPU clock after the underflow. If not, the TUNDF bit is set to 1 at the second rising edge of the CPU clock after the underflow.

Figure 19.4 Operating Example in Pulse Period Measurement Mode

19.8 Notes on Timer RJ

- Timer RJ0 stops counting after a reset. Set the values in the timer before the count starts.
- Read the timer in 16-bit units.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRJ0CR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRJ0CR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RJ0 underflow signal generated after the count starts.
- When using pulse period measurement mode, leave two or more periods of the timer RJ0 register immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit remains 0 (count stops) for zero or one cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RJ0 (1) other than the TCSTF bit.
  Timer RJ0 starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for zero or one cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RJ0 counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RJ0 (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RJ0: TRJ0CR, TRJ0IOC, TRJ0MR, and TRJ0

- When the TRJ0 register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- Do not set 0000h to the TRJ0 register in pulse width measurement mode and pulse period measurement mode.

20. Timer Extended Functions

20.1 Introduction

As extended functions of timer, there are the following two functions:

- Remote control carrier wave output function (timer RB1, timer RC)
- Remote control carrier wave input function (timer RB0, timer RJ0)

20.2 Register

20.2.1 Timer Carrier Wave I/O Control Register (TRCRIO)

Address 0190h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRJCRUND	TRJCREDG	—	TRJCRI	—	—	—	TRCCR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCCR0	Carrier wave output control bit	0: Normal 1: Carrier wave output	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	TRJCRI	Carrier wave input control bit	0: Normal 1: Carrier wave output	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRJCREDG	Measurement period end edge interrupt signal enable select bit	0: Off 1: On	R/W
b7	TRJCRUND	Underflow signal enable select bit	0: Off 1: On	R/W

20.3 Remote Control Carrier Wave Output Function

This function is used to output a remote control carrier waveform by combining outputs of timer RB1 and timer RC.

When an output waveform in programmable waveform generation mode of timer RB1 is selected as the count source for PWM mode of timer RC, this function is used to output a waveform generated by ANDing inverted output of timer RC at that time and output of timer RB1.

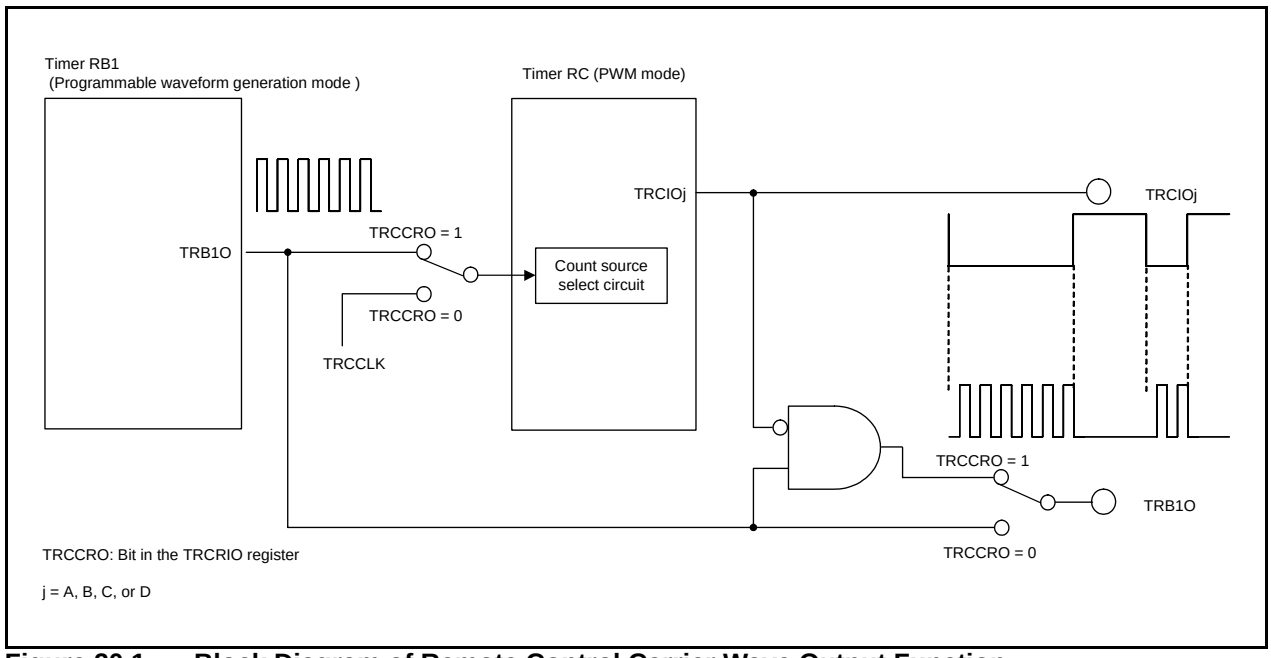


Figure 20.1 Block Diagram of Remote Control Carrier Wave Output Function

20.4 Operating Waveform

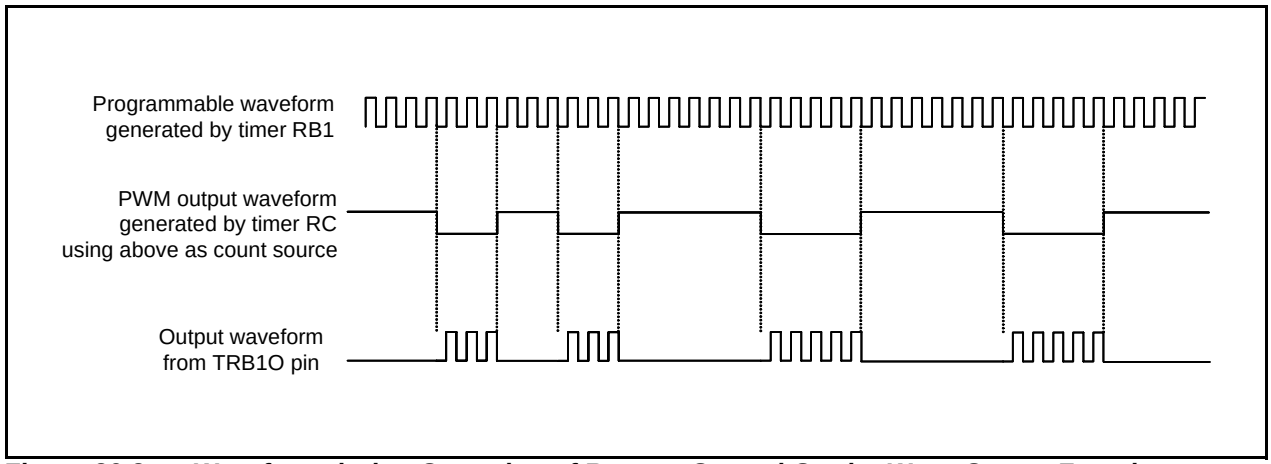


Figure 20.2 Waveform during Operation of Remote Control Carrier Wave Output Function

20.5 Remote Control Carrier Wave Input Function

This function can be used to combine an underflow of timer RJ0 and a measurement period end edge interrupt signal of timer RJ0 (in pulse period measurement mode) as the count source for timer RB0.
When an underflow of timer RJ0 is selected as the count source for timer RB0 and the TRJCRI bit is set to 1 (carrier wave input), one of the following can be selected as a count source depending on the combination of bits TRJCRUND and TRJCREDG.

- Both underflow of timer RJ0 and measurement period end edge interrupt signal
- Underflow of timer RJ0 only
- Measurement period end edge interrupt signal only

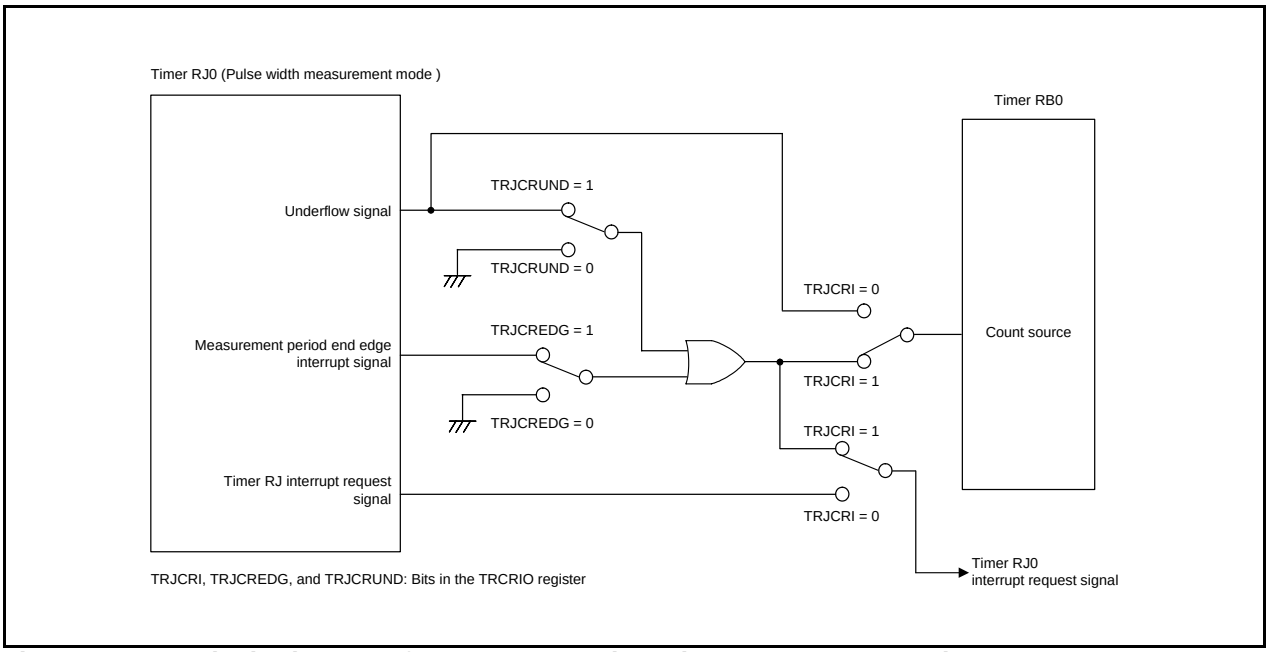


Figure 20.3 Block Diagram of Remote Control Carrier Wave Input Function

20.6 Operating Waveform

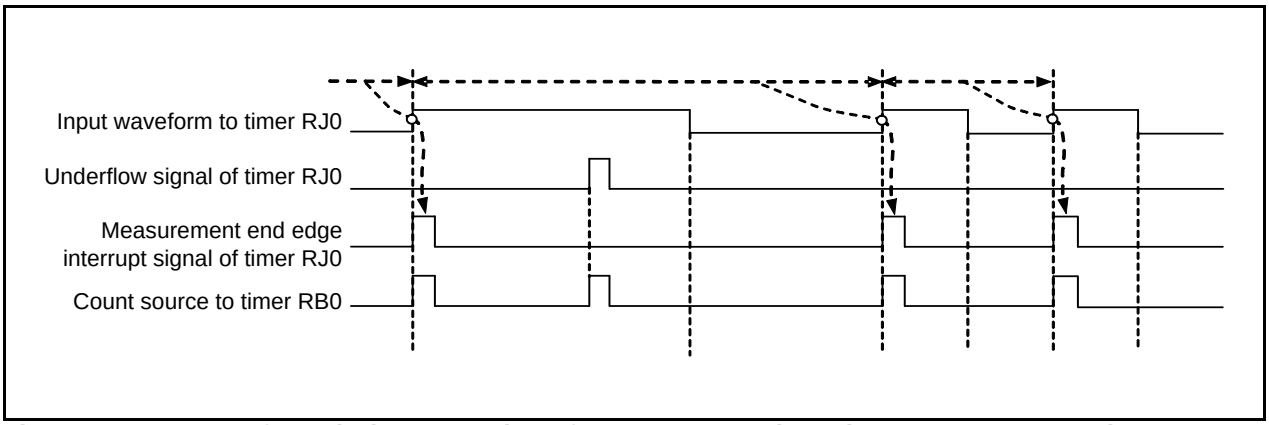


Figure 20.4 Waveform during Operation of Remote Control Carrier Wave Input Function (TRJCRUND = 1, TRJCREDG = 1, Timer RJ0: Pulse Width Measurement Mode)

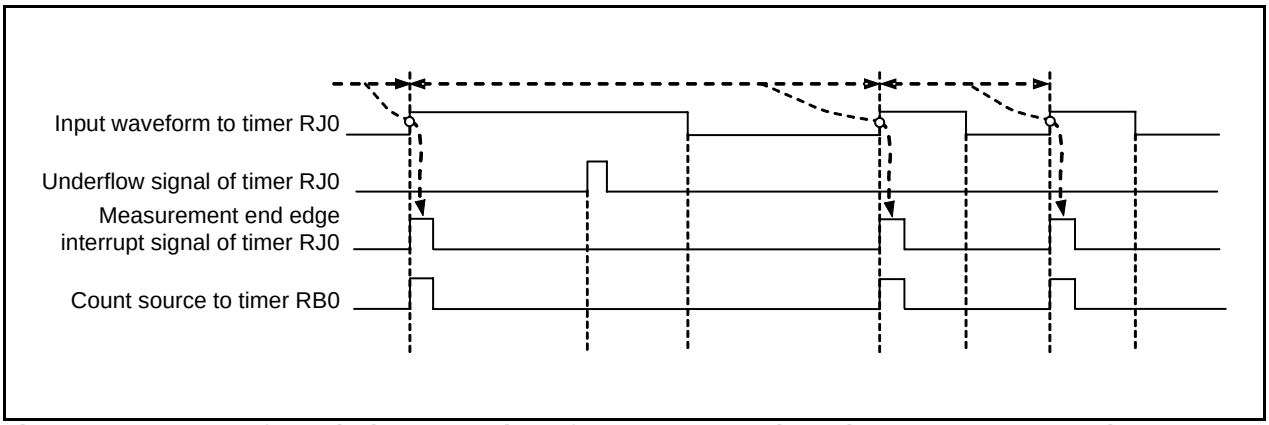


Figure 20.5 Waveform during Operation of Remote Control Carrier Wave Input Function (TRJCRUND = 0, TRJCREDG = 1, Timer RJ0: Pulse Width Measurement Mode)

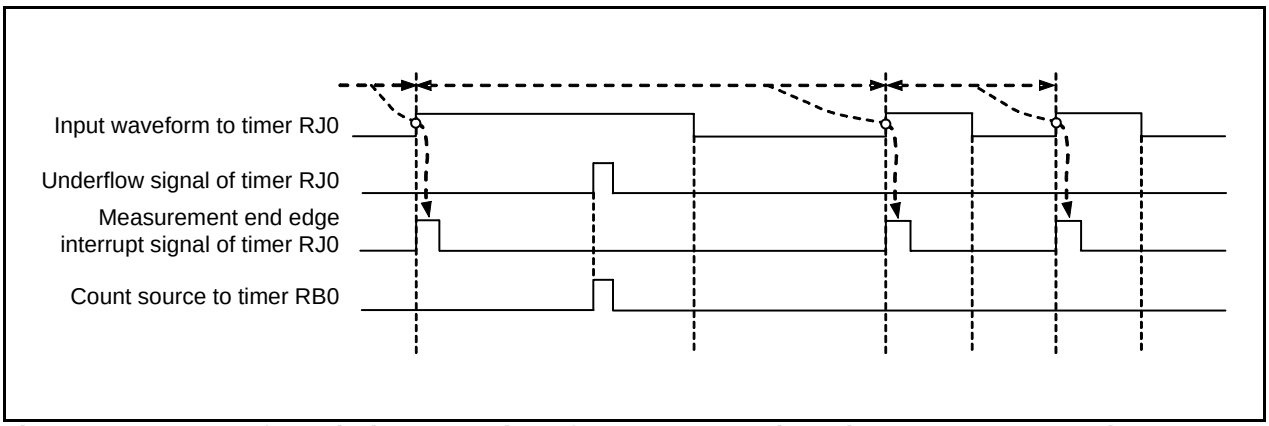
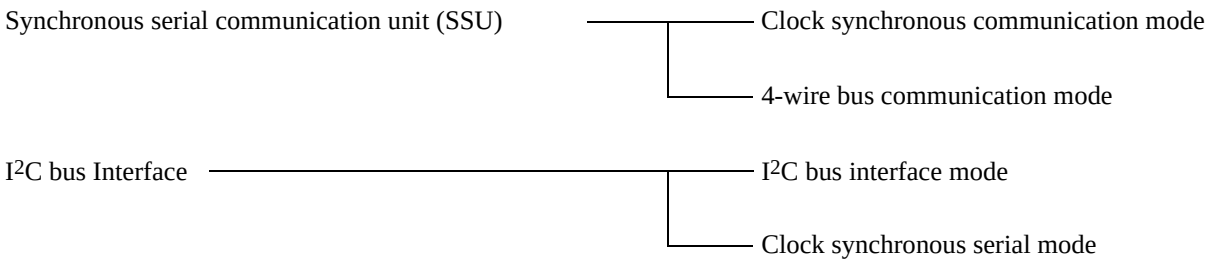


Figure 20.6 Waveform during Operation of Remote Control Carrier Wave Input Function TRJCRUND = 1, TRJCREDG = 0, Timer RJ0: Pulse Width Measurement Mode

21. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock synchronous serial interface



The clock synchronous serial interface uses the registers at addresses 0193h to 019Dh. Registers, bits, symbols, and functions vary even for the same addresses depending on the mode. Refer to the registers of each function for details. Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format, and data output format.

21.1 Mode Selection

The clock synchronous serial interface supports four modes.

Table 21.1 lists the Mode Selections. Refer to **22. Synchronous Serial Communication Unit (SSU)**, **23. I2C bus Interface** and the sections that follow for details of each mode.

Table 21.1 Mode Selections

IICSEL Bit in SSUIICSR Register	Bit 7 in 0198h (ICE Bit in ICCR1 Register)	Bit 0 in 019Dh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Synchronous serial communication unit	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

22. Synchronous Serial Communication Unit (SSU)

22.1 Introduction

The synchronous serial communication unit (SSU) supports clock synchronous serial data communication. Table 22.1 shows the Synchronous Serial Communication Unit Specifications. Figure 22.1 shows a Block Diagram of Synchronous Serial Communication Unit.

Table 22.1 Synchronous Serial Communication Unit Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 to 16 bits Continuous transmission and reception of serial data are enabled since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin SSO (I/O): Data I/O pin SCS (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operation as a slave device), an external clock is selected (input from the SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operation as the master device), an internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from the SSCK pin) is selected. • The clock polarity and the phase of SSCK can be selected.
Receive error detection	• Overrun error An overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when the next serial data reception is completed, the ORER bit in the SSSR register is set to 1 (overrun error).
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operation as the master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 (conflict error) if a low-level signal applies to the SCS pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operation as a slave device) and the SCS pin input changes state from low to high, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit end, transmit data empty, receive data full, overrun error, and conflict error) (1).
Selectable functions	• Data transfer direction Selectable MSB first or LSB first • SSCK clock polarity Selectable a low or high level when the clock stops • SSCK clock phase Selectable edges for data change and data download

Note:
1. All sources use a single interrupt vector table for the synchronous serial communication unit.

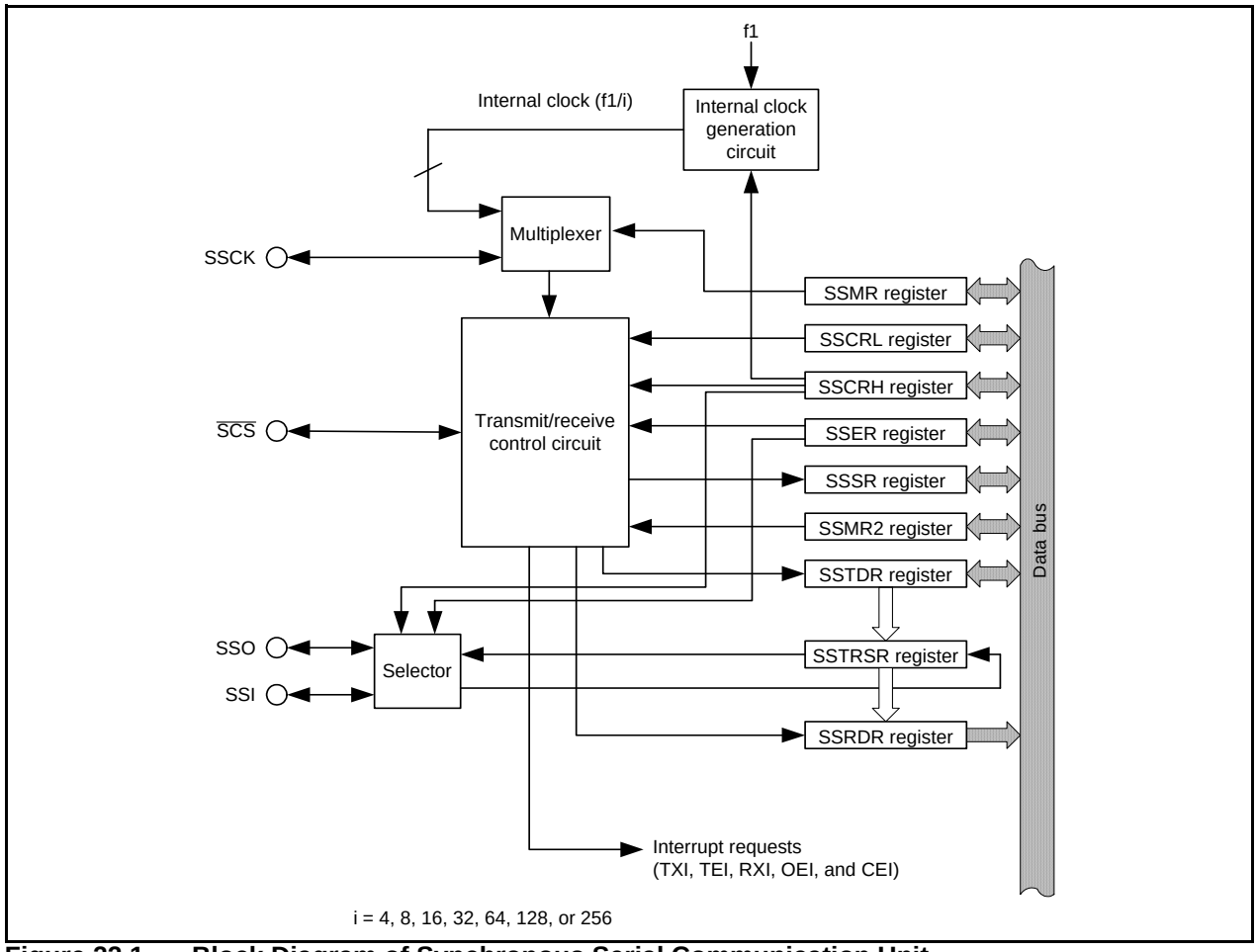


Figure 22.1 Block Diagram of Synchronous Serial Communication Unit

Table 22.2 Pin Configuration of Synchronous Serial Communication Unit

Pin Name	Assigned Pin	I/O	Function
SSI	P8_1	I/O	Data I/O
$\overline{\text{SCS}}$	P8_0	I/O	Chip-select signal I/O
SSCK	P8_2	I/O	Clock I/O
SSO	P8_3	I/O	Data I/O

22.2 Registers

22.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	—	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	Reseved bit	Set to 1.	R/W
b2	—	Reseved bit	Set to 0.	R/W
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTLCD	Reseved bit	Set to 1.	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	Reseved bit	Set to 1.	R/W

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

22.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I²C bus switch bit	0: SSU function selected 1: I²C bus function selected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

22.2.3 SS Bit Counter Register (SSBR)

Address 0193h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bit (1)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Note:
1. Do not write to bits BS0 to BS3 during SSU operation.

To set the SSBR register, set the RE bit in the SSER register to 0 (reception disabled) and the TE bit to 0 (transmission disabled).

Bits BS0 to BS3 (SSU Data Transfer Length Set Bit)

From 8 to 16 bits can be used as the SSU data transfer length.

22.2.4 SS Transmit Data Register (SSTDR)

Address 0195h to 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	This register stores transmit data. (1) When the SSTRSR register is detected as empty, the stored transmit data is transferred to the SSTRSR register and transmission starts. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, continuous transmission is enabled. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB first), the MSB-LSB inverted data is read after writing to the SSTDR register.	R/W

Note:
1. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSTDR register in 16-bit units.

22.2.5 SS Receive Data Register (SSRDR)

Address 0197h to 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	This register stores receive data. (1, 2) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next reception is enabled. Continuous reception is enabled using registers SSTRSR and SSRDR.	R

Notes:
1. When the ORER bit in the SSSR register is set to 1 (overrun error), the SSRDR register retains the data received before an overrun error occurs. When an overrun error occurs, the receive data is discarded.
2. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSRDR register in 16-bit units.

22.2.6 SS Control Register H (SSCRH)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RSSTP	MSS	—	—	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bit (1)	b2 b1 b0 0 0 0: f1/256 0 0 1: f1/128 0 1 0: f1/64 0 1 1: f1/32 1 0 0: f1/16 1 0 1: f1/8 1 1 0: f1/4 1 1 1: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	MSS	Master/slave device select bit (2)	0: Operation as a slave device 1: Operation as the master device	R/W
b6	RSSTP	Receive single stop bit (3)	0: Receive operation is continued after receiving 1 byte of data 1: Receive operation is completed after receiving 1 byte of data	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The set clock is used when the MSS bit is set to 1 (operates as master device).
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operation as the master device). The MSS bit is set to 0 (operation as a slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operation as a slave device).

22.2.7 SS Control Register L (SSCRL)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	SOL	SOLP	—	—	SRES	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	SRES	SSU control unit reset bit	When 1 is written to this bit, the SSU control unit and the SSTRSR register are reset. The value of the SSU internal register (1) is retained.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	—			
b4	SOLP	SOL write protect bit (2)	When 0 is written to this bit, the output level can be changed by the SOL bit. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	R/W
b5	SOL	Serial data output value setting bit	When read 0: Serial data output is low 1: Serial data output is high When written (2, 3) 0: Data output is low 1: Data output is high	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Registers SSBR, SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained.
   If the content of the SOL bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output.
   When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

22.2.8 SS Mode Register (SSMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter 3 to 0	b3 b2 b1 b0 0 0 0 0: 16 bits left 0 0 0 1: 1 bit left 0 0 1 0: 2 bits left 0 0 1 1: 3 bits left 0 1 0 0: 4 bits left 0 1 0 1: 5 bits left 0 1 1 0: 6 bits left 0 1 1 1: 7 bits left 1 0 0 0: 8 bits left 1 0 0 1: 9 bits left 1 0 1 0: 10 bits left 1 0 1 1: 11 bits left 1 1 0 0: 12 bits left 1 1 0 1: 13 bits left 1 1 1 0: 14 bits left 1 1 1 1: 15 bits left	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	CPHS	SSCK clock phase select bit (1)	0: Data change at odd edges (Data download at even edges) 1: Data change at even edges (Data download at odd edges)	R/W
b6	CPOS	SSCK clock polarity select bit (1)	0: High when clock stops 1: Low when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Transfer data with MSB first 1: Transfer data with LSB first	R/W

Note:

1. Refer to **22.3.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of bits CPHS and CPOS.
   When the SSUMS bit in the SSMR2 register is set to 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS bit to 0.

22.2.9 SS Enable Register (SSER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE	RE	—	—	CEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE	Conflict error interrupt enable bit	0: Conflict error interrupt request disabled 1: Conflict error interrupt request enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b4	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt requests disabled 1: Receive data full and overrun error interrupt requests enabled	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

22.2.10 SS Status Register (SSSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	—	—	ORER	—	CE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE	Conflict error flag (1)	0: No conflict error 1: Conflict error (2)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	ORER	Overrun error flag (1)	0: No overrun error 1: Overrun error (3)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	RDRF	Receive data register full flag (1, 4)	0: No data in the SSRDR register 1: Data in the SSRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: TDRE bit is set to 0 when transmitting the last bit of transmit data 1: TDRE bit is set to 1 when transmitting the last bit of transmit data	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: No data transferred from registers SSTDR to SSTRSR 1: Data transferred from registers SSTDR to SSTRSR	R/W

Notes:

1. Writing 1 to the CE, ORER, RDRF, TEND, or TDRE bit is disabled. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operation as the master device), the CE bit is set to 1 if a low-level signal is applied to the $\overline{SCS}$ pin input. Refer to **22.5.4 SCS Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operation as a slave device) and the $\overline{SCS}$ pin input changes the level from low to high during transfer, the CE bit is set to 1.
3. Indicates when an overrun error occurs during reception and completes in error. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1.
   After the ORER bit is set to 1 (overrun error), receive operation is disabled while the bit remains 1. Transmit operation is also disabled while the MSS bit is set to 1 (operation as the master device).
4. The RDRF bit is set to 0 when reading the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
   When reading these bits immediately after writing to the SSTDR register, insert three or more NOP instructions between the instructions used for writing and reading.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmission enabled).

To access the SSSR register successively, insert one or more NOP instructions between the instructions used for access.

22.2.11 SS Mode Register 2 (SSMR2)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	SSUMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SSUMS	SSU mode select bit (1)	0: Clock synchronous communication mode 1: 4-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data open-drain output select bit (1)	0: CMOS output (5) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bit (2)	b5 b4 0 0: Function as a port 0 1: Function as the $\overline{SCS}$ input pin 1 0: Function as the $\overline{SCS}$ output pin (3) 1 1: Function as the $\overline{SCS}$ output pin (3)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Function as a port 1: Function as the serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 4)	0: Standard mode (communication using 2 pins of data input and data output) 1: Bidirectional mode (communication using 1 pin of data input and data output)	R/W

Notes:
1. Refer to **22.3.2.1 Association between Data I/O Pins and SS Shift Register** for information on the combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. When the SOOS bit is set to 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).

22.3 Common Items for Multiple Modes

22.3.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.
To use the synchronous serial communication unit, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.
When the MSS bit in the SSCRH register is set to 1 (operation as the master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs a clock at the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.
When the MSS bit in the SSCRH register is set to 0 (operation as a slave device), an external clock can be selected and the SSCK pin functions as input.

22.3.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase, and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register.
Figure 22.2 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.
Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

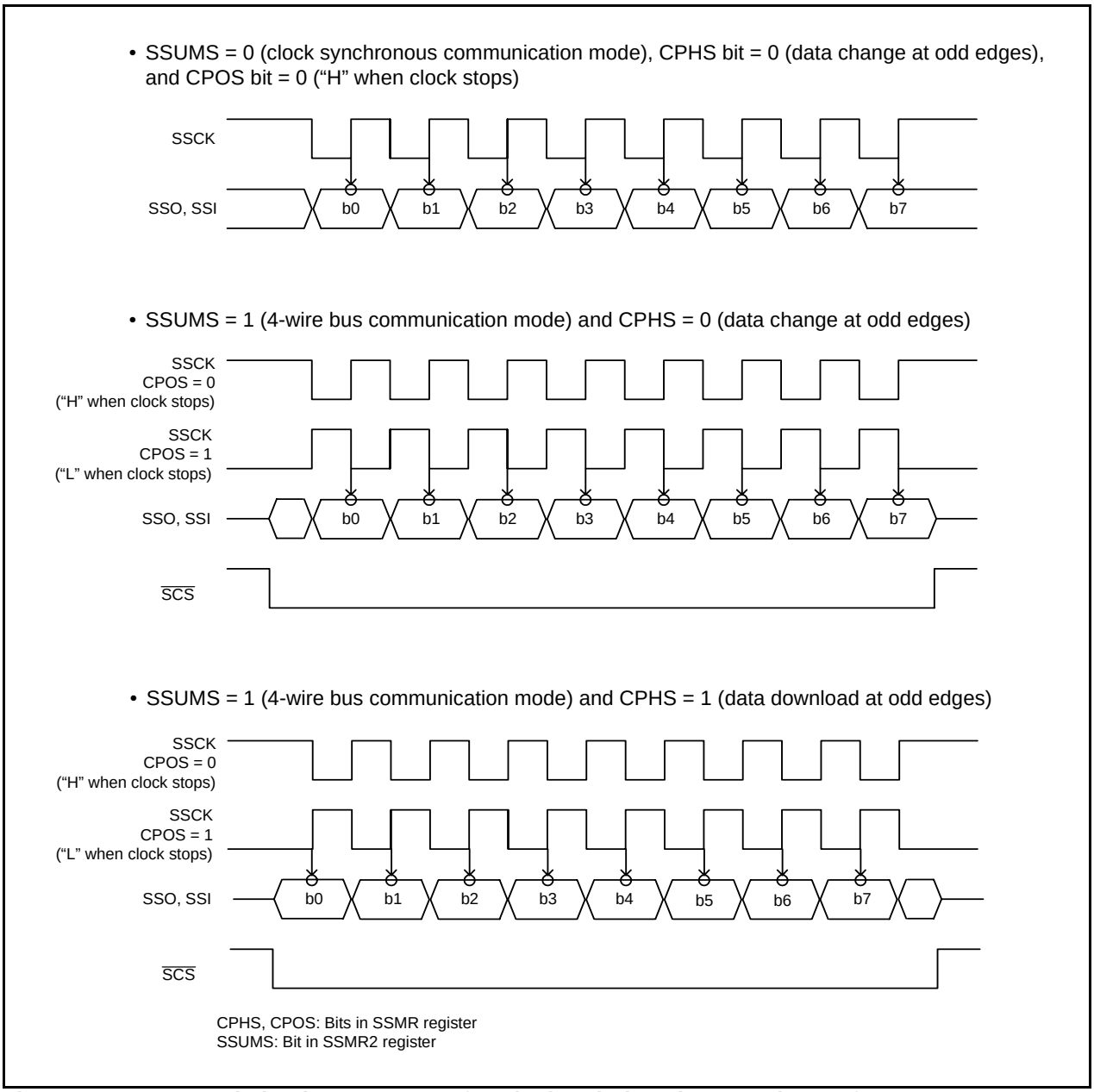


Figure 22.2 Association between Transfer Clock Polarity, Phase, and Transfer Data

22.3.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB first), bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

22.3.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and the SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register.
Figure 22.3 shows the Association between Data I/O Pins and SSTRSR Register.

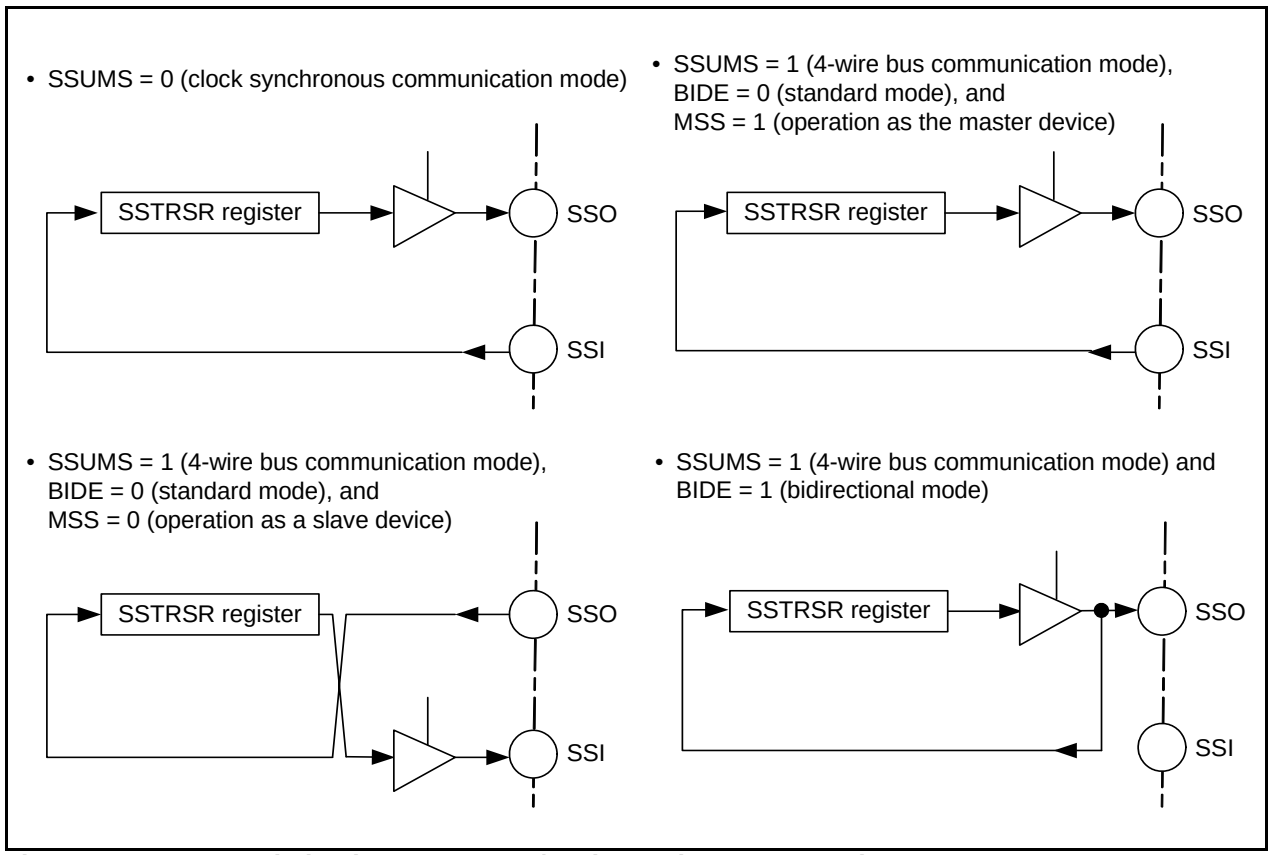


Figure 22.3 Association between Data I/O Pins and SSTRSR Register

22.3.3 Interrupt Requests

The synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, determining interrupt sources by flags is required.
Table 22.3 shows the Interrupt Requests of Synchronous Serial Communication Unit.

Table 22.3 Interrupt Requests of Synchronous Serial Communication Unit

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1 and TDRE = 1
Transmit end	TEI	TEIE = 1 and TEND = 1
Receive data full	RXI	RIE = 1 and RDRF = 1
Overrun error	OEI	RIE = 1 and ORER = 1
Conflict error	CEI	CEIE = 1 and CE = 1

CEIE, RIE, TEIE, TIE: Bits in SSER register
ORER, RDRF, TEND, TDRE: Bits in SSSR register

If the generation conditions in Table 22.3 are met, an interrupt request of the synchronous serial communication unit is generated. Set each interrupt source to 0 by the synchronous serial communication unit interrupt routine.

However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. If the TDRE bit is further set to 0 (data not transferred from registers SSTDR to SSTRSR), additional 1 byte may be transmitted.

22.3.4 Communication Modes and Pin Functions

The synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 22.4 shows the Association between Communication Modes and I/O Pins.

Table 22.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	— (1)	Input
				1	0	— (1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	— (1)	Input	Input
				1	0	Output	— (1)	Input
					1	Output	Input	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (2)	1	1	0	0	1	— (1)	Input	Input
				1	0	— (1)	Output	Input
			1	0	1	— (1)	Input	Output
				1	0	— (1)	Output	Output

Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS, BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE, RE: Bits in SSER register

22.4 Clock Synchronous Communication Mode

22.4.1 Initialization in Clock Synchronous Communication Mode

Figure 22.4 shows Initialization in Clock Synchronous Communication Mode. Before data transmission or reception, set the TE bit in the SSER register to 0 (transmission disabled) and the RE bit to 0 (reception disabled), and initialize the synchronous serial communication unit.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.

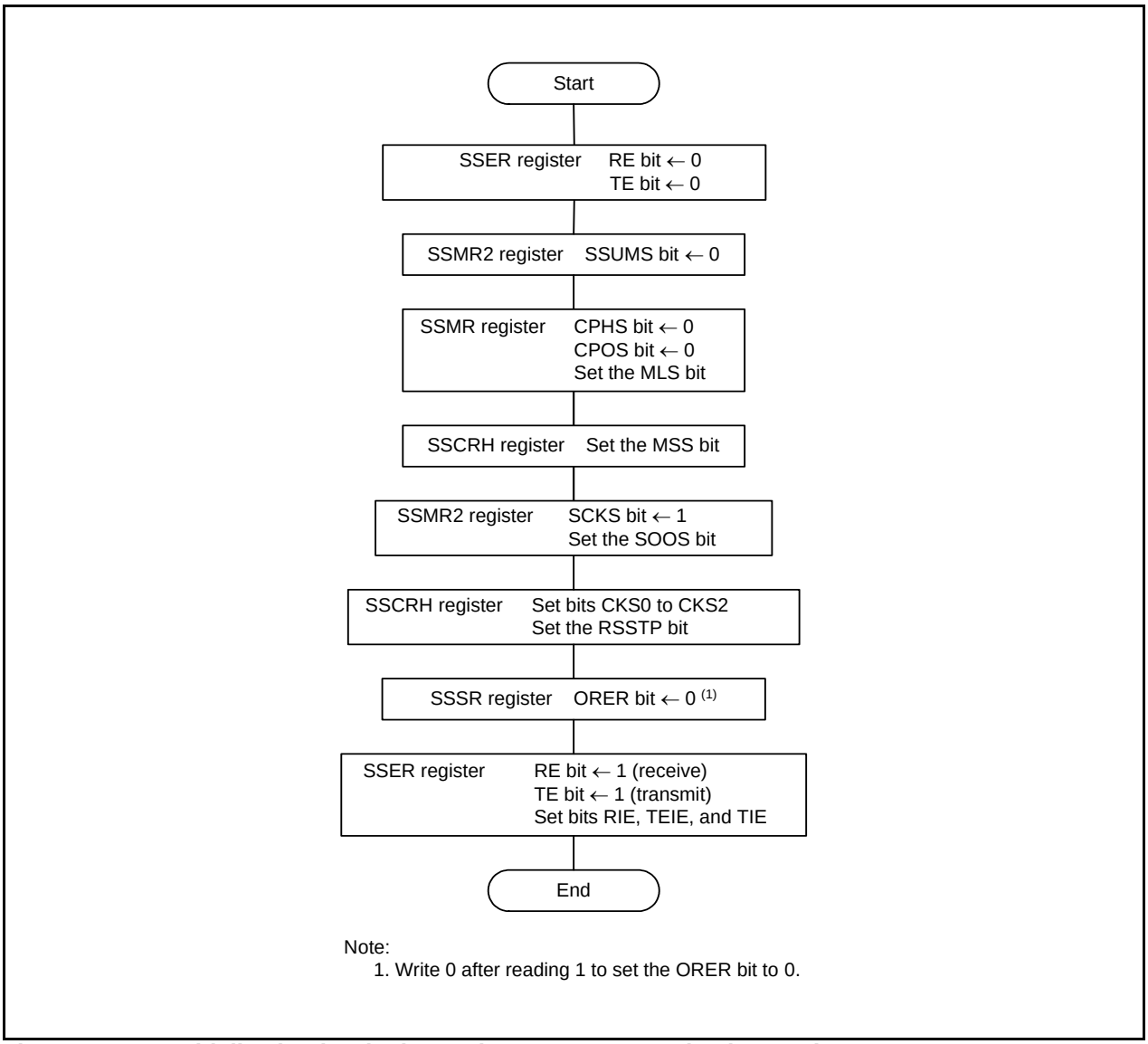


Figure 22.4 Initialization in Clock Synchronous Communication Mode

22.4.2 Data Transmission

Figure 22.5 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and data. When the synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit in the SSER register is set to 1 (transmission enabled) before writing the transmit data to the SSTDR register, the TDRE bit in the SSSR register is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, a TXI interrupt request is generated.

When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, a TEI interrupt request is generated. The SSCK pin is fixed high after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 (no overrun error) before transmission.

Figure 22.6 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

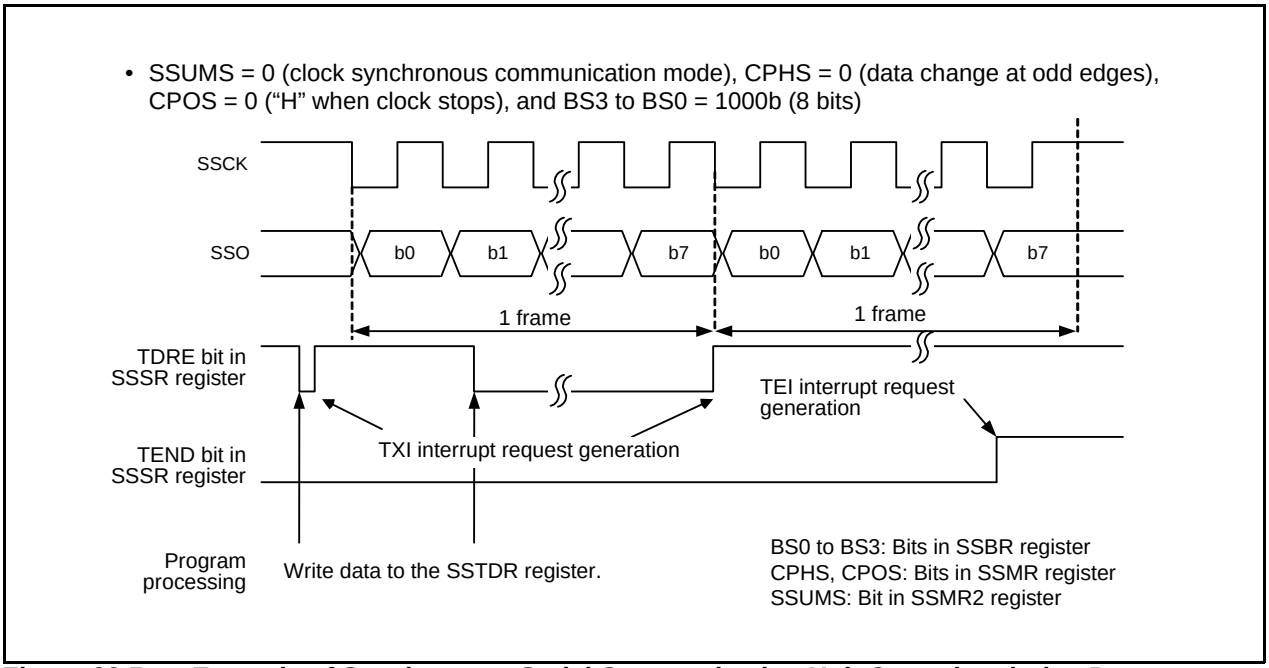
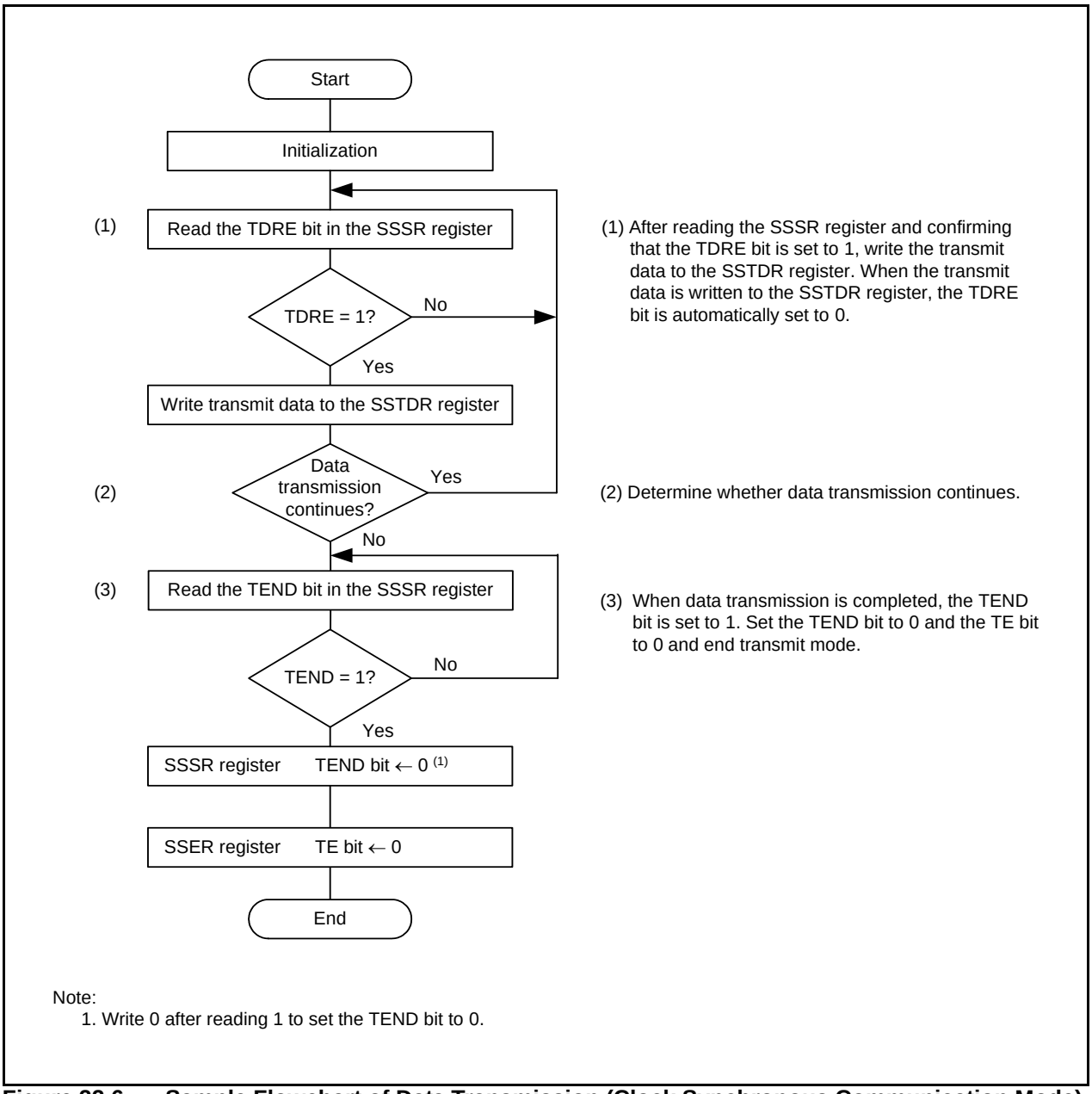


Figure 22.5 Example of Synchronous Serial Communication Unit Operation during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)



Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 22.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

22.4.3 Data Reception

Figure 22.7 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When the synchronous serial communication unit is set as a slave device, it inputs data synchronized with the input clock.

When the synchronous serial communication unit is set as the master device, it outputs a receive clock and starts receiving by performing dummy read from the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. If the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

When the synchronous serial communication unit operates as a master device and finish the data reception, read the receive data after setting the RSSTP bit in the SSCRH register to 1 (receive operation is completed after receiving 1 byte of data). The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (reception enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

Figure 22.8 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

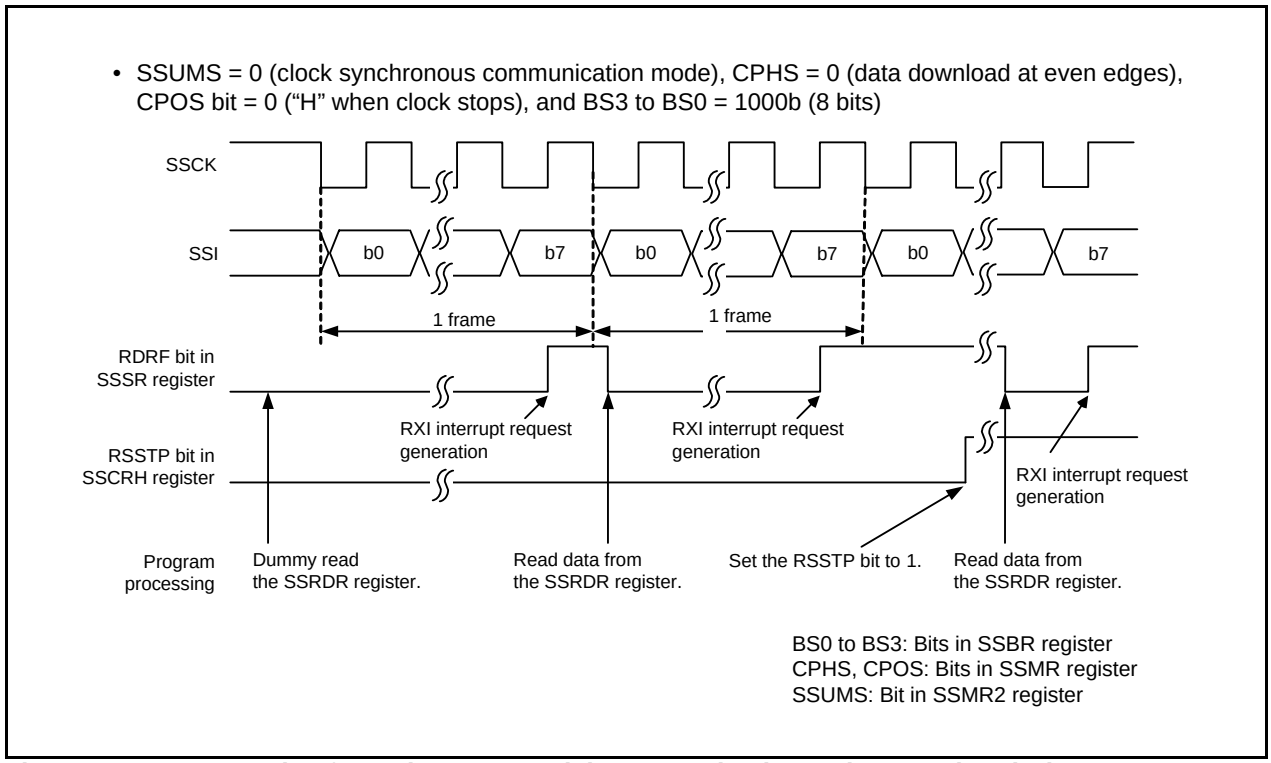


Figure 22.7 Example of Synchronous Serial Communication Unit Operation during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

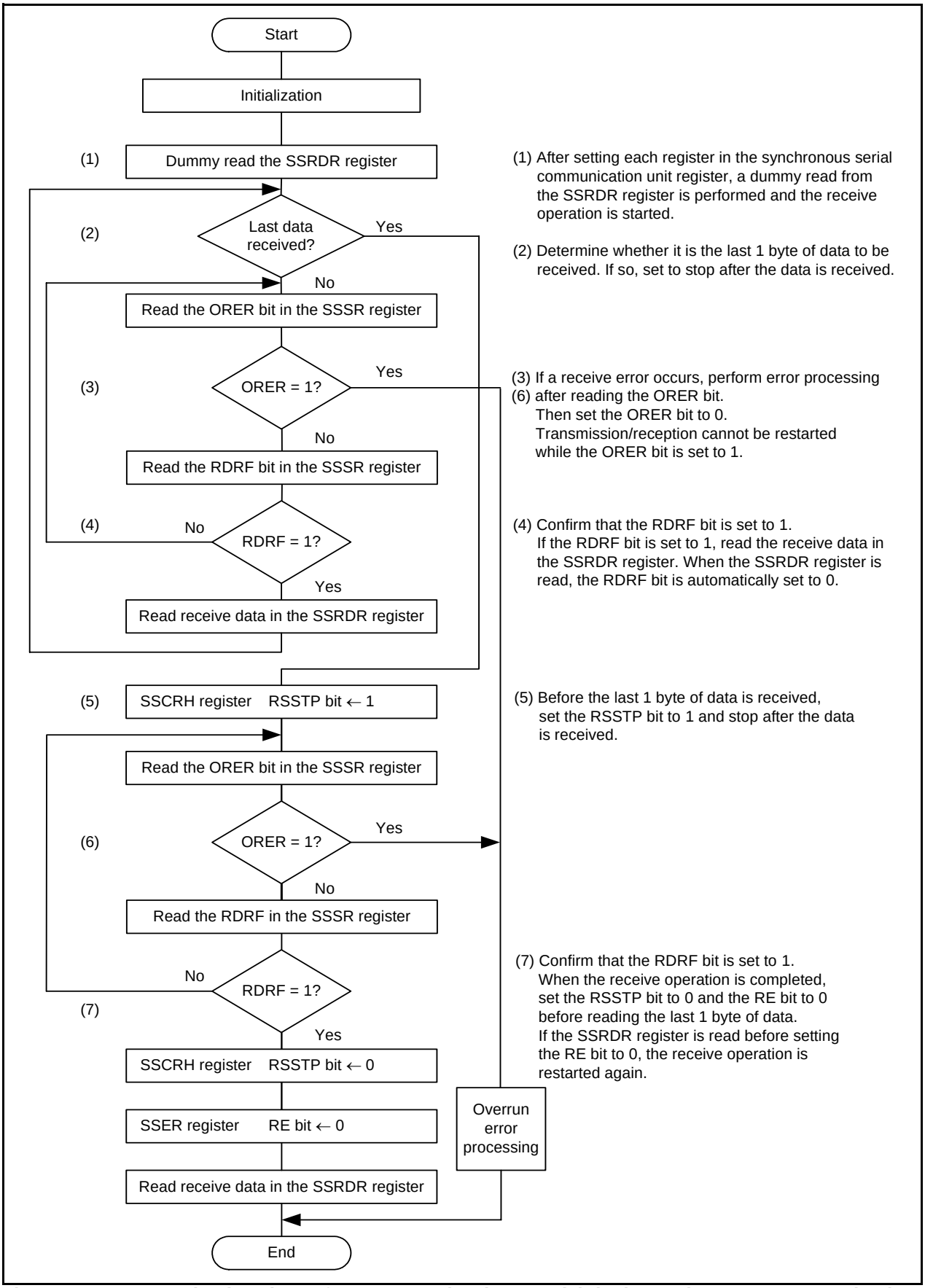


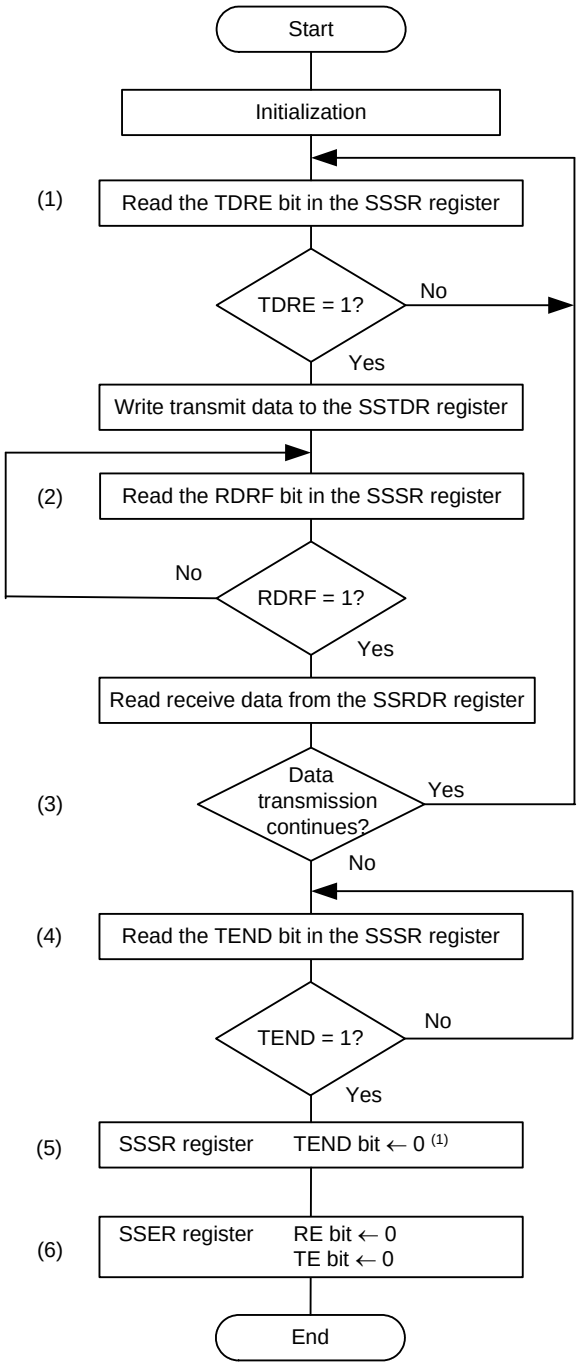
Figure 22.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

22.4.3.1 Data Transmission/Reception

Data transmission/reception is an operation combining data transmission and reception which were described earlier. Transmission/reception is started by writing data to the SSTDR register.
When the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.
Before switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (TE = RE = 1), set the TE bit to 0 (transmission disabled) and RE bit to 0 (reception disabled) once. After confirming that the TEND bit is set to 0 (TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1 (transmission enabled/reception enabled).
Figure 22.9 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).
When exiting transmit/receive mode after this mode is used (TE = RE = 1), a clock may be output if transmit/receive mode is exited after reading the SSRDR register. To avoid any clock outputs, perform either of the following:

- First set the RE bit to 0, and then set the TE bit to 0.
- Set bits TE and RE at the same time.

When subsequently switching to receive mode (TE = 0 and RE = 1), first set the SRES bit in the SSCRL register to 1, and set this bit to 0 to reset the SSU control unit and the SSTRSR register. Then, set the RE bit to 1.



(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.

(2) Confirm that the RDRF bit is set to 1. If the RDRF bit is set to 1, read receive data in the SSRDR register. When the SSRDR register is read, the RDRF bit is automatically set to 0.

(3) Determine whether data transmission continues.

(4) When the data transmission is completed, the TEND bit in the SSSR register is set to 1.

(5) Set the TEND bit to 0, and bits RE and TE
(6) in the SSER register to 0 before ending transmit/receive mode.

Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 22.9 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

22.5 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **22.3.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, the clock polarity, phase, and data settings are performed by using bits CPOS and CPHS in the SSMR register. For details, refer to **22.3.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When the synchronous serial communication unit is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{SCS}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{SCS}$ pin as input by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB first.

22.5.1 Initialization in 4-Wire Bus Communication Mode

Figure 22.10 shows Initialization in 4-Wire Bus Communication Mode. Before the data transmit/receive operation, set the TE bit in the SSER register to 0 (transmission disabled), the RE bit in the SSER register to 0 (reception disabled), and initialize the synchronous serial communication unit.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.

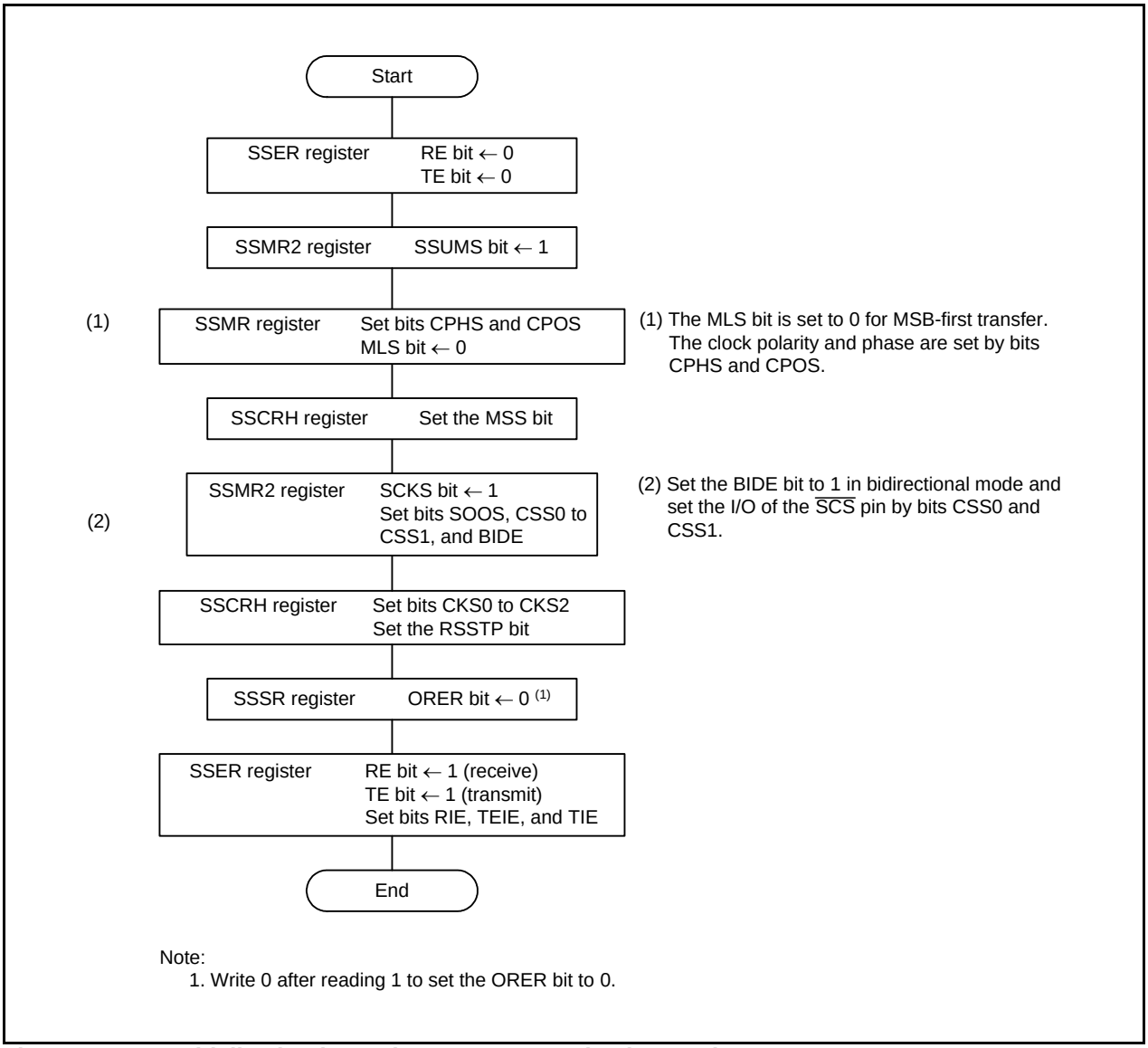


Figure 22.10 Initialization in 4-Wire Bus Communication Mode

22.5.2 Data Transmission

Figure 22.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During the data transmit operation, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and data. When the synchronous serial communication unit is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is low-input state.

When the transmit data is written to the SSTDR register after setting the TE bit in the SSER register to 1 (transmission enabled), the TDRE bit in the SSSR register is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, the TXI interrupt request is generated.

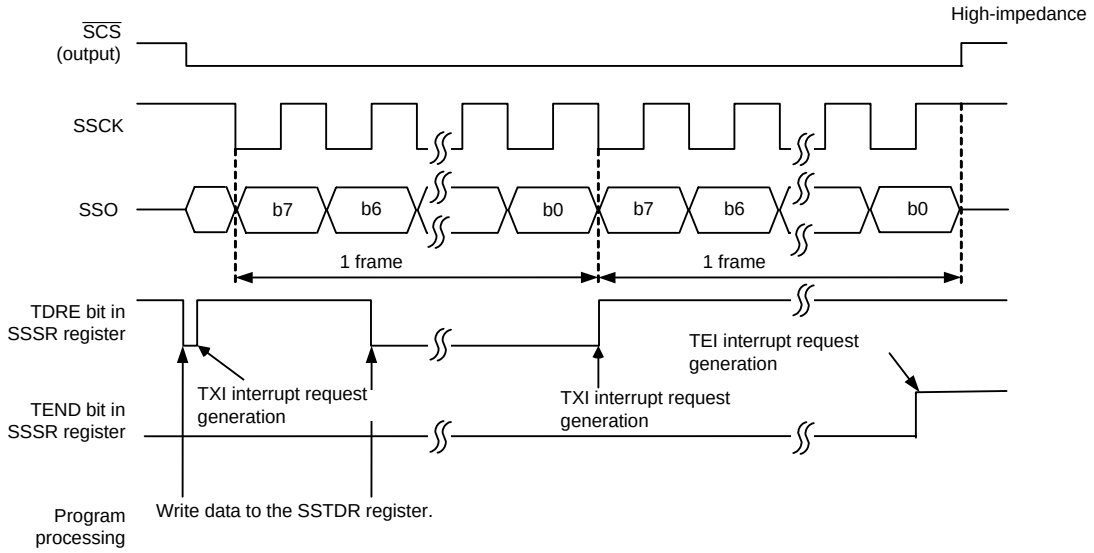
After one frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, the TEI interrupt request is generated. The SSCK pin remains high after transmit-end and the $\overline{SCS}$ pin is held high. When transmitting continuously while the $\overline{SCS}$ pin is held low, write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 (no overrun error) before transmission.

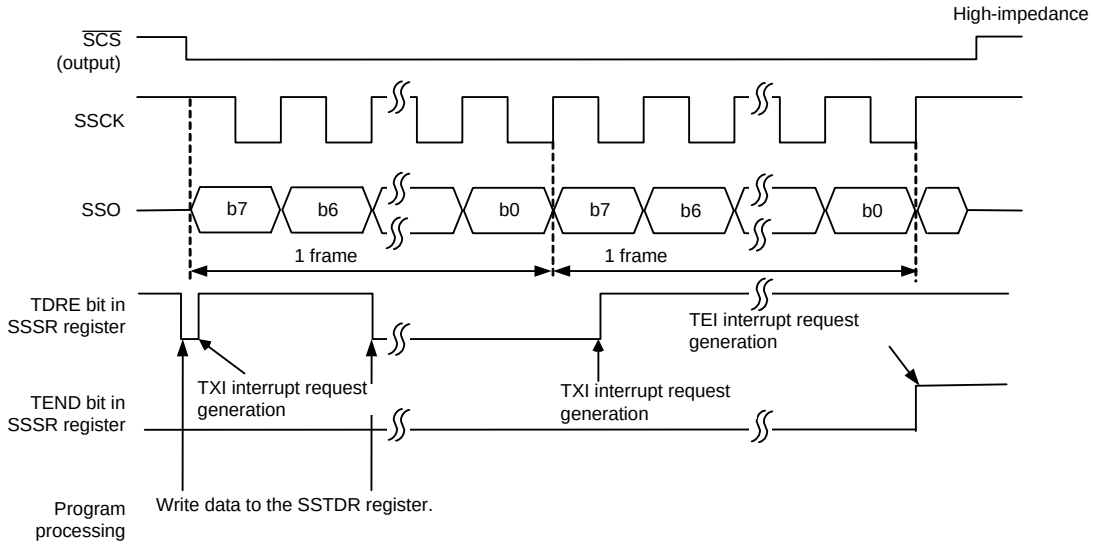
In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as the master device. The SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is high-input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 22.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data change at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data change at even edges). CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 22.11 Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

22.5.3 Data Reception

Figure 22.12 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When the synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin is low-input state.

When the synchronous serial communication unit is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read from the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

When the synchronous serial communication unit operates as a master device and finish the data reception, read the receive data after setting the RSSTP bit in the SSCRH register to 1 (receive operation is completed after receiving 1-byte data). The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (reception enabled), a receive clock is output again.

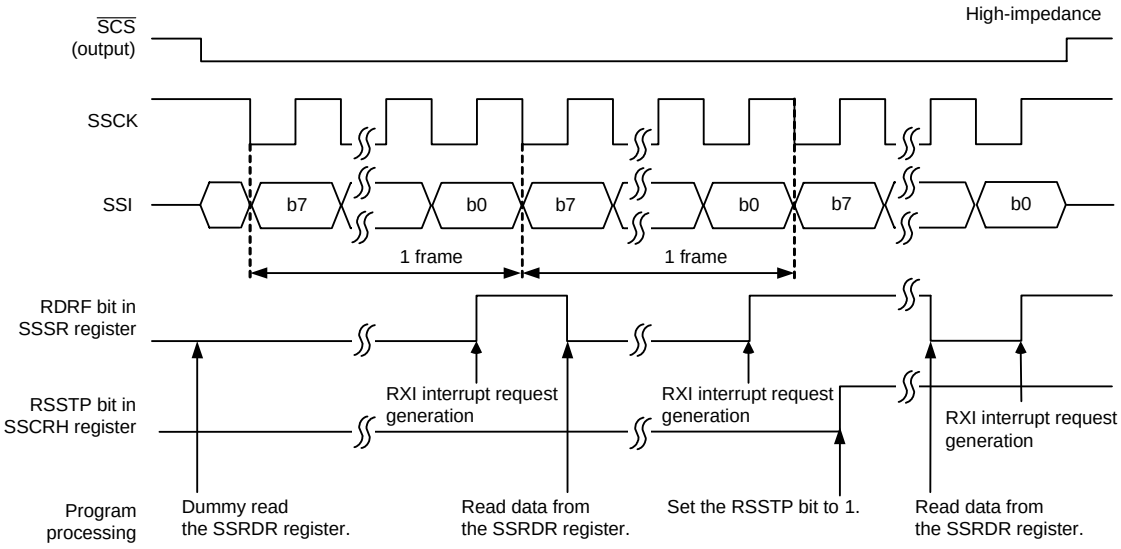
When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 (no overrun error) before restarting reception.

The timing at which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 22.12 shows when bits RDRF and ORER are set to 1.

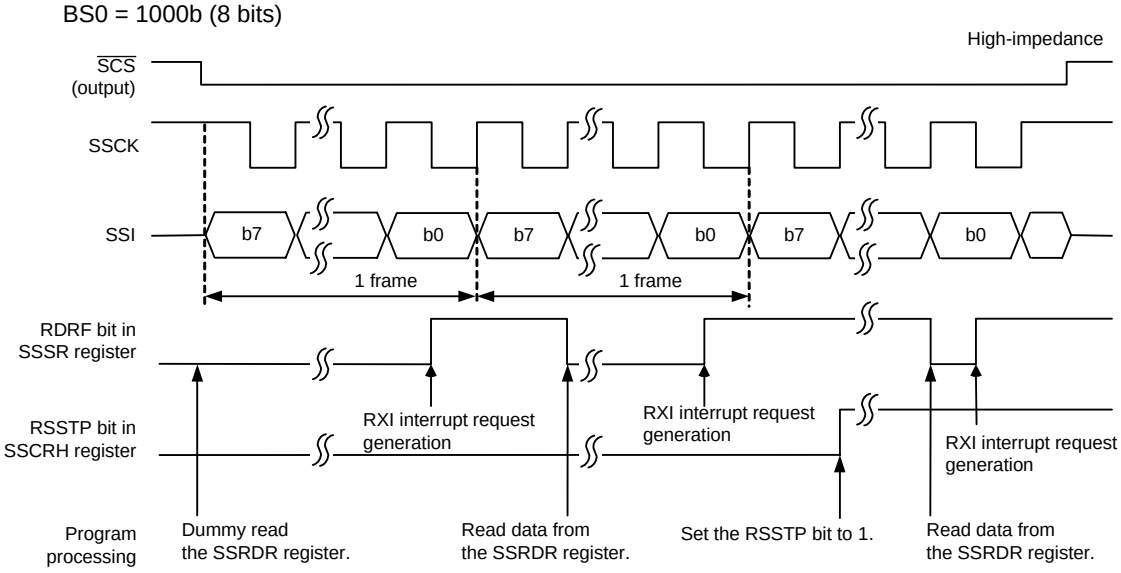
When the CPHS bit is set to 1 (data download at odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 22.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data download at even edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data download at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 22.12 Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

22.5.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the CSS1 bit is set to 1 (function as the $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operation as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If the synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held low in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operation as a slave device).
Figure 22.13 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

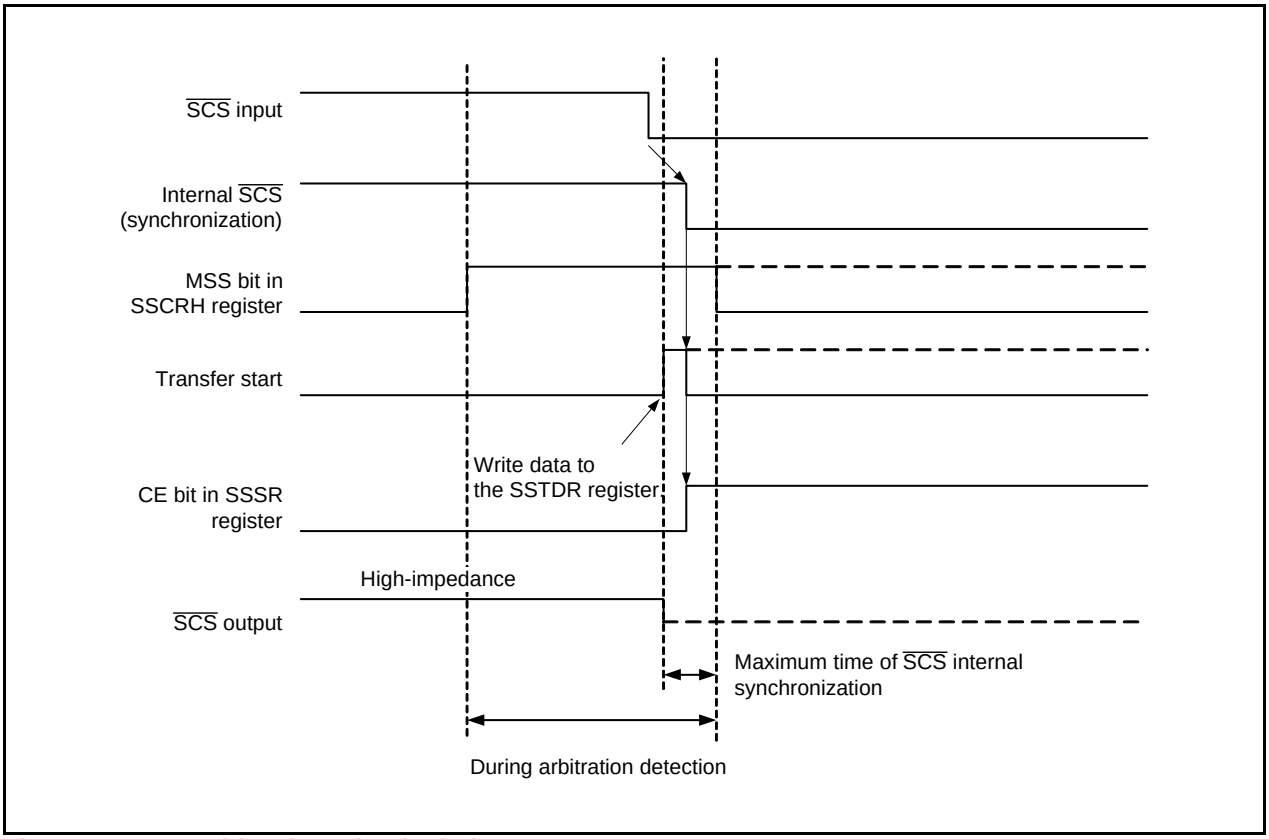


Figure 22.13 Arbitration Check Timing

22.6 Notes on Synchronous Serial Communication Unit (SSU)

To use the synchronous serial communication unit, set the IICSEL bit in the SSUIICSR register to 0 (SSU function selected).

23. I2C bus Interface

23.1 Introduction

The I2C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I2C bus.

Table 23.1 lists the I2C bus Interface Specifications. Figure 23.1 shows a Block Diagram of I2C bus interface, and Figure 23.2 shows the External Circuit Connection Example of Pins SCL and SDA. Table 23.2 lists the I2C bus Interface Pin Configuration.

* I2C bus is a trademark of Koninklijke Philips Electronics N. V.

Table 23.1 I2C bus Interface Specifications

Item	Specification
Communication formats	• I2C bus format - Selectable as master/slave device - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent) - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission - Bit synchronization/wait function (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, the SCL signal goes low and the interface stands by.) - Support for direct drive of pins SCL and SDA (N-channel open-drain output) • Clock synchronous serial format Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent)
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the ICCR1 register is set to 0 (slave mode) • External clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1 (master mode) • Internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and bits IICTCTWI and IICTCHALF in the PINSR register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial format) • Indicates an overrun error during reception. When the last bit of the next unit of data is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt sources	• I2C bus format ..... 6 sources (1) • Transmit data empty (including when slave address matches), transmit end, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial format ..... 4 sources (1) • Transmit data empty, transmit end, receive data full, and overrun error
Selectable functions	• I2C bus format Selectable output level for the acknowledge signal during reception • Clock synchronous serial format Selectable MSB first or LSB first as the data transfer direction • SDA digital delay Digital delay value for the SDA pin selectable by bits SDADLY0 to SDADLY1 in the PINSR register.

Note:

1. All sources use a single interrupt vector table for the I2C bus interface.

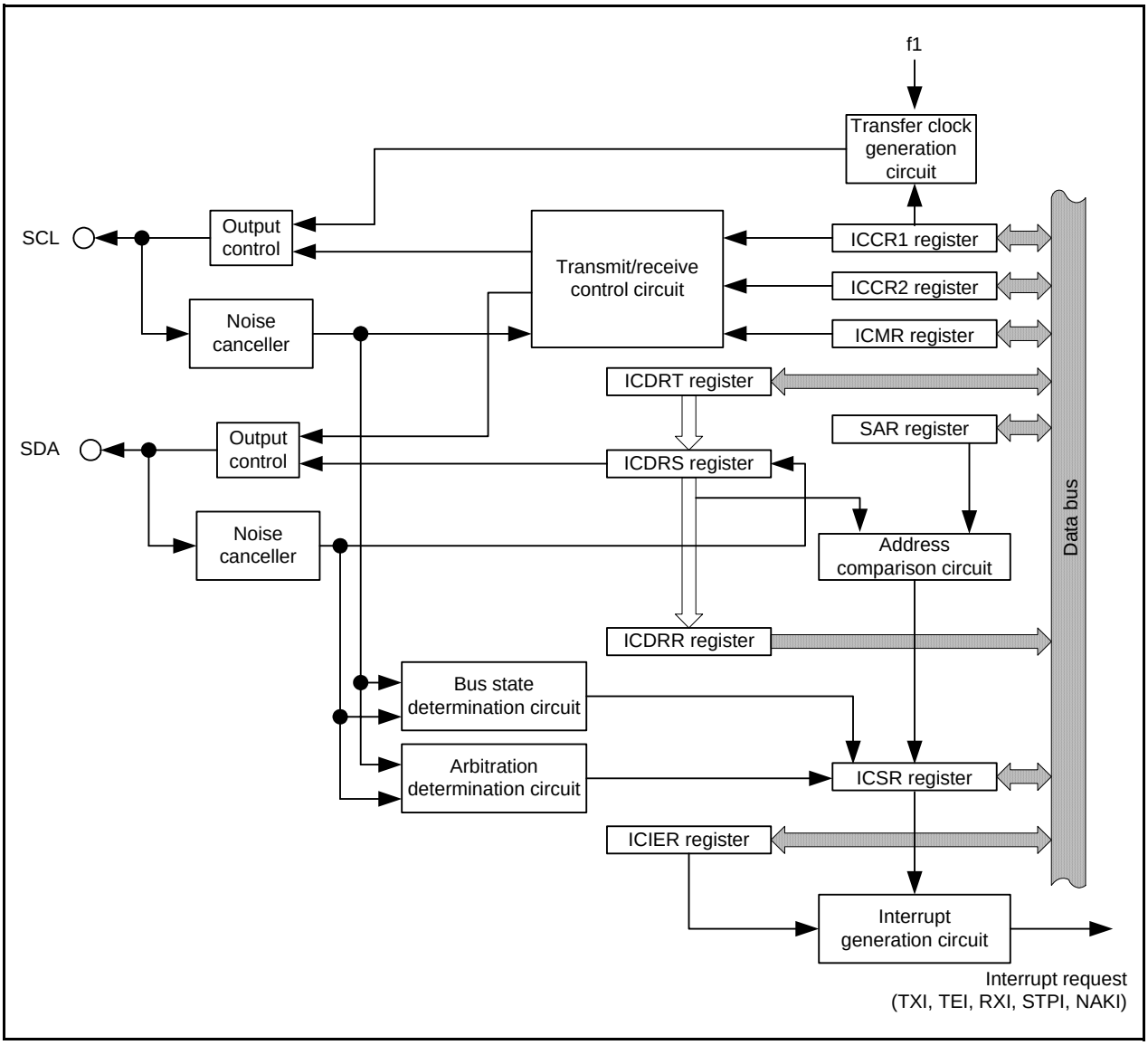


Figure 23.1 Block Diagram of I2C bus interface

Table 23.2 I2C bus Interface Pin Configuration

Pin Name	Assigned Pin	Function
SCL	P8_2	Clock I/O
SDA	P8_3	Data I/O

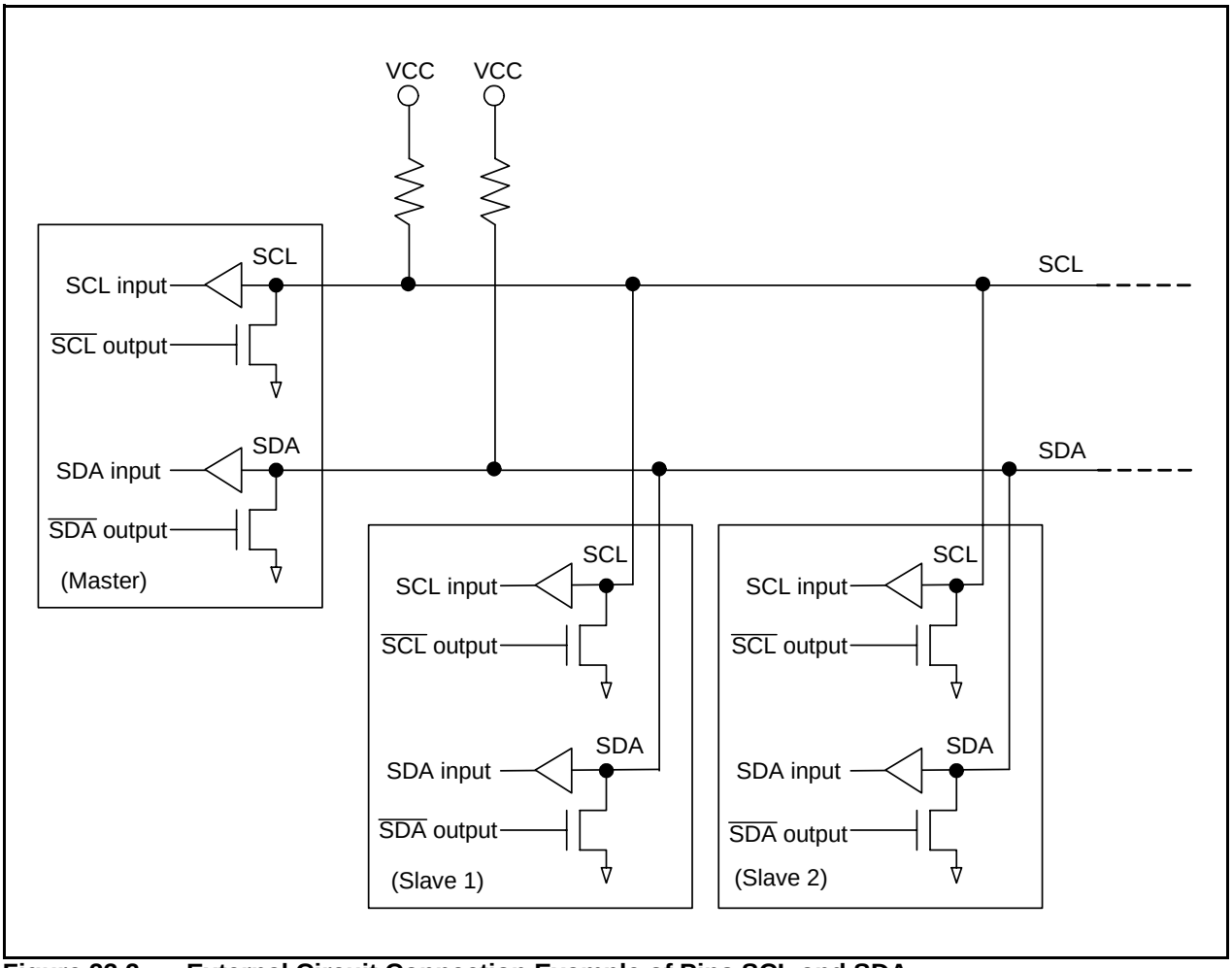


Figure 23.2 External Circuit Connection Example of Pins SCL and SDA

23.2 Registers

23.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	—	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	Reseved bit	Set to 1.	R/W
b2	—	Reseved bit	Set to 0.	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTLCD	Reseved bit	Set to 1.	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	Reseved bit	Set to 1.	R/W

Notes:

1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

23.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

23.2.3 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 2, 5, 7 to 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register.	R/W
b4	IICTCTWI	I2C double transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I2C half transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Note:
1. Do not set both the IICTCTWI and IICTCHALF bits to 1 when the I2C bus function is used. Set these bits to 0 when the SSU function is used.

23.2.4 IIC bus Transmit Data Register (ICDRT)

Address 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores transmit data. When the ICDRS register is detected as empty, the stored transmit data is transferred to the ICDRS register and transmission starts. When the next transmit data is written to the ICDRT register during the data transmission from the ICDRS register, continuous transmission is enabled. When the MLS bit in the ICMR register is set to 1 (data transfer with LSB first), the MSB-LSB inverted data is read after writing to the ICDRT register.	R/W

23.2.5 IIC bus Receive Data Register (ICDRR)

Address 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores receive data. When the ICDRS register receives 1 byte of data, the receive data is transferred to the ICDRR register and the next receive operation is enabled.	R

23.2.6 IIC bus Control Register 1 (ICCR1)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transmit clock select bit 3 to 0 (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transmission/reception select bit (2, 3, 6)	b5 b4 0 0: Slave Receive Mode (4) 0 1: Slave Transmit Mode 1 0: Master Receive Mode 1 1: Master Transmit Mode	R/W
b5	MST	Master/slave select bit (5, 6)		R/W
b6	RCVD	Reception disable bit	After reading the ICDRR register while the TRS bit is set to 0 (receive mode), 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I2C bus interface enable bit (7)	0: This module is halted (Pins SCL and SDA are set to the port function) 1: This module is enabled for transfer operations (Pins SCL and SDA are in the bus drive state)	R/W

Notes:

1. Set according to the necessary transfer rate in master mode. Refer to **Table 23.3 Transfer Rate Examples (1)** and **Table 23.4 Transfer Rate Examples (2)** for the transfer rate. This bit is used for maintaining the setup time in transmit mode of slave mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between transfer frames.
3. When the first 7 bits after the start condition in slave receive mode match the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1 (transmit mode).
4. In master mode with the I2C bus format, if arbitration is lost, bits MST and TRS are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode with the clock synchronous serial format, the MST bit is set to 0 and the I2C bus enters slave receive mode.
6. In multimaster operation, use the MOV instruction to set bits TRS and MST.
7. When writing 0 to the ICE bit or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined. Refer to **23.9 Notes on I2C bus Interface**.

23.2.7 IIC bus Control Register 2 (ICCR2)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	IICRST	I2C bus control block reset bit (5)	When hang-up occurs due to communication failure during the I2C bus interface operation, writing 1 resets the control block of the I2C bus interface without setting ports or initializing registers.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	SCLO	SCL monitor flag	0: SCL pin is set to low 1: SCL pin is set to high	R
b4	SDAOP	SDAO write protect bit	When rewriting the SDAO bit, write 0 simultaneously (1). When read, the content is 1.	R/W
b5	SDAO	SDA output value control bit	When read 0: SDA pin output is held low 1: SDA pin output is held high When written (1, 2) 0: SDA pin output is changed to low 1: SDA pin output is changed to high-impedance (High-level output via an external pull-up resistor)	R/W
b6	SCP	Start/stop condition generation disable bit	When writing to the to BBSY bit, write 0 simultaneously (3). When read, the content is 1. Writing 1 is invalid.	R/W
b7	BBSY	Bus busy bit (4, 5)	When read: 0: Bus is released (SDA signal changes from low to high while SCL signal is held high) 1: Bus is occupied (SDA signal changes from high to low while SCL signal is held high) When written (3): 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
2. Do not write to the SDAO bit during a transfer operation.
3. Enabled in master mode. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
4. Disabled when the clock synchronous serial format is used.
5. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit and the STOP bit in the ICSR register may become undefined. Refer to **23.9 Notes on I2C bus Interface**.

23.2.8 IIC bus Mode Register (ICMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter 2 to 0	I2C bus format (Read: Number of remaining transfer bits; Write: Number of next transfer data bits). (1, 2) b2 b1 b0 0 0 0: 9 bits (3) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial format (Read: Number of remaining transfer bits; Write: Always 000b). b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b1	BC1			R/W
b2	BC2			R/W
b3	BCWP	BC write protect bit	When rewriting bits BC0 to BC2, write 0 simultaneously. (2, 4) When read, the content is 1.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—	Reserved bit	Set to 0.	R/W
b6	WAIT	Wait insertion bit (5)	0: No wait states (Data and the acknowledge bit are transferred successively) 1: Wait state (After the clock of the last data bit falls, a low-level period is extended for two transfer clocks)	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first (6) 1: Data transfer with LSB first	R/W

Notes:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is low.
2. When writing to bits BC0 to BC2, write 0 to the BCWP bit simultaneously using the MOV instruction.
3. After data including the acknowledge bit is transferred, these bits are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is valid in master mode with the I2C bus format. It is invalid in slave mode with the I2C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I2C bus format is used.

23.2.9 IIC bus Interrupt Enable Register (ICIER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit. 1: In receive mode, 1 is transmitted as the acknowledge bit.	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from the receive device is set to 0. 1: In transmit mode, the acknowledge bit received from the receive device is set to 1.	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed. 1: When the receive acknowledge bit is set to 1, continuous transfer is halted.	R/W
b3	STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (2)	R/W
b4	NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/ overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/ overrun error interrupt request (1)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (1)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit in the ICSR register is set to 0.

23.2.10 IIC bus Status Register (ICSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	AL	AAS	ADZ
After Reset	0	0	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SAR register in slave receive mode (slave address detection and general call address detection).	R/W
b2	AL	Arbitration lost flag/ overrun error flag (1)	I2C bus format: This flag indicates that arbitration has been lost in master mode. This flag is set to 1 (3) when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held high at start condition detection in master transmit/receive mode Clock synchronous format: This flag indicates an overrun error. This flag is set to 1 when: • The last bit of the next unit of data is received while the RDRF bit is set to 1	R/W
b3	STOP	Stop condition detection flag (1, 7)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers ICDRS to ICDRR.	R/W
b6	TEND	Transmit end flag (1, 6)	I2C bus format: This flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is set to 1. Clock synchronous format: This flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers ICDRT to ICDRS and the CDRT register is empty • The TRS bit in the ICCR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:
1. Each bit is set to 0 by reading 1 before writing 0.
2. This flag is enabled in slave receive mode with the I2C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I2C bus Interface monitors the SDA pin and the data which the I2C bus Interface transmits is different, the AL flag is set to 1 and the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the ICDRR register.
6. Bits TEND and TDRE are set to 0 when data is written to the ICDRT register.
   When reading these bits immediately after writing to the ICDRT register, insert three or more NOP instructions between the instructions used for writing and reading.
7. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit may become undefined. Refer to **23.9 Notes on I2C bus Interface**.

When accessing the ICSR register successively, insert one or more NOP instructions between the instructions used for access.

23.2.11 Slave Address Register (SAR)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FS	Format select bit	0: I2C bus format 1: Clock synchronous serial format	R/W
b1	SVA0	Slave address 6 to 0	Set an address different from that of the other slave devices connected to the I2C bus. When the 7 high-order bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of the I2C bus format, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

23.2.12 IIC bus Shift Register (ICDRS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—

Bit	Function	R/W
b7 to b0	This register transmits and receives data. During transmission, data is transferred from registers ICRDT to ICDRS and transmitted from the SDA pin. During reception, data is transferred from registers ICDRS to the ICDRR after 1 byte of data is received.	—

23.3 Common Items for Multiple Modes

23.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0 (slave mode), the transfer clock is the external clock input from the SCL pin.
When the MST bit in the ICCR1 register is set to 1 (master mode), the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and the transfer clock is output from the SCL pin.
Tables 23.3 and 23.4 list Transfer Rate Examples.

Table 23.3 Transfer Rate Examples (1)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
					1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
					1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
			1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
		1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
			1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
					1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
				1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
					1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

Table 23.4 Transfer Rate Examples (2)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	1	0	0	0	0	f1/28	358 kHz	572 kHz	714 kHz	1142 kHz	1428 kHz
					1	f1/40	250 kHz	400 kHz	500 kHz	800 kHz	1000 kHz
				1	0	f1/48	208 kHz	334 kHz	416 kHz	666 kHz	834 kHz
					1	f1/64	156 kHz	250 kHz	312 kHz	500 kHz	626 kHz
			1	0	0	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
					1	f1/100	100 kHz	160 kHz	200 kHz	320 kHz	400 kHz
				1	0	f1/112	89 kHz	143 kHz	179 kHz	286 kHz	358 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
		1	0	0	0	f1/56	179 kHz	286 kHz	358 kHz	572 kHz	714 kHz
					1	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/96	104 kHz	167 kHz	208 kHz	334 kHz	416 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
			1	0	0	f1/160	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/200	50 kHz	80 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/224	45 kHz	71 kHz	89 kHz	143 kHz	179 kHz
					1	f1/256	39 kHz	63 kHz	78 kHz	125 kHz	156 kHz
1	0	0	0	0	0	f1/28	90 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/40	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/48	52 kHz	84 kHz	104 kHz	167 kHz	209 kHz
					1	f1/64	39 kHz	63 kHz	78 kHz	125 kHz	157 kHz
			1	0	0	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
					1	f1/100	25 kHz	40 kHz	50 kHz	80 kHz	100 kHz
				1	0	f1/112	22 kHz	36 kHz	45 kHz	72 kHz	90 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
		1	0	0	0	f1/56	45 kHz	72 kHz	90 kHz	143 kHz	179 kHz
					1	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
				1	0	f1/96	26 kHz	42 kHz	52 kHz	84 kHz	104 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
			1	0	0	f1/160	16 kHz	25 kHz	31 kHz	50 kHz	63 kHz
					1	f1/200	13 kHz	20 kHz	25 kHz	40 kHz	50 kHz
				1	0	f1/224	11 kHz	18 kHz	22 kHz	36 kHz	45 kHz
					1	f1/256	10 kHz	16 kHz	20 kHz	31 kHz	39 kHz

23.3.2 SDA Pin Digital Delay Selection

The digital delay value for the SDA pin can be selected by bits SDADLY0 to SDADLY1 in the PINSR register. Figure 23.3 shows the Operating Example of Digital Delay for SDA Pin.

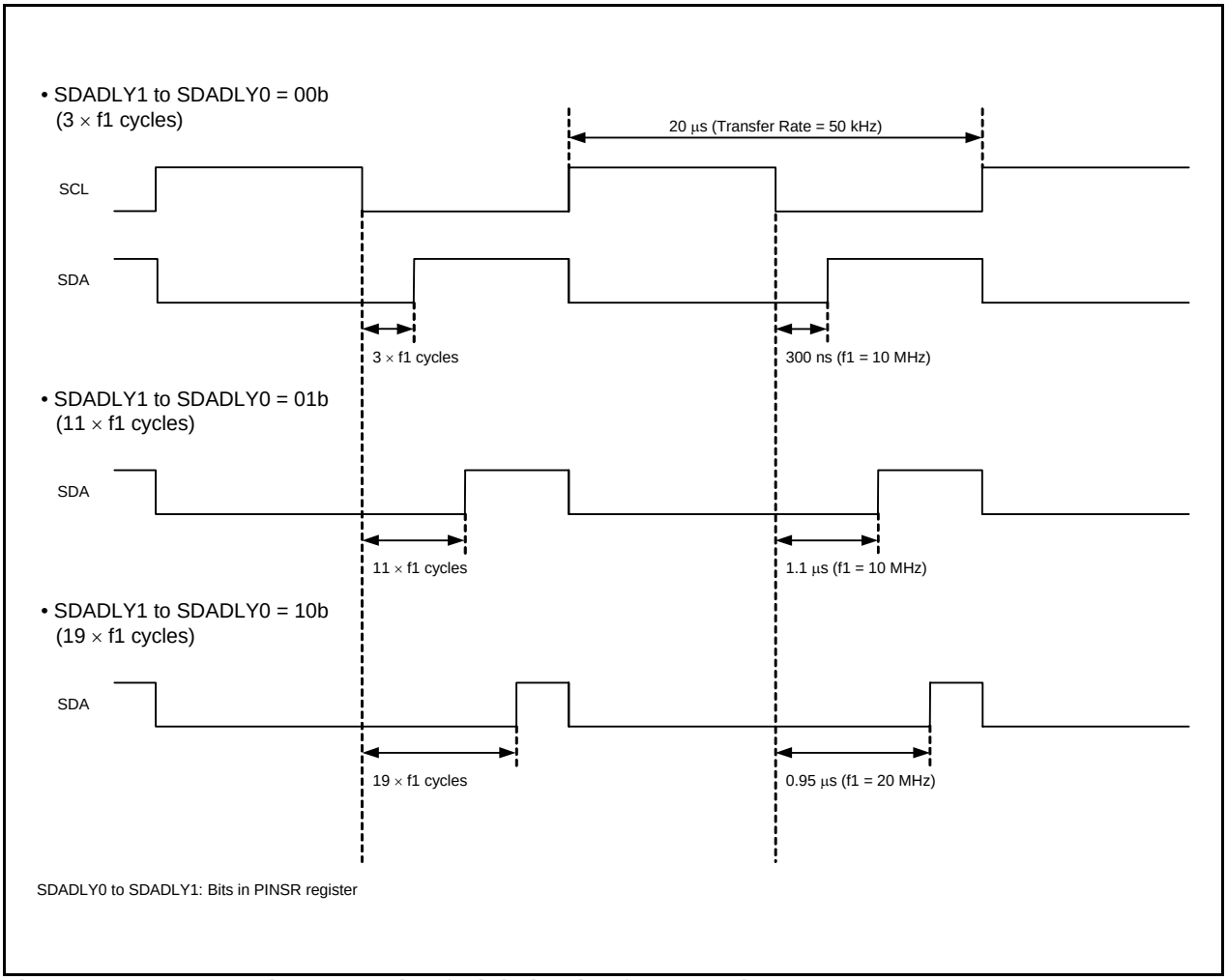


Figure 23.3 Operating Example of Digital Delay for SDA Pin

23.3.3 Interrupt Requests

The I2C bus interface has six interrupt requests when the I2C bus format is used and four interrupt requests when the clock synchronous serial format is used.

Table 23.5 lists the Interrupt Requests of I2C bus Interface.

Because these interrupt requests are allocated at the I2C bus interface interrupt vector table, the source must be determined bit by bit.

Table 23.5 Interrupt Requests of I2C bus Interface

Interrupt Request		Generation Condition	Format	
			I2C bus	Clock Synchronous Serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit end	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	NAKIE = 1 and AL = 1 (or NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration lost/overrun error			Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register
AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When generation conditions listed in Table 23.5 are met, an interrupt request of the I2C bus interface is generated. Set the interrupt generation conditions to 0 by the I2C bus interface interrupt routine.

However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the ICDRT register and the RDRF bit is automatically set to 0 by reading the ICDRR register. In particular, the TDRE bit is set to 0 when transmit data is written to the ICDRT register and set to 1 when data is transferred from the ICDRT register to the ICDRS register. If the TDRE bit is further set to 0, additional 1 byte may be transmitted.
Also, set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit is set to 0.

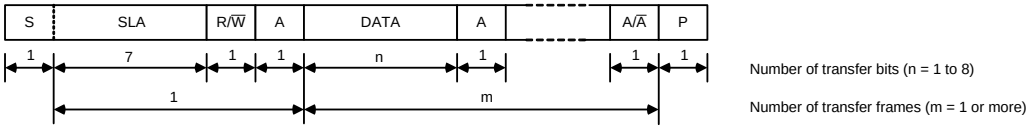
23.4 I2C bus Interface Mode

23.4.1 I2C bus Format

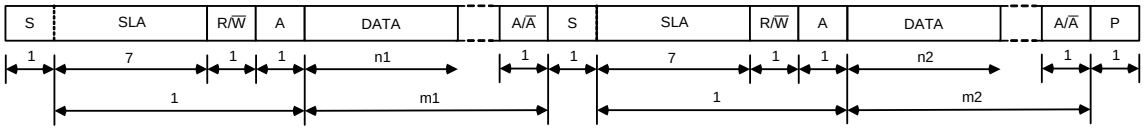
When the FS bit in the SAR register is set to 0, the I2C bus format is used for communication.
Figure 23.4 shows the I2C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I2C bus format

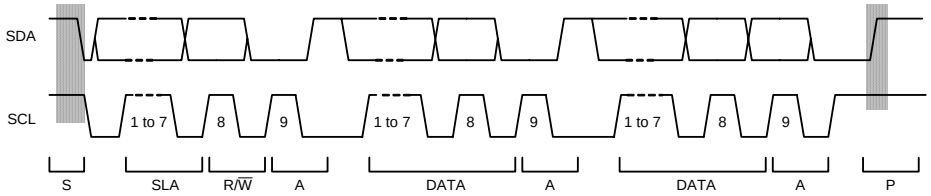
(a) I2C bus format (FS = 0)



(b) I2C bus format when start condition is retransmitted (FS = 0)



(2) I2C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from high to low while the SCL signal is held high.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception
Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to low.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from low to high while the SCL signal is held high.

Figure 23.4 I2C bus Format and Bus Timing

23.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 23.5 and 23.6 show the Operating Timing in Master Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are as follows:

(1) Set the STOP bit in the ICSR register to 0 for initialization, and set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then, set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting).

(2) After confirming that the bus is released by reading the BBSY bit in the ICCR2 register, set bits TRS and MST in the ICCR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.

(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from registers ICDRT to ICDRS), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). At this time, the TDRE bit is automatically set to 0. When data is transferred from registers ICDRT to ICDRS, the TDRE bit is set to 1 again.

(4) When 1 byte of data transmission is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming that the slave device is selected by reading the ACKBR bit in the ICIER register, write the 2nd byte of data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate a stop condition. Stop condition generation is enabled by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. The SCL signal is fixed low until data is ready or a stop condition is generated.

(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.

(6) When the number of bytes to be transmitted is written to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (NACKF bit in ICSR register = 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). Then, generate a stop condition before setting the TEND bit or the NACKF bit to 0.

(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

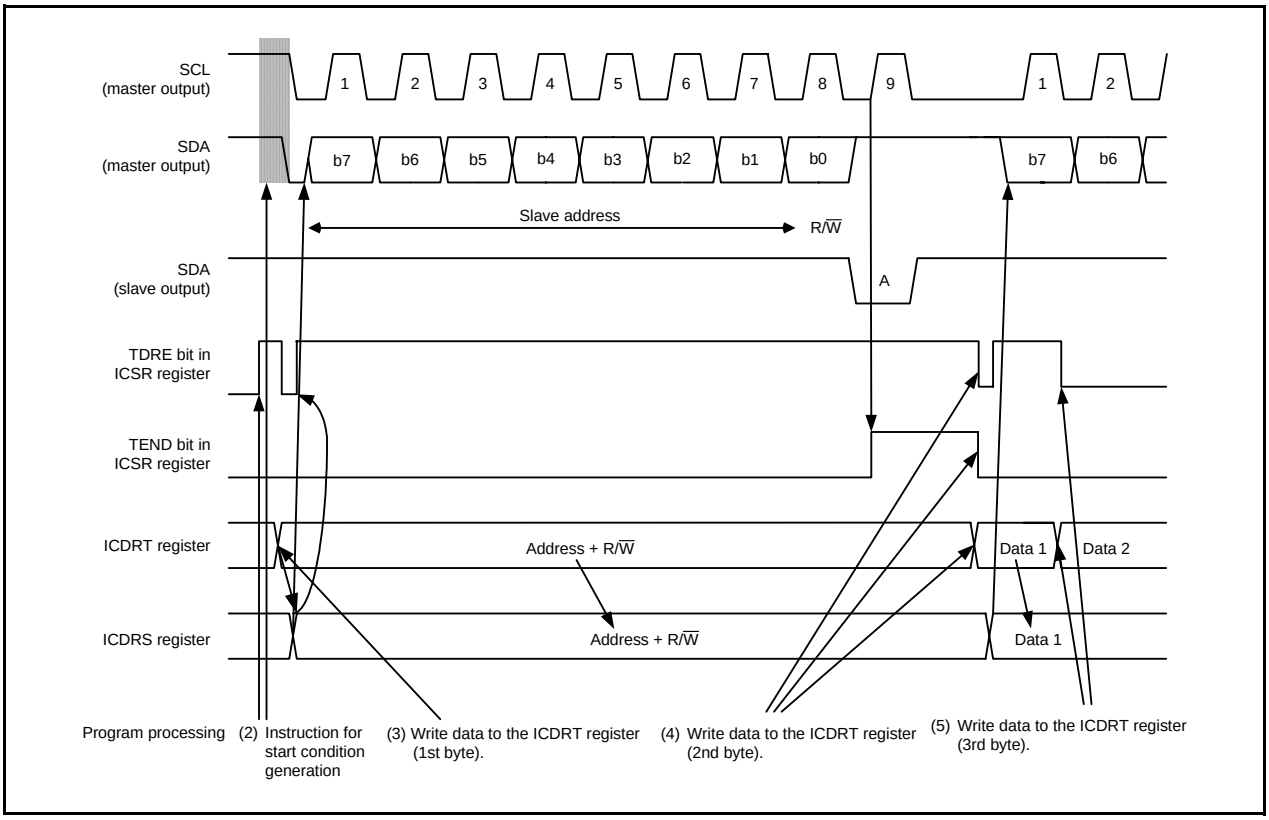


Figure 23.5 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (1)

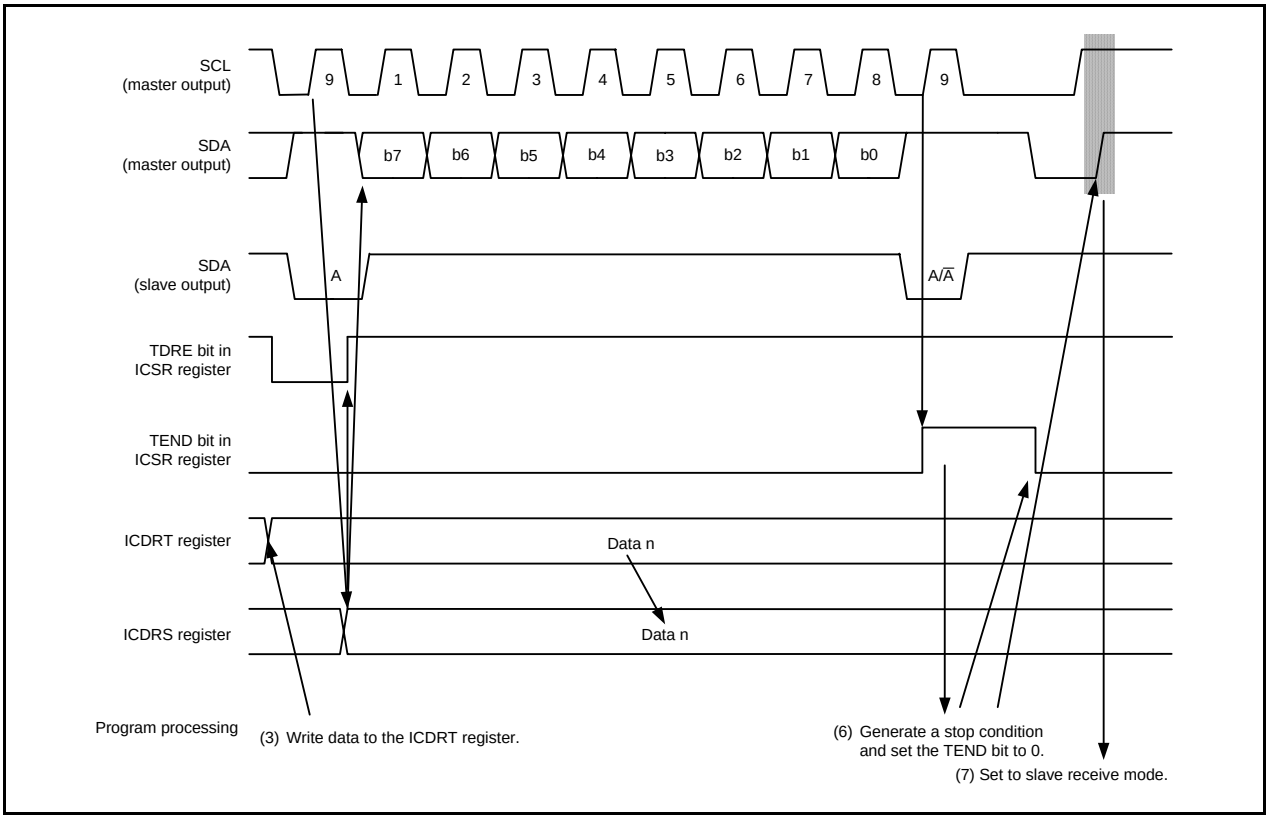


Figure 23.6 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (2)

23.4.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal. Figures 23.7 and 23.8 show the Operating Timing in Master Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in master receive mode are as follows:

(1) After setting the TEND bit in the ICSR register to 0, set the TRS bit in the ICCR1 register to 0 to switch from master transmit mode to master receive mode. Then set the TDRE bit in the ICSR register to 0.
(2) Dummy reading the ICDRR register starts receive operation. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When one frame of data reception is completed, the RDRF bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. If the ICDRR register is read at this time, the received data can be read and the RDRF bit is set to 0 simultaneously.
(4) Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If reading the ICDRR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed low until the ICDRR register is read.
(5) If the next frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (next receive operation disabled) before reading the ICDRR register, stop condition generation is enabled after the next receive operation.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition. When a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle. Refer to **23.9 Notes on I2C bus Interface**.
(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register and set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

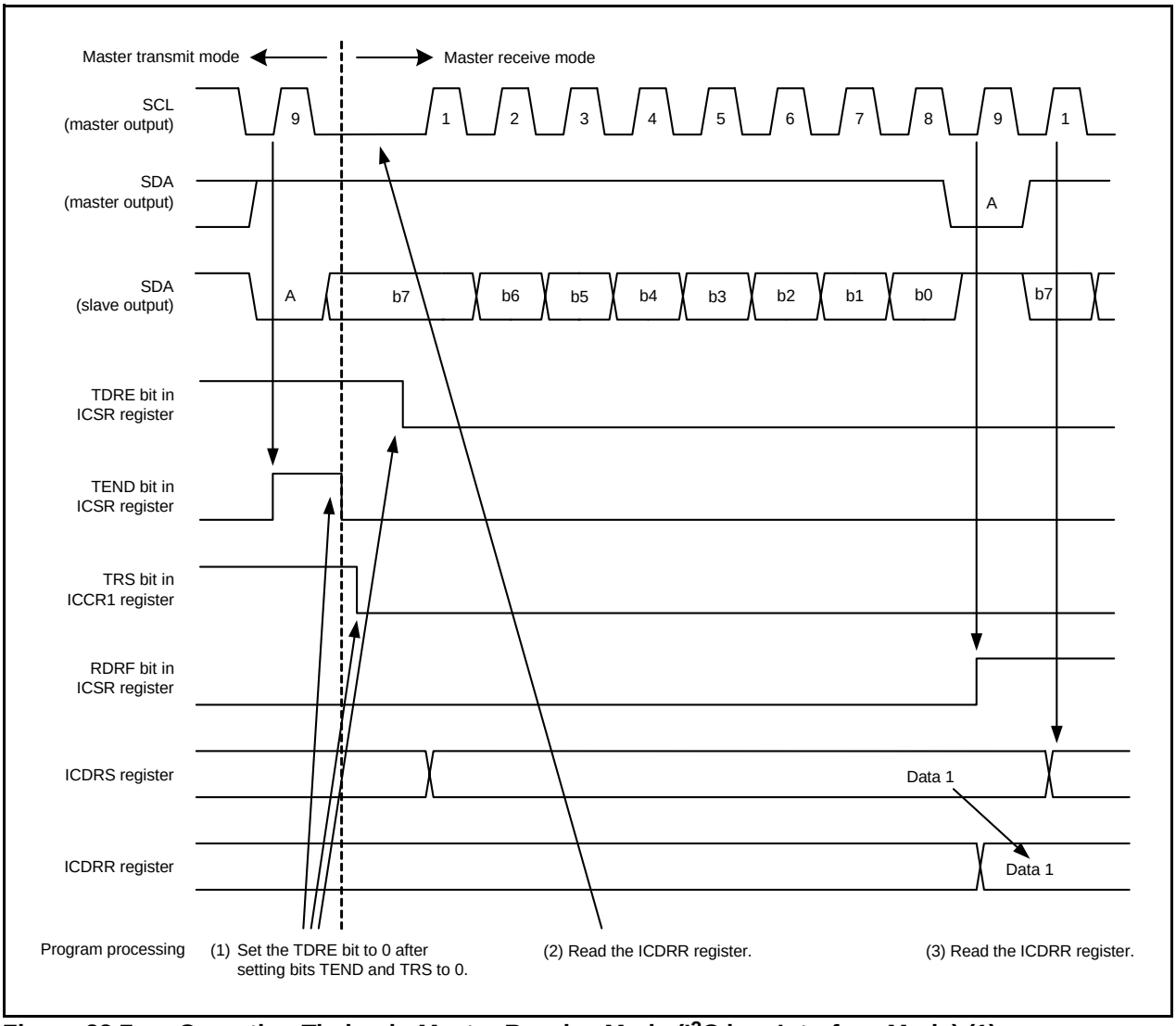


Figure 23.7 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (1)

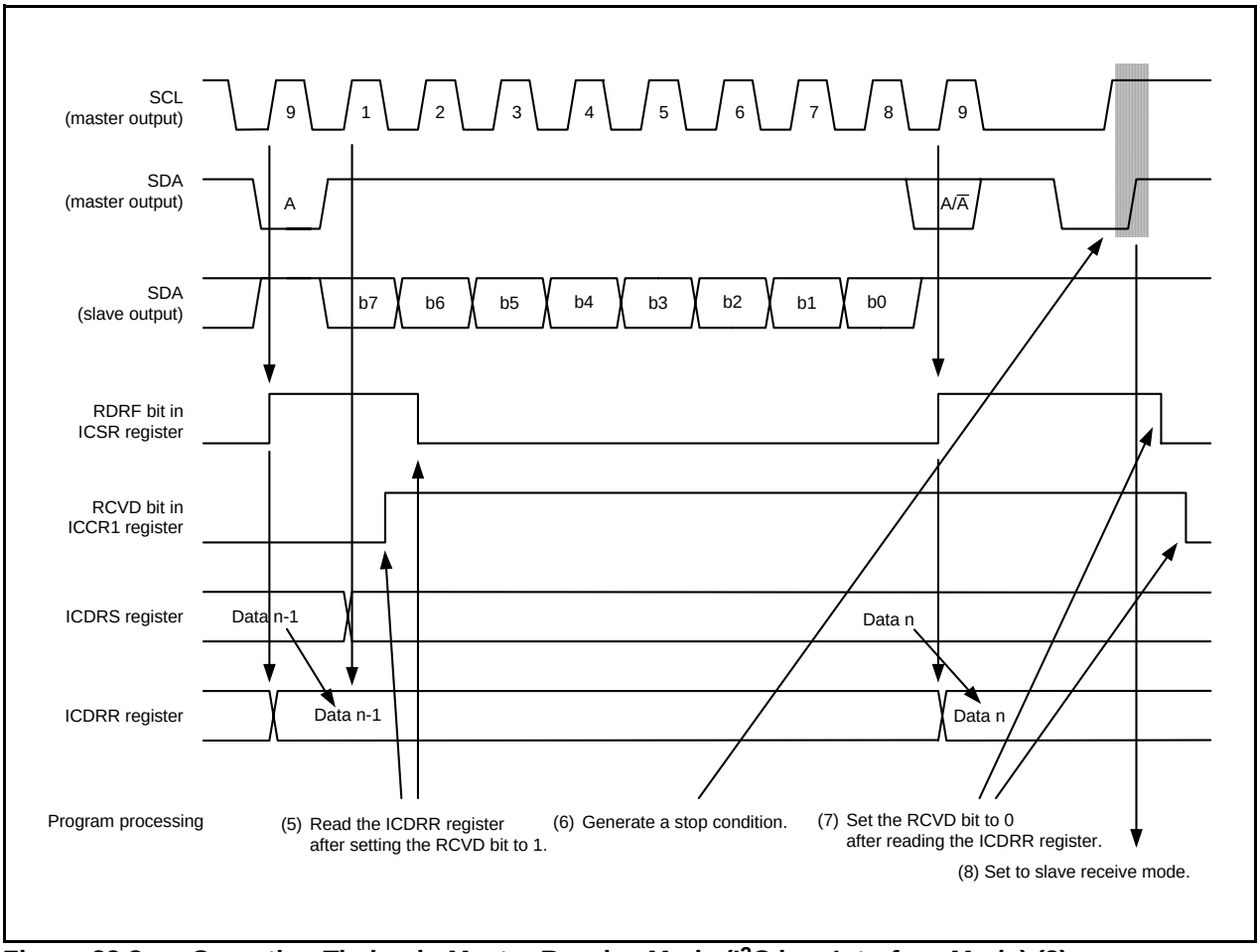


Figure 23.8 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (2)

23.4.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal.

Figures 23.9 and 23.10 show the Operating Timing in Slave Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. If the 8th bit of data (R/$\overline{W}$) is 1 at this time, bits TRS and TDRE in the ICSR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the ICDRT register every time the TDRE bit is set to 1.

(3) When the TDRE bit in the ICDRT register is set to 1 after the last transmit data is written to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and dummy read the ICDRR register to end the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

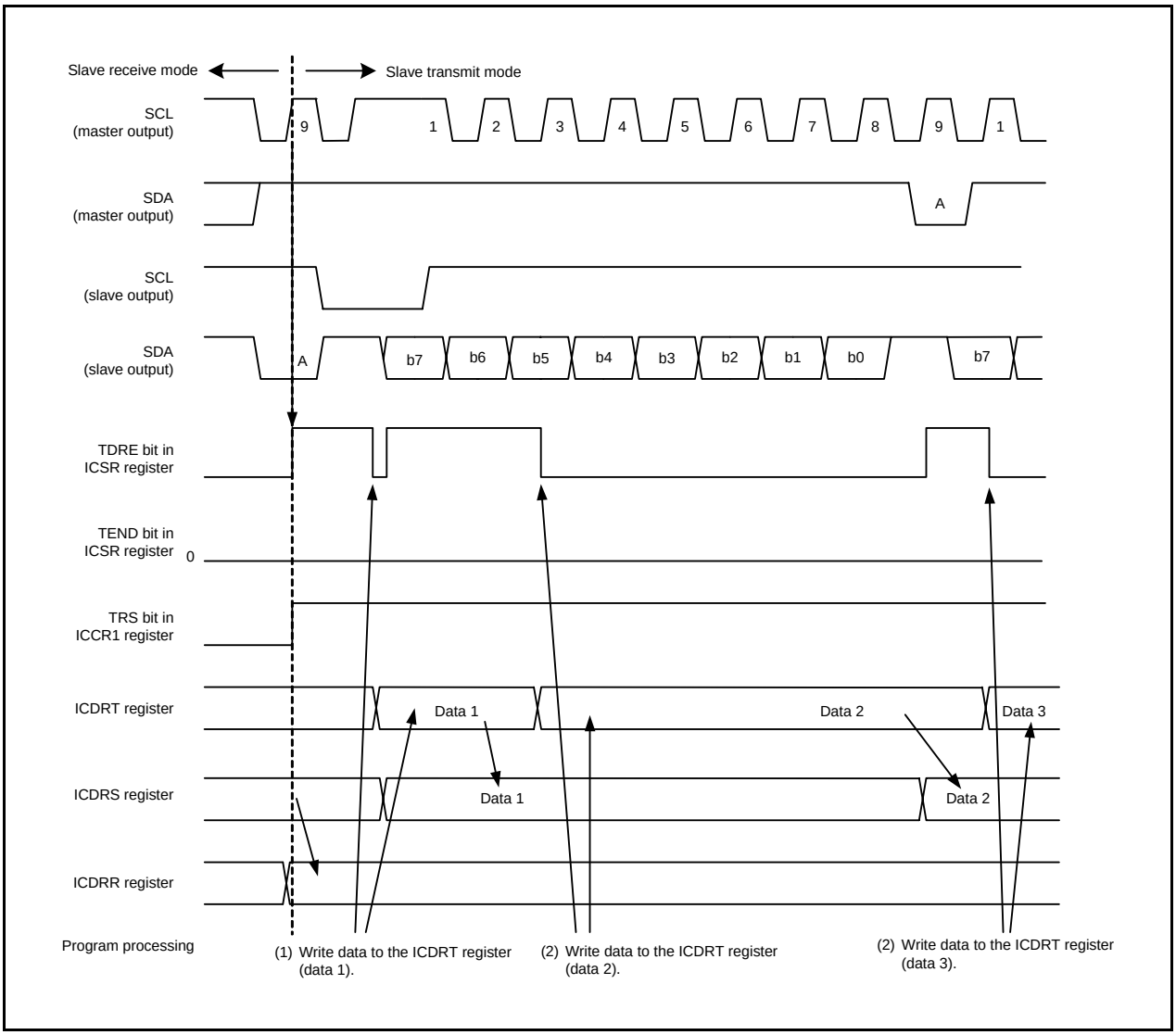


Figure 23.9 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (1)

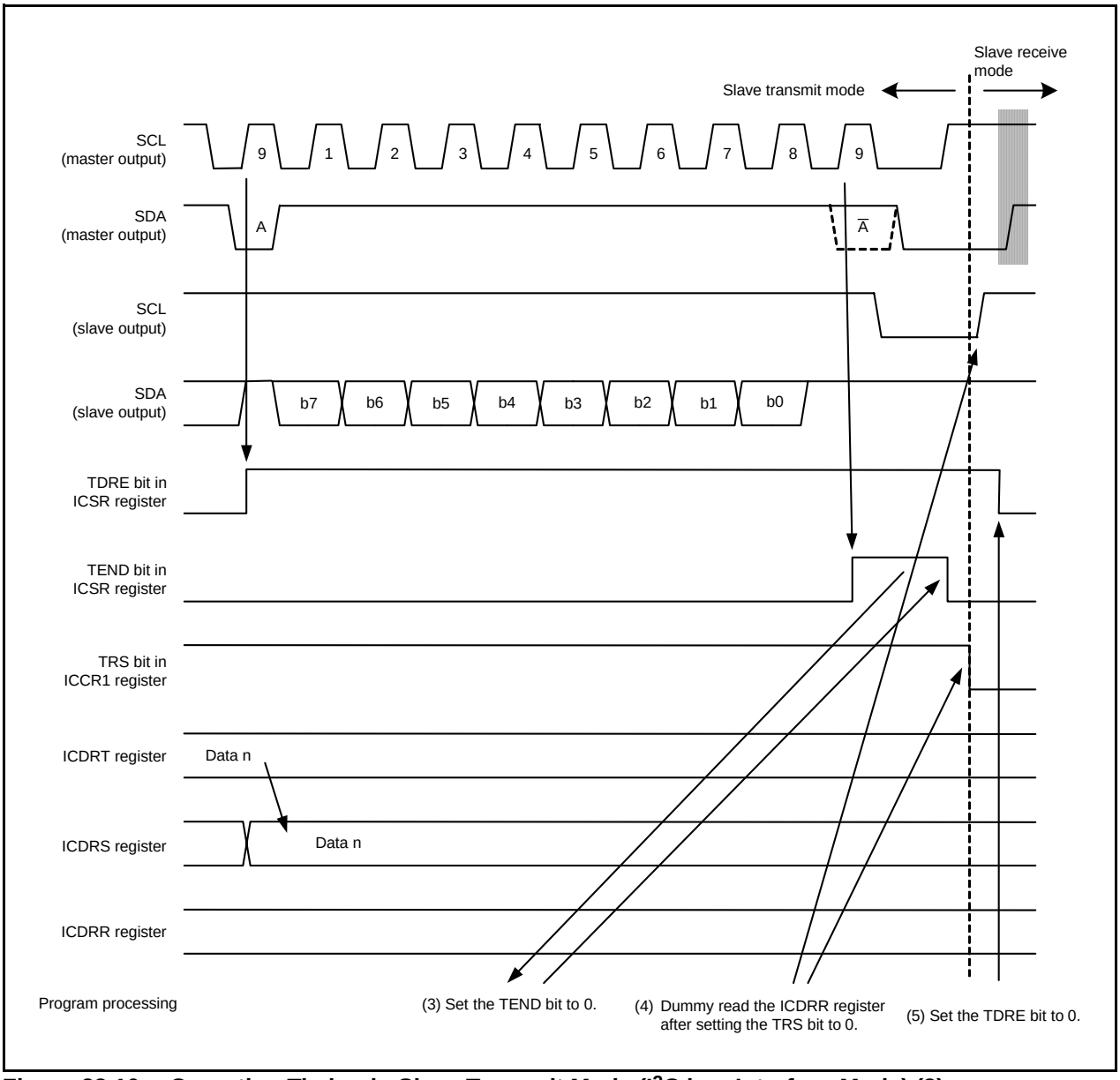


Figure 23.10 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (2)

23.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 23.11 and 23.12 show the Operating Timing in Slave Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. Since the RDRF bit in the ICSR register is set to 1 simultaneously, dummy read the ICDRR register (the read data is unnecessary because it indicates the slave address and R/W).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed low until the ICDRR register is read. The setting change of the acknowledge signal returned to the master device before reading the ICDRR register takes affect from the following transfer frame.

(4) Reading the last byte is also performed by reading the ICDRR register.

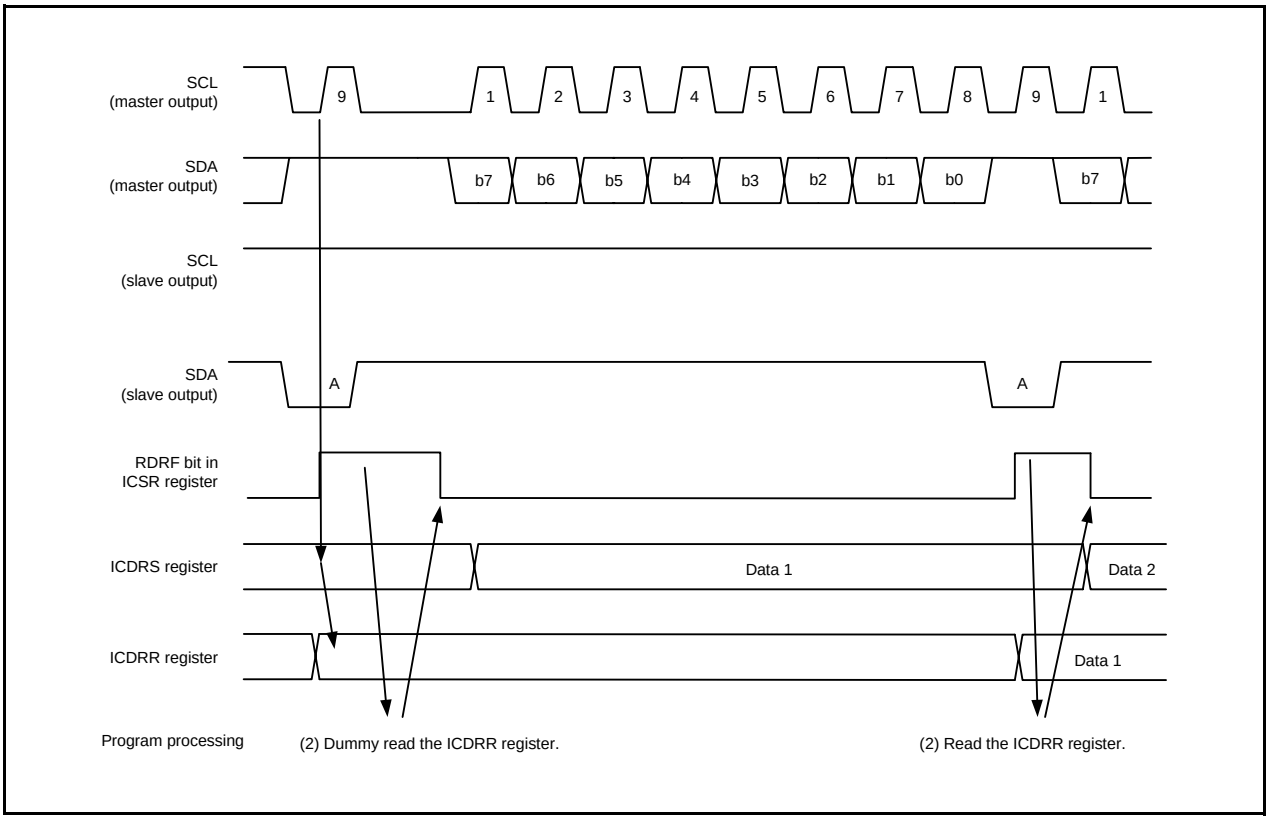


Figure 23.11 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (1)

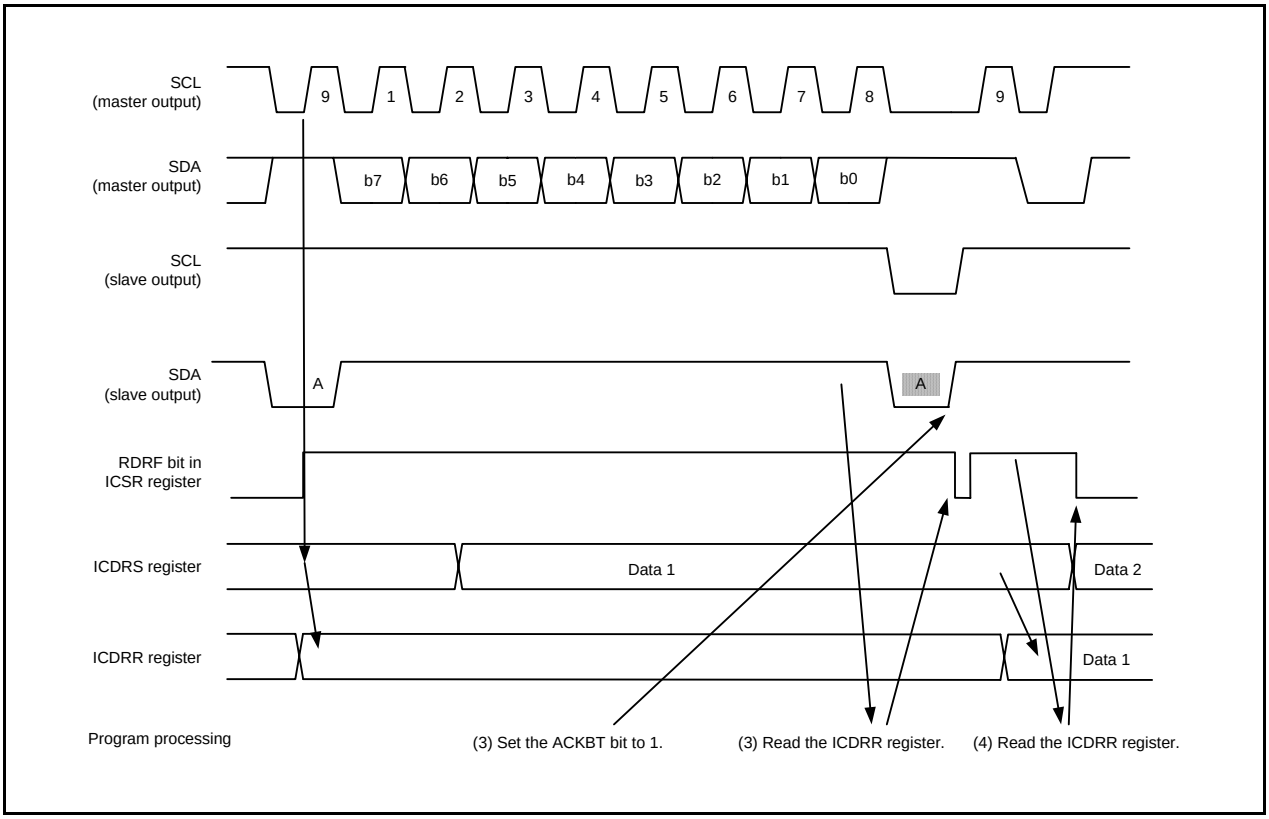


Figure 23.12 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (2)

23.5 Clock Synchronous Serial Mode

23.5.1 Clock Synchronous Serial Format

When the FS bit in the SAR register is set to 1, the clock synchronous serial format is used for communication. Figure 23.13 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1 (master mode), the transfer clock is output from the SCL pin. When the MST bit is set to 0 (slave mode), the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB first or LSB first can be selected as the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during transfer standby.

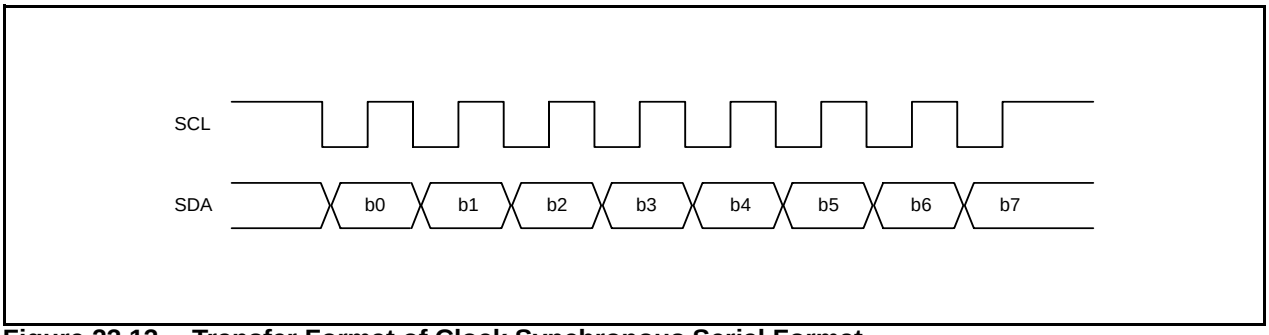


Figure 23.13 Transfer Format of Clock Synchronous Serial Format

23.5.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 (master mode) and input when the MST bit is set to 0 (slave mode).
Figure 23.14 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the ICCR1 register to 1 to select transmit mode. This will set the TDRE bit in the ICSR register to 1.
(3) After confirming that the TDRE bit is set to 1, write transmit data to the ICDRT register. Data is transferred from registers ICDRT to ICDRS and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the ICDRT register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is set to 1.

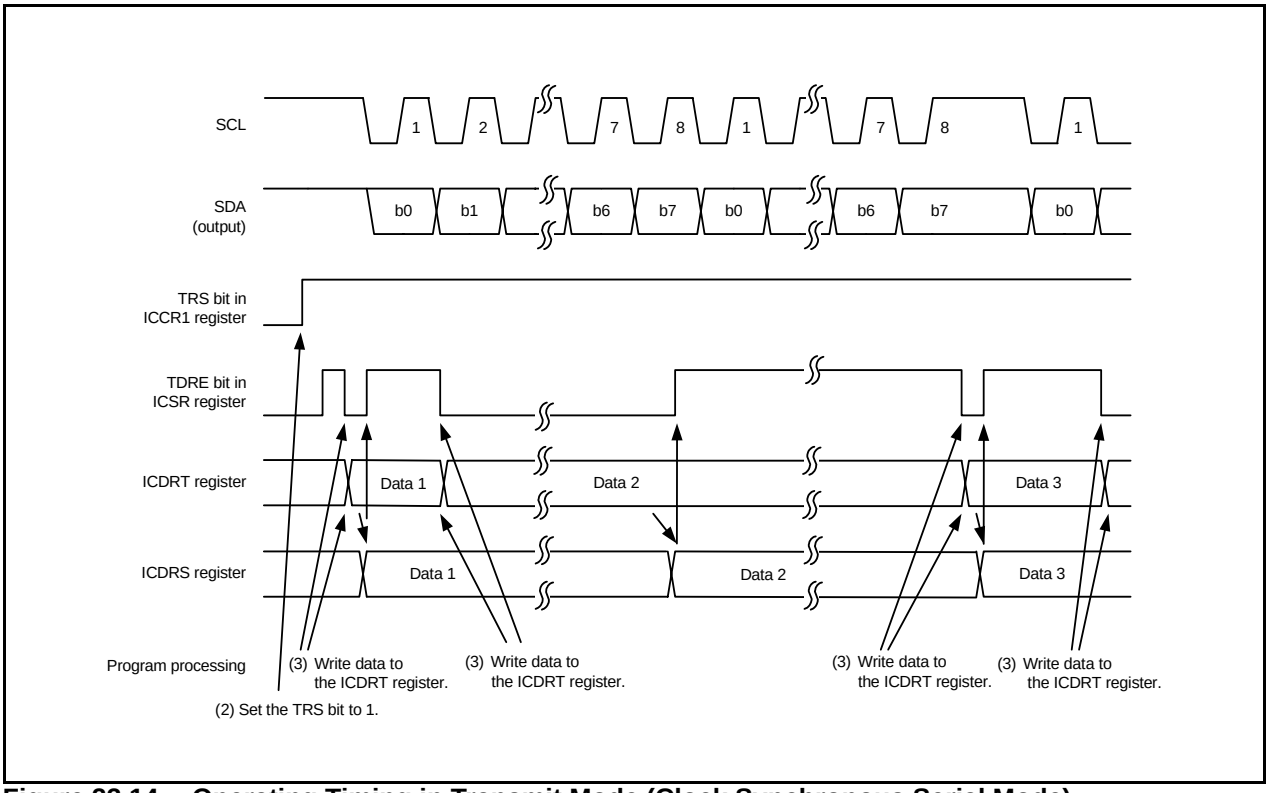


Figure 23.14 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

23.5.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 (master mode) and input when the MST bit is set to 0 (slave mode). Figure 23.15 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers ICDRS to ICDRR and the RDRF bit in the ICSR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, an overrun is detected and the AL bit in the ICSR register is set to 1. At this time, the last receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (next receive operation disabled) and read the ICDRR register. The SCL signal is fixed high after the following byte of data reception is completed.

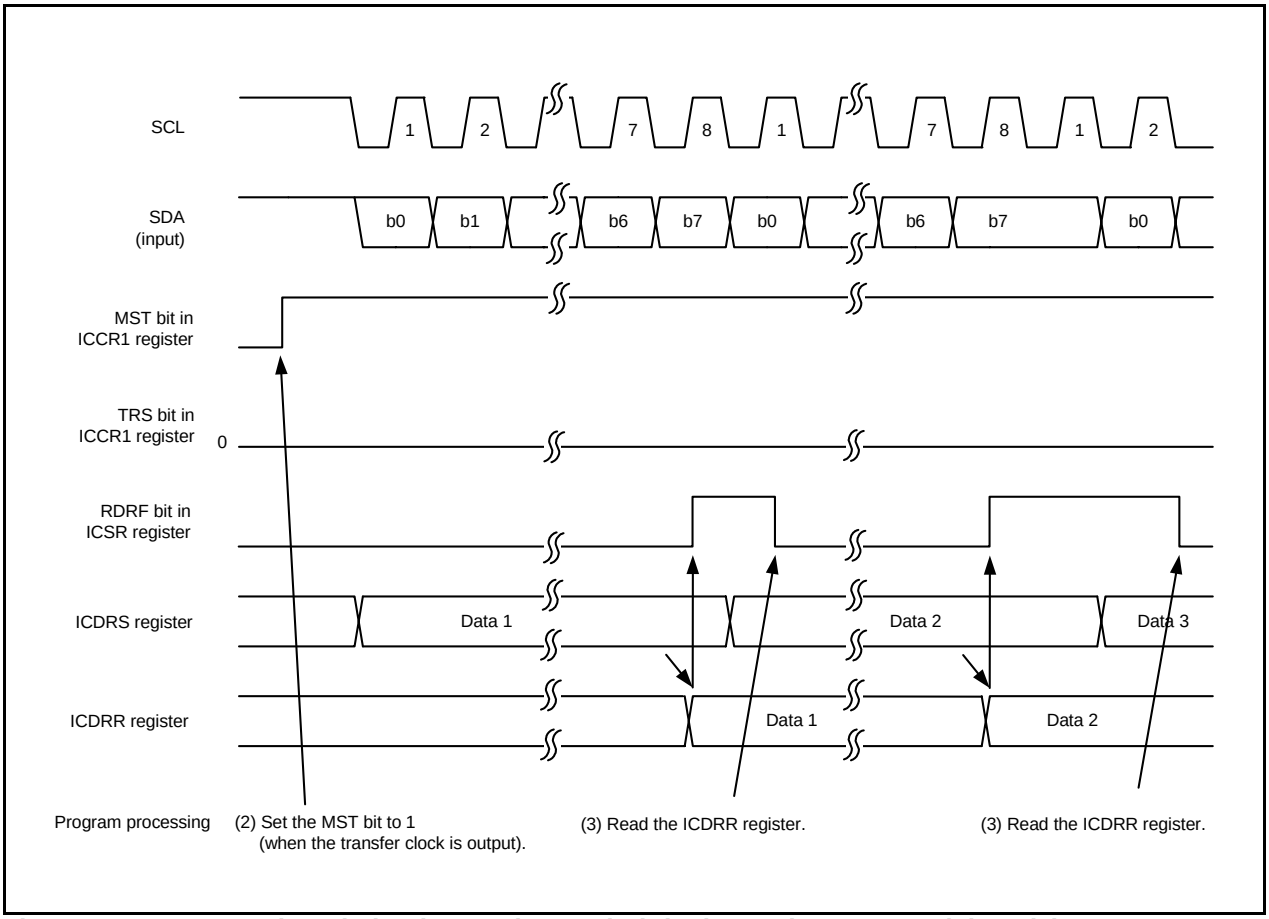


Figure 23.15 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

23.6 Register Setting Examples

Figures 23.16 to 23.19 show Register Setting Examples when using I2C bus interface.

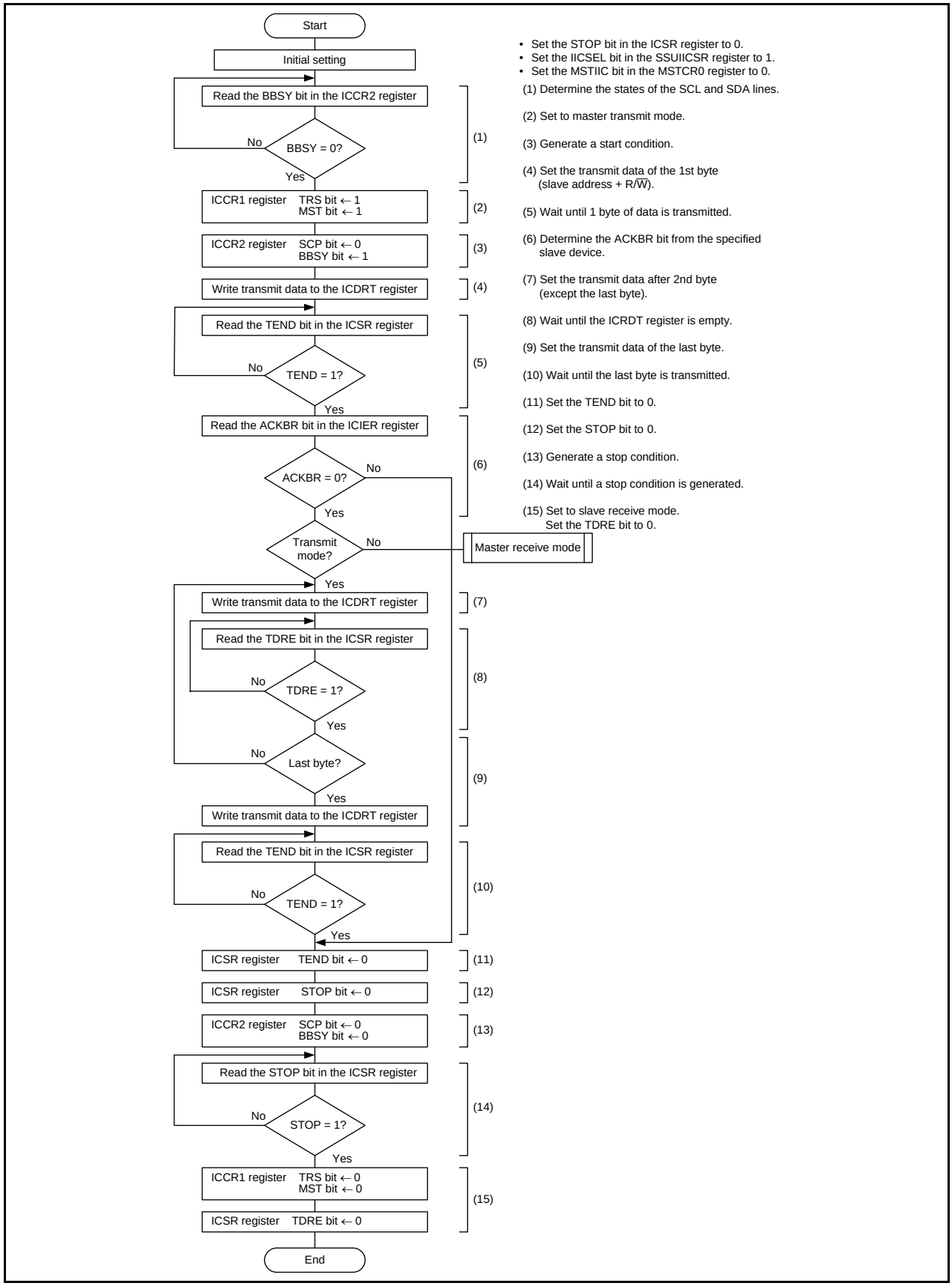
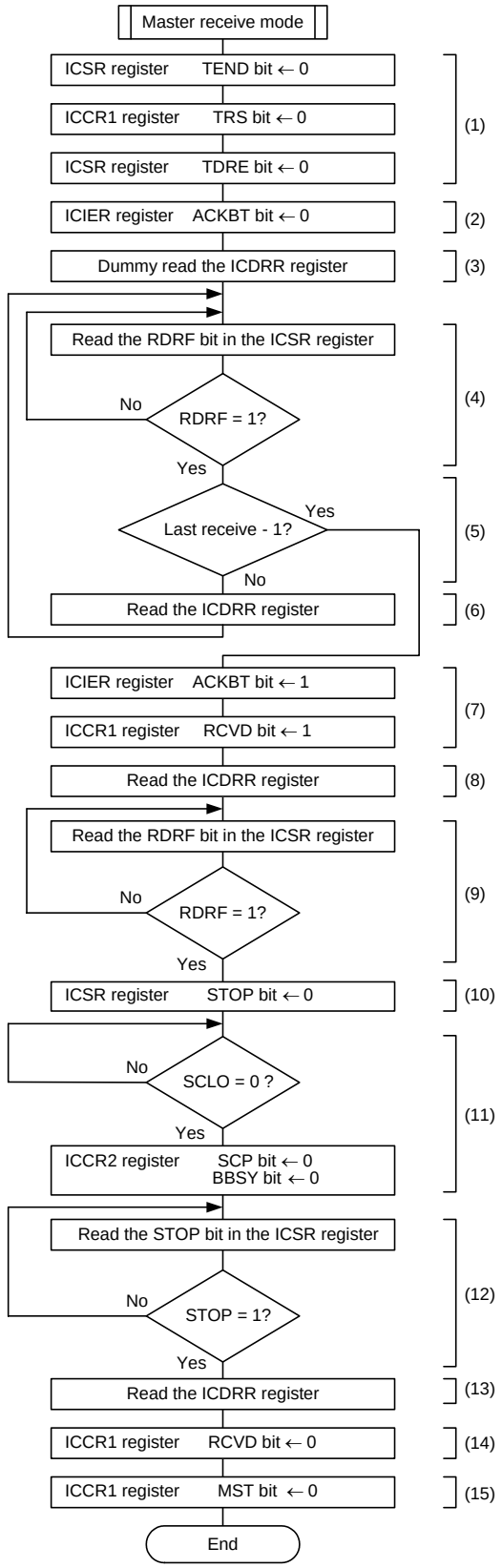


Figure 23.16 Register Setting Example in Master Transmit Mode (I2C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0. (1,2)

(2) Set the ACKBT bit to the transmit device. (1)

(3) Dummy read the ICDRR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition. (3)

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts while processing steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.
3. After confirming the falling edge of the 9th clock cycle of SCL, generate a stop condition. Refer to **23.9.1 Master Receive Mode**.

Figure 23.17 Register Setting Example in Master Receive Mode (I2C bus Interface Mode)

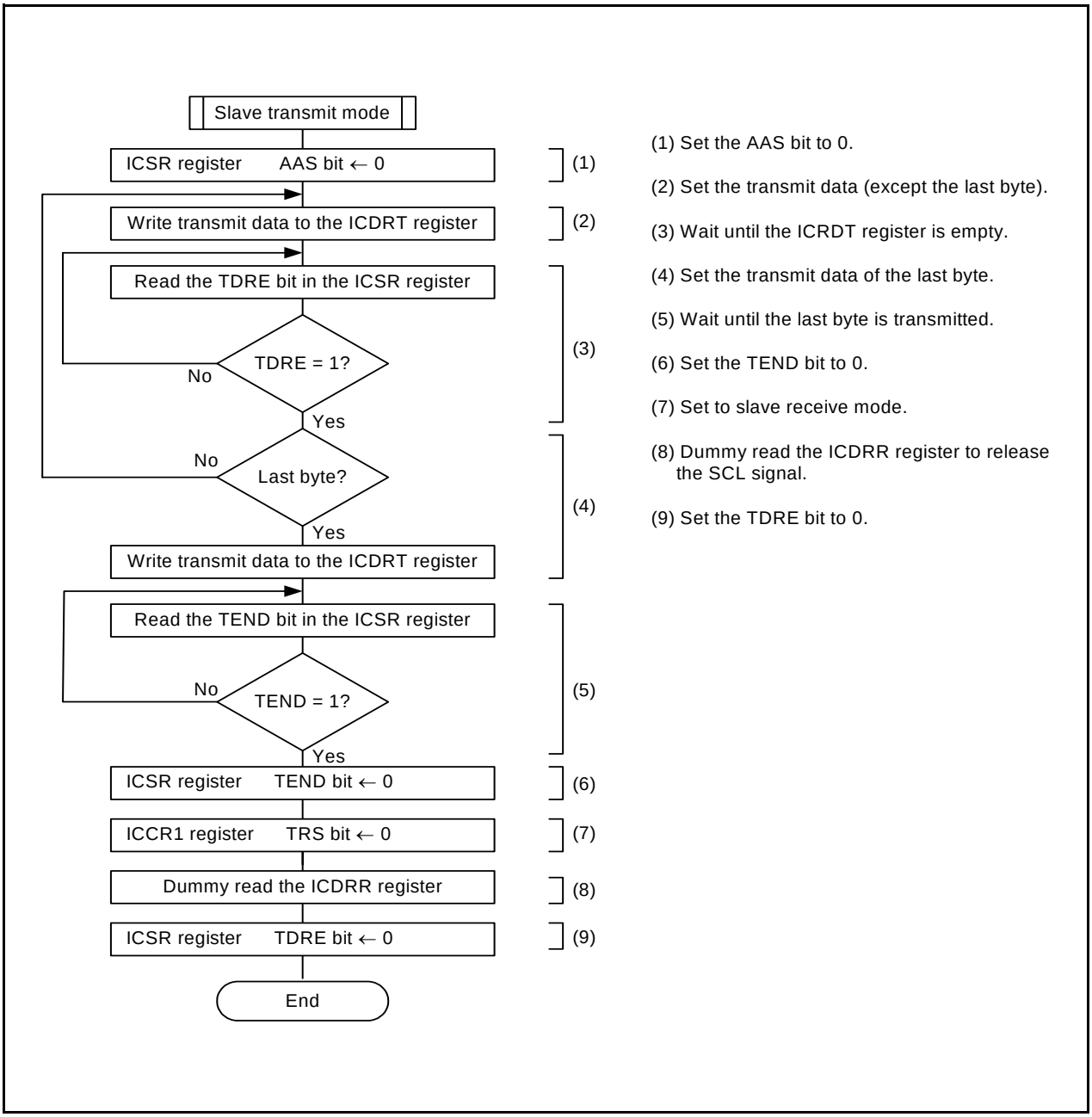
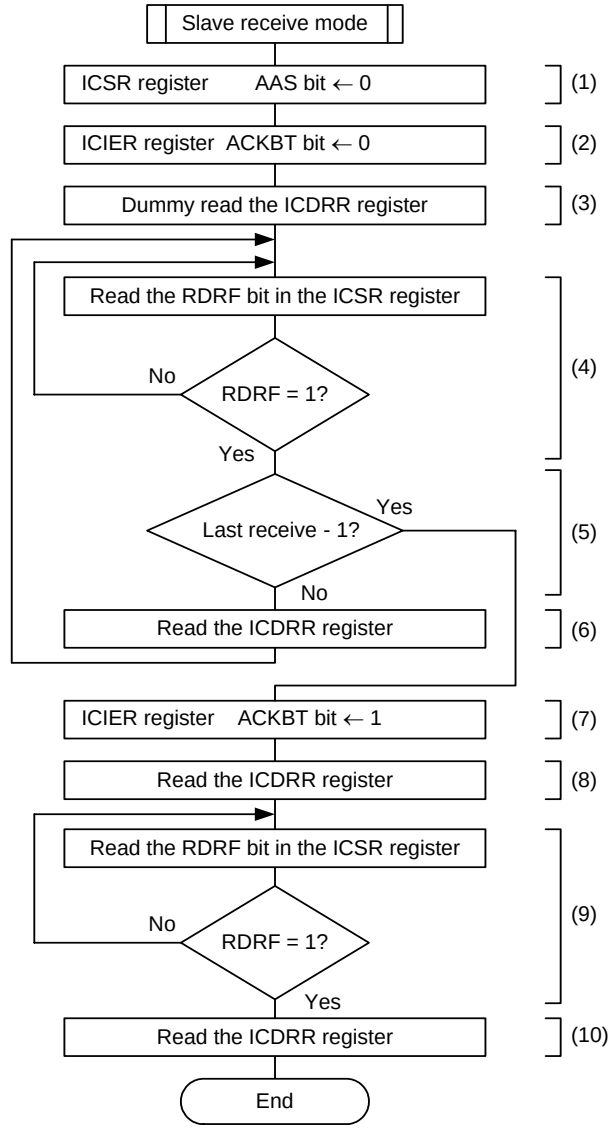


Figure 23.18 Register Setting Example in Slave Transmit Mode (I2C bus Interface Mode)



(1) Set the AAS bit to 0. (1)

(2) Set the ACKBT bit to the transmit device.

(3) Dummy read the ICDRR register.

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte. (1)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Read the receive data of the last byte.

Note:
1. For 1 byte of data reception, skip steps (2) to (6) after (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.

Figure 23.19 Register Setting Example in Slave Receive Mode (I2C bus Interface Mode)

23.7 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally.
Figure 23.20 shows a Block Diagram of Noise Canceller.
The noise canceller consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

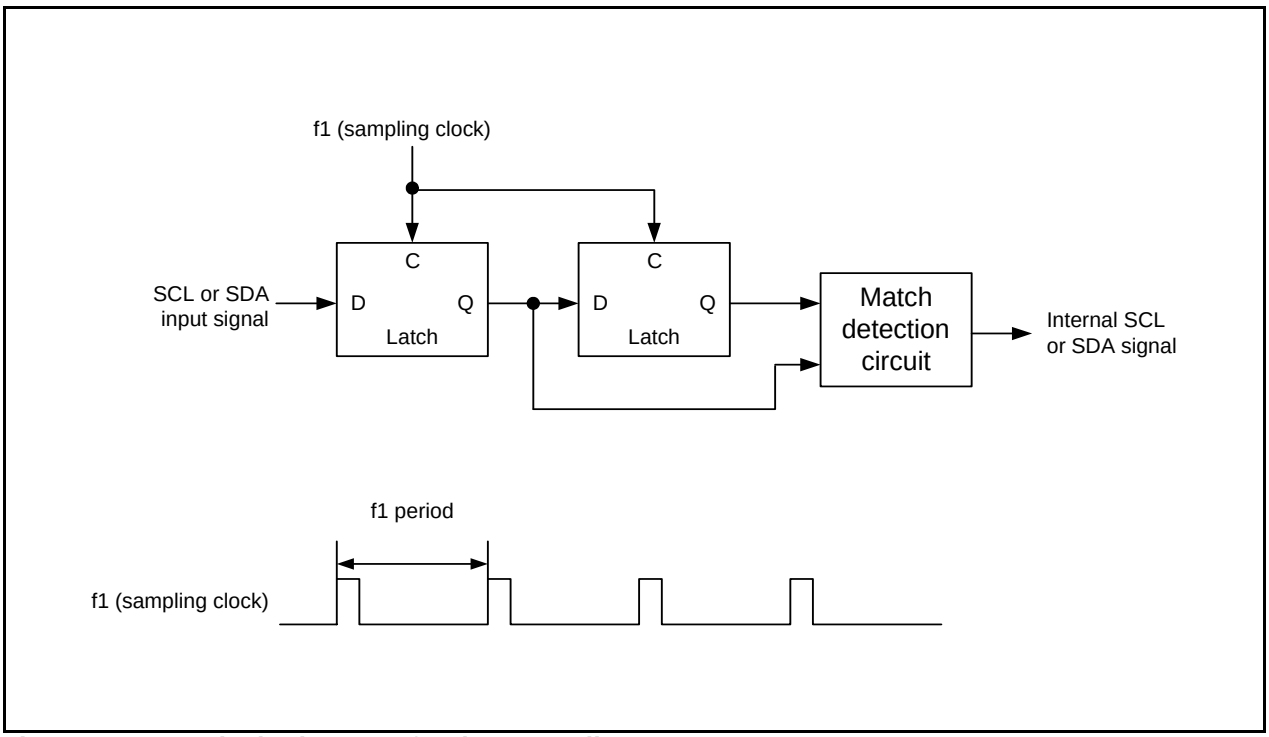


Figure 23.20 Block Diagram of Noise Canceller

23.8 Bit Synchronization Circuit

When the I2C bus interface is set to master mode, the high-level period may become shorter if:

- The SCL signal is held low by a slave device.
- The rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.

Figure 23.21 shows the Bit Synchronization Circuit Timing and Table 23.6 lists the Time between Changing SCL Signal from Low-Level Output to High-Impedance and Monitoring SCL Signal.

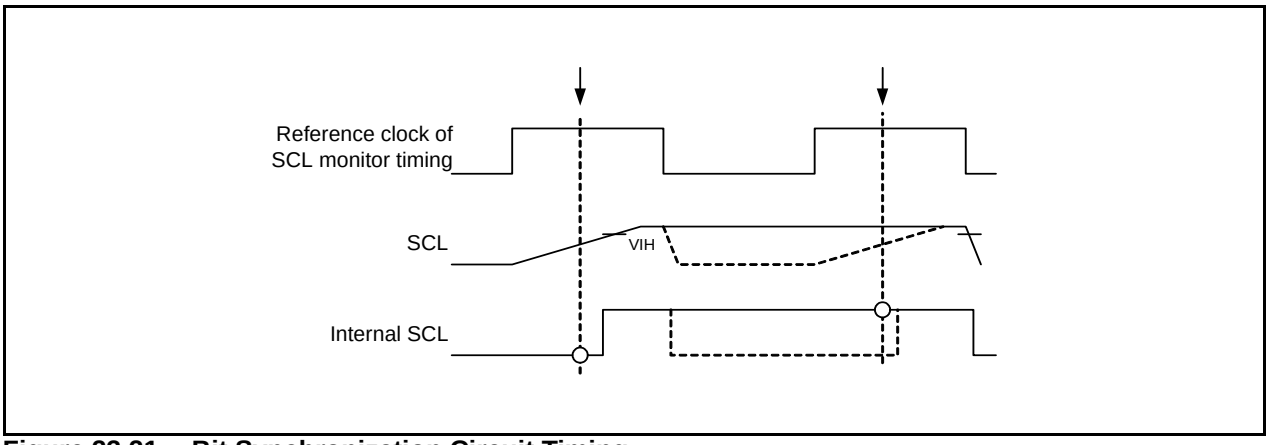


Figure 23.21 Bit Synchronization Circuit Timing

Table 23.6 Time between Changing SCL Signal from Low-Level Output to High-Impedance and Monitoring SCL Signal

ICCR1 Register		SCL Monitoring Time
CKS3	CKS2	
0	0	7.5Tcyc
	1	19.5Tcyc
1	0	17.5Tcyc
	1	41.5Tcyc

1Tcyc = 1/f1(s)

23.9 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

23.9.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

23.9.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

23.9.2 The ICE Bit in the ICCR1 Register and the IICRST Bit in the ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

23.9.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

23.9.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

23.9.2.3 Additional Descriptions Regarding the IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

24. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

24.1 Introduction

Table 24.1 lists the Flash Memory Version Performance. (Refer to the specifications in **Table 1.1** for items not listed in Table 24.1.)

Table 24.1 Flash Memory Version Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 24.1** and **Figure 24.2**.
Programming method		Byte units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method (2)	Blocks 0 to 5 (Program ROM)	Rewrite protect control in block units by the lock bit
	Blocks A and B (Data flash)	Individual rewrite protect control on blocks A and B by bits FMR14 and FMR15 in the FMR1 register
Number of commands		7 commands
Programming and erasure endurance (3)	Blocks 0 to 5 (Program ROM)	10,000 times
	Blocks A, B, C, and D (Data flash)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

Notes:
1. To program and erasure program ROM, use VCC = 1.8 V to 5.5 V as the supply voltage.
2. To program and erasure data flash, use VCC = 1.8 V to 5.5 V as the supply voltage.
3. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programing/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

Table 24.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	–

24.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 24.1 and Figure 24.2 show the Flash Memory Block Diagrams of R8C/LAPS Group.
The user ROM area contains program ROM and data flash.
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.

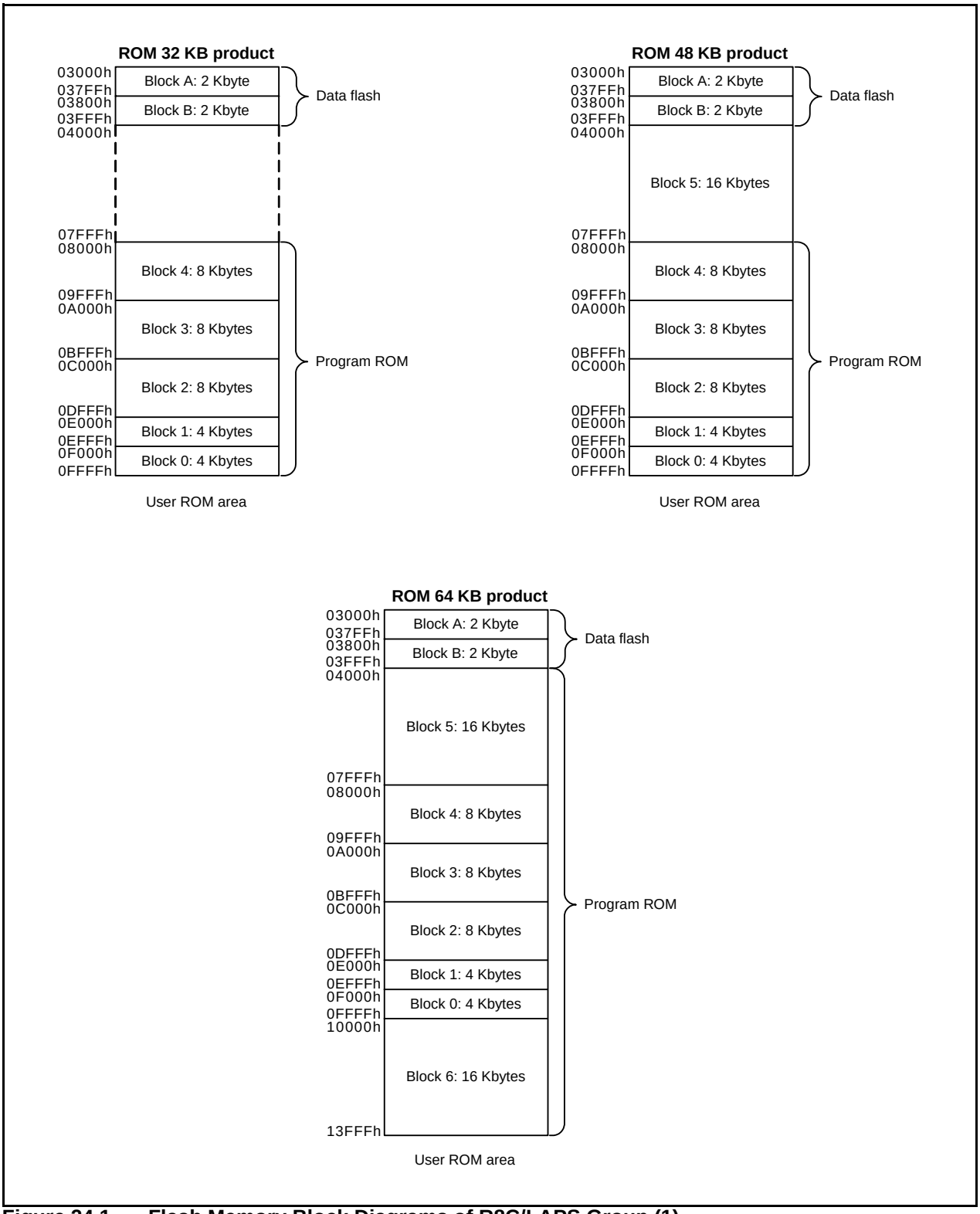


Figure 24.1 Flash Memory Block Diagrams of R8C/LAPS Group (1)

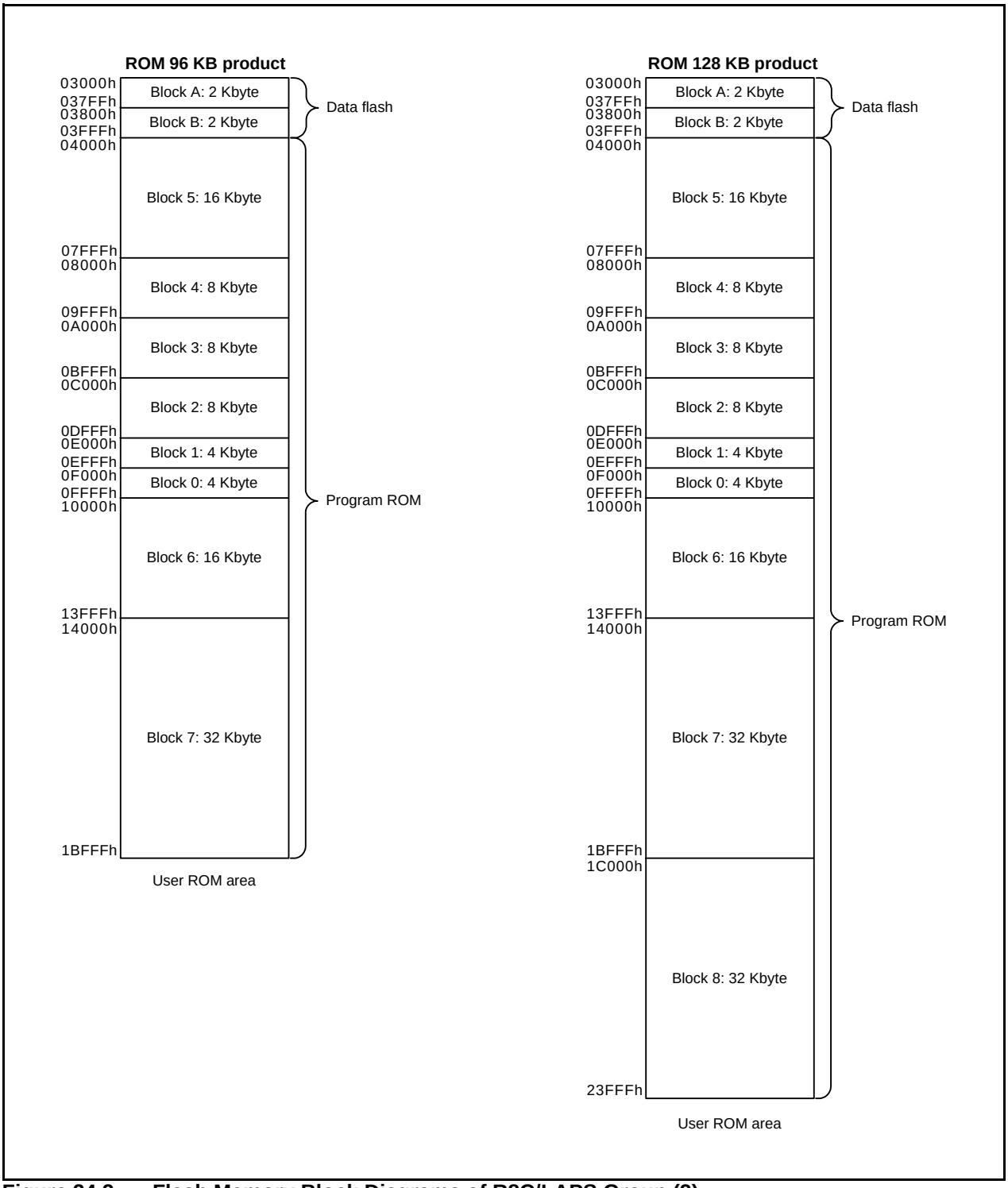


Figure 24.2 Flash Memory Block Diagrams of R8C/LAPS Group (2)

24.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

24.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **13. ID Code Areas**.

24.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **14. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the content of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

24.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

24.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has a suspend function (program-suspend, erase-suspend) which halts erase or program operation temporarily in CPU rewrite mode. During suspend, the flash memory can be read. For erase-suspend only, the flash memory can also be programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 24.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 24.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.)	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions	—	Program and block commands cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering suspend	Read array mode	Read array mode
CPU state during programming and block erasure	The CPU operates.	The CPU is put in a hold state during programming and block erasure. (I/O ports retain the states before the command execution).
Flash memory status detection	Read bits FST7, FST5, and FST4 in the FST register by a program.	Read bits FST7, FST5, and FST4 in the FST register by a program.
Conditions for entering erase-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
Conditions for entering program-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

24.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	FST3	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	FST3	Program-suspend status flag	0: Other than program-suspend 1: During program-suspend	R
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
   When writing 0 (no flash ready status interrupt request) to the RDYSTI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
   When writing 0 (no flash access error interrupt request) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash Ready Status Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:

- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it has been stopped.

BYSAEI Bit (Flash Access Error Interrupt Request Flag)

The BYSAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FMR0 register is set to 1 and while the flash memory is busy.
Or, read the data flash area while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST3 Bit (Program-Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when a program-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **24.4.11 Full Status Check**.

FST5 Bit (Erase Error/Blank Check Error Flag)

This is a read-only bit indicating the status of auto-erasure or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **24.4.11 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:

- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

24.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in low-speed on-chip oscillator mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **10.6.9 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

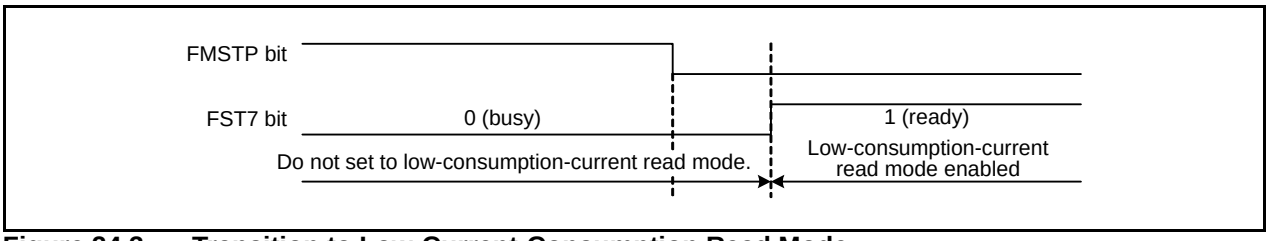


Figure 24.3 Transition to Low-Current-Consumption Read Mode

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a block program or erase command.
If the program or block erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program to the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erase command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly terminated and reading from the flash memory is enabled.

CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:

- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt request) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt request) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

24.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	FMR15	FMR14	FMR13	—	—	—
After Reset	0	0	0	0	0	0	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R
b2	—			R/W
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Disable interrupts between writing 1 and writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **24.4.9 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met:
- Completion of the program command
- Completion of the erase command
- Generation of a command sequence error
- Transition to erase-suspend
- The FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- The FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- The CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data Flash Block A Rewrite Disable Bit)

When the FMR 14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data Flash Block B Rewrite Disable Bit)

When the FMR 15 bit is set to 0, data flash block B accepts program and block erase commands.

24.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Suspend enable bit (1)	0: Suspend disabled 1: Suspend enabled	R/W
b1	FMR21	Suspend request bit (2)	0: Restart 1: Suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Suspend request disabled by interrupt request 1: Suspend request enabled by interrupt request	R/W
b3	—	Nothing is assigned. If necessary, set to 0.		—
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Note:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. Set the FMR27 bit to 1 after setting either of the following:
   • Set the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the suspend function is enabled.

FMR21 Bit (Suspend Request Bit)

When the FMR21 bit is set to 1, suspend mode is entered. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request for the enabled interrupt is generated, and suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- The FMR22 bit is set to 1 (suspend request enabled by interrupt request) when an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) at the time an interrupt request is generated during auto-erasure.
Set the FMR22 bit to 1 when using suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Current-Consumption Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), current consumption when reading the flash memory can be reduced. Refer to **10.6.10 Low-Current-Consumption Read Mode** for details.

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

24.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter suspend during auto-programming or auto-erasure, set the FMR20 bit to 1 (suspend enabled) and the FMR21 bit to 1 (suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST3 bit is set to 1 (during program-suspend) or the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST3 bit is set to 0, program completes, the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (restart), auto-programming or auto-erasure restarts. To confirm whether auto-programming or auto-erasure has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST3 bit is set to 0 (other than program-suspend) the FST6 bit is set to 0 (other than erase-suspend).

24.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed.

To enable the suspend function, execute the program or block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (suspend request enabled by interrupt request). Also, the interrupt to enter suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (suspend request) and auto-programming or auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (restart) to restart auto-programming or auto-erasure.

24.4.7 Suspend Operation

The suspend function halts the operation temporarily during auto-programming or auto-erasure.
When auto-programming or auto-erasure is suspended, the next operation can be executed. (Refer to **Table 24.4 Executable Operation during Suspend**.)

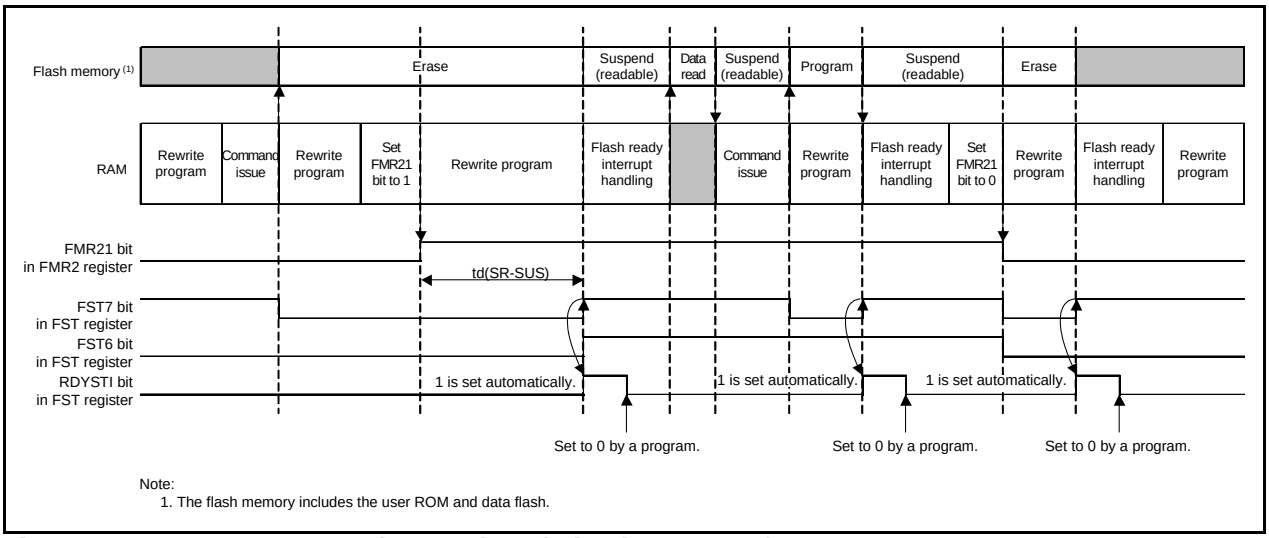
- To check the program-suspend, verify the FST7 bit is set to 1 (ready), then verify the FST3 bit is set to 1 (during program-suspend) to confirm whether programming has been suspended. (When the FST3 bit is set to 0 (other than program-suspend), programming completes.)
- To check the erase-suspend, verify the FST7 bit is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. (When the FST6 bit is set to 0 (other than erase-suspend), erasure completes.)

Figure 24.4 shows the Erase-Suspend Operation Timing in EW0 Mode.

Table 24.4 Executable Operation during Suspend

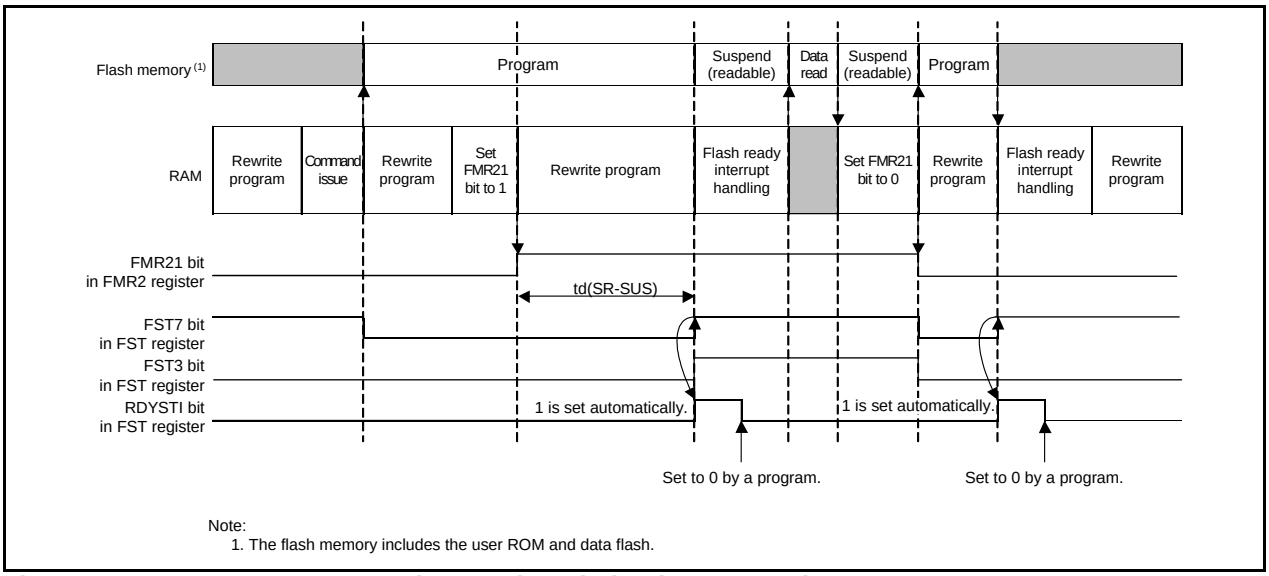
		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	D	D	D	D	E	E	N/A	N/A	N/A	D	E	E
	Program ROM	N/A	N/A	N/A	D	E	E	D	D	D	D	E	E
Areas during program execution before entering suspend	Data flash	D	D	D	D	D	E	N/A	N/A	N/A	D	D	E
	Program ROM	N/A	N/A	N/A	D	D	E	D	D	D	D	D	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
3. The MCU enters read array mode immediately after entering suspend.



Note:
1. The flash memory includes the user ROM and data flash.

Figure 24.4 Erase-Suspend Operation Timing in EW0 Mode



Note:
1. The flash memory includes the user ROM and data flash.

Figure 24.5 Program-Suspend Operation Timing in EW0 Mode

24.4.8 How to Set and Exit Each Mode

Figure 24.6 shows How to Set and Exit EW0 Mode and Figure 24.7 shows How to Set and Exit EW1 Mode (When Rewriting Data Flash) and EW1 Mode.

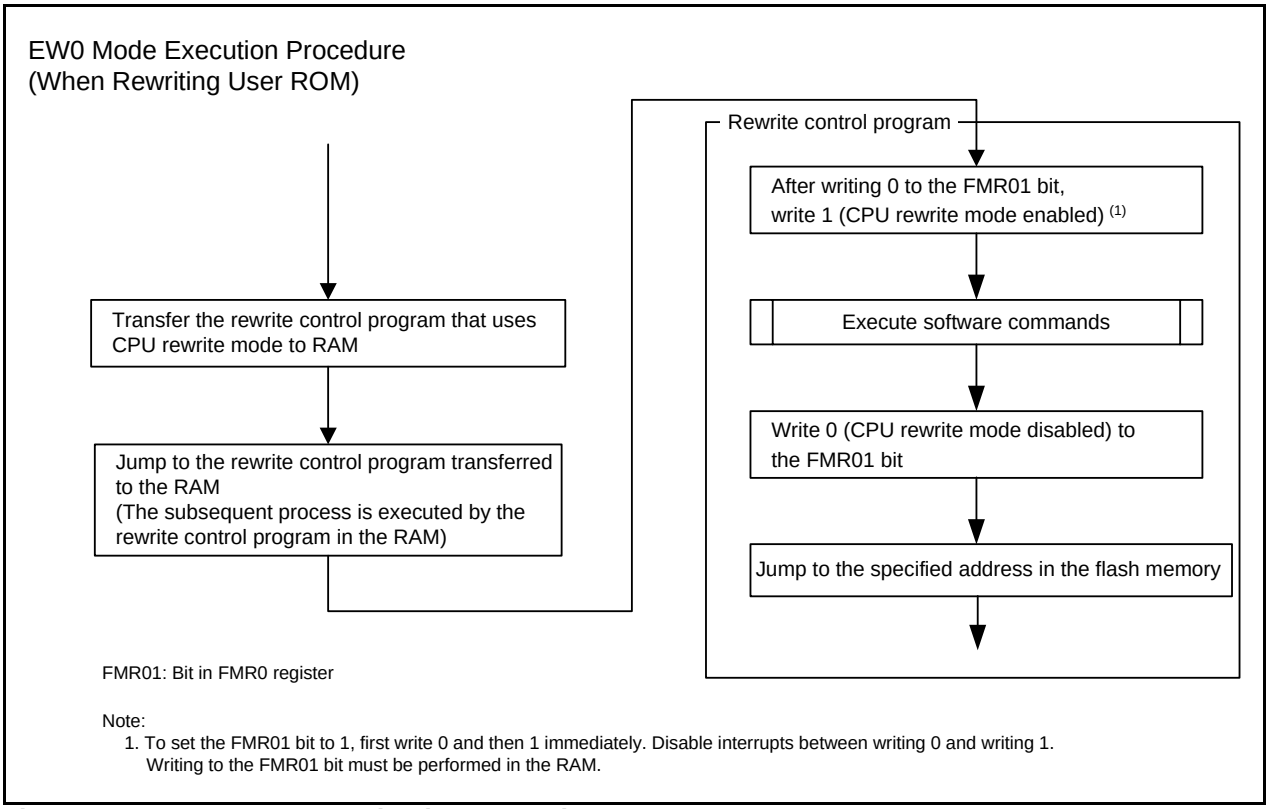


Figure 24.6 How to Set and Exit EW0 Mode

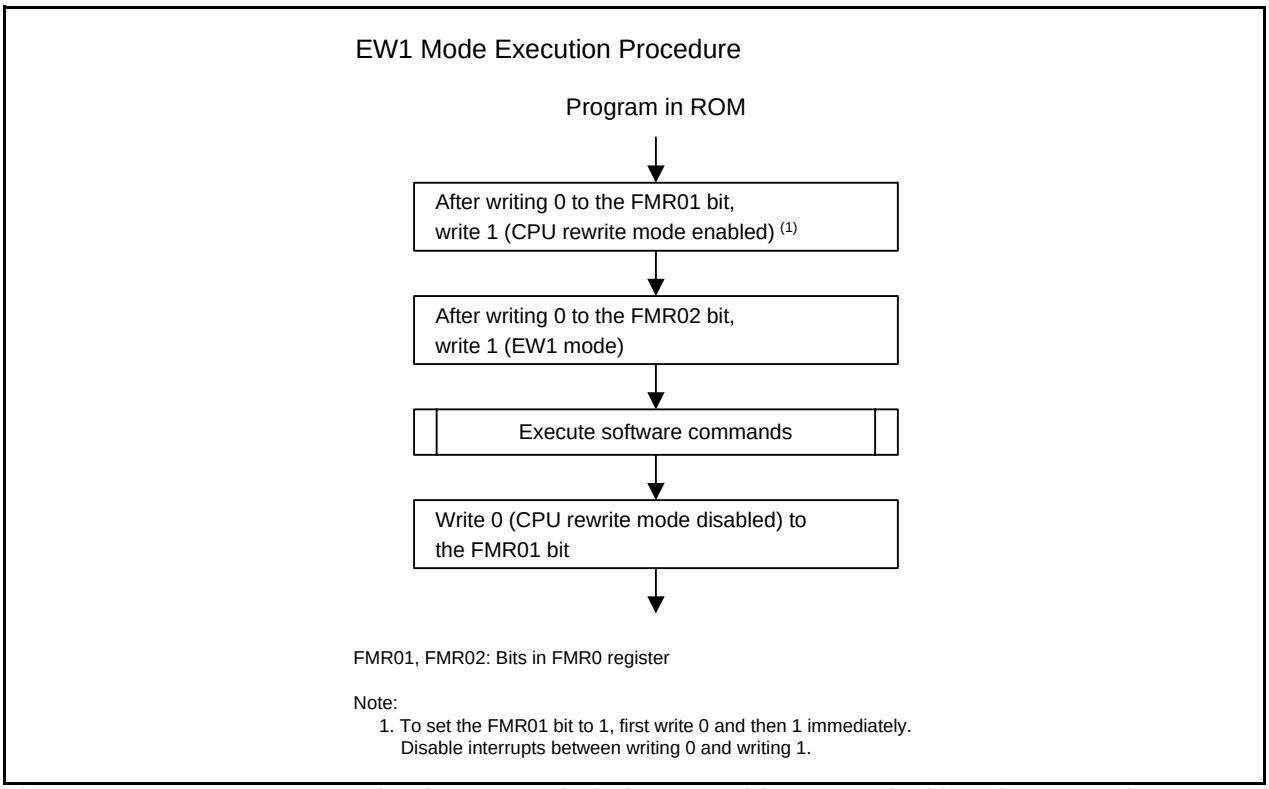


Figure 24.7 How to Set and Exit EW1 Mode (When Rewriting Data Flash) and EW1 Mode

24.4.9 Data Protect Function

Each block in the program ROM has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **24.4.10 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 24.8 shows the FMR13 Bit Operation Timing.

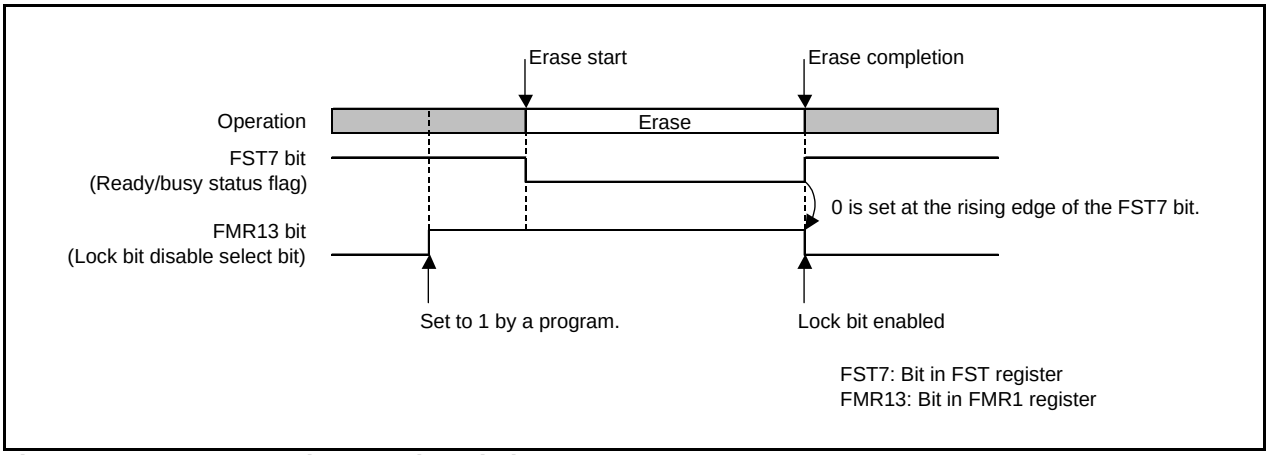


Figure 24.8 FMR13 Bit Operation Timing

24.4.10 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.

Table 24.5 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Clear status register	Write	×	50h			
Program (byte units)	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

WA: Write address (specify the even address to program in word units.)
WD: Write data
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area

24.4.10.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering erase-suspend.

24.4.10.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

24.4.10.3 Program Command

The program command is used to write data to the flash memory in 1-byte.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **24.4.11 Full Status Check**).
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Program commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Program commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).

Figure 24.9 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 24.10 shows a Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. If the FMR21 bit changes to 1 (suspend request) while the RDYSTIE bit is 1 and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when auto-programming suspends. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

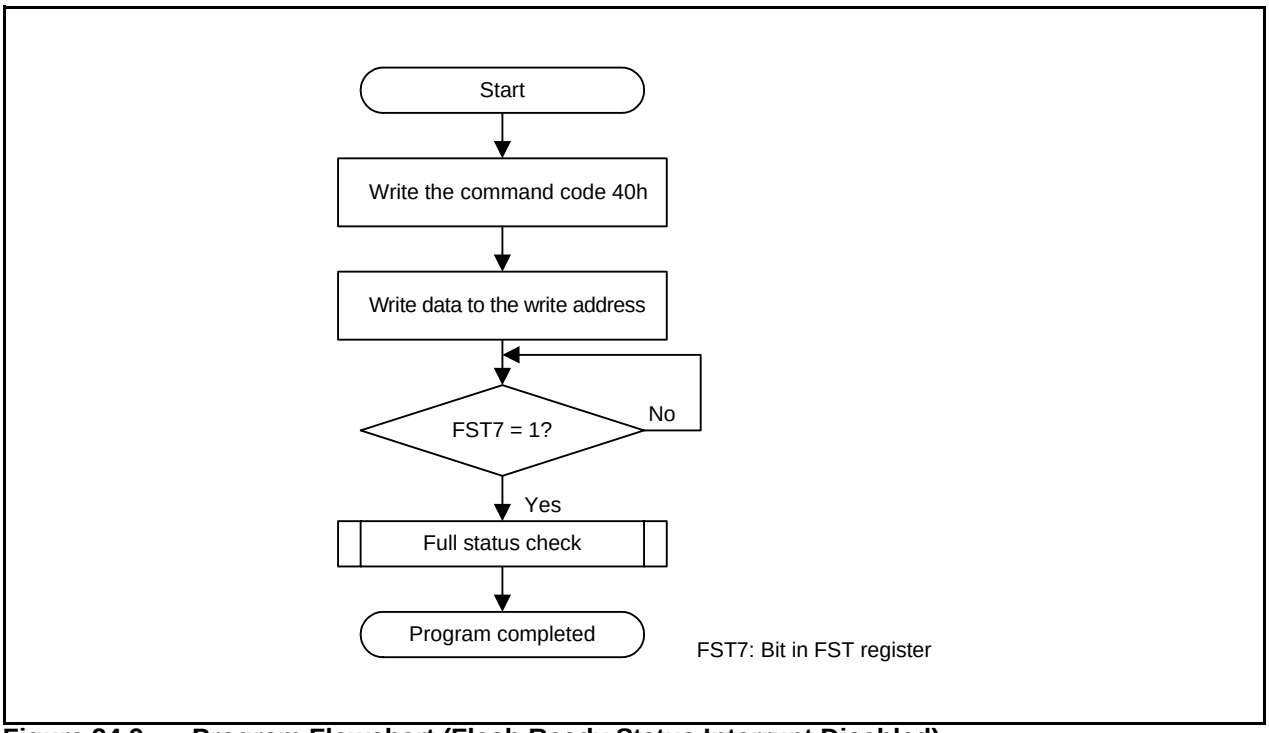
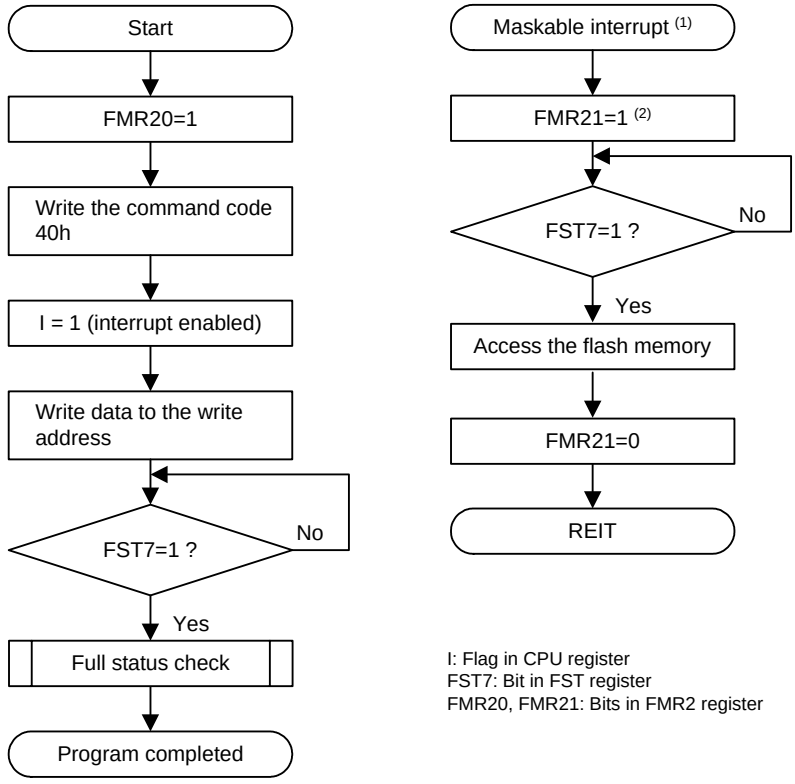
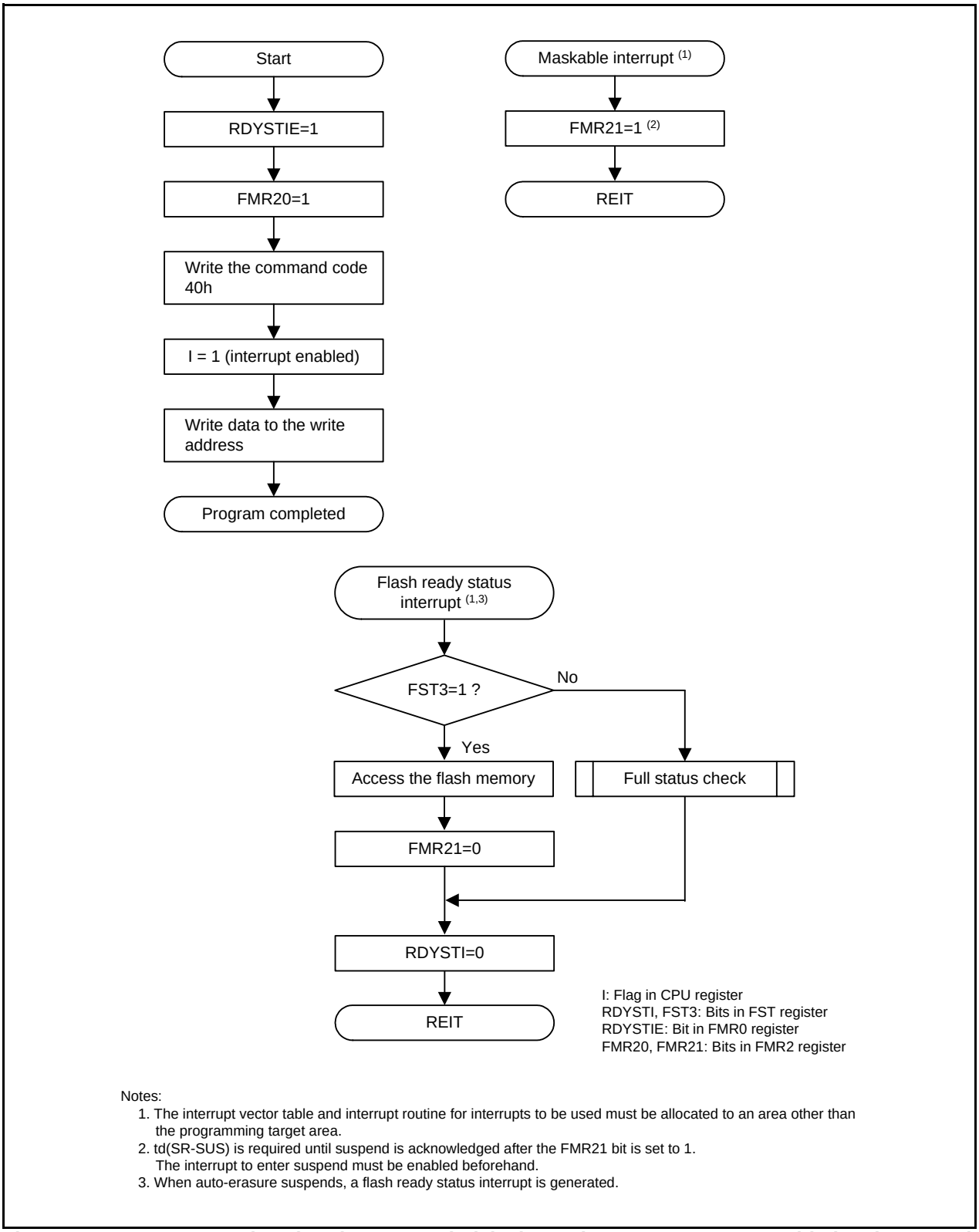


Figure 24.9 Program Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1. The interrupt to enter suspend must be enabled beforehand.

Figure 24.10 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1. The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 24.11 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.

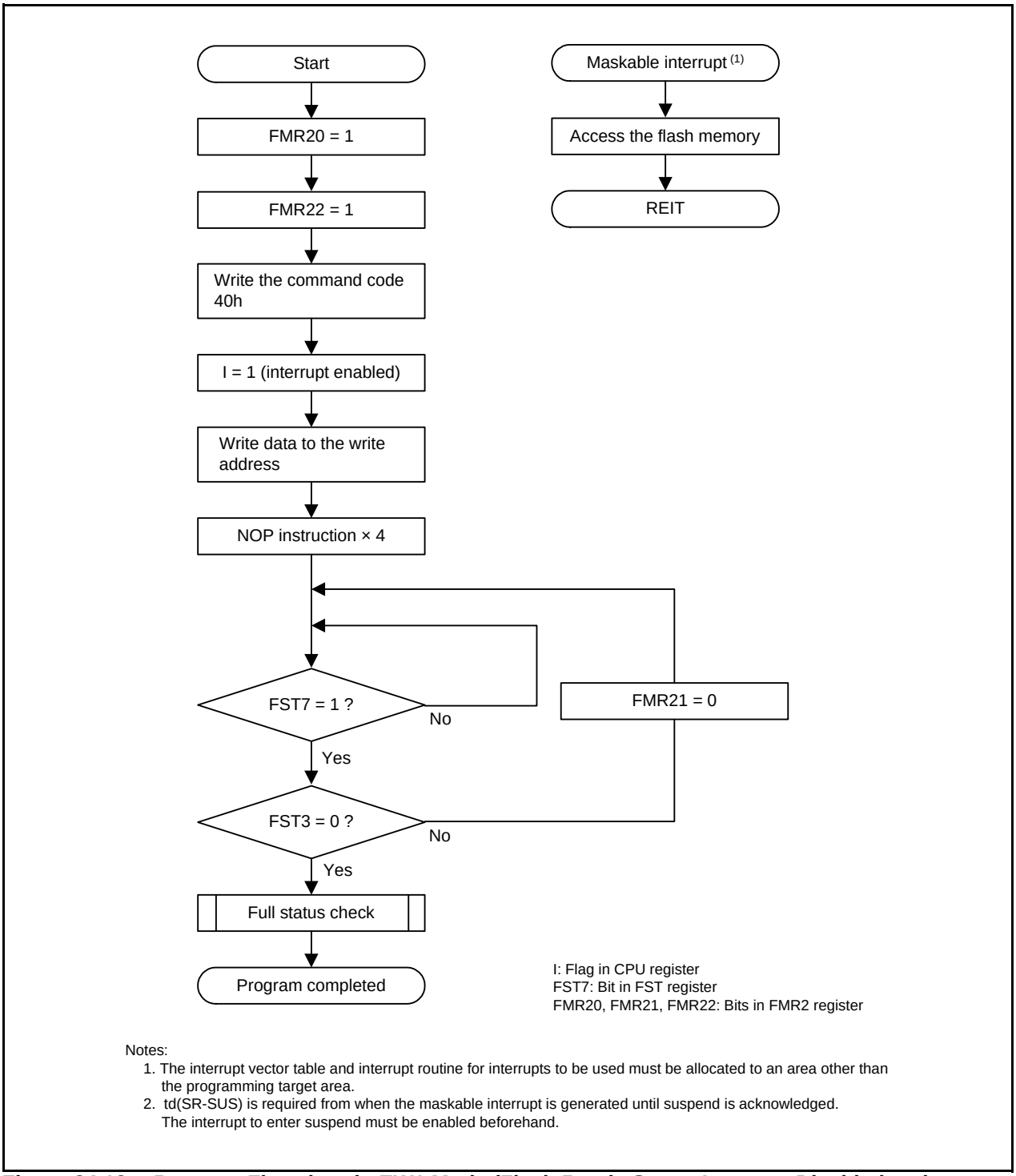


Figure 24.12 Program Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

24.4.10.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register. (Refer to **24.4.11 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).

Figure 24.13 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 24.14 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 24.15 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. If the FMR21 bit changes to 1 (suspend request) while the RDYSTIE bit is 1 and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

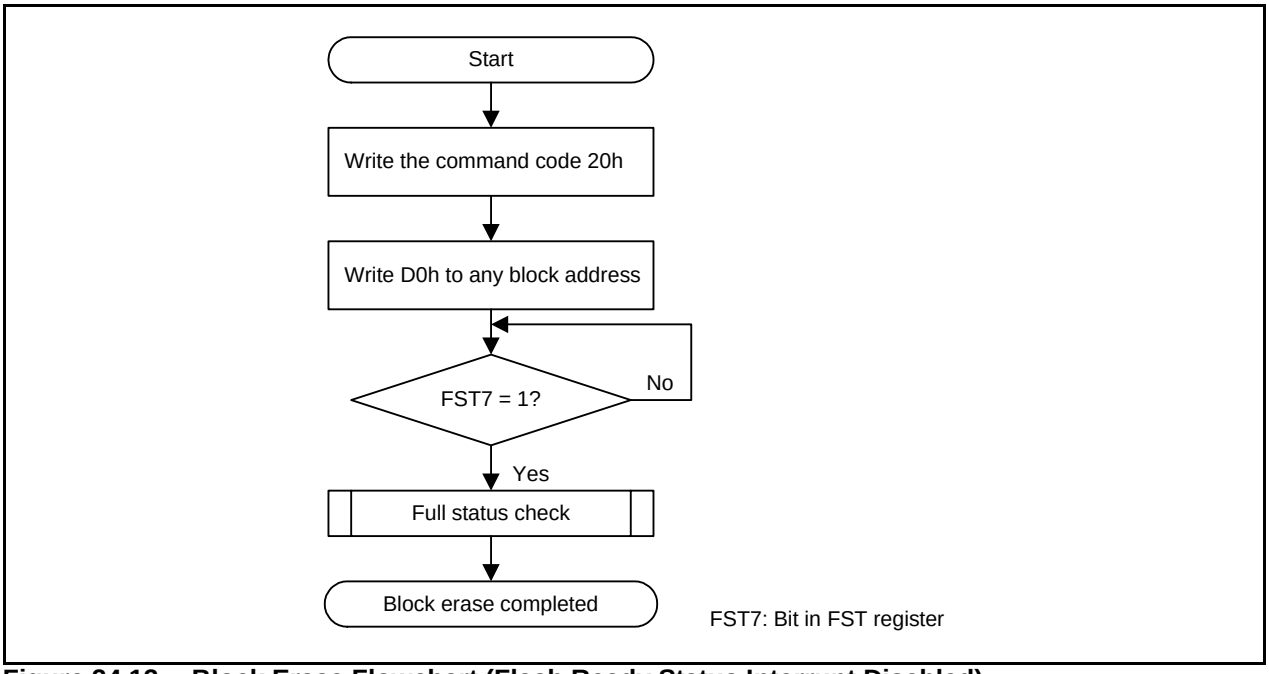
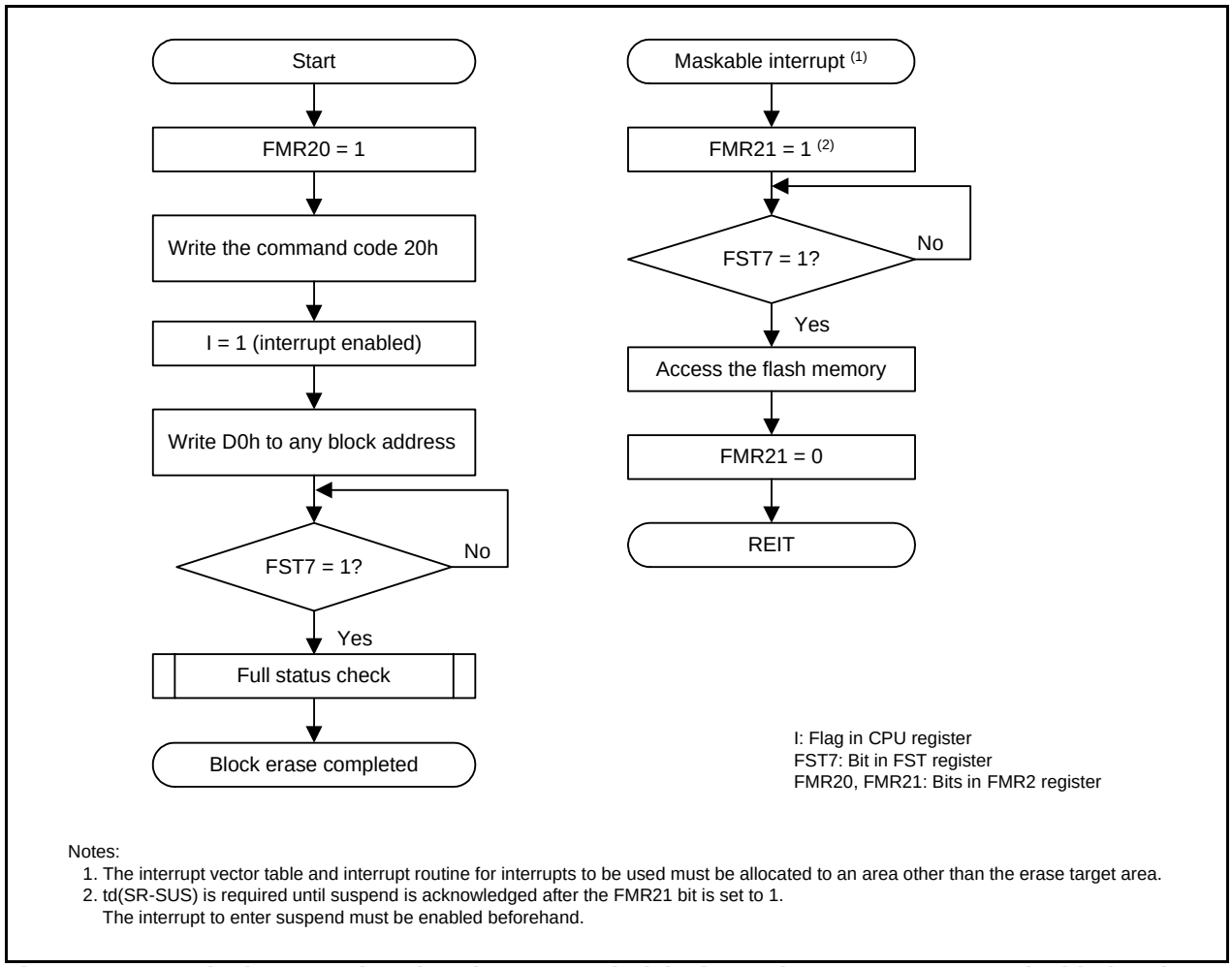
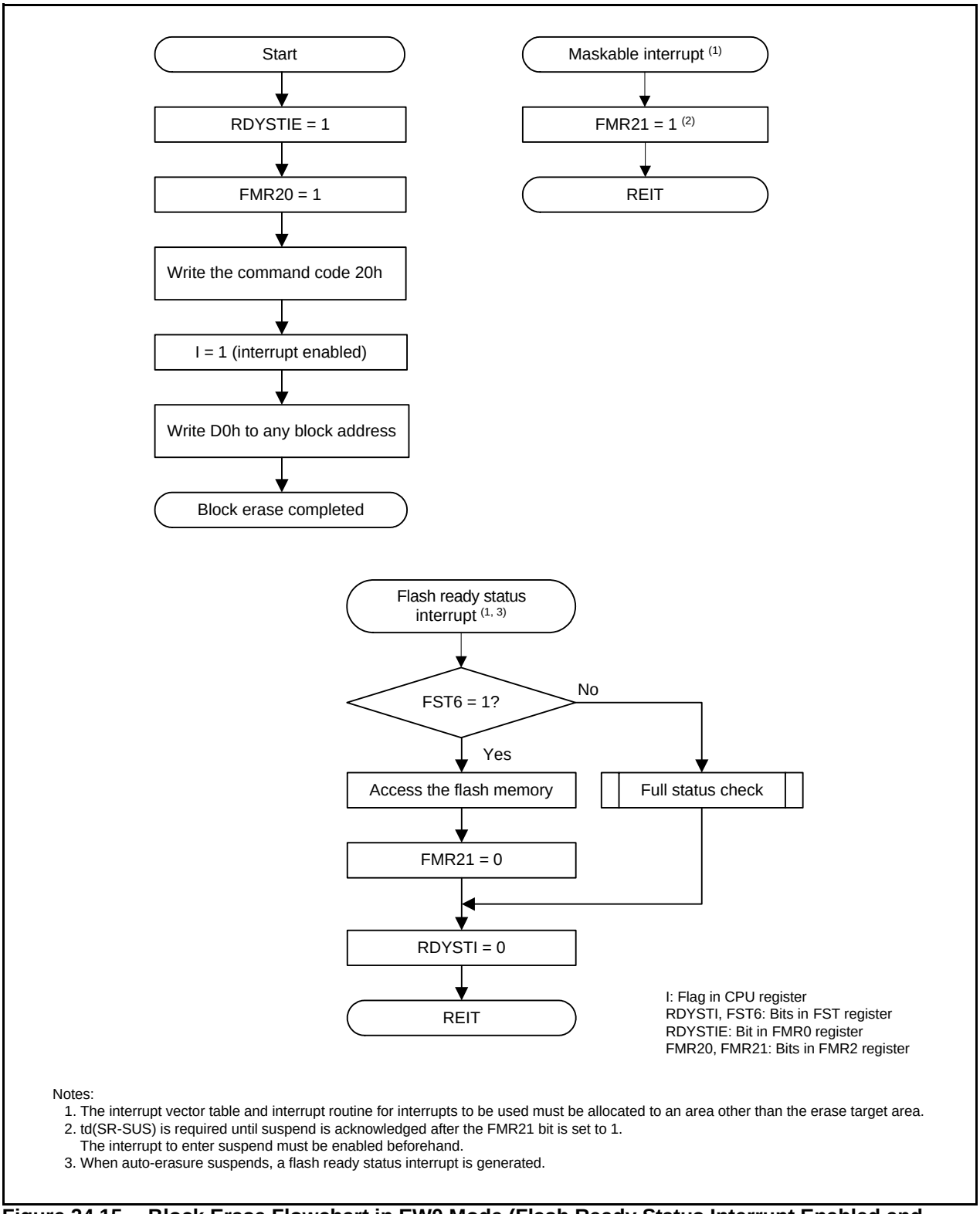


Figure 24.13 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.

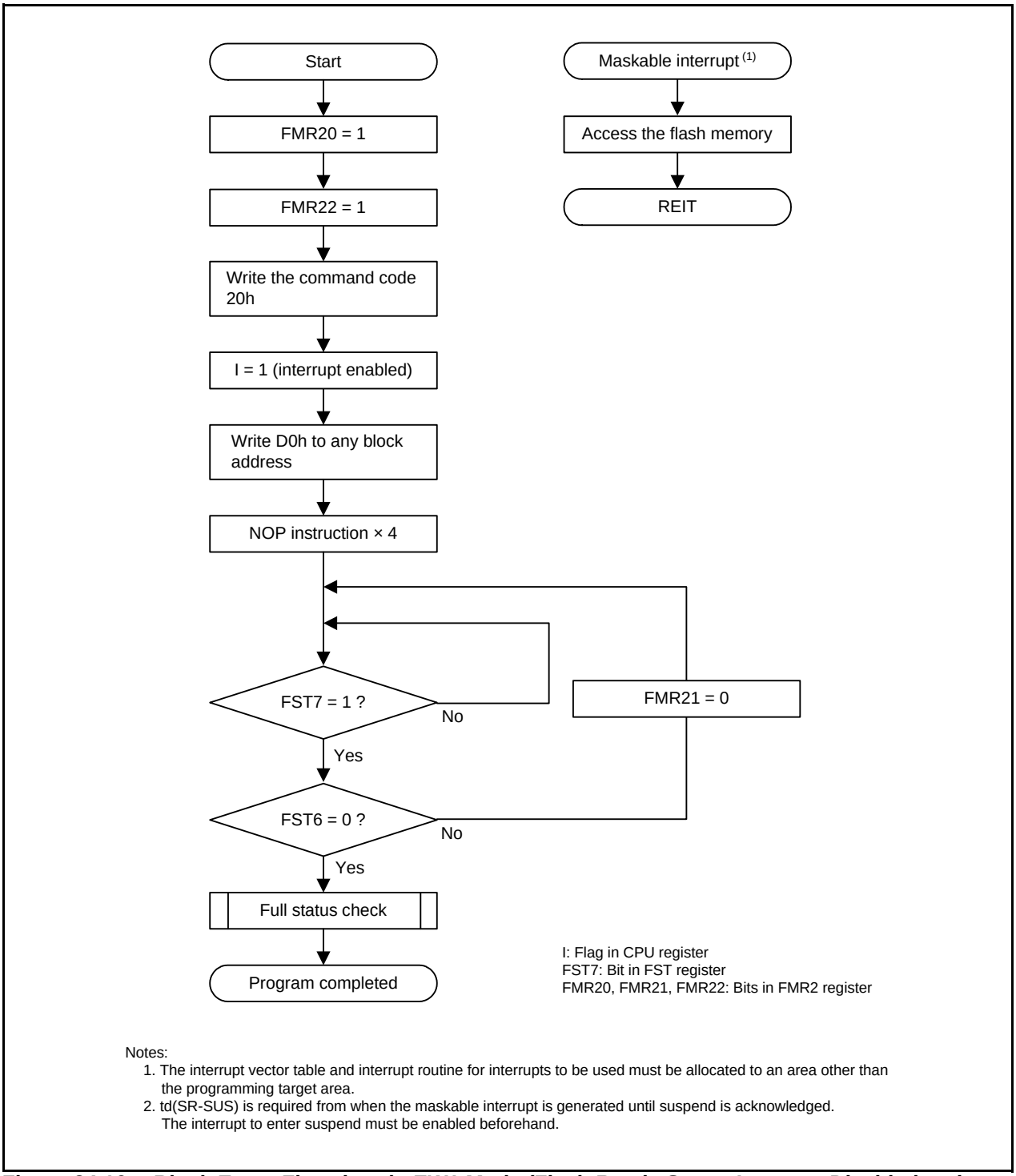
Figure 24.14 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 24.15 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 24.16 Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

24.4.10.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 24.17 shows the Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **24.4.9 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

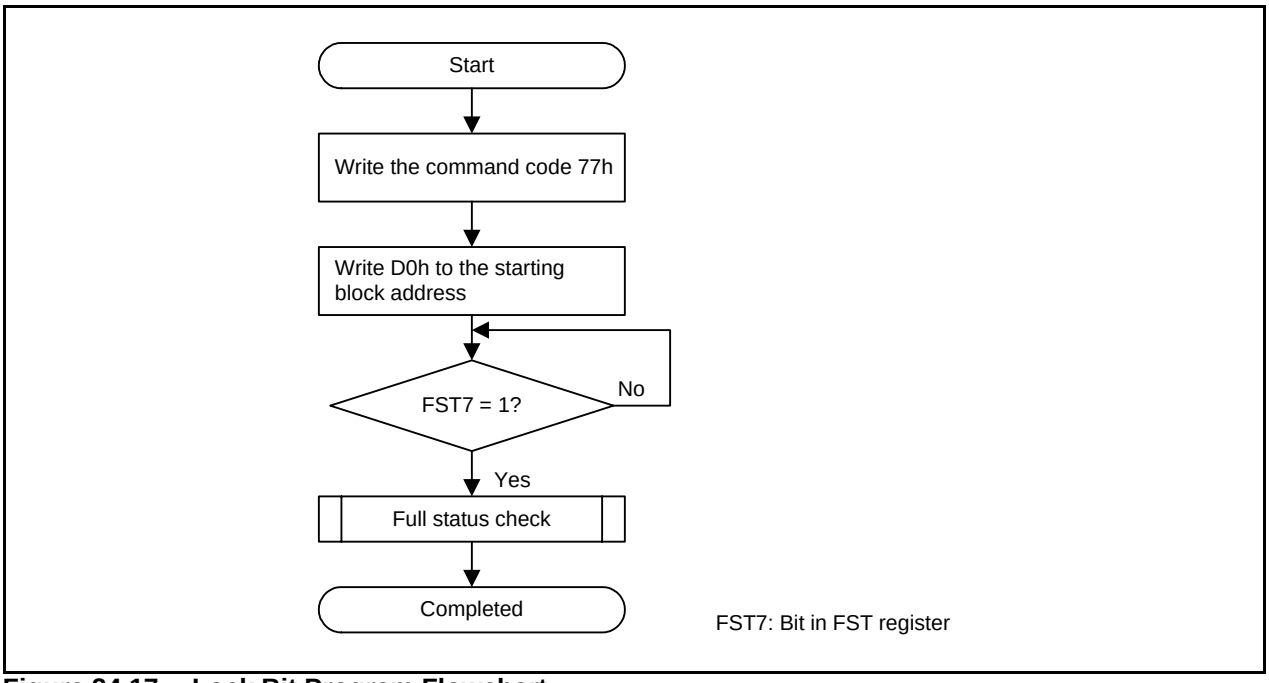


Figure 24.17 Lock Bit Program Flowchart

24.4.10.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any block in the program ROM area.
When 71h is written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 24.18 shows the Read Lock Bit Status Flowchart.

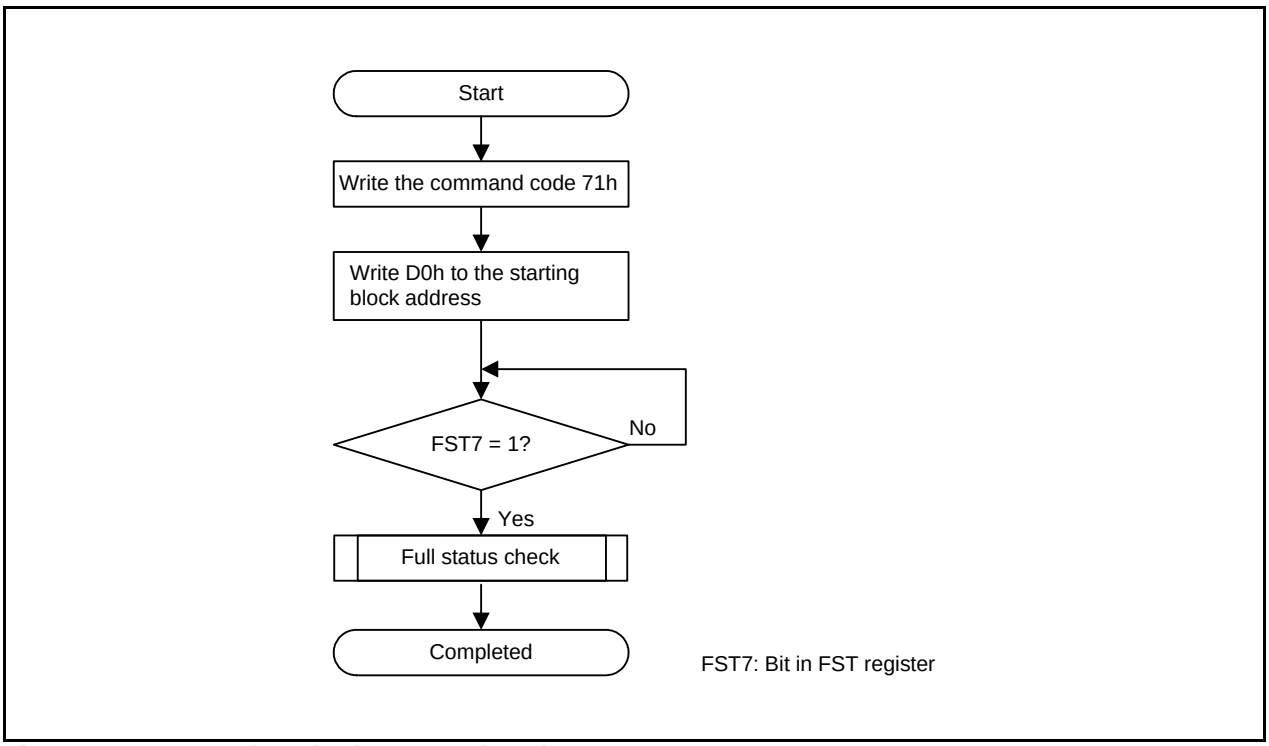


Figure 24.18 Read Lock Bit Status Flowchart

24.4.10.7 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register. (Refer to **24.4.11 Full Status Check**.). This command is used to verify the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).
Figure 24.19 shows the Block Blank Check Flowchart.

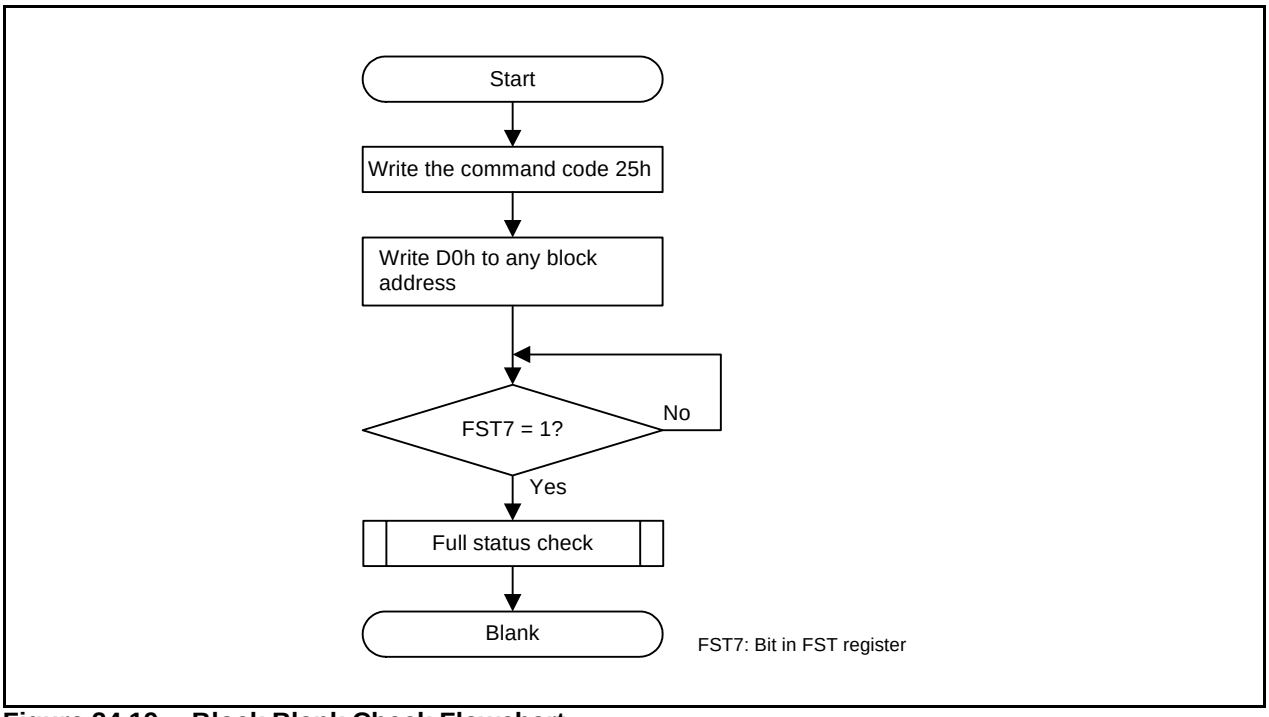


Figure 24.19 Block Blank Check Flowchart

This command is intended for programmer manufactures, not for general users.

24.4.11 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 24.6 lists the Errors and FST Register Status. Figure 24.20 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 24.6 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command (1). • The erase command is executed during erase-suspend • The program command or erase command is executed during program-suspend • The command is executed to the block during suspend
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the block blank check command is executed and data other than blank data FFh is read.
0	1	Program error	When the program command is executed, but auto-programming does not complete correctly.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0 (locked).

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

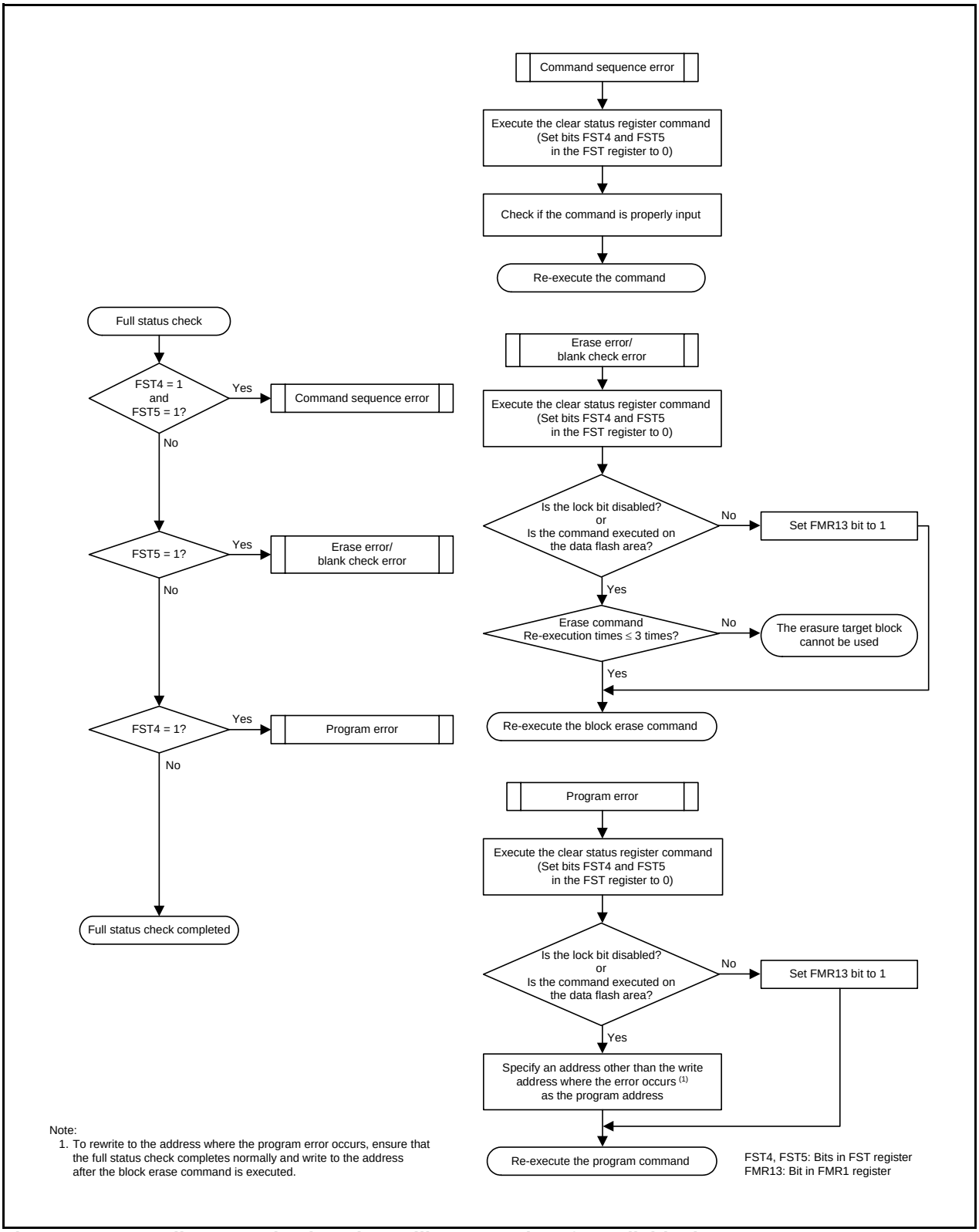


Figure 24.20 Full Status Check and Handling Procedure for Individual Errors

24.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples with Serial Programmer** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

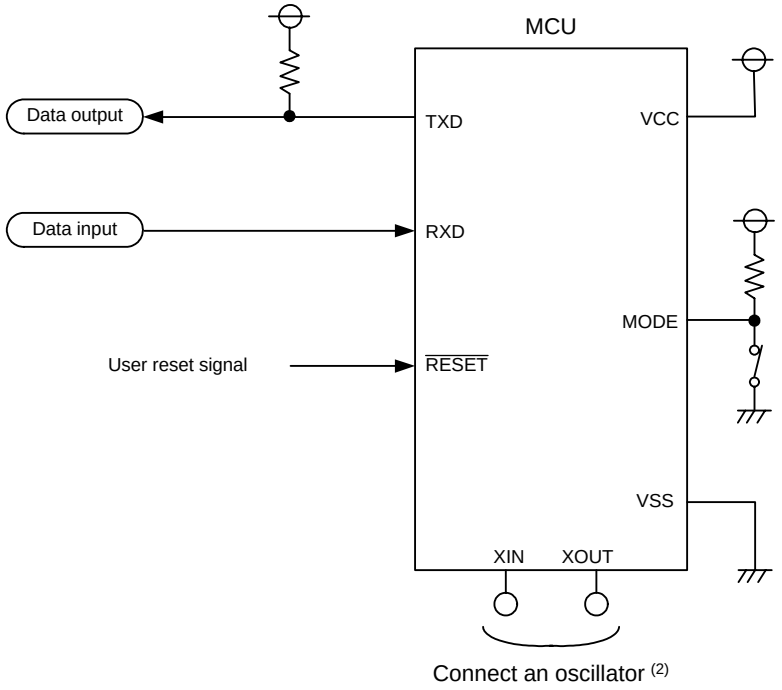
Table 24.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 24.21 shows Pin Handling in Standard Serial I/O Mode 2. Table 24.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 24.22 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 24.8 and rewriting the flash memory using the programmer, apply a high-level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

24.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **13. ID Code Areas** for details of the ID code check.

Table 24.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P9_0/XIN	P9_0 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P9_1/XOUT	P9_1 input/clock output	I/O	
MODE	MODE	I/O	Input a low-level signal.
P8_5	TXD output	O	Serial data output pin
P8_6	RXD input	I	Serial data input pin
Other I/O port pins		I	Input a high-level signal, output a low-level signal, or leave open.

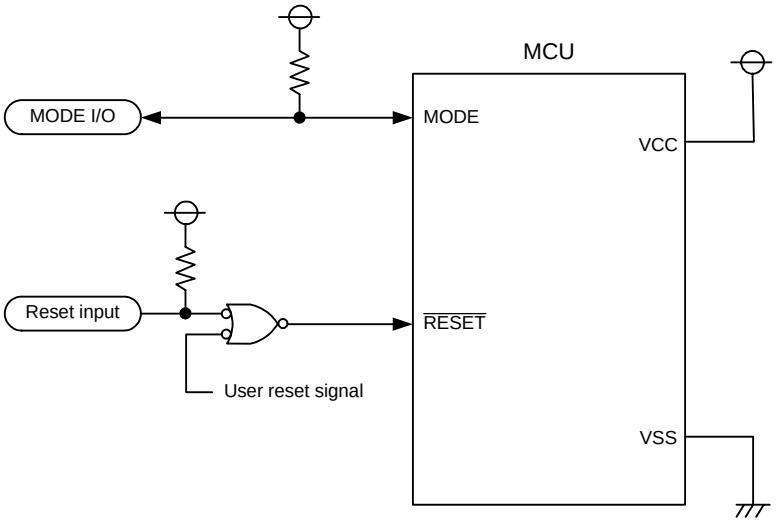


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Refer to **Appendix 2 Connection Examples with Serial Programmer**.

Figure 24.21 Pin Handling in Standard Serial I/O Mode 2

Table 24.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P9_0/XIN	P9_0 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P9_1/XOUT	P9_1 input/clock output	I/O	
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.
Other I/O port pins		I	Input a high-level signal, output a low-level signal, or leave open.



Notes:
1. Controlled pins and external circuits vary depending on the programmer.
   Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 24.22 Pin Handling in Standard Serial I/O Mode 3

24.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figures 24.1 and 24.2 can be rewritten.

24.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten. (Refer to the **24.3.2 ROM Code Protect Function**.)

24.7 Notes on Flash Memory

24.7.1 CPU Rewrite Mode

24.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

24.7.1.2 Interrupts

Tables 24.9 and 24.10 list CPU Rewrite Mode Interrupts (1) and (2), respectively.

Table 24.9 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.

FMR21, FMR22: Bits in FMR2 register

Table 24.10 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step (Note 1)
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Do not use during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

24.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.

- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts between writing 1 and writing 0.

- The FMR14 or FMR15 bit in the FMR1 register

24.7.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

24.7.1.5 Programming

Do not write additions to the already programmed address.

24.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
When the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

24.7.1.7 Programming and Erasure Voltage for Flash Memory

To program and erasure program ROM, use VCC = 1.8 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 1.8 V.

24.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

24.7.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
. The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **10.6 Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

25. Electrical Characteristics

25.1 Absolute Maximum Ratings

Table 25.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–20 °C ≤ T_{opr} ≤ 85 °C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Note:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit**.

25.2 Recommended Operating Conditions

Table 25.2 Recommended Operating Conditions
(Vcc = 1.8 to 5.5 V and Topr = −20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc	Supply voltage					1.8	–	5.5	V
Vss	Supply voltage					–	0	–	V
VIH	Input “H” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V
VIL	Input “L” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.05 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)				–	–	−160	mA
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)				–	–	−80	mA
IOH(peak)	Peak output “H” current	Port P8 (2)				–	–	−40	mA
		Other pins				–	–	−10	mA
IOH(avg)	Average output “H” current (1)	Port P8 (2)				–	–	−20	mA
		Other pins				–	–	−5	mA
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)				–	–	160	mA
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)				–	–	80	mA
IOL(peak)	Peak output “L” current	Port P8 (2)				–	–	40	mA
		Other pins				–	–	10	mA
IOL(avg)	Average output “L” current (1)	Port P8 (2)				–	–	20	mA
		Other pins				–	–	5	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	2	–	20	MHz
					2.0 V ≤ Vcc ≤ 2.7 V	2	–	20	MHz
					1.8 V ≤ Vcc < 2.0 V	2	–	20	MHz
–	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	10	MHz
					2.0 V ≤ Vcc ≤ 2.7 V	–	–	10	MHz
					1.8 V ≤ Vcc < 2.0 V	–	–	10	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	0	–	8	MHz
					2.0 V ≤ Vcc ≤ 2.7 V	0	–	8	MHz
					1.8 V ≤ Vcc < 2.0 V	0	–	8	MHz

Notes:
1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

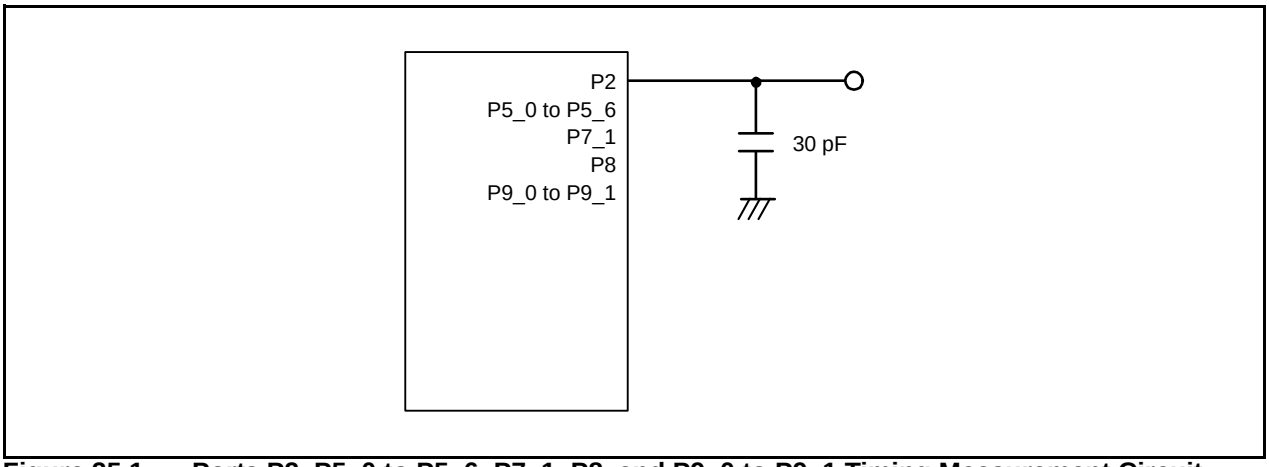


Figure 25.1 Ports P2, P5_0 to P5_6, P7_1, P8, and P9_0 to P9_1 Timing Measurement Circuit

25.3 Peripheral Function Characteristics

Table 25.3 Flash Memory (Program ROM) Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time		–	0.2	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 25.4 Flash Memory (Data flash Block A and Block B) Characteristics (V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time (program/erase endurance ≤ 10,000 times)		–	150	–	µs
–	Block erase time (program/erase endurance ≤ 10,000 times)		–	0.055	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		−20	–	85	°C
–	Data hold time (6)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

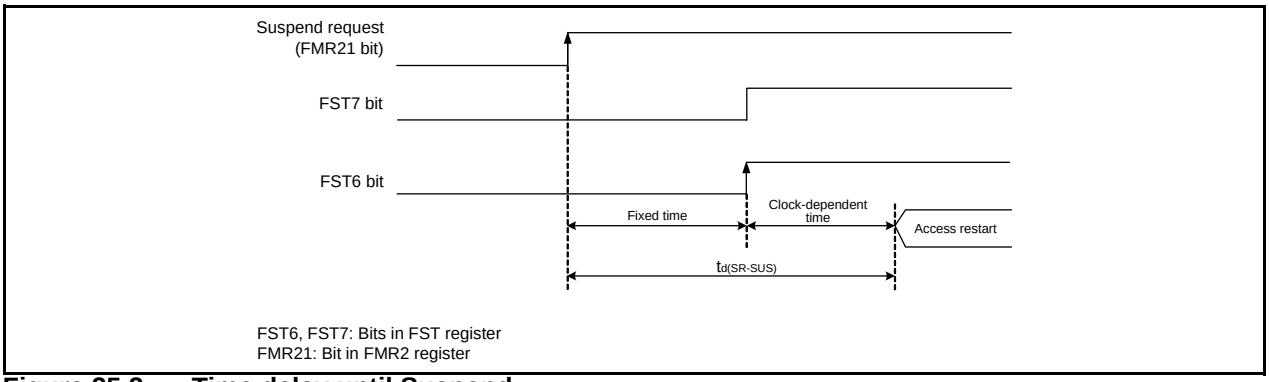


Figure 25.2 Time delay until Suspend

Table 25.5 Voltage Detection 0 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	50	500	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	100	500	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V		–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 25.6 Voltage Detection 1 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc		4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		–	0.07	–	V
		Vdet1_6 to Vdet1_F selected		–	0.10	–	V
–	Voltage detection 1 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	250	500	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 25.7 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.)

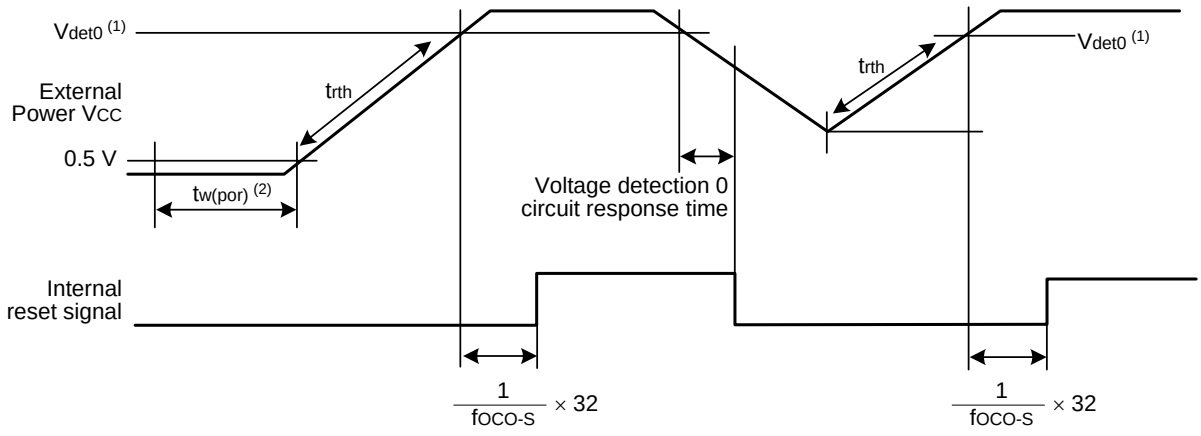
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 (1)	At the falling of V_{CC}		3.70	4.0	4.30	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit			–	0.10	–	V
–	Voltage detection 2 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	200	500	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 25.8 Power-on Reset Circuit Characteristics (1)
(T_{opr} = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		0	–	50,000	mV/ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 25.3 Power-on Reset Circuit Characteristics

Table 25.9 Low-speed On-Chip Oscillator Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time		–	–	35	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	2	–	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
–	Oscillation stability time		–	–	35	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	2	–	µA

Table 25.10 Power Supply Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = 25 °C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (1)		–	–	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

25.4 DC Characteristics

Table 25.11 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter		Condition			Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P8 (1)	V_{CC} = 5V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Other pins	V_{CC} = 5V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P8 (1)	V_{CC} = 5V	I_{OL} = 20 mA	–	–	2.0	V
			Other pins	V_{CC} = 5V	I_{OL} = 5 mA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, INT5, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRCTRG, TRCCLK, SSI, SCL, SDA, SSO				0.05	0.5	–	V
		$\overline{RESET}$				0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V			–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V			–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V			20	40	80	kΩ
R_{fXIN}	Feedback resistance	XIN				–	2.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode			1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 25.12 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition						Standard			Unit
			Oscillation Circuit XIN (2)	Low-Speed On-Chip Oscillator	CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	125 kHz	No division	–		–	4.7	10	mA
			16 MHz	125 kHz	No division	–		–	3.9	8	mA
			10 MHz	125 kHz	No division	–		–	2.3	–	mA
			20 MHz	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	3.1	–	mA
			20 MHz	125 kHz	Divide-by-8	–		–	1.8	–	mA
			16 MHz	125 kHz	Divide-by-8	–		–	1.5	–	mA
			10 MHz	125 kHz	Divide-by-8	–		–	1.0	–	mA
		Low-speed on-chip oscillator mode	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	110	320	µA
			Off	125 kHz	Divide-by-8	FMSTP = 1 VCA20 = 0		–	63	220	µA
		Wait mode	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.8	33	µA
		Stop mode	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	–	1.2	–	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V

Table 25.13 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P8 (1)	I_{OH} = –5 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P8 (1)	I_{OL} = 5 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT5}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRCTRG, TRCCLK, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V		–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V		25	80	140	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 25.14 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition						Standard			Unit
			Oscillation Circuit XIN (2)	Low-Speed on-Chip Oscillator	CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	125 kHz	No division	–		–	4.7	10	mA
			10 MHz	125 kHz	No division	–		–	2.3	6	mA
			20 MHz	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	2.9	–	mA
			20 MHz	125 kHz	Divide-by-8	–		–	1.8	–	mA
			10 MHz	125 kHz	Divide-by-8	–		–	1.0	–	mA
		Low-speed on-chip oscillator mode	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Wait mode	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
		Stop mode	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	–	1.2	–	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V

Table 25.15 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P8 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P8 (1)	I_{OL} = 2 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT5}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRCTRG, TRCCLK, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V		–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V		85	220	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 25.16 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition						Standard			Unit
			Oscillation Circuit XIN (2)	Low-Speed On-Chip Oscillator	CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	8 MHz	125 kHz	No division	–		–	2.1	–	mA
			8 MHz	125 kHz	Divide-by-8	–		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Wait mode	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
		Stop mode	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	–	1.2	–	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 2.2 V

25.5 AC Characteristics

Table 25.17 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_{H}	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

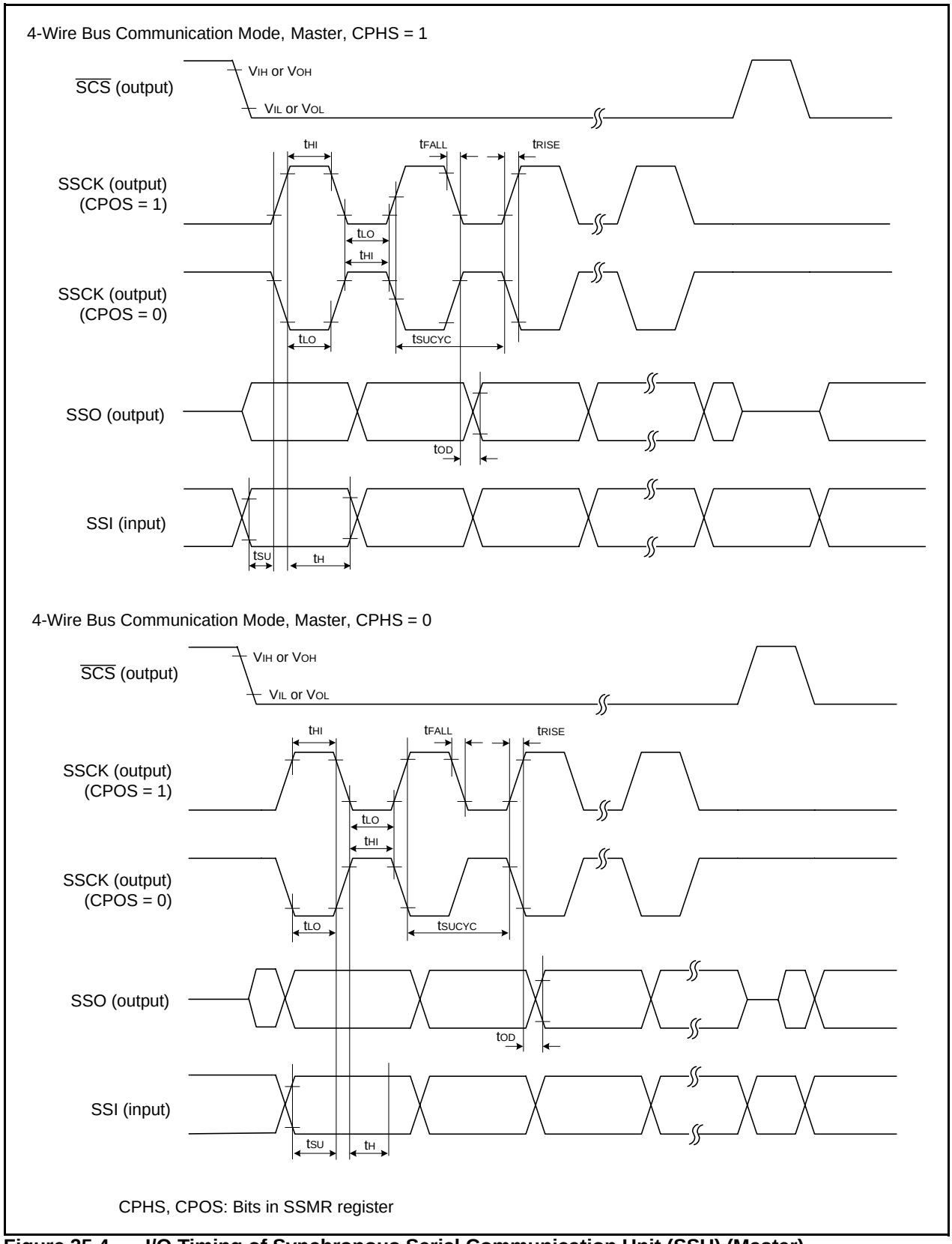


Figure 25.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

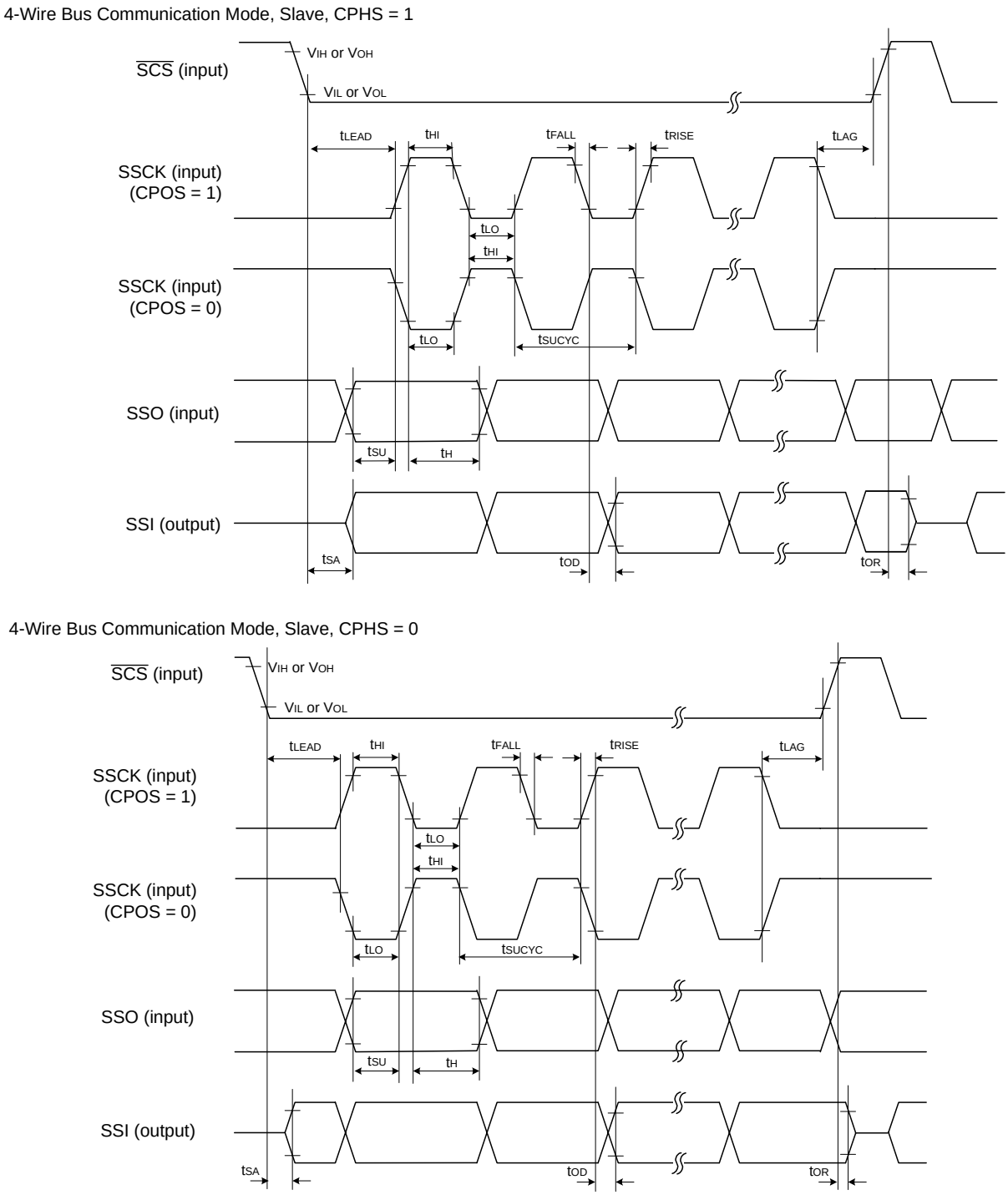


Figure 25.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

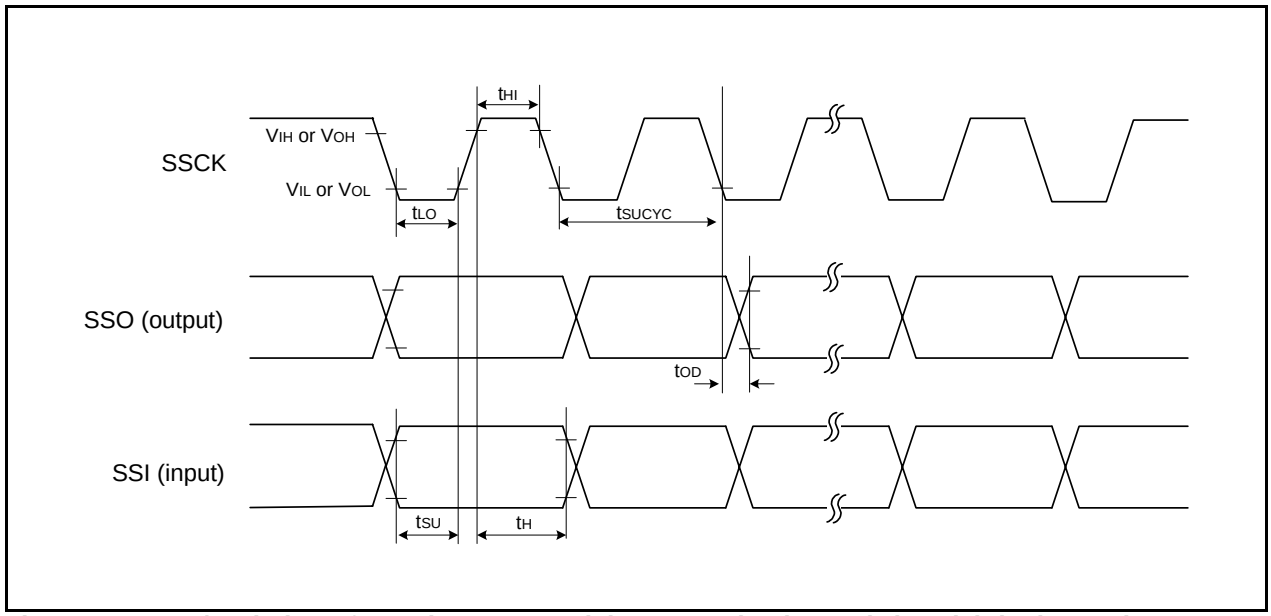
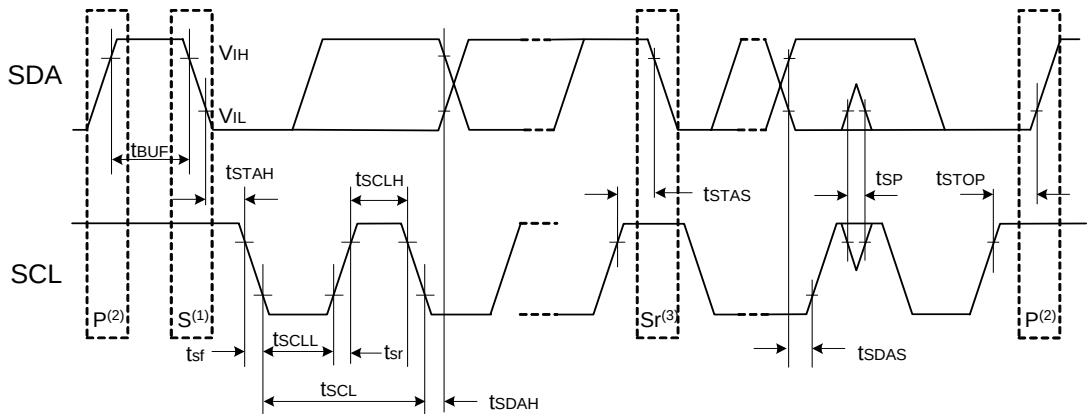


Figure 25.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 25.18 Timing Requirements of I²C bus Interface (1)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600 (1)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300 (1)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 500 (1)	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$ (1)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (1)	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (1)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (1)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (1)	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC}$ + 40 (1)	–	–	ns
t_{SDAH}	Data input hold time		10	–	–	ns

Note:
1. $1t_{CYC}$ = 1/f1(s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 25.7 I/O Timing of I²C bus Interface

Table 25.19 External Clock Input (XIN)
(Vss = 0 V and Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	50	–	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	24	–	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	24	–	24	–	ns

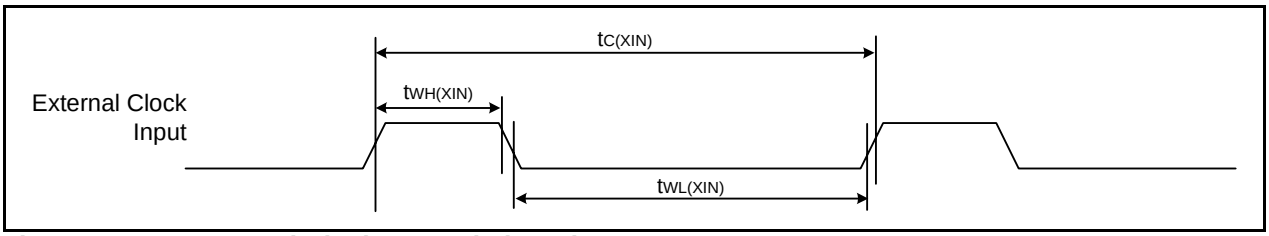


Figure 25.8 External Clock Input Timing Diagram

Table 25.20 Timing Requirements of TRJ0IO
(Vss = 0 V and Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJ0IO input cycle time	500	–	300	–	100	–	ns
$t_{WH(TRJIO)}$	TRJ0IO input “H” width	200	–	120	–	40	–	ns
$t_{WL(TRJIO)}$	TRJ0IO input “L” width	200	–	120	–	40	–	ns

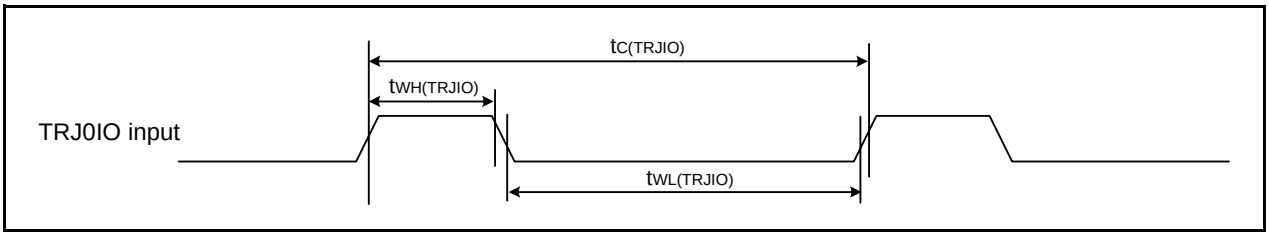


Figure 25.9 Input Timing of TRJ0IO

Table 25.21 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 3, 5) and Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)
(V_{SS} = 0 V and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	380 (1)	–	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	380 (2)	–	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

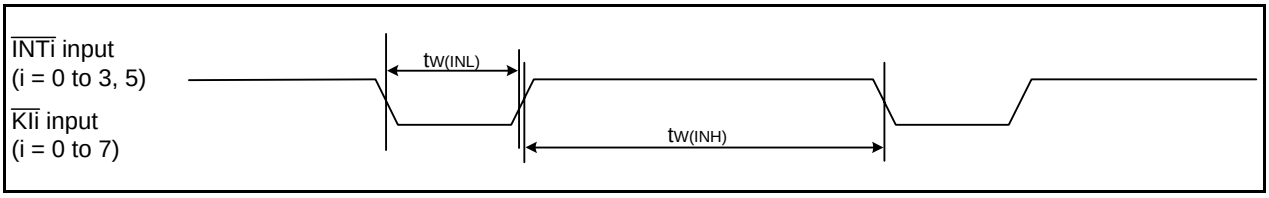


Figure 25.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$

26. Usage Notes

26.1 Notes on Clock Generation Circuit

26.1.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

26.1.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

26.2 Notes on Power Control

26.2.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) first and then set the CM10 bit in the CM1 register to 1. An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to registers CM0 and CM1 enabled
        FSET    I           ; Interrupt enabled
        BSET    0,CM1       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

26.2.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode. Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).
To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled). An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        FSET    I           ; Interrupt enabled
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register disabled
        FSET    I           ; Interrupt enabled
```

26.2.3 Reducing Internal Power Using VCA20 Bit

Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode.

To enter wait mode by setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode), follow the procedure shown in Figure 10.5 to set the procedure for reducing internal power consumption using the VCA20 bit.

To enter wait mode by executing WAIT instruction, follow the procedure shown in Figure 10.6 to set the procedure for reducing internal power consumption using the VCA20 bit.

26.3 Notes on Interrupts

26.3.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0 (no interrupt requested).
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

26.3.2 SP Setting

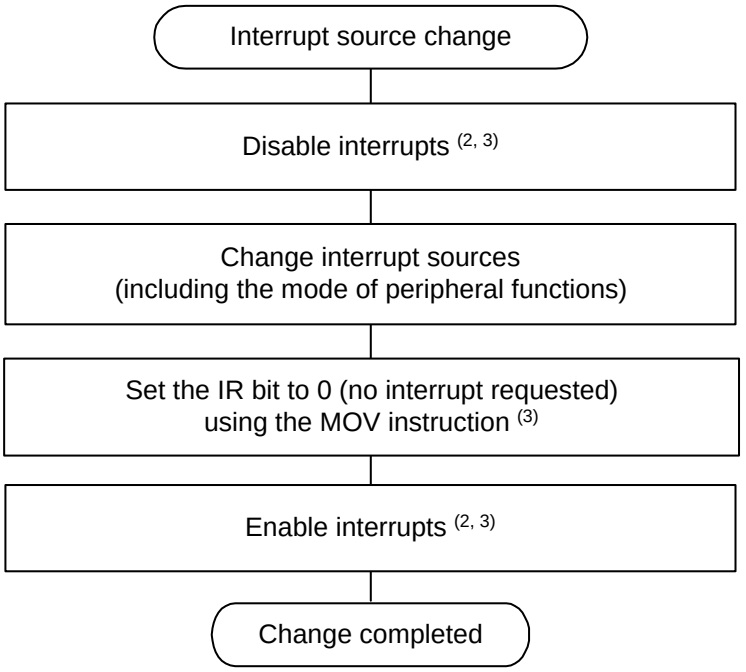
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

26.3.3 External Interrupt, Key Input Interrupt

Either the low-level width or high-level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$, and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to **Table 25.21 Timing Requirements of External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3, 5) and Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 7)**.

26.3.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 26.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: Bit in the interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt requested). Refer to **12.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 26.1 Procedure Example for Changing Interrupt Sources

26.3.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:
AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.
Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    POPC    FLG             ; Enable interrupts
```

26.4 Notes on ID Code Areas

26.4.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

26.5 Notes on Option Function Select Area

26.5.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h) ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

26.6 Notes on Timer RB

- Timer RBi stops counting after a reset. Set the values in the timer RBi and timer RBi prescalers before the count starts.
- Even if the prescaler and timer RBi is read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBiCR register to 0 (count stops) or setting the TOSSP bit in the TRBiOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for one or two cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit. Timer RB starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 (during count operation) for one or two cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RBi counting is stopped when the TCSTF bit is set to 0 (count stops).
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RBi:
     TRBiCR, TRBiOCR, TRBiIOC, TRBiMR, TRBiPRE, TRBiSC, and TRBiPR

- When the TSTOP bit in the TRBiCR register is set to 1 during timer operation, timer RBi stops immediately.
- When 1 is written to the TOSST or TOSSP bit in the TRBiOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. When 1 is written to the TOSSP bit during the period between when 1 is written to the TOSST bit and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, when 1 is written to the TOSST bit during the period between when 1 is written to the TOSSP bit and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RJ0 as the count source for timer RB0, set timer RJ0 in timer mode, pulse output mode, or event counter mode. Underflow of timer RJ0 cannot be selected as the count source for timer RB1.

26.6.1 Timer Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR register (i = 0 or 1) is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

26.6.2 Programmable Waveform Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

26.6.3 Programmable One-Shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

26.6.4 Programmable Wait One-shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

26.7 Notes on Timer RC

26.7.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRC register cleared by compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.W   TRC,DATA       ;Read
```

26.7.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA     ;Read
```

26.7.3 Count Source Switching

- Stop the count before switching the count source.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

26.7.4 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 18.1 Timer RC Operating Clocks**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 18.5 Block Diagram of Digital Filter**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).
- When the input capture function is used, if an edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in the TRCIOR0 or TRCIOR1 register is input to the TRCIOj pin, the IMFj bit in the TRCSR register is set to 1 even when the TSTART bit in the TRCMR register is 0 (count stops).

26.7.5 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

26.8 Notes on Timer RJ

- Timer RJ0 stops counting after a reset. Set the values in the timer before the count starts.
- Read the timer in 16-bit units.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRJ0CR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRJ0CR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RJ0 underflow signal generated after the count starts.
- When using pulse period measurement mode, leave two or more periods of the timer RJ0 register immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit remains 0 (count stops) for zero or one cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RJ0 (1) other than the TCSTF bit.
  Timer RJ0 starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for zero or one cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RJ0 counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RJ0 (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RJ0: TRJ0CR, TRJ0IOC, TRJ0MR, and TRJ0

- When the TRJ0 register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- Do not set 0000h to the TRJ0 register in pulse width measurement mode and pulse period measurement mode.

26.9 Notes on Synchronous Serial Communication Unit (SSU)

To use the synchronous serial communication unit, set the IICSEL bit in the SSUIICSR register to 0 (SSU function selected).

26.10 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

26.10.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

26.10.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

26.10.2 The ICE Bit in the ICCR1 Register and the IICRST Bit in the ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

26.10.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

26.10.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

26.10.2.3 Additional Descriptions Regarding the IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

26.11 Notes on Flash Memory

26.11.1 CPU Rewrite Mode

26.11.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

26.11.1.2 Interrupts

Tables 26.1 and 26.2 list CPU Rewrite Mode Interrupts (1) and (2), respectively.

Table 26.1 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.

FMR21, FMR22: Bits in FMR2 register

Table 26.2 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step (Note 1)
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Do not use during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

26.11.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts between writing 1 and writing 0.
- The FMR14 or FMR15 bit in the FMR1 register

26.11.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

26.11.1.5 Programming

Do not write additions to the already programmed address.

26.11.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
When the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

26.11.1.7 Programming and Erasure Voltage for Flash Memory

To program and erasure program ROM, use VCC = 1.8 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 1.8 V.

26.11.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

26.11.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
. The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **10.6 Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

26.12 Notes on Noise

26.12.1 Inserting Bypass Capacitor between Pins VCC and VSS as Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) using the shortest and thickest wire possible.

26.12.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

26.13 Note on Supply Voltage Fluctuation

After reset is deasserted, the supply voltage applied to the VCC pin must meet either or both the allowable ripple voltage Vr (vcc) or ripple voltage falling gradient dVr (vcc)/dt shown in Figure 26.2.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr (vcc)	Allowable ripple voltage			0.1 VCC	V
dVr (vcc)/dt	Ripple voltage falling gradient			10	V/ms

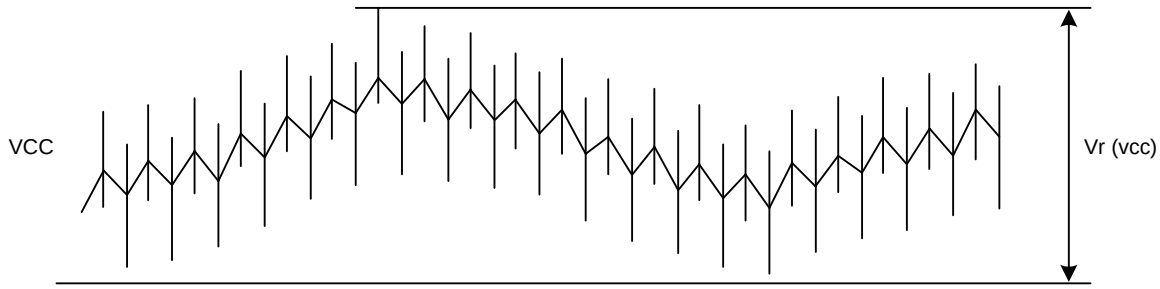


Figure 26.2 Definition of Ripple Voltage

27. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/LAPS Group, take note of the following:

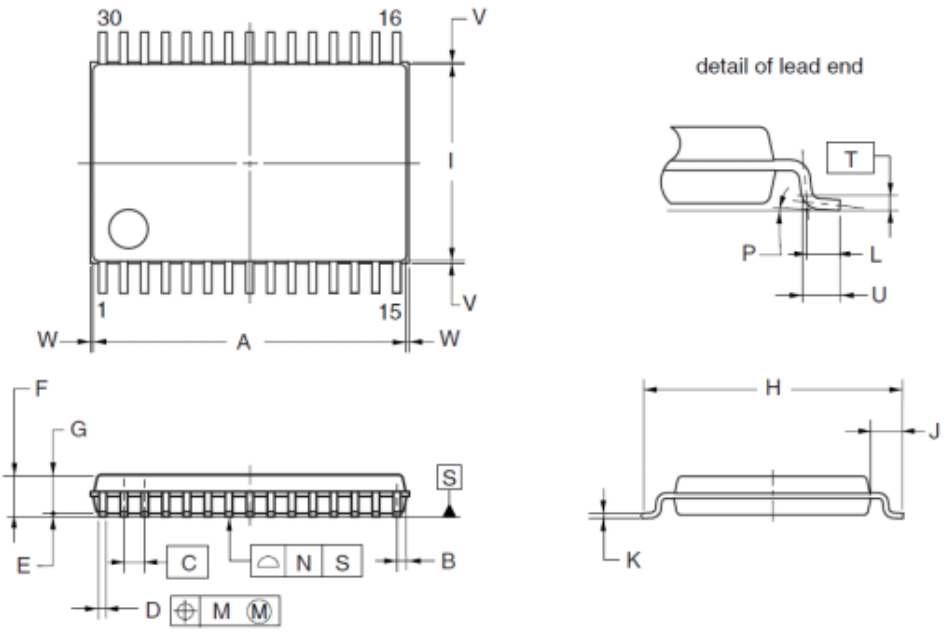
(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 1.8 to 5.5 V. Set the supply voltage to 1.8 V or above for rewriting the flash memory.

Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

● SSOP-30 package dimension



(UNIT:mm)

ITEM	DIMENSIONS
A	9.70±0.10
B	0.30
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

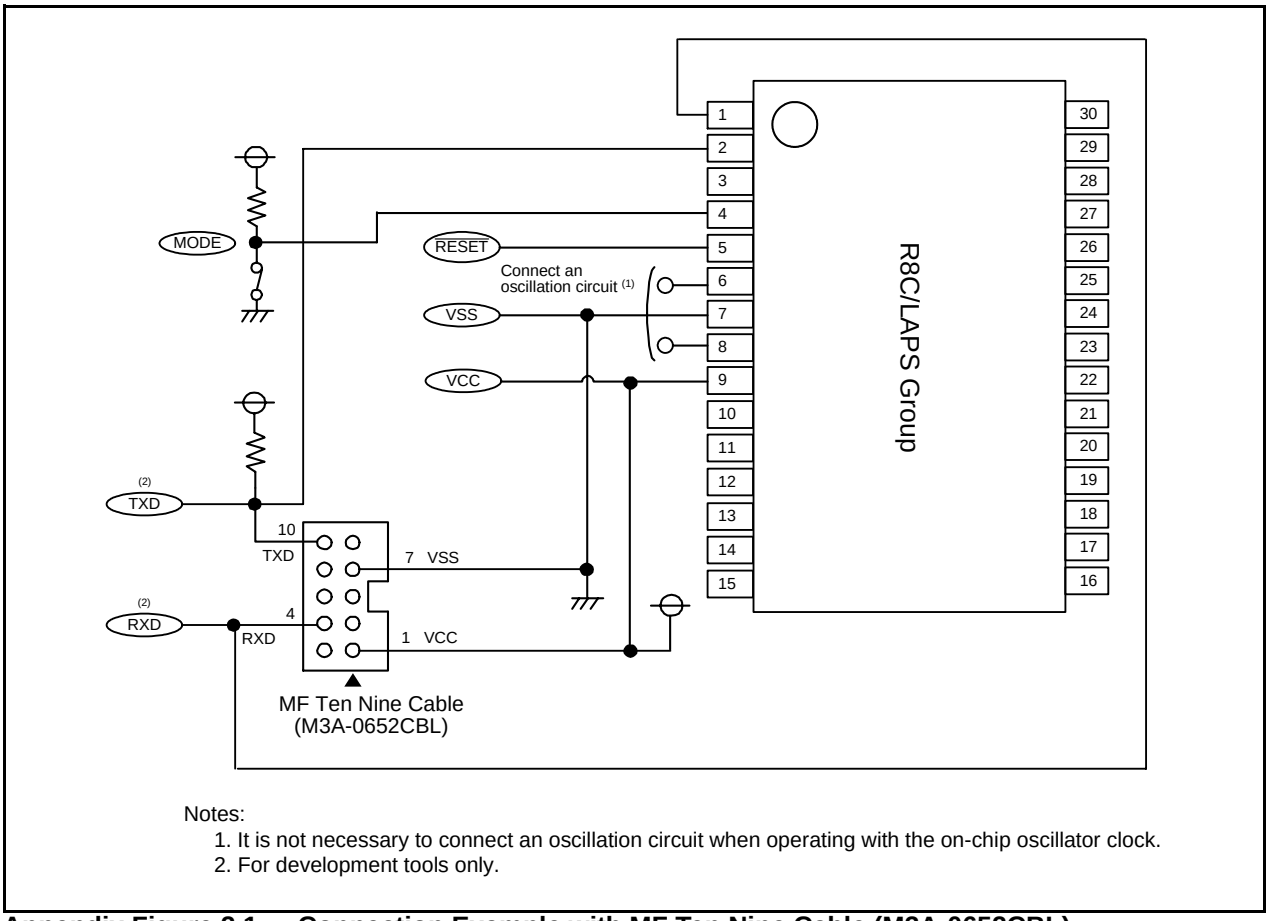
P30MC-65-CAB

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

Appendix 2. Connection Examples with Serial Programmer

Appendix Figure 2.1 shows Connection Example with MF Ten Nine Cable (M3A-0652CBL).

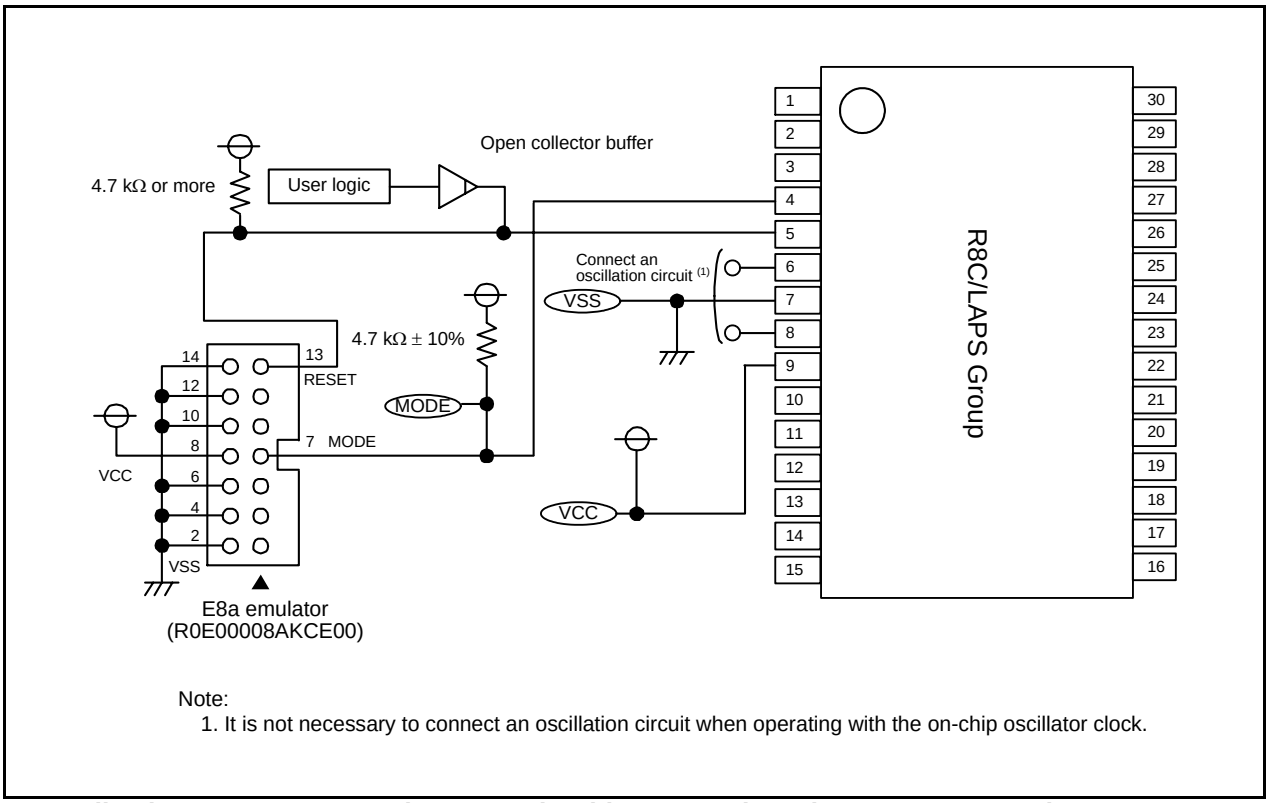


Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. For development tools only.

Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)

Appendix 3. Connection Examples with E8a Emulator

Appendix Figure 3.1 shows Connection Example with E8a Emulator (R0E00008AKCE00).



Note:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.

Appendix Figure 3.1 Connection Example with E8a Emulator (R0E00008AKCE00)

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REVISION HISTORY	R8C/LAPS Group User's Manual: Hardware

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		Page	Summary
0.10	Dec 28, 2010	—	First Edition issued
1.00	Sep 22, 2011	All pages	"Preliminary" and "Under development" deleted
		1	1.1.1 revised
		39	6.2.4 Note 1, Note 2, Note 4, Note 5 revised
		42	6.2.7 Note 1 revised
		64	7.5.7 Note 1 added
		83	9.2.2 Note 2, Note 6 revised
		84	9.2.3 Note 3 revised
		87	9.5.4 revised
		90	Figure 9.4 Title revised
		91	9.7.1 revised
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		95	10.2.3 Note 3 revised
		97	10.2.5 Note 1, Note 2, Note 4, Note 5 revised
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		99	10.4.2 revised, 10.4.3 added
		101	10.4.6 Title added
		102	10.4.7 Title added, (2) revised
		104	10.5.3 (2) revised
		106	10.6.8 revised, Figure 10.5 added
		107	Figure 10.6 Titile revised
		110	10.7.2 revised
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		182	17.7.3 revised
		205	18.4.1 revised
		206	18.4.2 revised
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		212	18.5.3 revised
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