

## Section 14 Electrical Specifications

### 14.1 Absolute Maximum Ratings

Table 14-1 lists the absolute maximum ratings.

**Table 14-1. Absolute Maximum Ratings (Preliminary)**

Item	Symbol	Rating	Unit	
Supply voltage	$V_{CC}$	-0.3 to +7.0	V	
Programming voltage	$V_{PP}$	-0.3 to +13.5	V	
Input voltage	Ports 1-6	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	V
	Port 7	$V_{IN}$	-0.3 to $AV_{CC} + 0.3$	V
Analog supply voltage	$AV_{CC}$	-0.3 to +7.0	V	
Analog input voltage	$V_{AN}$	-0.3 to $AV_{CC} + 0.3$	V	
Operating temperature	$T_{opr}$	Regular specifications:	-20 to +75	°C
		Wide-range specifications:	-40 to +85	°C
Storage temperature	$T_{stg}$	-55 to +125	°C	

Note: Exceeding the absolute maximum ratings shown in table 14-1 can permanently destroy the chip.

### 14.2 Electrical Characteristics

#### 14.2.1 DC Characteristics

Table 14-2 lists the DC characteristics of the 5V versions of the H8/329 Series. Table 14-3 lists the DC characteristics of the 3V versions. Table 14-4 gives the allowable current output values of the 5V versions. Table 14-5 gives the allowable current output values of the 3V versions.

**Table 14-2. DC Characteristics (5V Versions) (Preliminary)**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ \*,  $V_{SS} = AV_{SS} = 0V$ ,  
 $T_A = -20$  to  $75^\circ C$  (regular specifications),  $T_A = -40$  to  $85^\circ C$  (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Measurement conditions	
Schmitt trigger input voltage (1)	P67-P62, P60,	$V_{T-}$	1.0	—	—	V	
	P47, P44-P40	$V_{T+}$	—	—	$V_{CC} \times 0.7$	V	
		$V_{T+} - V_{T-}$	0.4	—	—	V	
Input High voltage (2)	$\overline{RES}$ , $\overline{STBY}$ , $NMI$ , MD1, MD0 EXTAL	$V_{IH}$	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	P77-P70		2.0	—	$AV_{CC} + 0.3$	V	
Input High voltage	Input pins other than (1) and (2) above	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	
Input Low voltage (3)	$\overline{RES}$ , $\overline{STBY}$ , MD1, MD0	$V_{IL}$	-0.3	—	0.5	V	
Input Low voltage	Input pins other than (1) and (3) above	$V_{IL}$	-0.3	—	0.8	V	
Output High voltage	All output pins	$V_{OH}$	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu A$
			3.5	—	—	V	$I_{OH} = -1.0$ mA
Output Low voltage	All output pins	$V_{OL}$	—	—	0.4	V	$I_{OL} = 1.6$ mA
	Ports 1 and 2		—	—	1.0	V	$I_{OL} = 10.0$ mA
Input leakage current	$\overline{RES}$	$ I_{in} $	—	—	10.0	$\mu A$	$V_{IN} = 0.5V$ to $V_{CC} - 0.5V$
	$\overline{STBY}$ , $NMI$ , MD1, MD0		—	—	1.0	$\mu A$	
	P77-P70		—	—	1.0	$\mu A$	$V_{IN} = 0.5V$ to $AV_{CC} - 0.5V$
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6	$ I_{TSI} $	—	—	1.0	$\mu A$	$V_{IN} = 0.5V$ to $V_{CC} - 0.5V$
Input pull-up MOS current	Ports 1, 2, 3	$-I_p$	30	—	250	$\mu A$	$V_{IN} = 0V$

Note: \* Connect  $AV_{CC}$  to the power supply (+5V) even when the A/D converter is not used.

**Table 14-2. DC Characteristics (5V Versions) (Preliminary) (cont.)**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ \*1,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -20$  to  $75^\circ C$  (regular specifications),  $T_A = -40$  to  $85^\circ C$  (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Measurement conditions
Input capacitance	RES	$C_{IN}$	—	—	60	pF	$V_{IN} = 0V$
	NMI		—	—	30	pF	$f = 1\text{ MHz}$
	All input pins except RES and NMI		—	—	15	pF	$T_A = 25^\circ C$
Current dissipation*2	Normal operation	$I_{CC}$	—	12	25	mA	$f = 6\text{ MHz}$
			—	16	30	mA	$f = 8\text{ MHz}$
			—	20	40	mA	$f = 10\text{ MHz}$
	Sleep mode		—	8	15	mA	$f = 6\text{ MHz}$
			—	10	20	mA	$f = 8\text{ MHz}$
			—	12	25	mA	$f = 10\text{ MHz}$
Standby modes*3	—	0.01	5.0	$\mu A$			
Analog supply current	During A/D conversion	$I_{CC}$	—	0.6	1.5	mA	
	Waiting		—	0.01	5.0	$\mu A$	
RAM standby voltage		$V_{RAM}$	2.0	—	—	V	

Notes: \*1 Connect  $AV_{CC}$  to the power supply (+5V) even when the A/D converter is not used.

\*2 Current dissipation values assume that  $V_{IH\text{ min}} = V_{CC} - 0.5V$ ,  $V_{IL\text{ max}} = 0.5V$ , all output pins are in the no-load state, and all input pull-up transistors are off.

\*3 For these values it is assumed that  $V_{RAM} \leq V_{CC} < 4.5V$  and  $V_{IH\text{ min}} = V_{CC} \times 0.9$ ,  $V_{IL\text{ max}} = 0.3V$ .

**Table 14-3. DC Characteristics (3V Versions) (Preliminary)**

Conditions:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%^{*1}$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -20$  to  $75^{\circ}C$

Item		Symbol	Min	Typ	Max	Unit	Measurement conditions
Schmitt trigger input voltage*2 (1)	P67-P62, P60,	$V_{T-}$	$V_{CC} \times 0.15$	—	—	V	
	P47, P44-P40	$V_{T+}$	—	—	$V_{CC} \times 0.7$	V	
		$V_{T+} - V_{T-}$	0.2	—	—	V	
Input High voltage*2 (2)	RES, STBY MD1, MD0 EXTAL, NMI	$V_{IH}$	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	P77-P70		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Input pins other than (1) and (2) above		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input Low voltage*2 (3)	RES, STBY MD1, MD0	$V_{IL}$	-0.3	—	$V_{CC} \times 0.1$	V	
	Input pins other than (1) and (3) above		-0.3	—	$V_{CC} \times 0.15$	V	
Output High voltage	All output pins	$V_{OH}$	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -200 \mu A$
			$V_{CC} - 0.9$	—	—	V	$I_{OH} = -1 \text{ mA}$
Output Low voltage	All output pins	$V_{OL}$	—	—	0.4	V	$I_{OL} = 0.8 \text{ mA}$
	Ports 1 and 2		—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
Input leakage current	RES	$ I_{IN} $	—	—	10.0	$\mu A$	$V_{IN} = 0.5$ to $V_{CC} - 0.5V$
	STBY, NMI, MD1, MD0		—	—	1.0	$\mu A$	$V_{IN} = 0.5$ to $AV_{CC} - 0.5V$
	P77-P70		—	—	1.0	$\mu A$	$V_{IN} = 0.5$ to $AV_{CC} - 0.5V$
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6	$ I_{TSI} $	—	—	1.0	$\mu A$	$V_{IN} = 0.5$ to $V_{CC} - 0.5V$
Input pull-upMOS current	Ports 1, 2, 3	$-I_P$	3	—	120	$\mu A$	$V_{IN} = 0V$

Notes: \*1 Connect  $AV_{CC}$  to the power supply (+3V) even when the A/D converter is not used.

\*2 In the range  $3.3V < V_{CC} < 4.5V$ , for the input levels of  $V_{IH}$  and  $V_{T}$ , apply the higher of the values given for the 5V and 3V versions. For  $V_{IL}$  and  $V_{T-}$ , apply the lower of the values given for the 5V and 3V versions.

**Table 14-3. DC Characteristics (3V Versions) (Preliminary) (cont.)**

Conditions:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ \*1,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -20$  to  $70^\circ C$

Item		Symbol	Min	Typ	Max	Unit	Measurement conditions
Input capacitance	RES	$C_{IN}$	—	—	60	pF	$V_{IN} = 0V$
	NMI		—	—	30	pF	$f = 1\text{ MHz}$
	All input pins except RES and NMI		—	—	15	pF	$T_A = 25^\circ C$
Current dissipation*2	Normal operation	$I_{CC}$	—	4	—	mA	$f = 3\text{ MHz}$
			—	6	12	mA	$f = 5\text{ MHz}$
	Sleep mode		—	3	—	mA	$f = 3\text{ MHz}$
			—	4	8	mA	$f = 5\text{ MHz}$
	Standby modes*3		—	0.01	5.0	$\mu A$	
Analog supply current	During A/D conversion	$A I_{CC}$	—	0.6	1.5	mA	
	Waiting		—	0.01	5.0	$\mu A$	
RAM backup voltage (in standby modes)		$V_{RAM}$	2.0	—	—	V	

Notes: \*1 Connect  $AV_{CC}$  to the power supply (+3V) even when the A/D converter is not used.

\*2 Current dissipation values assume that  $V_{IH\text{ min.}} = V_{CC} - 0.5V$ ,  $V_{IL\text{ max.}} = 0.5V$ , all output pins are in the no-load state, and all input pull-up transistors are off.

\*3 For these values it is assumed that  $V_{RAM} \leq V_{CC} < 2.7V$  and  $V_{IH\text{ min.}} = V_{CC} \times 0.9$ ,  $V_{IL\text{ max.}} = 0.3V$ .

**Table 14-4. Allowable Output Current Sink Values (5V Versions) (Preliminary)**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -20$  to  $75^\circ C$  (regular specifications),  $T_A = -40$  to  $85^\circ C$  (wide-range specifications)

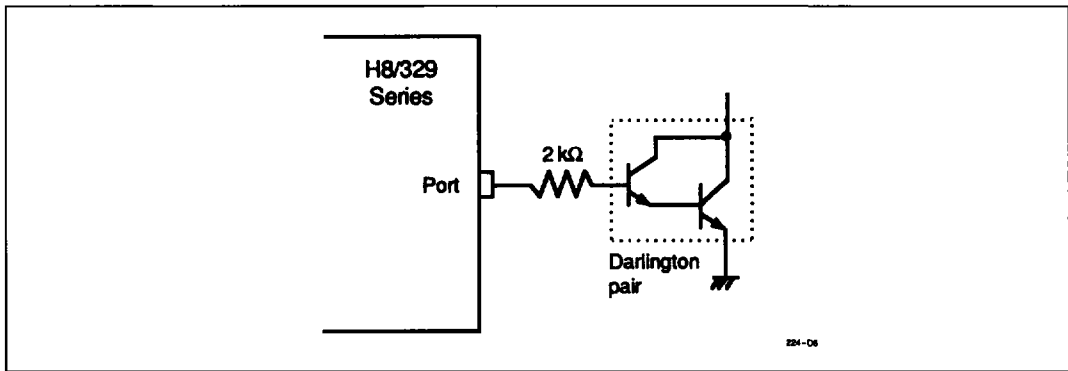
Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	$I_{OL}$	—	—	10	mA
	Other output pins		—	—	2.0	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	$\Sigma I_{OL}$	—	—	80	mA
	Total of all output		—	—	120	mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Allowable output High current sink (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

**Table 14-5. Allowable Output Current Sink Values (3V Versions) (Preliminary)**

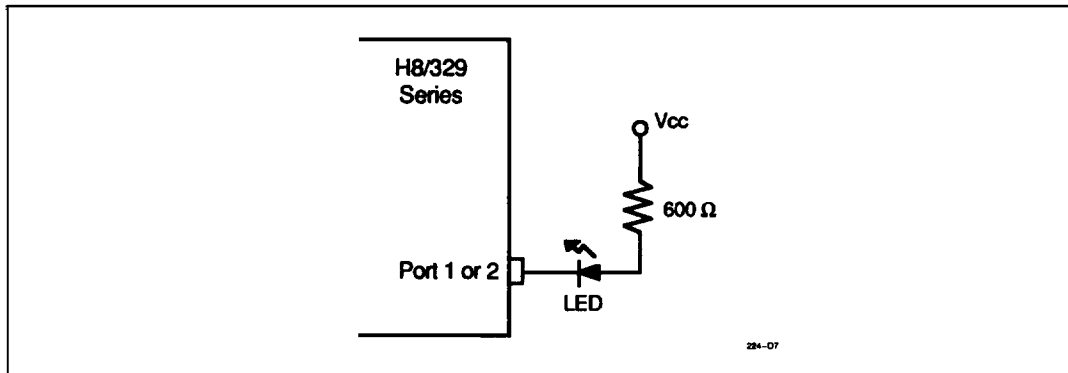
Conditions:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -20$  to  $75^\circ C$

Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	$I_{OL}$	—	—	2	mA
	Other output pins		—	—	1	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	$\Sigma I_{OL}$	—	—	40	mA
	All output pins		—	—	60	mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output High current sink (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in tables 14-4 and 14-5. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 14-1 and 14-2.



**Figure 14-1. Example of Circuit for Driving a Darlington Pair (5V Versions)**



**Figure 14-2. Example of Circuit for Driving an LED (5V Versions)**

### 14.2.2 AC Characteristics

The AC characteristics of the H8/329 Series are listed in three tables. Bus timing parameters are given in table 14-6, control signal timing parameters in table 14-7, and timing parameters of the on-chip supporting modules in table 14-8.

**Table 14-6. Bus Timing (Preliminary)**

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5$  MHz to maximum operating frequency,

$T_A = -20$  to  $75^\circ\text{C}$  (regular specifications),

$T_A = -40$  to  $85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5$  MHz to maximum operating frequency,

$T_A = -20$  to  $75^\circ\text{C}$

Item	Symbol	Condition B		Condition A				Unit	Measurement conditions		
		5 MHz		6 MHz		8 MHz				10 MHz	
		Min	Max	Min	Max	Min	Max			Min	Max
Clock cycle time	$t_{cyc}$	200	2000	166.7	2000	125	2000	100	2000	ns	Fig. 14-4
Clock pulse width Low	$t_{CL}$	70	—	65	—	45	—	35	—	ns	Fig. 14-4
Clock pulse width High	$t_{CH}$	70	—	65	—	45	—	35	—	ns	Fig. 14-4
Clock rise time	$t_{Cr}$	—	25	—	15	—	15	—	15	ns	Fig. 14-4
Clock fall time	$t_{Cf}$	—	25	—	15	—	15	—	15	ns	Fig. 14-4
Address delay time	$t_{AD}$	—	90	—	70	—	60	—	50	ns	Fig. 14-4
Address hold time	$t_{AH}$	30	—	30	—	25	—	20	—	ns	Fig. 14-4
Address strobe delay time	$t_{ASD}$	—	80	—	70	—	60	—	40	ns	Fig. 14-4
Write strobe delay time	$t_{WSD}$	—	80	—	70	—	60	—	50	ns	Fig. 14-4
Strobe delay time	$t_{SD}$	—	90	—	70	—	60	—	50	ns	Fig. 14-4
Write strobe pulse width*	$t_{WSW}$	200	—	200	—	150	—	120	—	ns	Fig. 14-4
Address setup time 1*	$t_{AS1}$	25	—	25	—	20	—	15	—	ns	Fig. 14-4
Address setup time 2*	$t_{AS2}$	105	—	105	—	80	—	65	—	ns	Fig. 14-4
Read data setup time	$t_{RDS}$	90	—	70	—	50	—	35	—	ns	Fig. 14-4
Read data hold time	$t_{RDH}$	0	—	0	—	0	—	0	—	ns	Fig. 14-4
Read data access time*	$t_{ACC}$	—	300	—	270	—	210	—	170	ns	Fig. 14-4
Write data delay time	$t_{WDD}$	—	125	—	85	—	75	—	75	ns	Fig. 14-4
Write data setup time	$t_{WDS}$	10	—	20	—	10	—	5	—	ns	Fig. 14-4
Write data hold time	$t_{WDH}$	30	—	30	—	25	—	20	—	ns	Fig. 14-4
Wait setup time	$t_{WTS}$	60	—	40	—	40	—	40	—	ns	Fig. 14-5
Wait hold time	$t_{WTH}$	20	—	10	—	10	—	10	—	ns	Fig. 14-5

Note: \* Values at maximum operating frequency



**Table 14-7. Control Signal Timing (Preliminary)**

Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5$  MHz to maximum operating frequency,

$T_A = -20$  to  $75^\circ\text{C}$  (regular specifications),

$T_A = -40$  to  $85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5$  MHz to maximum operating frequency,

$T_A = -20$  to  $75^\circ\text{C}$

Item	Symbol	Condition B		Condition A						Unit	Measurement conditions
		5 MHz		6 MHz		8 MHz		10 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
RES setup time	$t_{RESS}$	300	—	200	—	200	—	200	—	ns	Fig. 14-6
RES pulse width	$t_{RESW}$	10	—	10	—	10	—	10	—	$t_{CYC}$	Fig. 14-6
NMI setup time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	$t_{NMIS}$	300	—	150	—	150	—	150	—	ns	Fig. 14-7
NMI hold time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	$t_{NMIH}$	10	—	10	—	10	—	10	—	ns	Fig. 14-7
Interrupt pulse width for recovery from soft- ware standby mode (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	$t_{NMIW}$	300	—	200	—	200	—	200	—	ns	Fig. 14-7
Crystal oscillator settling time (reset)	$t_{osc1}$	20	—	20	—	20	—	20	—	ms	Fig. 14-8
Crystal oscillator settling time (software standby)	$t_{osc2}$	10	—	10	—	10	—	10	—	ms	Fig. 14-9

**Table 14-8. Timing Conditions of On-Chip Supporting Modules (Preliminary)**Condition A:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5$  MHz to maximum operating frequency, $T_A = -20$  to  $75^\circ\text{C}$  (regular specifications), $T_A = -40$  to  $85^\circ\text{C}$  (wide-range specifications)Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $\phi = 0.5$  MHz to maximum operating frequency,

Item	Symbol	Condition B		Condition A				Unit	Measurement conditions				
		5 MHz	6 MHz	8 MHz	10 MHz	Min	Max						
FRT	Timer output delay time	$t_{FOD}$	—	150	—	100	—	100	—	100	ns	Fig. 14-10	
	Timer input setup time	$t_{FTIS}$	80	—	50	—	50	—	50	—	ns	Fig. 14-10	
	Timer clock input setup time	$t_{FTCS}$	80	—	50	—	50	—	50	—	ns	Fig. 4-11	
	Timer clock pulse width	$t_{FTWCH}$ $t_{FTCWL}$	1.5	—	1.5	—	1.5	—	1.5	—	$t_{CYC}$	Fig. 4-11	
TMR	Timer output delay time	$t_{TMOD}$	—	150	—	100	—	100	—	100	ns	Fig. 14-12	
	Timer reset input setup time	$t_{TMRS}$	80	—	50	—	50	—	50	—	ns	Fig. 14-14	
	Timer clock input setup time	$t_{TMCS}$	80	—	50	—	50	—	50	—	ns	Fig. 14-13	
	Timer clock pulse width (single edge)	$t_{TMCWH}$	1.5	—	1.5	—	1.5	—	1.5	—	$t_{CYC}$	Fig. 14-13	
	Timer clock pulse width (both edges)	$t_{TMCWL}$	2.5	—	2.5	—	2.5	—	2.5	—	$t_{CYC}$	Fig. 14-13	
SCI	Input clock cycle	(Async)	$t_{SCYC}$	2	—	2	—	2	—	2	—	$t_{CYC}$	Fig. 14-15
		(Sync)	$t_{SCYC}$	6	—	6	—	6	—	6	—	$t_{CYC}$	Fig. 14-15
	Transmit data delay time (Sync)	$t_{TXD}$	—	200	—	100	—	100	—	100	ns	Fig. 14-15	
	Receive data setup time (Sync)	$t_{RXS}$	150	—	100	—	100	—	100	—	ns	Fig. 14-15	
	Receive data hold time (Sync)	$t_{RXH}$	150	—	100	—	100	—	100	—	ns	Fig. 14-15	
	Input clock pulse width	$t_{SCKW}$	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	$t_{SCYC}$	Fig. 14-16	
Ports	Output data delay time	$t_{PWD}$	—	150	—	100	—	100	—	100	ns	Fig. 14-17	
	Input data setup time	$t_{PRS}$	80	—	50	—	50	—	50	—	ns	Fig. 14-17	
	Input data hold time	$t_{PRH}$	80	—	50	—	50	—	50	—	ns	Fig. 14-17	

• Measurement Conditions for AC Characteristics

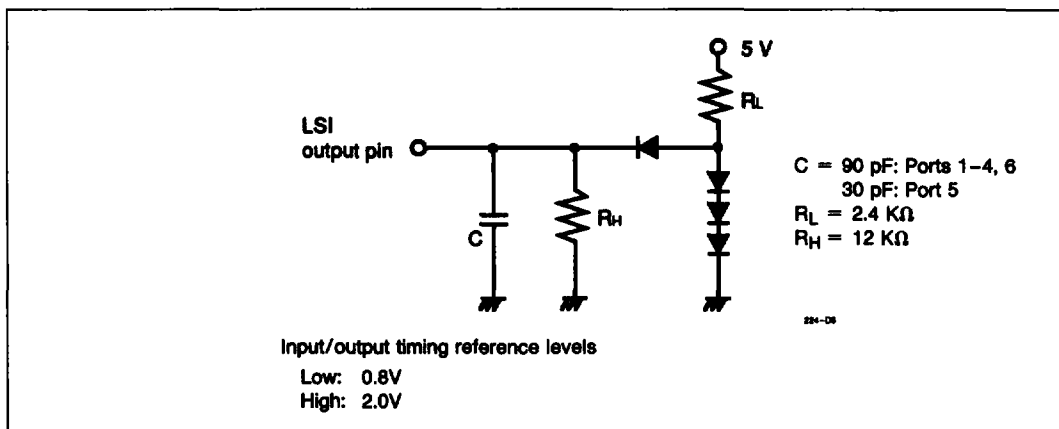


Figure 14-3. Output Load Circuit

14.2.3 A/D Converter Characteristics

Table 14-9 lists the characteristics of the on-chip A/D converter.

Table 14-9. A/D Converter Characteristics (Preliminary)

Condition A:  $V_{CC} = AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $\phi = 0.5 \text{ MHz}$  to maximum operating frequency,  $T_A = -20$  to  $75^\circ\text{C}$  (regular specifications),

$T_A = -40$  to  $85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 3.0V \pm 10\%$ ,  $AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $\phi = 0.5 \text{ MHz}$  to maximum operating frequency,  $T_A = -20$  to  $75^\circ\text{C}$

Item	Condition B			Condition A									Measurement Unit
	5 MHz			6 MHz			8 MHz			10 MHz			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)*	—	—	24.4	—	—	20.4	—	—	15.25	—	—	12.2	$\mu\text{s}$
Analog input capacitance	—	—	20	—	—	20	—	—	20	—	—	20	pF
Allowable signal source impedance	—	—	10	—	—	10	—	—	10	—	—	10	k $\Omega$
Nonlinearity error	—	—	$\pm 1$	—	—	$\pm 1$	—	—	$\pm 1$	—	—	$\pm 1$	LSB
Offset error	—	—	$\pm 1$	—	—	$\pm 1$	—	—	11	—	—	$\pm 1$	LSB
Full-scale error	—	—	$\pm 1$	—	—	$\pm 1$	—	—	$\pm 1$	—	—	$\pm 1$	LSB
Quantizing error	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	LSB
Absolute accuracy	—	—	$\pm 1.5$	—	—	$\pm 1.5$	—	—	$\pm 1.5$	—	—	$\pm 1.5$	LSB

Note: \* At maximum operating frequency

## 14.3 MCU Operational Timing

This section provides the following timing charts:

- |   |                        |
|---|------------------------|
| 14.3.1 Bus Timing                       | Figures 14-4 to 14-5   |
| 14.3.2 Control Signal Timing            | Figures 14-6 to 14-9   |
| 14.3.3 16-Bit Free-Running Timer Timing | Figures 14-10 to 14-11 |
| 14.3.4 8-Bit Timer Timing               | Figures 14-12 to 14-14 |
| 14.3.5 SCI Timing                       | Figures 14-15 to 14-16 |
| 14.3.6 I/O Port Timing                  | Figure 14-17           |

### 14.3.1 Bus Timing

#### (1) Basic Bus Cycle (without Wait States) in Expanded Modes

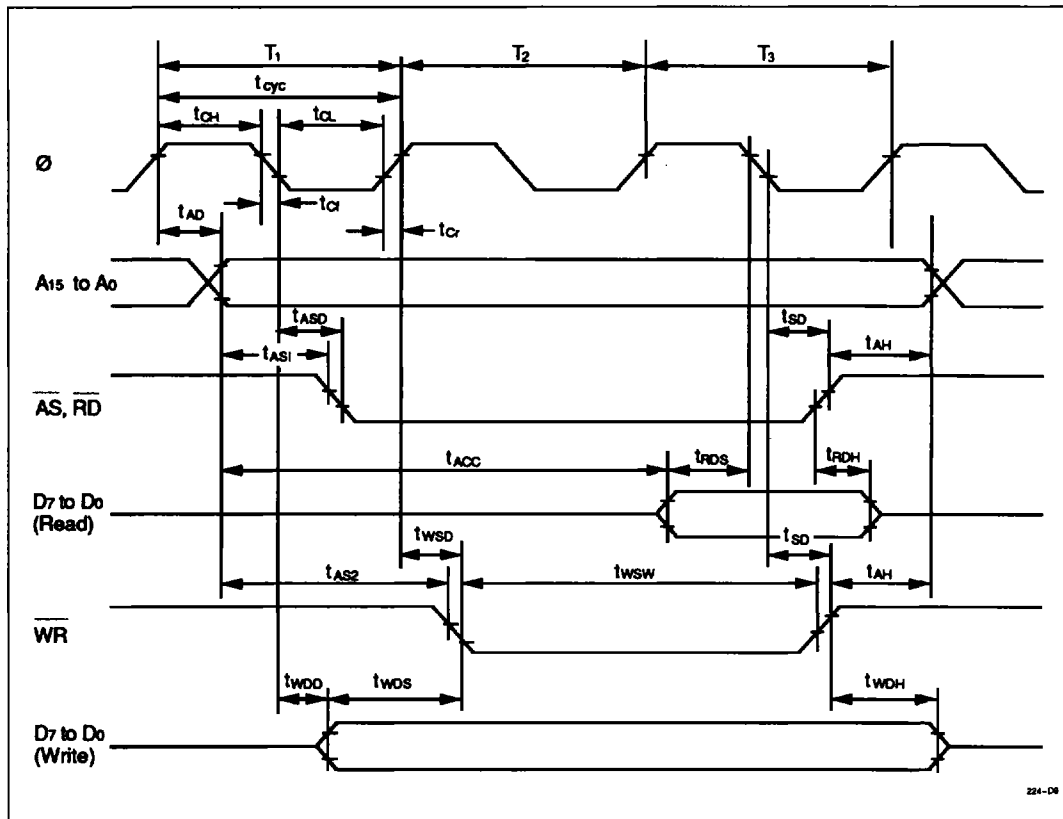


Figure 14-4. Basic Bus Cycle (without Wait States) in Expanded Modes

## (2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

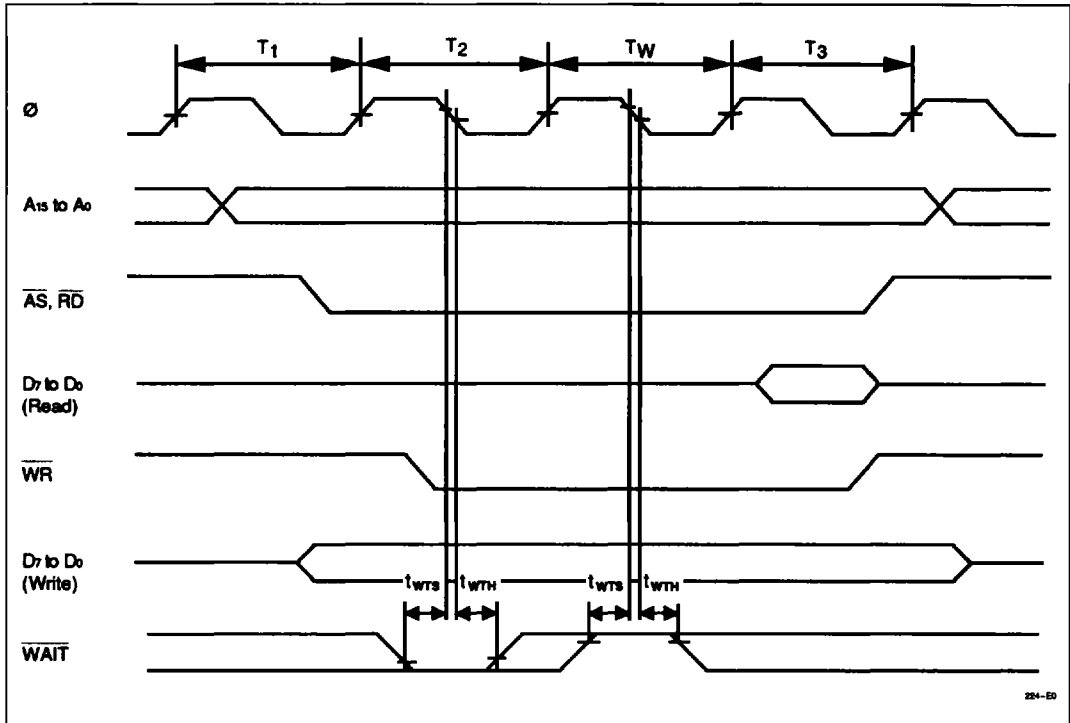


Figure 14-5. Basic Bus Cycle (with 1 Wait State) in Expanded Modes (Modes 1 and 2)

### 14.3.2 Control Signal Timing

#### (1) Reset Input Timing

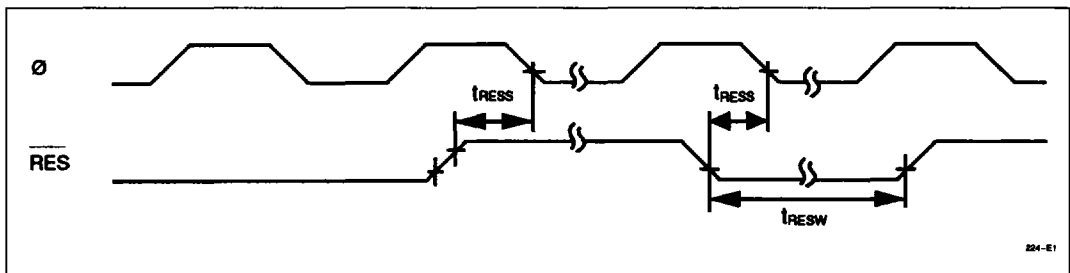


Figure 14-6. Reset Input Timing

## (2) Interrupt Input Timing

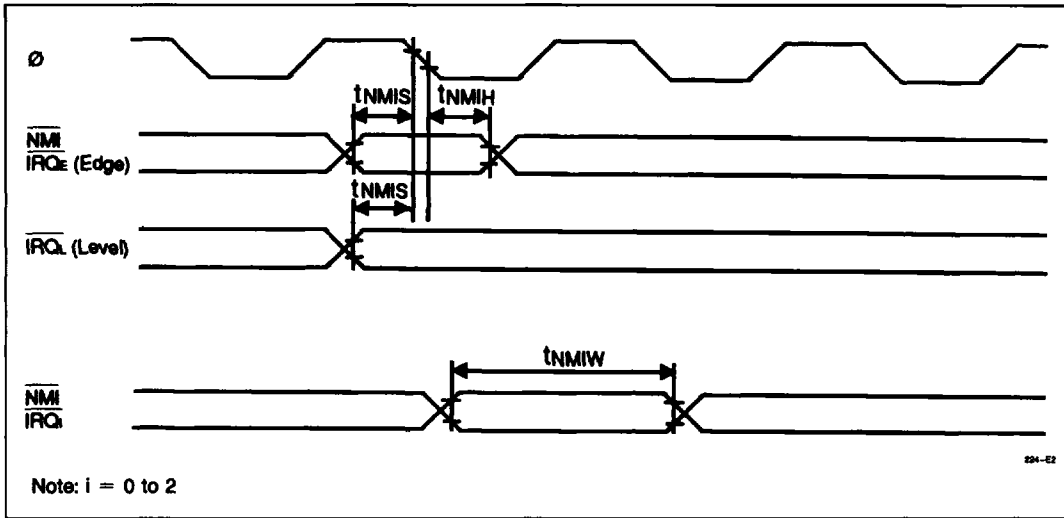


Figure 14-7. Interrupt Input Timing

### (3) Clock Settling Timing

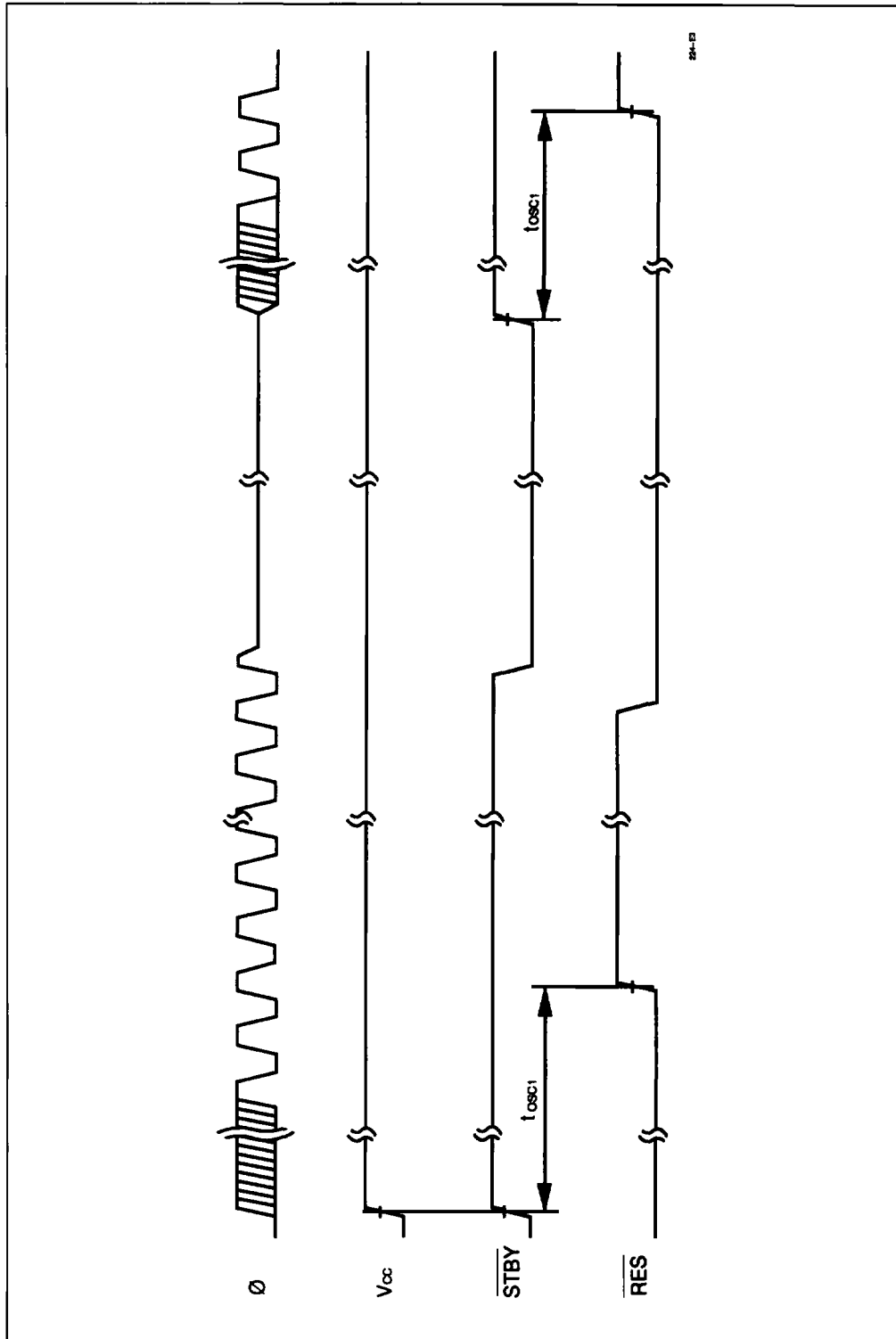
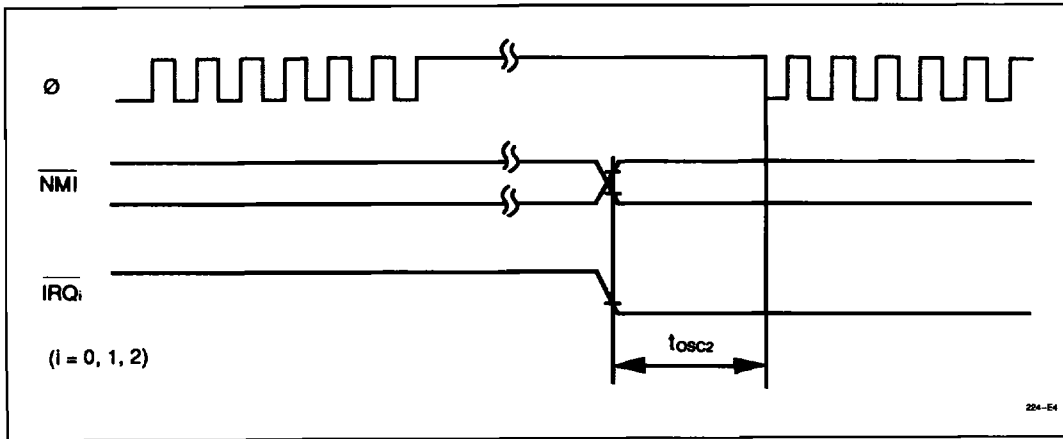


Figure 14-8. Clock Settling Timing

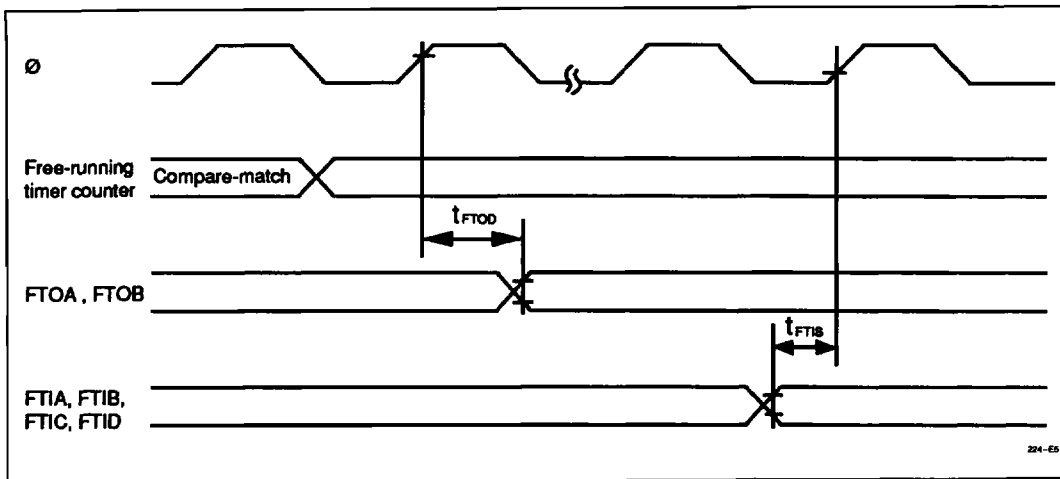
**(4) Clock Settling Timing for Recovery from Software Standby Mode**



**Figure 14-9. Clock Settling Timing for Recovery from Software Standby Mode**

**14.3.3 16-Bit Free-Running Timer Timing**

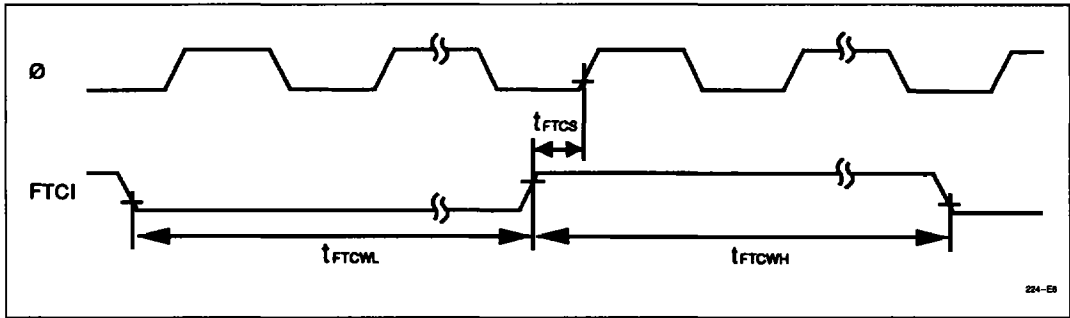
**(1) Free-Running Timer Input/Output Timing**



**Figure 14-10. Free-Running Timer Input/Output Timing**



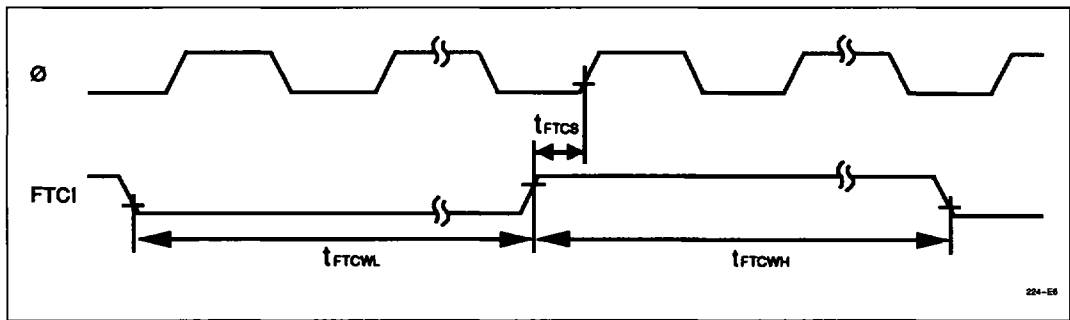
**(2) External Clock Input Timing for Free-Running Timer**



**Figure 14-11. External Clock Input Timing for Free-Running Timer**

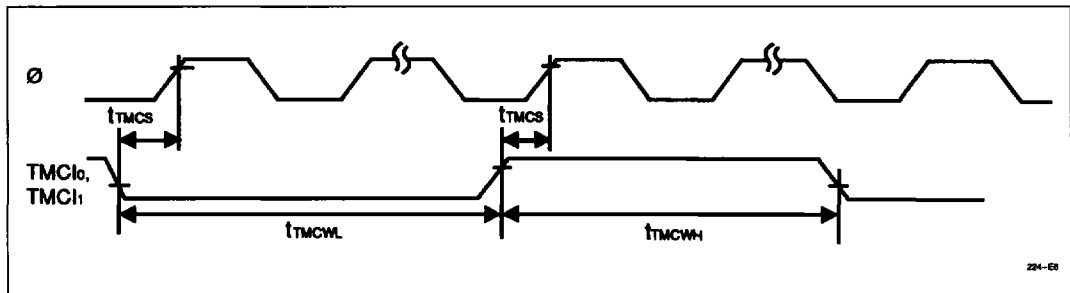
**14.3.4 8-Bit Timer Timing**

**(1) 8-Bit Timer Output Timing**



**Figure 14-12. 8-Bit Timer Output Timing**

**(2) 8-Bit Timer Clock Input Timing**



**Figure 14-13. 8-Bit Timer Clock Input Timing**

### (3) 8-Bit Timer Reset Input Timing

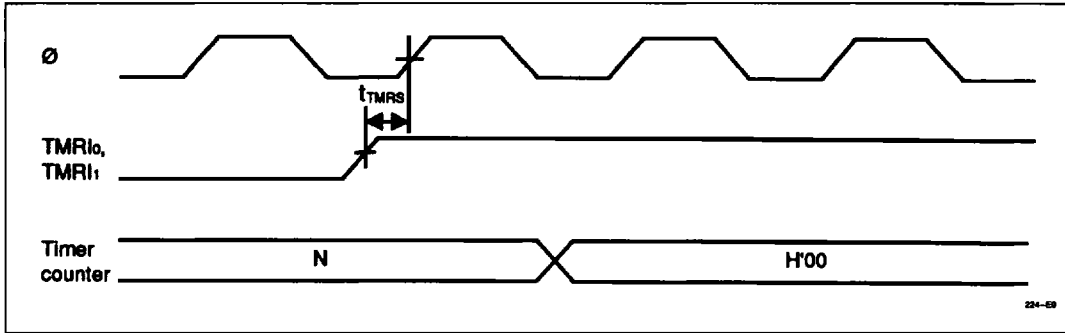


Figure 14-14. 8-Bit Timer Reset Input Timing

## 14.3.5 Serial Communication Interface Timing

### (1) SCI Input/Output Timing

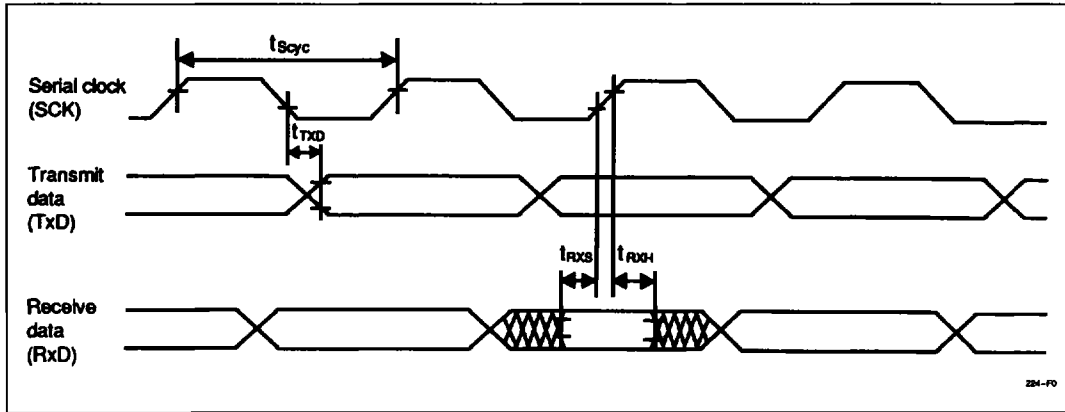


Figure 14-15. SCI Input/Output Timing (Synchronous Mode)

## (2) SCI Input Clock Timing

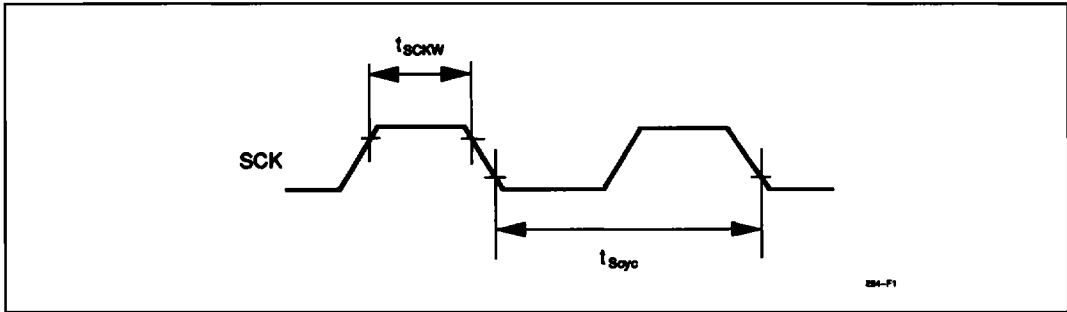


Figure 14-16. SCI Input Clock Timing

### 14.3.6 I/O Port Timing

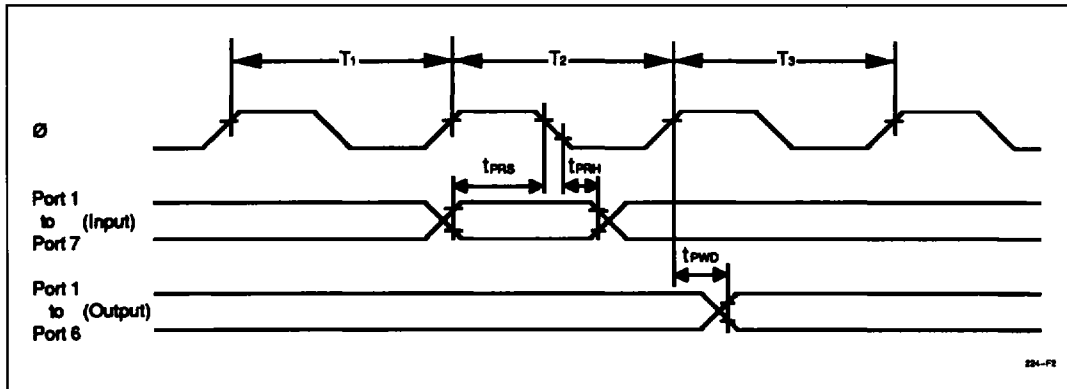


Figure 14-17. I/O Port Input/Output Timing