M80C186EB-16, -13, -8

16-Bit High-Integration Embedded Processor

The M80C186EB is a second generation CHMOS High-Integration microprocessor. It has features that are new to the M80C186 family and include a STATIC CPU core, an enhanced Chip Select decode unit, two independent Serial Channels, I/O ports, and the capability of Idle or Powerdown low power modes.

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    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

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The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

M80C186EB-16, -13, -8
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- **Full Static Operation**
- **True CMOS Inputs and Outputs**
- **−55°C to +125°C Operating Temperature Range**

- **Integrated Feature Set**
  - **Low-Power Static CPU Core**
  - **Two Independent UARTs each with an Integral Baud Rate Generator**
  - **Two 8-Bit Multiplexed I/O Ports**
  - **Programmable Interrupt Controller**
  - **Three Programmable 16-Bit Timer/Counters**
  - **Clock Generator**
  - **Ten Programmable Chip Selects with Integral Wait-State Generator**
  - **Memory Refresh Control Unit**
  - **System Level Testing Support (ONCE Mode)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Speed Versions Available:**
  - **16 MHz (M80C186EB-16)**
  - **13 MHz (M80C186EB-13)**
  - **8 MHz (M80C186EB-8)**
- **Low-Power Operating Modes:**
  - **Idle Mode Freezes CPU Clocks but keeps Peripherals Active**
  - **Powerdown Mode Freezes All Internal Clocks**
- **Complete System Development Support**
  - **ASM86 Assembler, PL/M 86, Pascal 86, Fortran 86, C-86, and System Utilities**
  - **In-Circuit Emulator (ICE™-186EB)**
- **Supports M80C187 Numeric Coprocessor Interface**
- **Available In:**
  - **88-Lead Pin Grid Array (MG80C186EB)**

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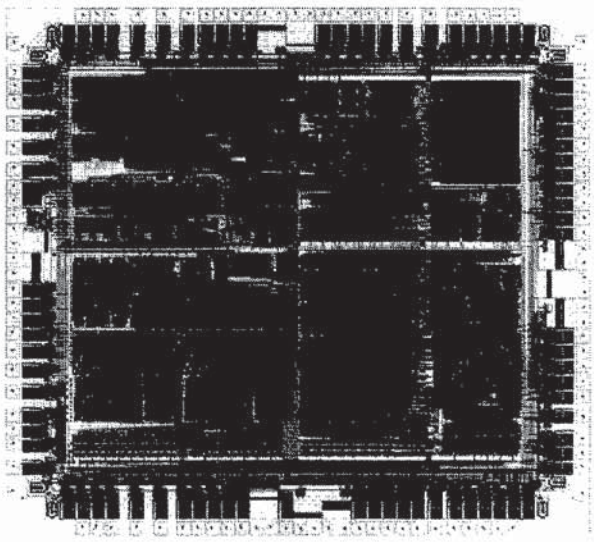
The M80C186EB is a second generation CHMOS High-Integration microprocessor. It has features that are new to the M80C186 family and include a STATIC CPU core, an enhanced Chip Select decode unit, two independent Serial Channels, I/O ports, and the capability of Idle or Powerdown low power modes.



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M80C186EB-16, -13, -8
16-Bit High-Integration Embedded Processor

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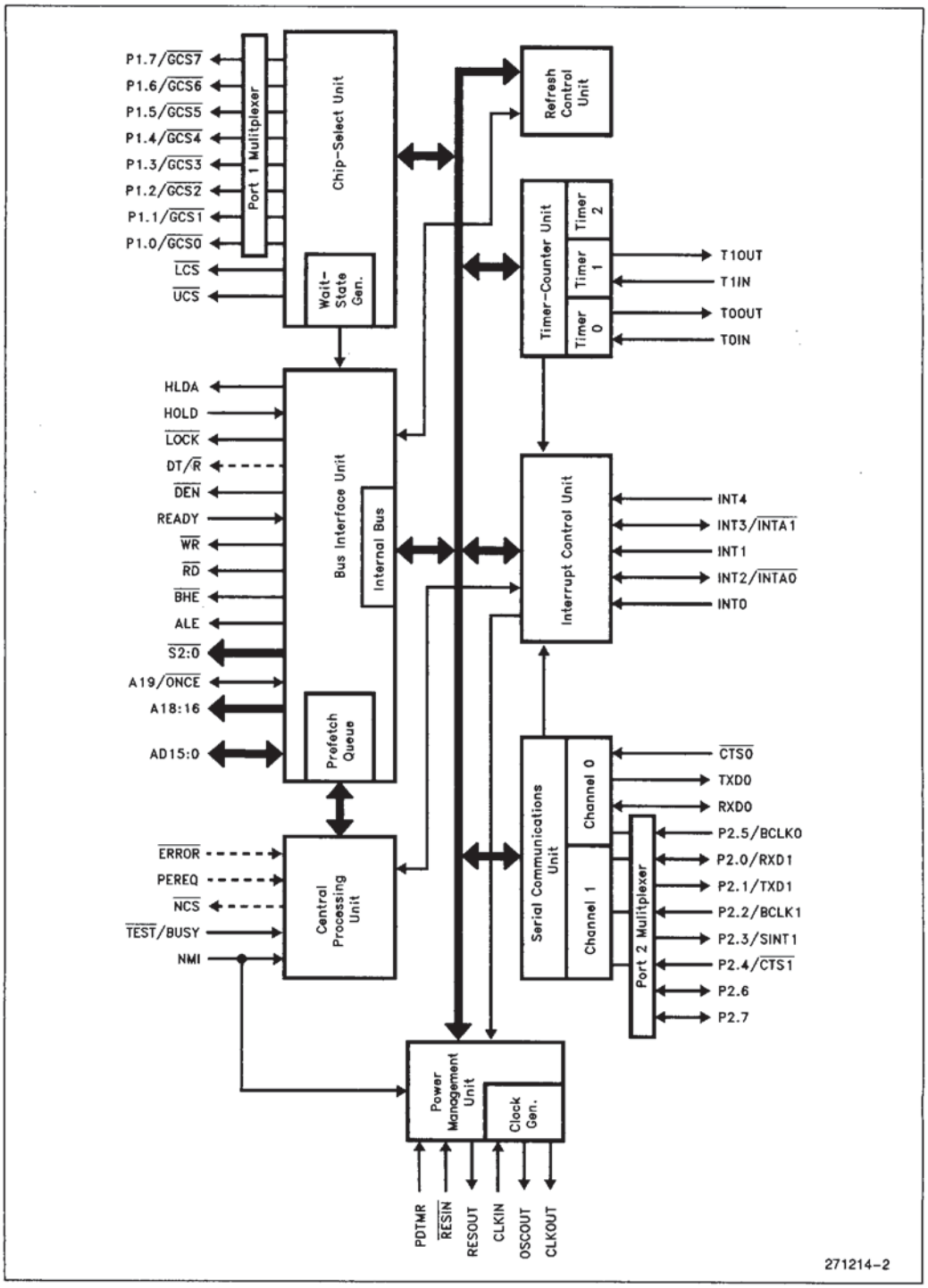

Figure 1. M80C186EB Block Diagram

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INTRODUCTION

The M80C186EB is the first product in a new generation of low-power, high-integration microprocessors. It enhances the existing 186 family by offering new features and new operating modes. The M80C186EB is object code compatible with the M80C186/M80C188 microprocessors.

The feature set of the M80C186EB meets the needs of low power, space critical applications. Low-Power applications benefit from the static design of the CPU core and the integrated peripherals. Minimum current consumption is achieved by providing a Powerdown mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space critical applications benefit from the integration of commonly used system peripherals. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface, and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 129 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters and sixteen multiplexed I/O port pins round out the feature set of the M80C186EB.

OVERVIEW

Figure 1 shows a block diagram of the M80C186EB. The Execution Unit (EU) is an enhanced M8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instruction, and full static operation. The Bus Interface Unit (BIU) is the same as that found on the original 186 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used to allow communication between the BIU and internal peripherals.

M80C186EB Core Architecture

REGISTER SET

The M8086, M8088, M80186, M80C186 and M80C188 all contain the same basic set of registers, instructions, and addressing modes. The M80C186EB is upward compatible with all of these microprocessors.

The M80C186EB base architecture has fourteen 16-bit registers as shown in Figure 2. There are eight general purpose registers which may be used for arithmetic and logic operands. Four of these registers (AX, BX, CX and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers. The other four registers (BP, SI, DI and SP) may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Another four 16-bit registers (CS, DS, ES, SS) select the segments of memory that are immediately addressable for code, stack, and data. There are two remaining special purpose registers (IP and F) that record or alter certain aspects of the M80C186EB processor state.

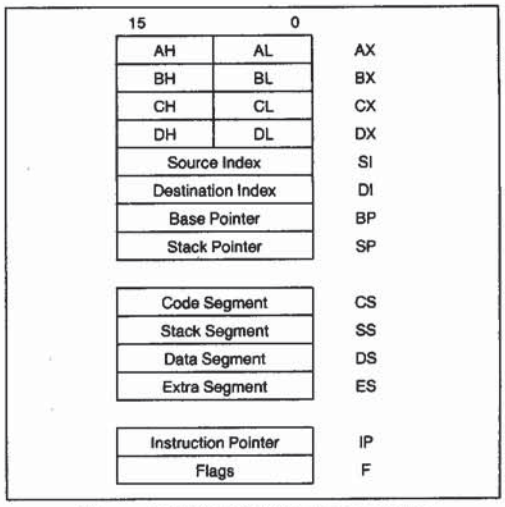

Figure 2. M80C186EB Register Set

INSTRUCTION SET

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An M80C186EB instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory.

MEMORY ORGANIZATION

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base segment values are contained in one of four internal segment registers (code, data stack, extra). The physical address is calculated by shifting the base value left by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 3). The resulting 20-bit address allows for a 1 Mbyte address range.

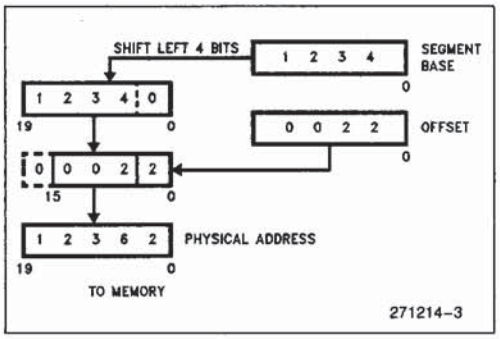

Figure 3. Two Component Address

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for a physical address generation is implied by the addressing mode used (see Table 1). Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The code, stack, data, and extra segments may coincide for simple programs.

Table 1. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data
Stack	Stack (SS)	All stack pushes and pops; any memory references which use the BP register as a base
External	Extra (ES)	All String instruction references which use the DI register as an index
Local Data	Data (DS)	All other data references

ADDRESSING MODES

The M80C186EB provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

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GENERAL PURPOSE

MOV
PUSH
POP
PUSHA
POPA
XCHG
XLAT

INPUT/OUTPUT

IN
OUT

ADDRESS OBJECT

LEA
LDS
LES

FLAG TRANSFER

LAHF
SAHF
PUSHF
POPF

ADDITION

ADD
INC
AAA
DAA

SUBSTRACTION

SUB
SBB
DEC
NEG
CMP
AAS
DAS

MULTIPLICATION

MUL
IMUL
AAM

DIVISION

DIV
IDIV
AAD
CBW
CWD

STRING OPERATIONS

MOVS
INS
OUTS
CMPS
SCAS
LODS
STOS
REP
REPE/REPZ
REPNE/REPNZ

LOGICALS

NOT
AND
OR
XOR
TEST

SHIFTS

SHL/SAL
SHR
SAR

ROTATES

ROL
ROR
RCL
RCR

FLAG OPERATIONS

STC
CLC
CMC
STD
CLD
STI
CLI

EXTERNAL SYNCHRONIZATION

HLT
WAIT
LOCK

NO OPERATION

NOP

HIGH LEVEL INSTRUCTIONS

ENTER
LEAVE
BOUND

CONDITIONAL TRANSFERS

JA/JNBE
JAE/JNB
JB/JNAE
JBE/JNA
JC
JE/JZ
JG/JNLE
JGE/JNL
JL/JNGE
JLE/JNG
JNC
JNE/JNZ
JNO
JNP/JP0
JNS
JO
JP/JPE
JS

UNCONDITIONAL TRANSFERS

CALL
RET
JMP

ITERATION CONTROLS

LOOP
LOOPE/LOOPZ
LOOPNE/LOOPNZ
JCXZ

INTERRUPTS

INT
INTO
IRET

Figure 4. M80C186EB Instruction Set

Any carry out from the 16-bit addition is ignored. 8-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

DATA TYPES

The M80C186EB directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using the M80C187 Numerics Coprocessor.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component, or a 16-bit segment base component and a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 Kbyte to 64 Kbytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4 bits) of the byte.
- *Floating Point:* A signed 32-, 64- or 80-bit real number representation. Floating point operands are supported when using the M80C187 Numeric Coprocessor.

In general, individual data elements must fit within defined segment limits.

INTERRUPTS

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (F) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, software (program) initiated, and instruction exception initiated. Hardware initiated interrupts occur in response to an external or internal input and are classified as nonmaskable or maskable.

Programs may cause an interrupt by executing the "INT" instruction. Instruction exceptions occur when an illegal opcode has been fetched into the queue and is read by the execution unit. Another type of exception can be generated when executing an "ESC" instruction.

For all cases except the "ESC" exception, the return address from an exception will point at the instruction immediately following the instruction causing the exception. The return address after an "ESC" exception will point back to the ESC instruction causing the exception, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31 are reserved by Intel. Table 2 shows the M80C186EB predefined type and default priority levels. For each interrupt, an 8-bit vector (Vector Type) identifies the appropriate table entry. Multiplying the 8-bit vector by 4 defines the vector address. INT instructions contain or imply the vector type and allow access to all 256 interrupts.

Table 2. M80C186EB Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions
Divide Error	0	00H	1	DIV, IDIV
Single Step Interrupt	1	04H	1A	All
Non-Maskable Interrupt	2	08H	1	INT 2 or NMI
One Byte Interrupt	3	0CH	1	INT
Interrupt on Overflow	4	10H	1	INT0
Array Bounds Check	5	14H	1	BOUND
Invalid OP-Code	6	18H	1	Illegal Inst
ESC OP-Code Interrupt	7	1CH	1	ESC OP-Codes
Timer 0 Interrupt	8	20H	2	
Reserved	9–11	24H–2CH		
INT0 Interrupt	12	30H	5	
INT1 Interrupt	13	34H	6	
INT2 Interrupt	14	38H	7	
INT3 Interrupt	15	3CH	8	
Numerics Exception	16	40H	1	ESC OP-Codes
INT4 Interrupt	17	44H	4	
Timer1 Interrupt	18	48H	2A	
Timer2 Interrupt	19	4CH	2B	
UART 0 Receive Interrupt	20	50H	3	
UART 0 Transmit Interrupt	21	54H	3A	
Reserved	22–31	58H–7CH		

BUS INTERFACE UNIT

The M80C186EB core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information, and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. A READY input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

A HOLD/HLDA protocol is provided by the local bus controller to allow multiple bus masters to share the same local bus. When the M80C186EB relinquishes control of the local bus, it floats certain bus control signals to allow another bus master to drive these pins directly. Refer to the Pin Description section to determine which pins the M80C186EB will float during a HOLD/HLDA bus exchange.

The M80C186EB local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the mulitplexed address/data bus.

CLOCK GENERATOR

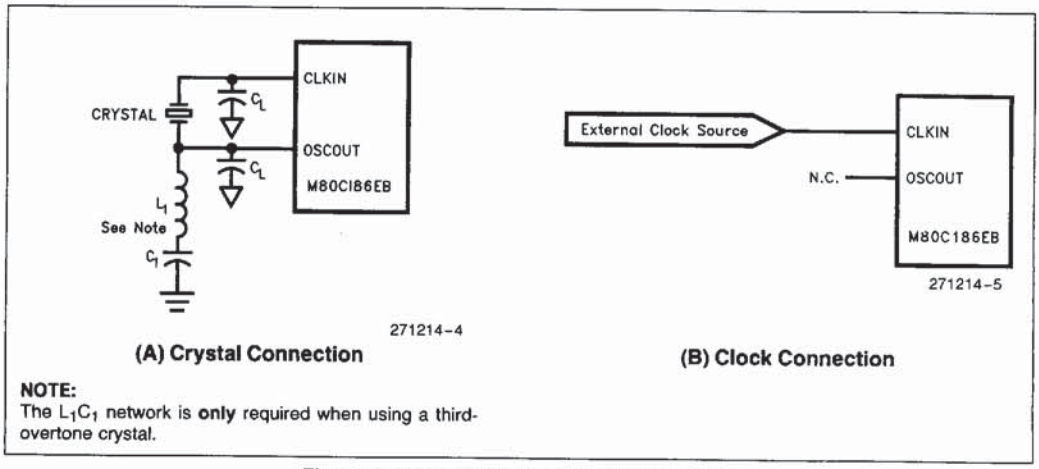
The M80C186EB provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 5 shows the various operating modes of the M80C186EB oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	40Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max



NOTE:
The L_1C_1 network is **only** required when using a third-overtone crystal.

Figure 5. M80C186EB Clock Configurations

M80C186EB Peripheral Architecture

The M80C186EB has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or serial channels).

The list of integrated peripherals include:

- 7-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 10-Output Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 Byte address boundary. During bus cycles that access the PCB, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle). However, READY is ignored and the contents of the data bus during a read operation is ignored.

The starting address of the PCB is controlled by a relocation register and can overlap any of the memory or I/O regions programmed into the Chip Select Unit. In this case, the overlapped chip select will not go active when the PCB is read or written.

Figure 6 provides a list of the registers associated with the PCB. The Register Bit Summary at the end of this specification individually lists all of the registers and identifies each of their programming attributes.

INTERRUPT CONTROL UNIT

The M80C186EB can receive interrupts from a number of sources, both internal and external. The interrupt control unit serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit (ICU) or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and Serial channel 0. External interrupt sources come from the five input pins INT4:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the Timer and Serial channel each have only one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer and Serial channel units.

The M80C186EB ICU provides a mechanism for expanding the number of external interrupt sources. Two pairs of pins can be independently configured to support an external slave interrupt controller (82C59A). Each pair of external pins can be expanded to support 64 interrupts, making it possible for the M80C186EB to support a total of 129 external interrupts.

The ICU may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the ICU whenever it is convenient.

TIMER/COUNTER UNIT

The M80C186EB Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts, etc.

Each timer has at least one 16-bit compare register and one 16-bit count register. Timers 0 and 1 each have an additional 16-bit compare register. The count register is incremented every fourth CPU clock cycle (internal clocking), every time Timer2 expires (Timers 0 and 1 only), or every Low-to-High transition on the timer input pin (Timers 0 and 1 only). The input clock to Timers 0 and 1 must not exceed one fourth the operating frequency of the M80C186EB. When the count register matches the value programmed into the compare register, several operations may happen.

All three timers can generate an interrupt when the compare register matches the value in the count register. Additionally, Timers 0 and 1 have an output pin that can change state or pulse when the compare condition occurs.

PCB Offset	Function
00H	Reserved
02H	End Of Interrupt
04H	Poll
06H	Poll Status
08H	Interrupt Mask
0AH	Priority Mask
0CH	In-Service
0EH	Interrupt Request
10H	Interrupt Status
12H	Timer Control
14H	Serial Control
16H	INT4 Control
18H	INT0 Control
1AH	INT1 Control
1CH	INT2 Control
1EH	INT3 Control
20H	Reserved
22H	Reserved
24H	Reserved
26H	Reserved
28H	Reserved
2AH	Reserved
2CH	Reserved
2EH	Reserved
30H	Timer0 Count
32H	Timer0 Compare A
34H	Timer0 Compare B
36H	Timer0 Control
38H	Timer1 Count
3AH	Timer1 Compare A
3CH	Timer1 Compare B
3EH	Timer1 Control

PCB Offset	Function
40H	Timer2 Count
42H	Timer2 Compare
44H	Reserved
46H	Timer2 Control
48H	Reserved
4AH	Reserved
4CH	Reserved
4EH	Reserved
50H	Reserved
52H	Port0 Pin
54H	Port0 Control
56H	Port0 Latch
58H	Port1 Direction
5AH	Port1 Pin
5CH	Port1 Control
5EH	Port1 Latch
60H	Serial0 Baud
62H	Serial0 Count
64H	Serial0 Control
66H	Serial0 Status
68H	Serial0 RBUF
6AH	Serial0 TBUF
6CH	Reserved
6EH	Reserved
70H	Serial1 Baud
72H	Serial1 Count
74H	Serial1 Control
76H	Serial1 Status
78H	Serial1 RBUF
7AH	Serial1 TBUF
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	GCS0 Start
82H	GCS0 Stop
84H	GCS1 Start
86H	GCS1 Stop
88H	GCS2 Start
8AH	GCS2 Stop
8CH	GCS3 Start
8EH	GCS3 Stop
90H	GCS4 Start
92H	GCS4 Stop
94H	GCS5 Start
96H	GCS5 Stop
98H	GCS6 Start
9AH	GCS6 Stop
9CH	GCS7 Start
9EH	GCS7 Stop
A0H	LCS Start
A2H	LCS Stop
A4H	UCS Start
A6H	UCS Stop
A8H	Relocation
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Refresh Base
B2H	Refresh Time
B4H	Refresh Control
B6H	Refresh Address
B8H	Power Control
BAH	Reserved
BCH	Step ID
BEH	Reserved

PCB Offset	Function
C0H	Reserved
C2H	Reserved
C4H	Reserved
C6H	Reserved
C8H	Reserved
CAH	Reserved
CCH	Reserved
CEH	Reserved
D0H	Reserved
D2H	Reserved
D4H	Reserved
D6H	Reserved
D8H	Reserved
DAH	Reserved
DCH	Reserved
DEH	Reserved
E0H	Reserved
E2H	Reserved
E4H	Reserved
E6H	Reserved
E8H	Reserved
EAH	Reserved
ECH	Reserved
EEH	Reserved
F0H	Reserved
F2H	Reserved
F4H	Reserved
F6H	Reserved
F8H	Reserved
FAH	Reserved
FCH	Reserved
FEH	Reserved

Figure 6. M80C186EB Peripheral Control Block Registers

Other timer programming options include:

- All three timers can be set to halt or continue after a compare match.
- Timers 0 and 1 can be reset or retriggered using their respective input pins.
- TCU registers can be read or written at any time.

SERIAL COMMUNICATIONS UNIT

The Serial Control Unit (SCU) of the M80C186EB contains two independent channels. Each channel is identical in operation except that only channel 0 is supported by the integrated interrupt controller (channel 1 has an external interrupt pin). Each channel has its own baud rate generator that is independent of the Timer/Counter Unit, and can be internally or externally clocked at up to one half the M80C186EB operating frequency.

Each serial channel supports one synchronous and four asynchronous modes of operation and is compatible with the serial ports of the MCS®-51 and MCS®-96 family of products. Data field length can be 7-, 8-, or 9-bits with optional odd or even parity (generated and checked) and one stop bit (generated and checked). The 9-bit mode has an optional "addressing" feature to simplify interprocessor communication. Each serial port is doubled buffered in both transmit and receive operation (data can be read or written to a buffer register while data is shifted into or out of a shifting register, respectively).

A Clear-To-Send input pin can be programmed to prevent data transmission if the pin is sampled inactive. Serial channel 0 is supported by the integrated interrupt controller, providing separate receive and transmit vector types. Serial channel 1 has an external interrupt pin which OR's the receive and transmit interrupts. This external interrupt pin can be routed to either the external pins of the ICU, the NMI pin, or any other external system interrupt controller. Status bits are provided to allow polling of the serial channels if interrupts are not desired.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit register logic. A 1x baud clock is provided in the synchronous mode.

Additional features of the SCU include:

- Framing error, receive buffer overrun error, and parity error detection.
- Break detect.
- Break send.

CHIP-SELECT UNIT

The M80C186EB Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait-states) into the current bus cycle and automatically terminate a bus cycle independent of the condition of the READY input pin.

Each of the chip-selects can be programmed to go active for either memory or I/O accesses. $\overline{\text{UCS}}$ is the only chip-select that is active after a reset and is enabled for memory addresses in the range 0FFC00H to 0FFFFFH (this allows a boot-ROM to be accessed using $\overline{\text{UCS}}$). Every chip-select has a programmable start and stop register that defines the active region for the chip-select, and the ready characteristics for the region.

The start and stop address fields are 10 bits in length and are matched against the upper 10 bits of either the memory or I/O address. A 10-bit compare results in a granularity of 1 Kbytes for memory accesses and 64 bytes for I/O accesses. Each chip select can be disabled by programming its start address greater than its stop address or by clearing its enable bit.

Each chip-select can be programmed to automatically insert wait-states, and to control whether the external READY input is to be ignored or used. The M80C186EB bus controller will wait the programmed number of wait-states before the external READY pin can be used to extend or terminate the bus cycle.

Overlapping of chip-selects is allowed. However, each one that overlaps will go active. If any overlapping chip-select has been programmed to use external ready, the bus control unit will insert the least amount of programmed wait-states programmed before the external ready pin is used. If all overlapped chip-selects ignore external ready, the bus controller will insert the maximum number of programmed wait-states. Any chip-select that overlaps the Peripheral Control Block (PCB) will not go active for that portion of the address range allocated to the PCB.

The Generic Chip-Selects (GCS7:0) are multiplexed with an output only Port function. Any channel that is being used as a chip-select must be disabled as a port pin by correctly programming the port pin control registers (see the following section).

I/O PORT UNIT

The I/O Port Unit (IPU) on the M80C186EB supports two 8-bit channels of input, output, or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Most of Port 2 is multiplexed with the serial channel pins. Port 2 pins are limited to either an output or input function depending on the operation of the serial pin it is multiplexed with.

Two bits of Port 2 are not multiplexed with any other peripheral functions and can be used as either an input or an output function. A port direction register is used to define the function of the port pin. The output for these two pins are open drain.

Besides a direction register, each port channel has a data latch register, port pin register, and a port multiplexer control register.

REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. The address generator is incremented only after the refresh bus cycle is run. This ensures that all address combinations will be presented to the memory array even if the refresh bus cycle is not run before another request is generated. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

The chip-select unit is active during refresh bus cycles. This means that a chip-select will go active if the refresh address is within the limits specified for the channel. In addition, $\overline{BHE}$ and A0 are both driven high during refresh bus cycles (this is normally an invalid bus condition). Data on the AD15:0 bus is ignored.

A pending refresh request will attempt to abort a HOLD/HLDA bus exchange. HLDA is deasserted when a refresh request is pending and a bus HOLD is already in progress. HOLD must then be released in order for the M80C186EB to execute the refresh bus cycle.

POWER MANAGEMENT UNIT

The M80C186EB Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides three power modes: Active, Idle, and Powerdown.

Active Mode indicates that all units on the M80C186EB are functional and the device consumes maximum power (depending on the level of peripheral operation). Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally). An unmasked interrupt, NMI, or reset will cause the M80C186EB to exit the Idle mode.

The Powerdown mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to just transistor junction leakage. An NMI or processor reset will cause the M80C186EB to exit the Powerdown Mode. A timing pin is provided to establish the length of time between exiting Powerdown and resuming device operation. (Length of time depends on startup time of crystal oscillator and is application dependent.)

M80C187 Interface

The M80C186EB supports the direct connection of the M80C187 Numerics Coprocessor.

ONCE Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the M80C186EB has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the A19/$\overline{ONCE}$ pin LOW (0) during a processor reset (this pin is weakly held to a HIGH (1) level) while $\overline{RESIN}$ is active.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the M80C186EB PGA package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

The M80C186EB pins are described in this section. Table 3 presents the legend for interpreting the pin descriptions in Table 4. Figure 7 provides an example pin description entry. The "I/O" signifies that the pins are bidirectional (i.e., have both an input and output function). The "S" indicates that, as an input, the signal is synchronized to CLKOUT for proper operation. The "H(Z)" indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low. P(X) Indicates that these pins will retain its current value when Idle or Powerdown Modes are entered.

All pins float while the processor is in the ONCE Mode, except OSCOUT (OSCOUT is required for crystal operation).

Name	Type	Description
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information are transferred during the data phase of the bus cycle.

Figure 7. Example Pin Description Entry

Table 3. Pin Description Nomenclature

Symbol	Description
I	Input Only Pin
O	Output Only Pin
I/O	Pin can be either input or output
—	Pin "must be" connected as described
S(..)	Synchronous. Input must meet setup and hold times for proper operation of the processor. The pin is: S(E) edge sensitive S(L) level sensitive
A(..)	Asynchronous. Input must meet setup and hold only to guarantee recognition. The pin is: A(E) edge sensitive A(L) level sensitive
H(..)	While the processor's bus is in the Hold Acknowledge state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) remains active H(X) retains current state
R(..)	While the processor's $\overline{\text{RES}}$ line is low, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(WH) weak pullup R(WL) weak pulldown
P(..)	While Idle or Powerdown modes are active, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Z) floats P(Q) remains active(1) P(X) retains current state

NOTE:
1. Any pin that specifies P(Q) are valid for Idle Mode. All pins are P(X) for Powerdown Mode.

Table 4. M80C186EB Pin Descriptions

Name	Type	Description
V_{CC}		**POWER** connections consist of four pins which must be shorted externally to a V_{CC} board plane.
V_{SS}		**GROUND** connections consist of six pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required M80C186EB operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{RESIN}$	I A(L)	**RESet IN** causes the M80C186EB to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the M80C186EB begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the M80C186EB is currently in the reset state. RESOUT will remain active as long as $\overline{RESIN}$ remains active.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the M80C186EB waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{TEST}$/BUSY	I A(E)	**TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW). $\overline{TEST}$ is alternately known as BUSY when interfacing with an M80C187 numerics coprocessor.
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A18:16 A19/$\overline{ONCE}$	H(Z) R(WH) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle. During a processor reset ($\overline{RESIN}$ active), A19/$\overline{ONCE}$ is used to enable ONCE mode. A18:16 must not be driven low during reset or improper M80C186EB operation may result.

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Table 4. M80C186EB Pin Descriptions (Continued)

Name	Type	Description
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.
$\overline{BHE}$	O H(Z) R(Z) P(X)	**Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding: A0 $\overline{BHE}$ Encoding 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation
$\overline{RD}$	O H(Z) R(Z) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus.
$\overline{WR}$	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device.
READY	I A(L) S(L)	**READY** input to signal the completion of a bus cycle. READY must be active to terminate any M80C186EB bus cycle, unless it is ignored by correctly programming the Chip-Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bi-directional transceivers when buffering a M80C186EB system. $\overline{DEN}$ is active only when data is to be transferred on the bus.
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an M80C186EB system.
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The M80C186EB will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.

Table 4. M80C186EB Pin Descriptions (Continued)

Name	Type	Description
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The M80C186EB will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the M80C186EB has relinquish control of the local bus. When HLDA is asserted, the M80C186EB will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{NCS}$	O H(1) R(1) P(1)	**Numerics Coprocessor Select** output is generated when accessing a numerics coprocessor.
$\overline{ERROR}$	I A(L)	**ERROR** input that indicates the last numerics coprocessor operation resulted in an exception condition. An interrupt TYPE 16 is generated if $\overline{ERROR}$ is sampled active at the beginning of a numerics operation.
PEREQ	I A(L)	**CoProcessor REQuest** signals that a data transfer between an External Numerics Coprocessor and Memory is pending.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset.
P1.0/$\overline{GCS0}$ P1.1/$\overline{GCS1}$ P1.2/$\overline{GCS2}$ P1.3/$\overline{GCS3}$ P1.4/$\overline{GCS4}$ P1.5/$\overline{GCS5}$ P1.6/$\overline{GCS6}$ P1.7/$\overline{GCS7}$	O H(X)/H(1) R(1) P(X)/P(1)	These pins provide a multiplexed function. If enabled, each pin can provide a **Generic Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output **Port.** As an output port pin, the value of the pin can be read internally.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

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Table 4. M80C186EB Pin Descriptions (Continued)

Name	Type	Description
INT0 INT1 INT4	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{INTA0}$ and $\overline{INTA1}$ to interface with an external slave controller.
INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide a multiplexed function. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an INTERRUPT ACKNOWLEDGE handshake signal to allow interrupt expansion.
P2.7 P2.6	I/O A(L) H(X) R(Z) P(X)	Bidirectional, open-drain **Port** pins.
$\overline{CTS0}$ P2.4/$\overline{CTS1}$	I A(L)	**Clear-To-Send** input is used to prevent the transmission of serial data on their respective TXD signal pin. $\overline{CTS1}$ is multiplexed with an input only port function.
TXD0 P2.1/TXD1	O H(X)/H(Q) R(1) P(X)/P(Q)	**Transmit Data** output provides serial data information. TXD1 is multiplexed with an output only **Port** function. During synchronous serial communications, TXD will function as a clock output.
RXD0 P2.0/RXD1	I/O A(L) R(Z) H(Q) P(X)	**Receive Data** input accepts serial data information. RXD1 is multiplexed with an input only **Port** function. During synchronous serial communications, RXD is bi-directional and will become an output for transmission or data (TXD becomes the clock).
P2.5/BCLK0 P2.2/BCLK1	I A(L)/A(E)	**Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. BCLKx is multiplexed with an input only **Port** function, and cannot exceed a clock rate greater than one-half the operating frequency of the M80C186EB.
P2.3/SINT1	O H(X)/H(Q) R(0) P(X)/P(Q)	**Serial INTerrupt** output will go active to indicate serial channel 1 requires service. SINT1 is multiplexed with an output only **Port** function.

M80C186EB PINOUT

Table 5 lists the M80C186EB pin names with package location for the 88-Lead Pin Grid Array (PGA) component. Figure 8 depicts the complete M80C186EB pinout as viewed from the bottom side of the component.

Table 5. MG80C186EB Pin Assignments

PLCC	PGA	Name
11	1A	$\overline{DEN}$
10	2B	$\overline{S0}$
9	1B	$\overline{S1}$
8	2C	$\overline{S2}$
7	1C	$\overline{BHE}$
6	2D	ALE
5	1D	$\overline{WR}$
4	2E	$\overline{RD}$
3	1E	$\overline{ERROR}$
2	2F	V_{SS}
1	1F	V_{CC}
84	2G	V_{SS}
83	1G	A19/$\overline{ONCE}$
82	2H	A18
81	1H	A17
80	2J	A16
79	1J	AD15
78	2K	AD7
77	1K	AD14
76	2L	AD6
75	1L	AD13
—	2M	N/C

PLCC	PGA	Name
74	1M	AD5
73	1N	AD12
72	2N	AD4
71	3M	AD11
70	3N	AD3
69	4M	AD10
68	4N	AD2
67	5M	AD9
66	5N	AD1
65	6M	V_{SS}
64	6N	V_{CC}
63	7M	V_{SS}
—	7N	N/C
62	8M	AD8
61	8N	AD0
60	9M	$\overline{NCS}$
59	9N	P2.2/BCLK1
58	10M	P2.1/TXD1
57	10N	P2.0/RXD1
56	11M	P2.4/$\overline{CTS1}$
55	11N	P2.3/SINT1
54	12M	P2.5/BLCK0

PLCC	PGA	Name
—	12N	N/C
53	13N	RXD0
52	13M	TXD0
51	12L	$\overline{CTS0}$
50	13L	P2.6
49	12K	P2.7
48	13K	T1IN
47	12J	T1OUT
46	13J	T0IN
45	12H	T0OUT
44	13H	CLKOUT
43	12G	V_{SS}
42	13G	V_{CC}
41	12F	CLKIN
40	13F	OSCOUT
39	12E	PEREQ
38	13E	RESOUT
37	12D	$\overline{RESIN}$
36	13D	PDTMR
35	12C	INT4
34	13C	INT3
33	12B	INT2

PLCC	PGA	Name
—	13B	N/C
32	13A	INT1
31	12A	INT0
30	11B	$\overline{UCS}$
29	11A	$\overline{LCS}$
28	10B	P1.0/$\overline{GCS0}$
27	10A	P1.1/$\overline{GCS1}$
26	9B	P1.2/$\overline{GCS2}$
25	9A	P1.3/$\overline{GCS3}$
24	8B	P1.4/$\overline{GCS4}$
23	8A	V_{CC}
22	7B	V_{SS}
21	7A	P1.5/$\overline{GCS5}$
20	6B	P1.6/$\overline{GCS6}$
19	6A	P1.7/$\overline{GCS7}$
18	5B	READY
17	5A	NMI
16	4B	DRT/$\overline{R}$
15	4A	$\overline{LOCK}$
14	3B	$\overline{TEST}$/BUSY
13	3A	HOLD
12	2A	HLDA

3

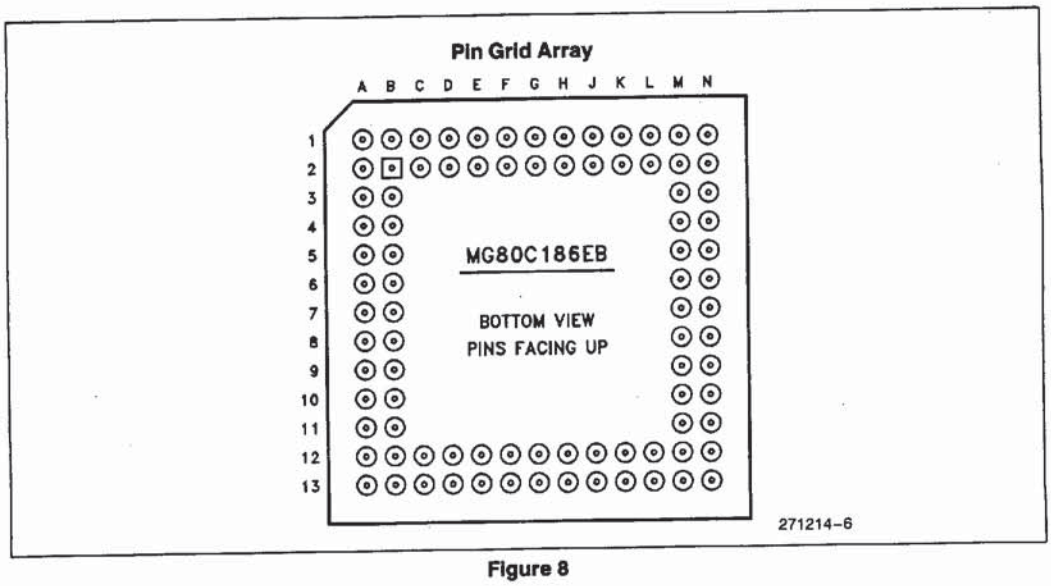

Figure 8

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temp Under Bias	−55°C to +125°C
Supply Voltage with respect to V_{SS}	−0.5V to +6.5V
Voltage on other Pins with respect to V_{SS}	−0.5V to V_{CC} +0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency M80C186EB-16	0	32	MHz
	M80C186EB-13	0	26.08	MHz
	M80C186EB-8	0	16	MHz
T_C	Case Temperature Under Bias	−55	+125	°C

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RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every M80C186EB-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system. Liberal decoupling capacitance should be placed near the M80C186EB. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the M80C186EB V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (INT0:4) should be connected to V_{CC} through a pull-up resistor (in the range of 50 KΩ). **Leave any unused output pin or any NC pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	(Note 8)
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (Min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (Min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.50		V	
I_{LI1}	Input Leakage Current for pins: AD15:0, READY, HOLD, $\overline{RESIN}$, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, P2.6, P2.7		±15	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LI2}	Input Leakage Current for Pin: CLKIN		±50	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{I1}	Input Current for Pin: $\overline{ERROR}$	−7	−0.275	mA	V_{IN} = 0V
I_{I2}	Input Current for Pin: PEREQ	+0.275	+7	mA	V_{IN} = V_{CC}
I_{LO}	Output Leakage Current		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Notes 2, 7)
I_{CC}	Supply Current Cold (RESET) M80C186EB-16		90	mA	(Note 3)
	M80C186EB-13		73	mA	(Note 3)
	M80C186EB-8		45	mA	(Note 3)
I_{ID}	Supply Current Idle M80C186EB-16		63	mA	(Note 4)
	M80C186EB-13		48	mA	(Note 4)
	M80C186EB-8		31	mA	(Note 4)
I_{PD}	Supply Current Powerdown M80C186EB-16		100	μA	(Note 5)
	M80C186EB-13		100	μA	(Note 5)
	M80C186EB-8		100	μA	(Note 5)
CIN	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
COUT	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 6)

NOTES:
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
6. Output Capacitance is the capacitive load of a floating output pin.
7. OSC out is not tested.
8. A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$ are not tested.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the M80C186EB is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the M80C186EB would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 11). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 10 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.583 \times 10 \approx 28 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

3

Table 11. Device Capacitance (C_{DEV}) Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.583	1.02	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.408	0.682	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—M80C186EB-16

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	32	MHz	1
T_C	CLKIN Period	31.25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3, 11
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3, 11
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time		6	ns	1, 5
T_{PF}	CLKOUT Fall Time		6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	1	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	1	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	1	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	1	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1, 11
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1, 11
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper M80C186EB operation.
11. Not tested.

AC SPECIFICATIONS

AC Characteristics—M80C186EB-13

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	26.08	MHz	1
T_C	CLKIN Period	38.34	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time		6	ns	1, 5
T_{PF}	CLKOUT Fall Time		6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	1	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	1	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	1	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	1	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1, 11
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1, 11
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper M80C186EB operation.
11. Not tested.

AC Characteristics—M80C186EB-8

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	16	MHz	1
T_C	CLKIN Period	62.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	27	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time		6	ns	1, 5
T_{PF}	CLKOUT Fall Time		6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	1	30	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	1	35	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	1	30	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	1	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1, 11
T_{CLOF}	$\overline{DEN}$, AD15:0	0	35	ns	1, 11
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper M80C186EB operation.
11. Not tested.

Relative Timings (M80C186EB-16, -13, -8)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	$\overline{ONCE}$ Hold from $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.

Serial Port Mode 0 Timings (M80C186EB-16, -13, -8)

Symbol	Parameter	Min	Max	Unit	Notes
T_{XLXL}	TXD Clock Period	T (n + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (n > 1)	2T − 35	2T + 35	ns	1
T_{XLXH}	TXD Clock Low to Clock High (n = 1)	T − 35	T + 35	ns	1
T_{XHXL}	TXD Clock High to Clock Low (n > 1)	(n − 1) T − 35	(n − 1) T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (n = 1)	T − 35	T + 35	ns	1
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n > 1)	(n − 1) T − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1, 3
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Hold after TXD Clock High	0		ns	1, 3

NOTES:
1. See Figure 14 for waveforms.
2. n is the value of the BxCMP register ignoring the ICLK Bit (i.e., ICLK = 0).
3. Guaranteed, not tested.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 9. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

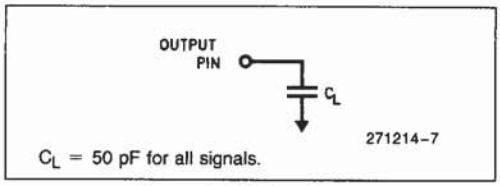


Figure 9. AC Test Load

AC TIMING WAVEFORMS

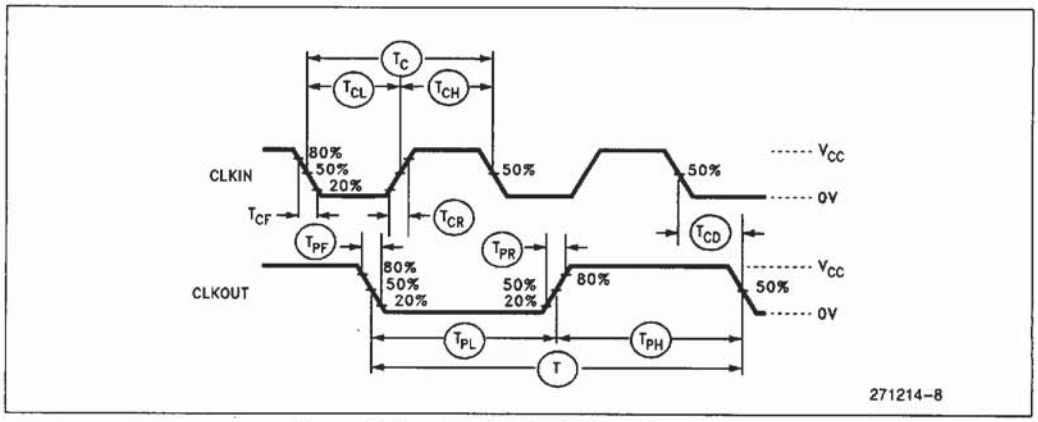
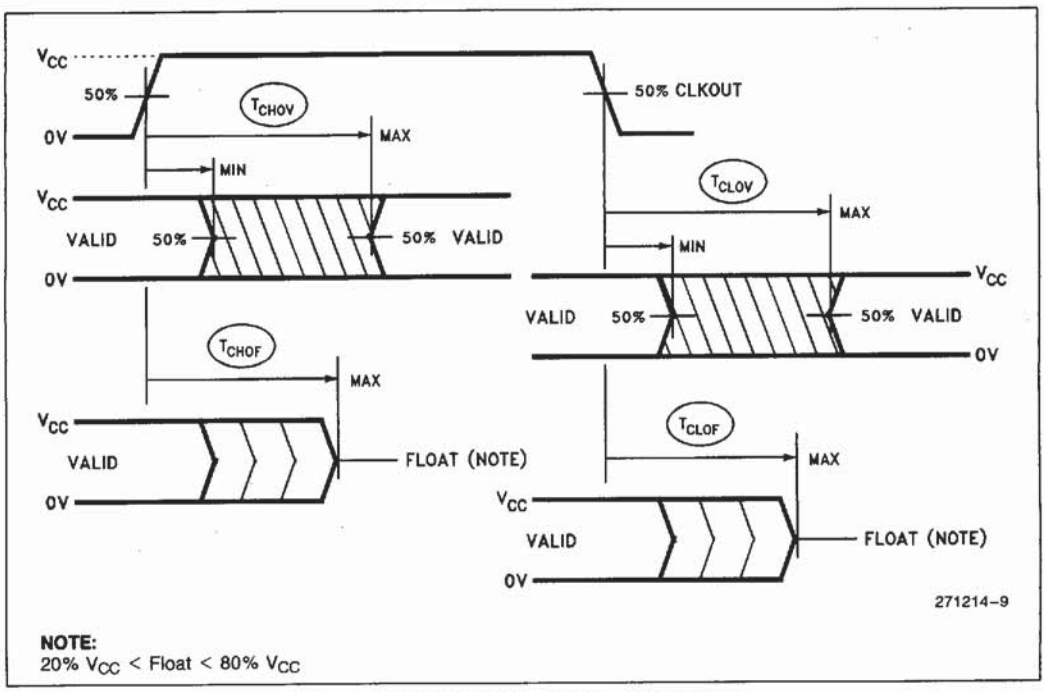


Figure 10. Input and Output Clock Waveform

3



NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 11. Output Delay and Float Waveform

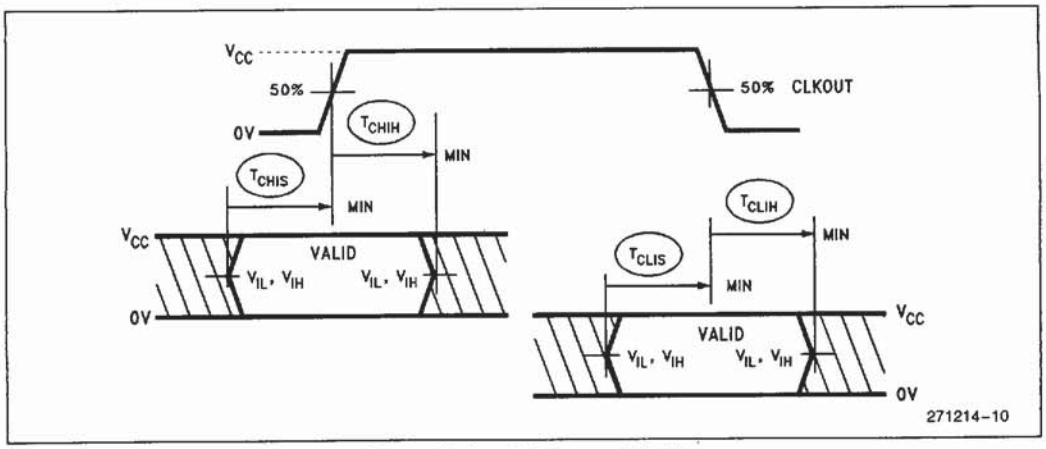


Figure 12. Input Setup and Hold

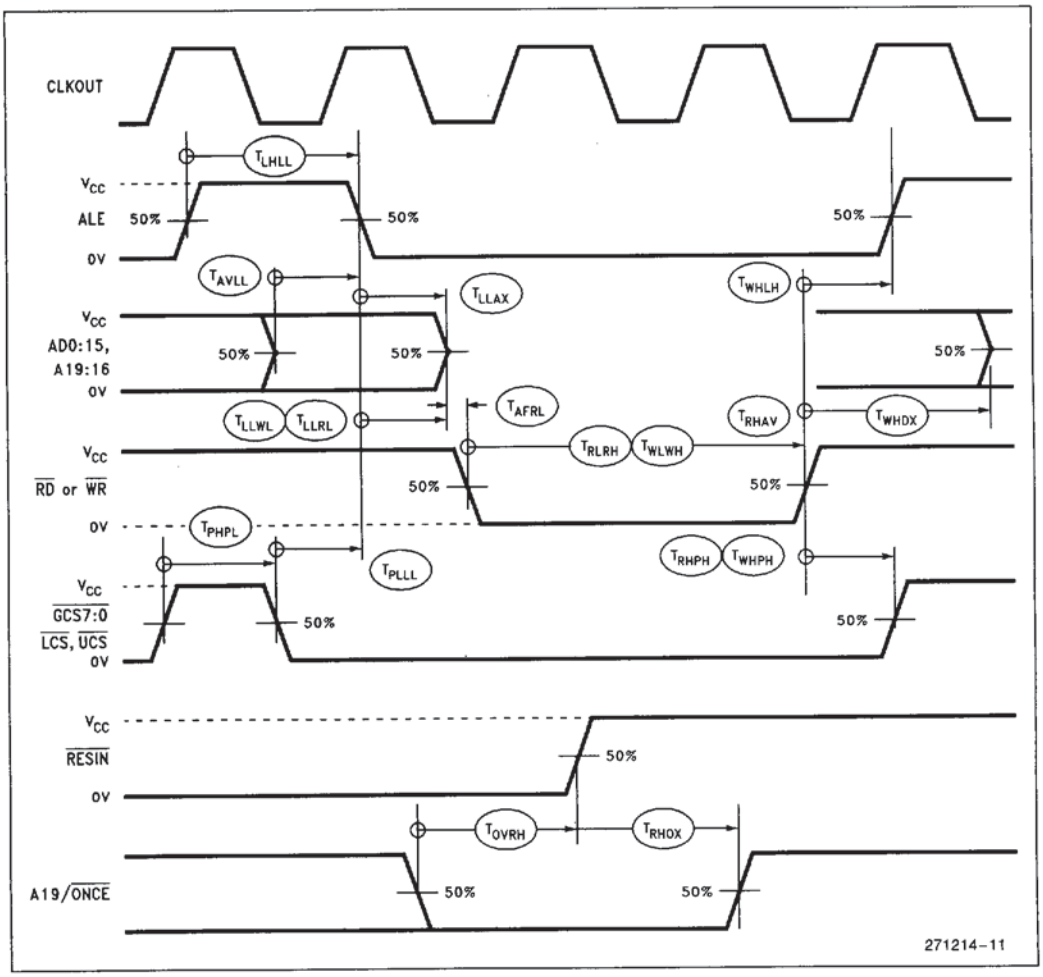


Figure 13. Relative Signal Waveform

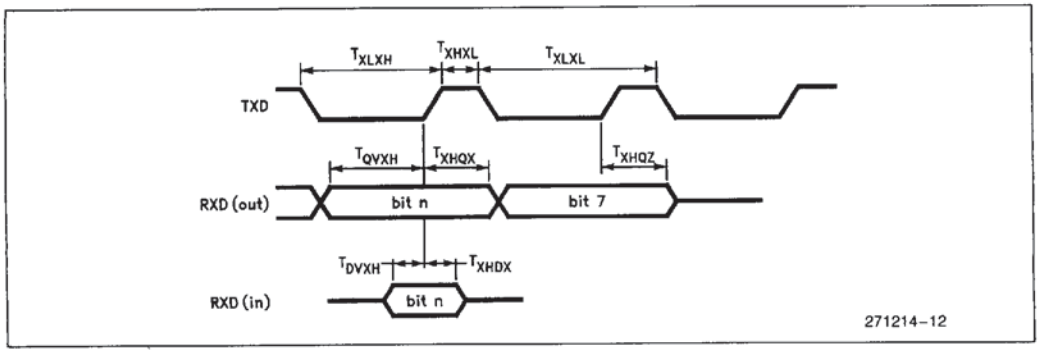


Figure 14. Serial Port Mode 0 Waveform

DERATING CURVES

TYPICAL OUTPUT DELAY VARIATIONS VERSUS LOAD CAPACITANCE

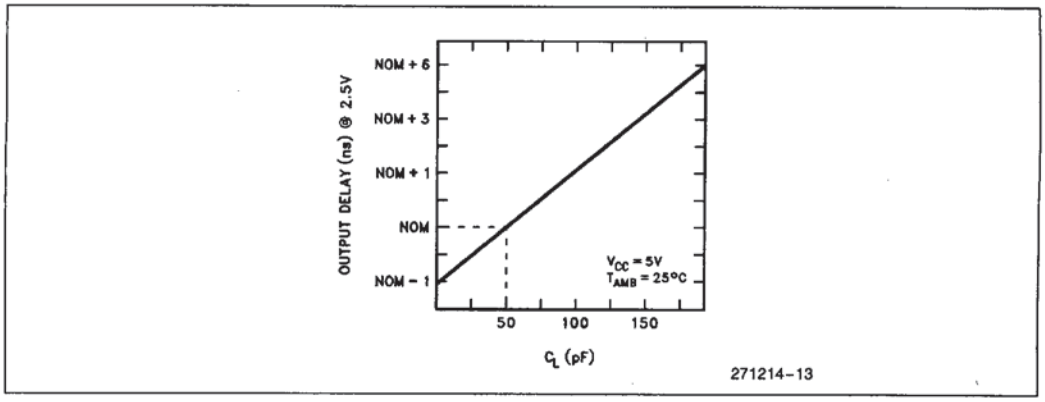


Figure 15

TYPICAL RISE AND FALL VARIATIONS VERSUS LOAD CAPACITANCE

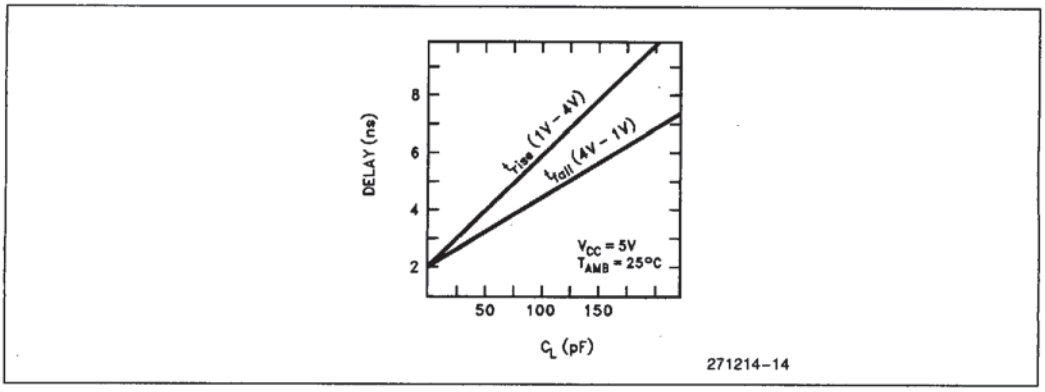


Figure 16

RESET

The M80C186EB will perform a reset operation any time the $\overline{\text{RESIN}}$ pin active. The $\overline{\text{RESIN}}$ pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{\text{RESIN}}$ must be held active (low) in order to guarantee correct initialization of the M80C186EB. **Failure to provide $\overline{\text{RESIN}}$ while the device is powering up will result in unspecified operation of the device.**

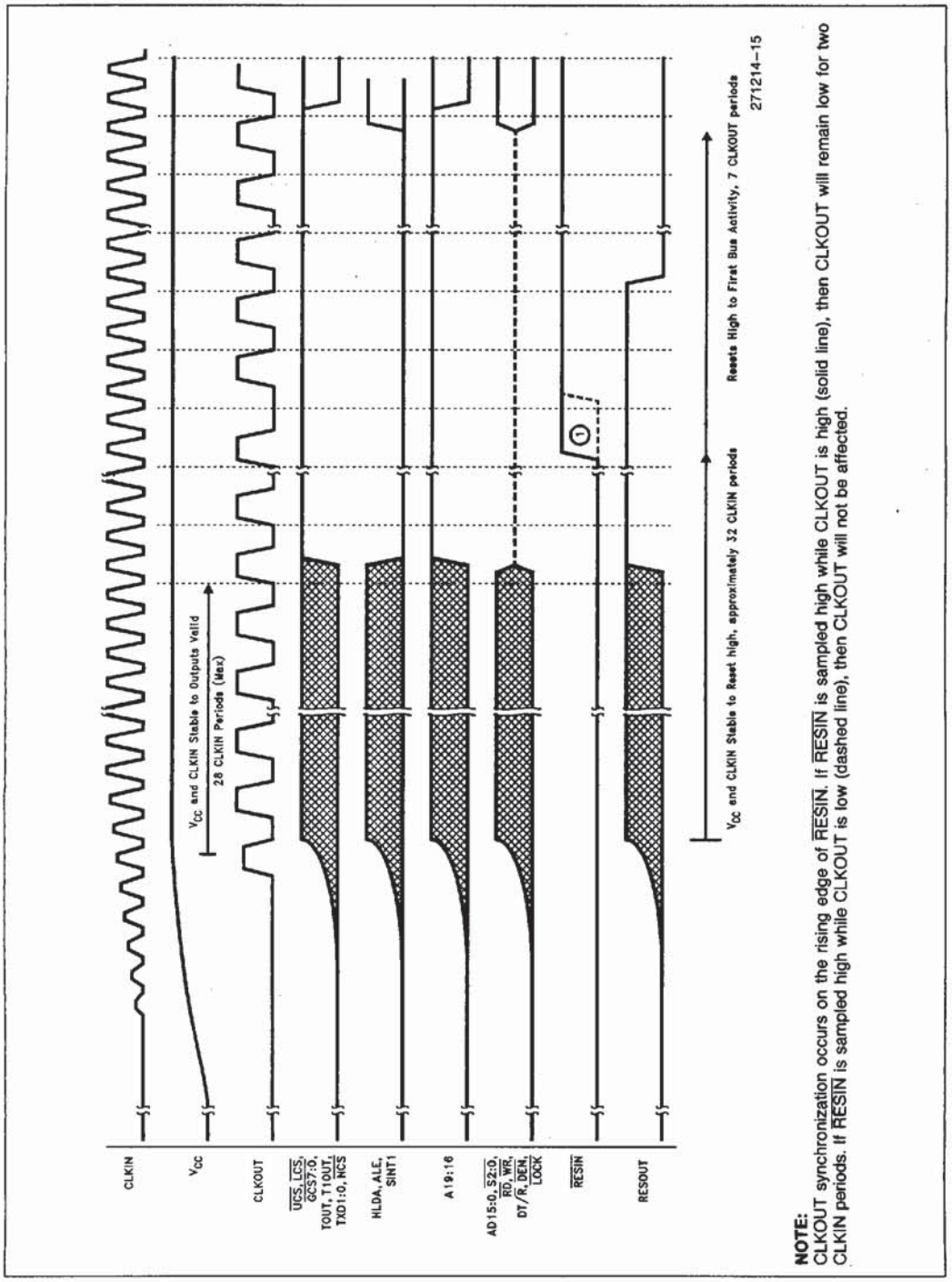
Figure 17 shows the correct reset sequence when first applying power to the M80C186EB. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the M80C186EB. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the M80C186EB. When attaching a crystal to the device, $\overline{\text{RESIN}}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{\text{RESIN}}$ pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{\text{RESIN}}$ is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 18 shows the timing sequence when $\overline{\text{RESIN}}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the M80C186EB to a known operating state. Any bus operation that is in progress at the time $\overline{\text{RESIN}}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{\text{RESIN}}$ is active, bus signals $\overline{\text{LOCK}}$, A19/$\overline{\text{ONCE}}$, and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only 19/$\overline{\text{ONCE}}$ can be overdriven to a low and is used to enable $\overline{\text{ONCE}}$ Mode. Forcing $\overline{\text{LOCK}}$ or A18:16 low at any time while $\overline{\text{RESIN}}$ is low is prohibited and will cause unspecified device operation.

3

COLD RESET WAVEFORMS



NOTE:
CLKOUT synchronization occurs on the rising edge of $\overline{RESIN}$. If $\overline{RESIN}$ is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If $\overline{RESIN}$ is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.

Figure 17

WARM RESET WAVEFORMS

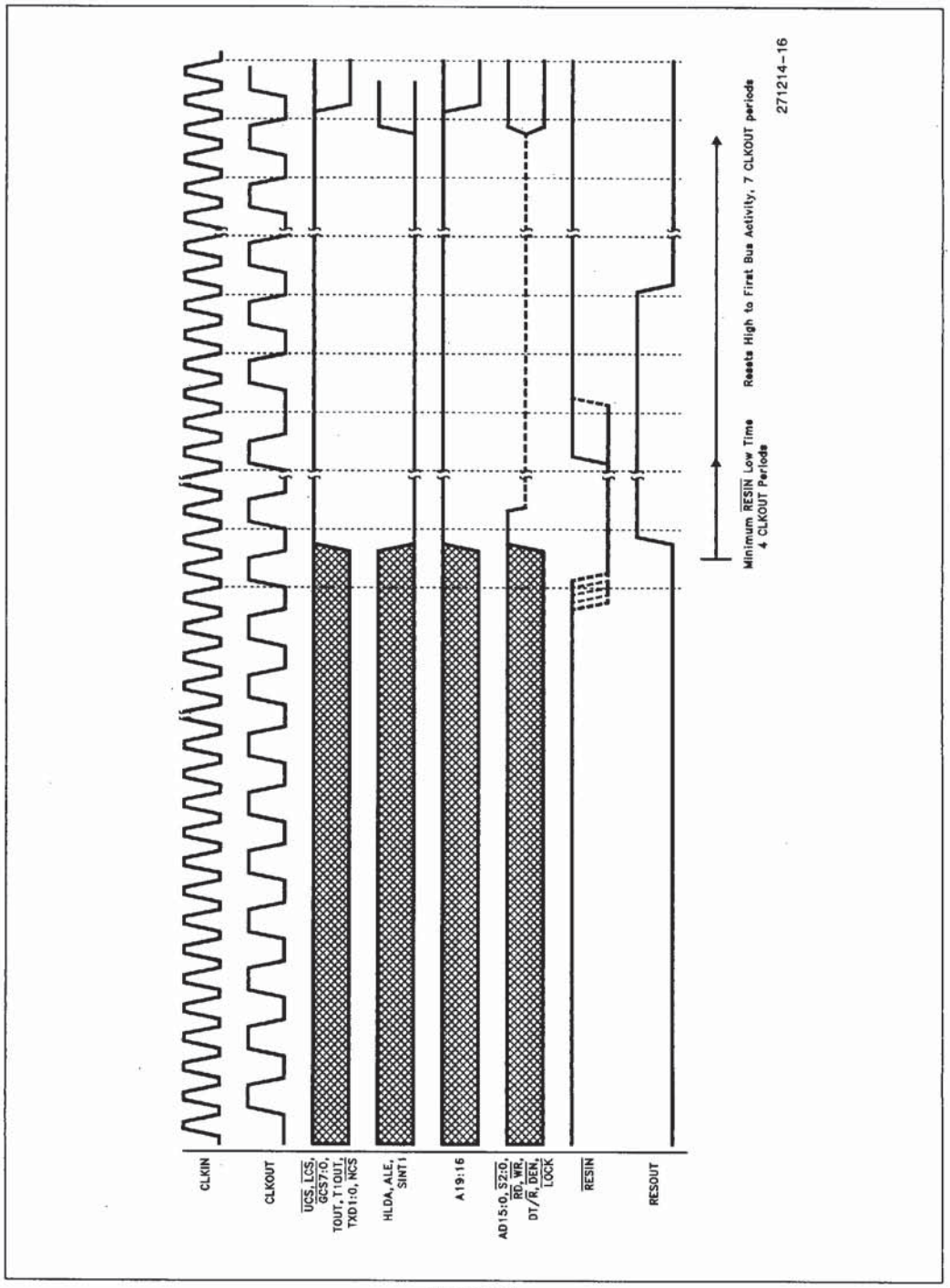


Figure 18

BUS CYCLE WAVEFORMS

Figures 19 through 25 present the various bus cycles that are generated by the M80C186EB. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.

Figure 19 shows the M80C186EB bus state diagram. A typical bus cycle will consist of four consecutive states labeled T1, T2, T3 and T4. A TI state exists when no bus cycle is pending. A TI state can occur if the pre-fetch queue is full, the BIU is waiting for the completion of an effective address calculation, or the BIU is told to wait for a pending EU bus operation. The latter case will occur most often during the sequencing of an interrupt acknowledge or during the execution of numerics escape instructions.

Aside from TI states, multiple T3 states can occur during a bus cycle if READY is not returned in time (or the CSU has been programmed to automatically insert wait-states). A T3 state will be followed by either a T4 state (if a bus cycle is pending), or a TI state (if no bus cycle is pending). Only multiple T3 or TI states can exist (i.e., there is no way to extend the T1, T2 or T4 states).

Figures 20 and 21 present a typical bus read and write operation respectively. Bus read operations include memory, I/O, instruction fetch, and refresh bus cycles. Bus write operations include memory and I/O bus cycles. The only variation among the different bus cycles would be the range of address generated and the state of the status signals.

The Halt bus cycle is shown in Figure 22. Note that the condition of the AD15:0 pin can be either floating or driving depending on the operation of the bus cycle that preceded the Halt. The pins will float if the previous bus cycle was a read, otherwise they will drive. None of the control signals (e.g., $\overline{RD}$, $\overline{WR}$, $\overline{DEN}$, etc.) will be activated, however.

Figure 23 shows the sequence of bus cycles run when an interrupt is acknowledged and the ICU has been programmed for Cascade Mode. Note the address information is not valid for the two bus cycles run, however, also note that $\overline{RD}$ and $\overline{WR}$ are not generated. Vector information needs to be returned during the second bus cycle.

Figures 24 and 25 present the operation of bus HOLD. Figure 24 shows how bus HOLD is entered and exited under normal operating conditions. Figure 25 shows the effect specific bus signals have when a refresh bus cycle request has been generated and the bus is currently unavailable due to a bus HOLD.

The effects of READY on bus operation is shown in Figure 26. READY is useful in extending the bus cycle to meet the various access requirements for memory and peripheral devices in the system. Additional T3 states added to the bus cycle have been appropriately labeled Tw.

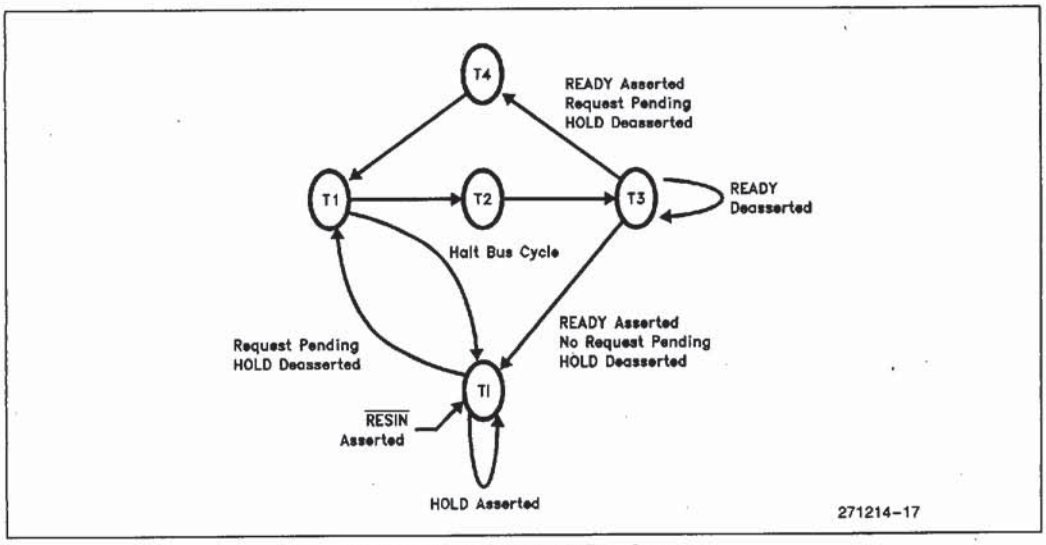


Figure 19. M80C186EB Bus States

MEMORY READ, I/O READ, INSTRUCTION FETCH AND REFRESH WAVEFORM

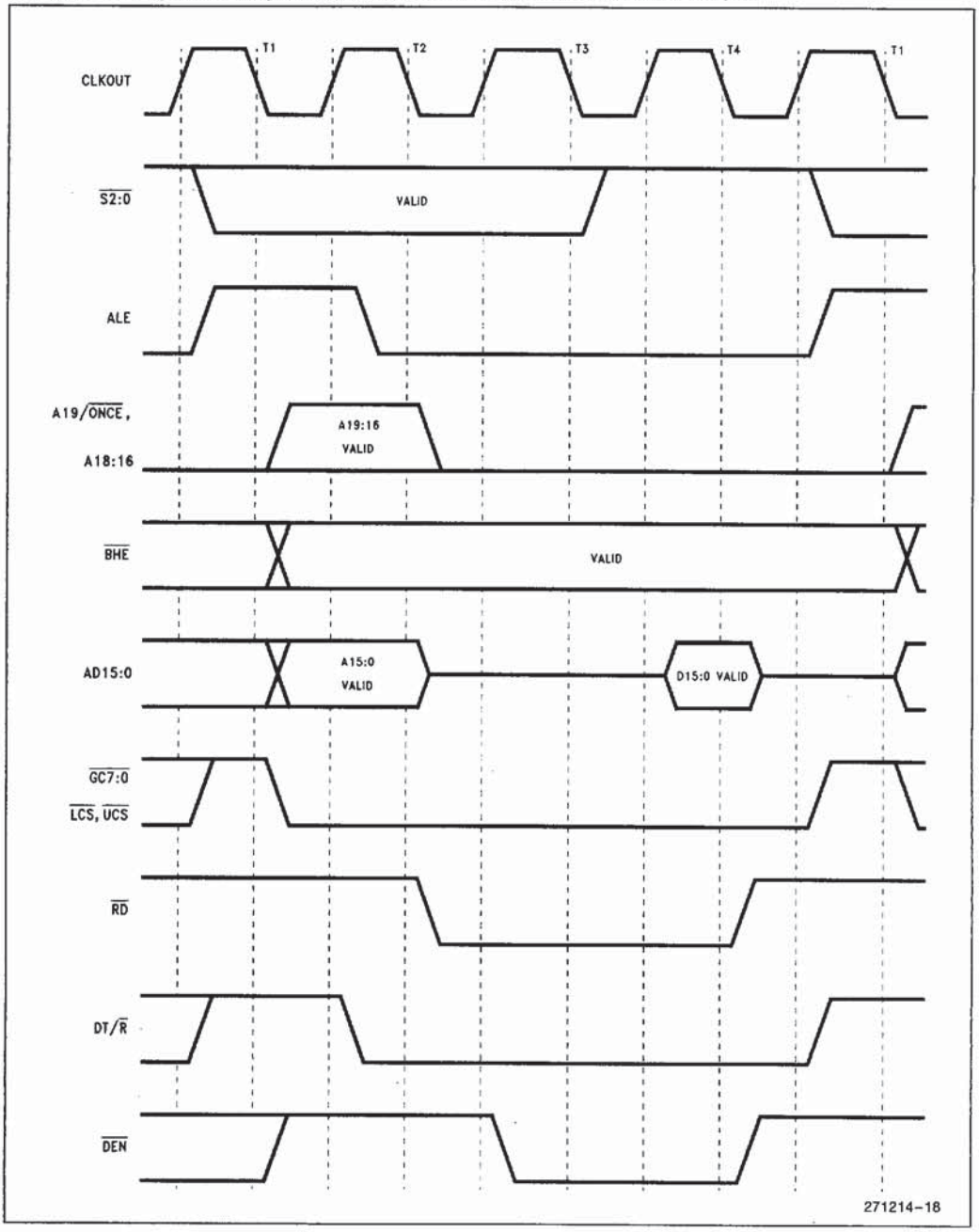


Figure 20

MEMORY WRITE AND I/O WRITE CYCLE WAVEFORM

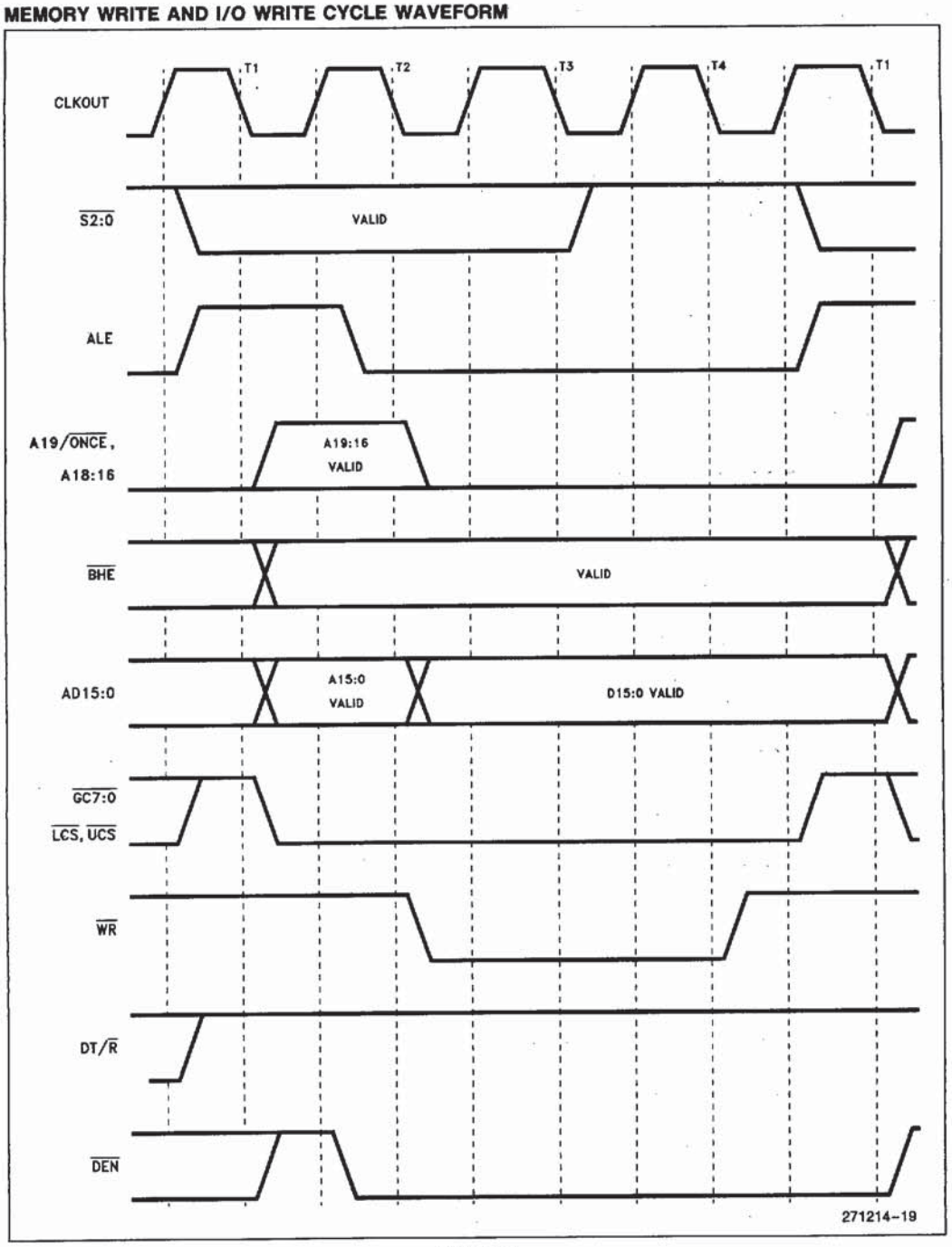
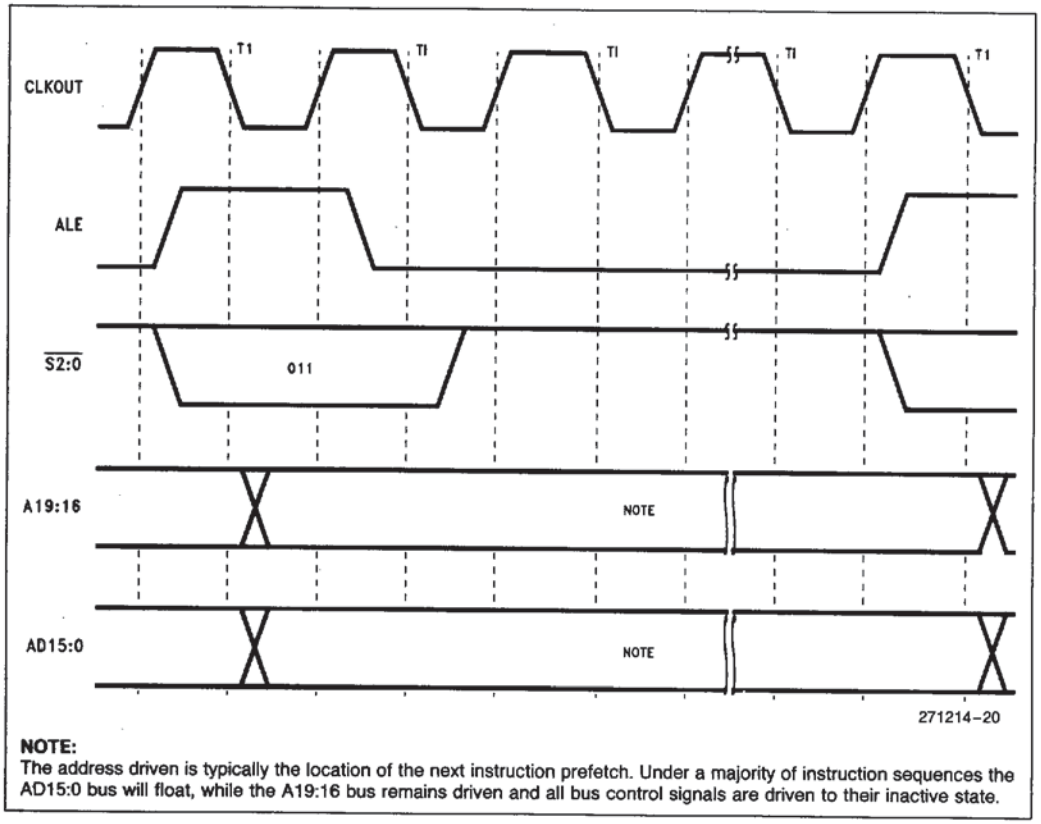


Figure 21

HALT CYCLE WAVEFORM



NOTE:
The address driven is typically the location of the next instruction prefetch. Under a majority of instruction sequences the AD15:0 bus will float, while the A19:16 bus remains driven and all bus control signals are driven to their inactive state.

Figure 22

CASCADE MODE INTERRUPT ACKNOWLEDGE CYCLE WAVEFORM

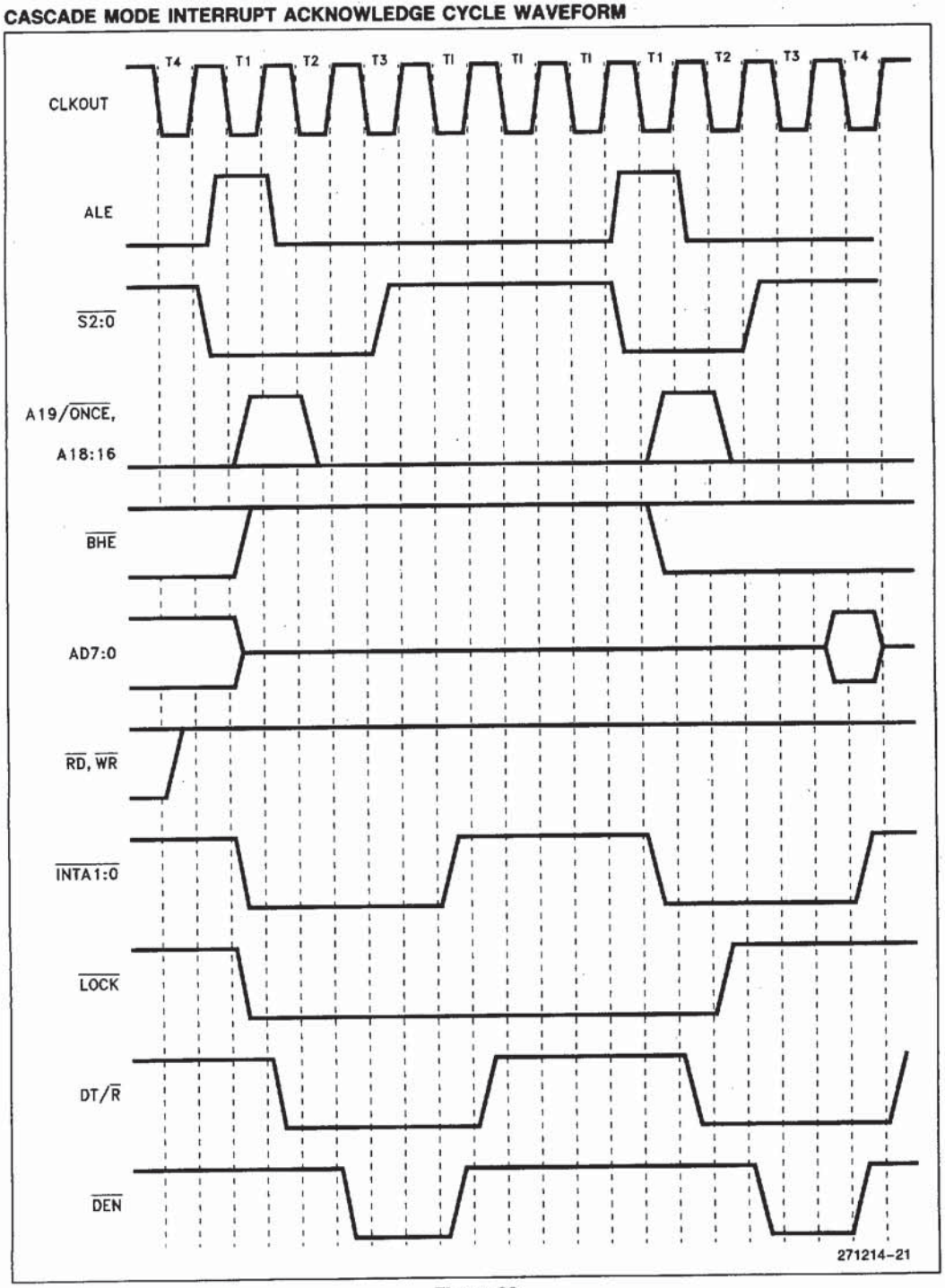


Figure 23

HOLD/HLDA CYCLE WAVEFORMS

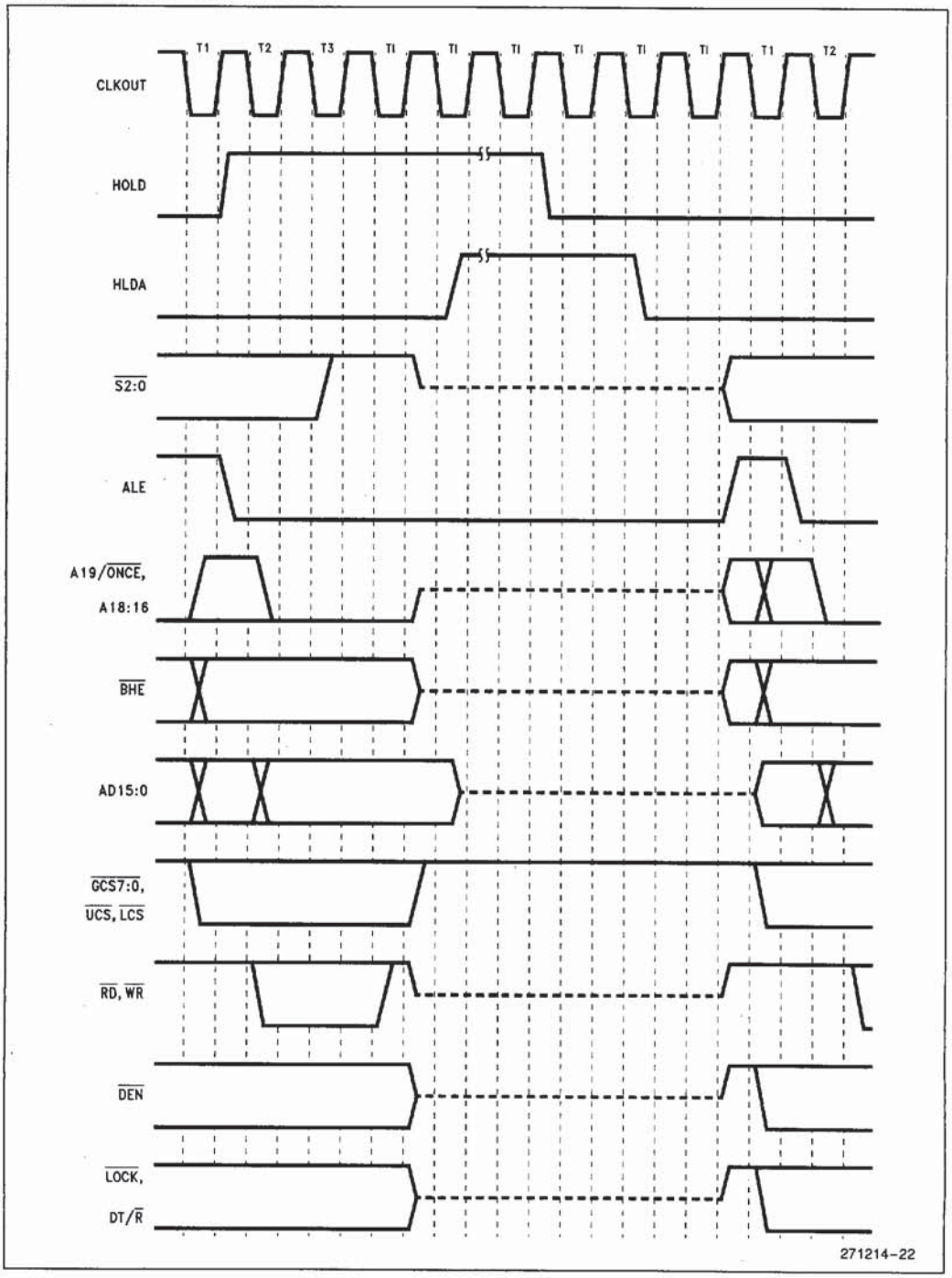
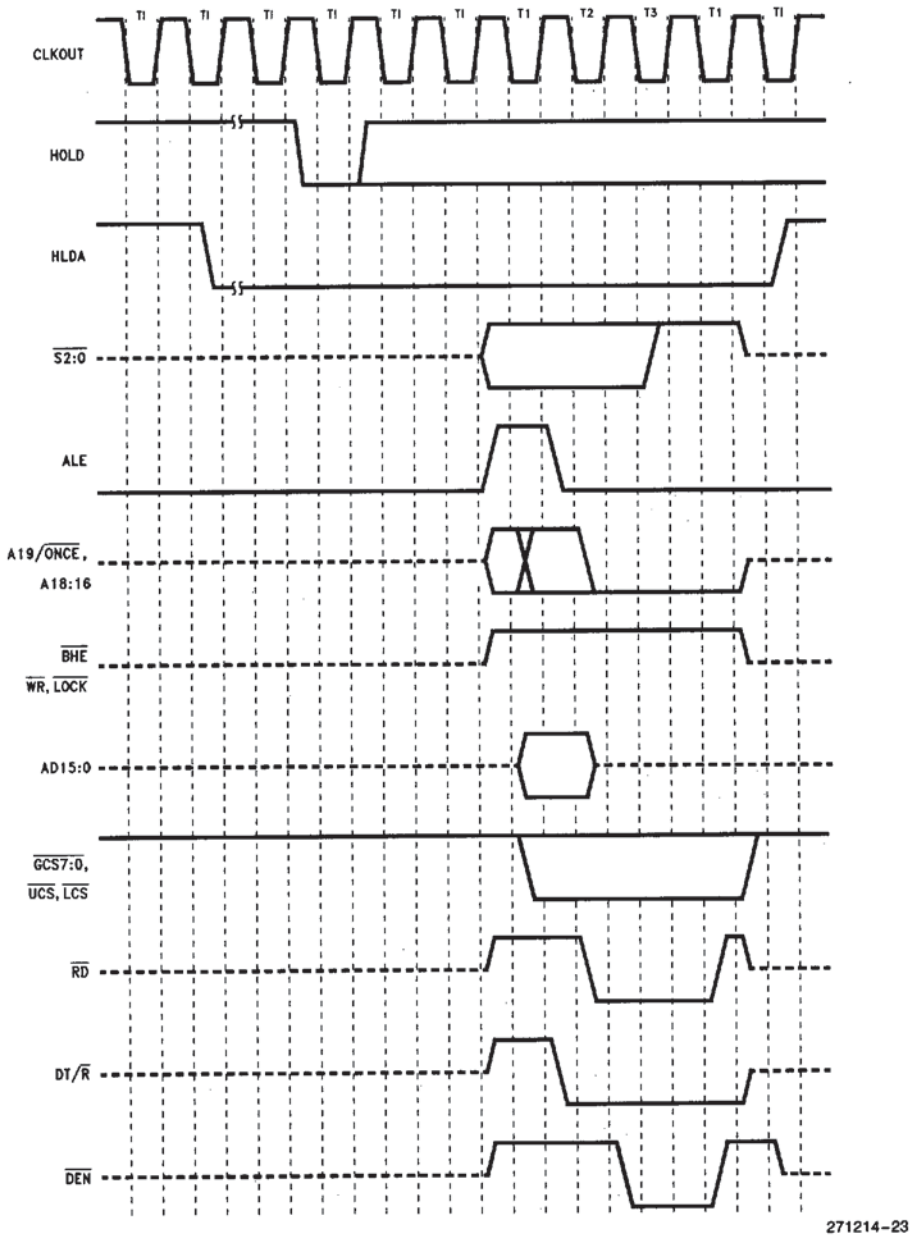


Figure 24

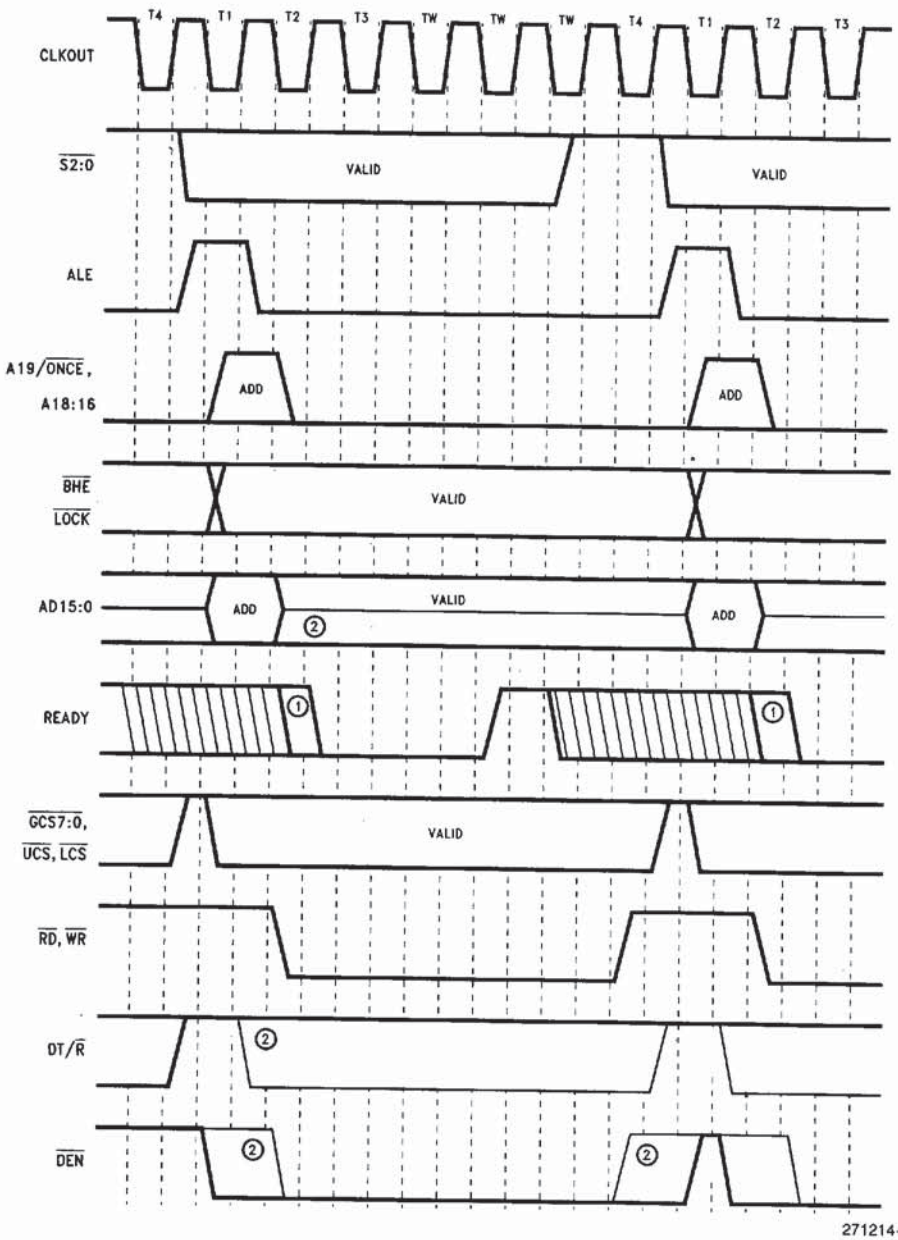
REFRESH DURING HLDA CYCLE WAVEFORM



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 25

READY CYCLE WAVEFORM



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 26

REGISTER BIT SUMMARY

Figures 27 through 34 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is **not** guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes.

Not all defined register bits can be read and/or written, although most registers are read/write. Some registers, like the P1DIR register, exist but do not have any effect on the operation of the M80C186EB. For example, the Port1 pins are output only and cannot be changed by programming the P1DIR register. However, the P1DIR register can still be read and written—which allows the P1DIR register to be used as a temporary 8-bit data register.

Reads and writes to any of the PCB registers will cause a bus cycle to be run externally, however, none of the chip selects will go active (even if they overlap the PCB address range). Data read back from the AD15:0 bus is ignored, and all cycles will take zero wait states (except accesses to the Timer/Counter registers which take one wait state due to internal synchronization).

Figures 27 and 28 present the registers associated with the Interrupt Control Unit (ICU). A write to the MASK (08H) register will also effect the corresponding MSK bit in each of the control registers (e.g., setting the TMR bit in the MASK register will also set the MSK bit in the TMRCON register).

The Timer/Counter Unit registers are presented in Figure 29. The compare and count registers are **not** initialized after reset and must be set correctly during initialization to ensure the timer operates correctly the first time it is enabled.

Figure 30 presents the I/O Port Unit (IPU) registers. Only PD6 and PD7 or of the P2DIR register have any effect on the direction of the port pins (P2.6 and P2.7 respectively). The unused bits of P2DIR and all the bits of P1DIR can be thought of having latches that can be read and written. The two PxLTCH registers have all 8-bits implemented, however, only those port pins which can function as outputs actually use the value programmed into the latch. Otherwise (like the P1DIR register), the registers can be thought of being an 8-bit data register.

Figure 31 presents the register bit definitions of the Serial Communications Unit (SCU). The transmit and receive buffer registers are both readable and writeable. Note that a read from SxSTS register will clear all of the status information (except for CTS, which actually is derived from the pin itself).

The Chip-Select Unit (CSU) registers are presented in Figure 32 and the Refresh Control Unit (RCU) registers are presented in Figure 33. The RFADDR register will indicate the current refresh address when read, and a write to the register will change the next refresh address generated.

Figure 34 presents the PWRCON register and STEPID register. The STEPID register contains a stepping identifier that may or may not change any time there is a change to the M80C186EB silicon die. The STEPID is for Intel use and can change at any time.

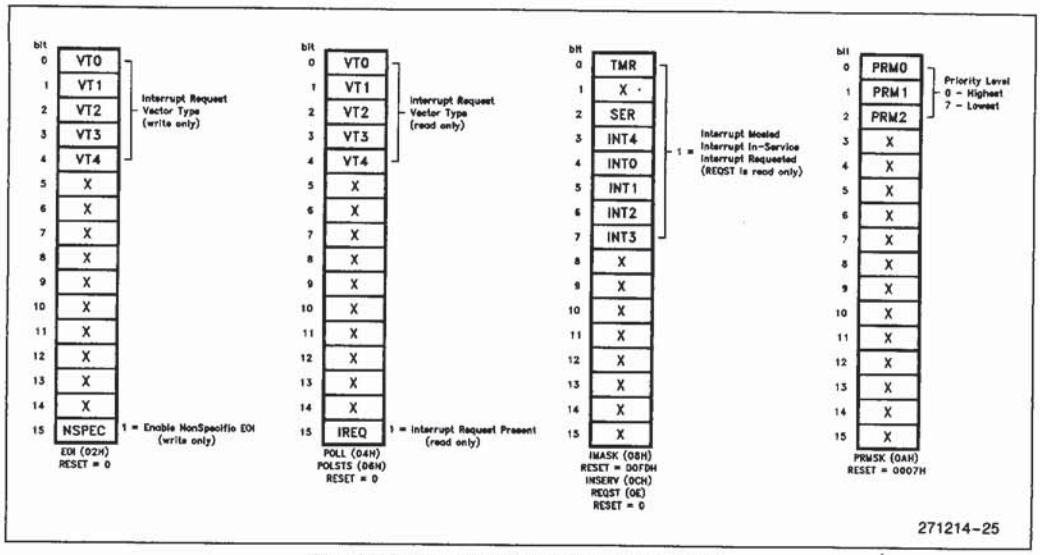


Figure 27. Interrupt Control Unit Registers

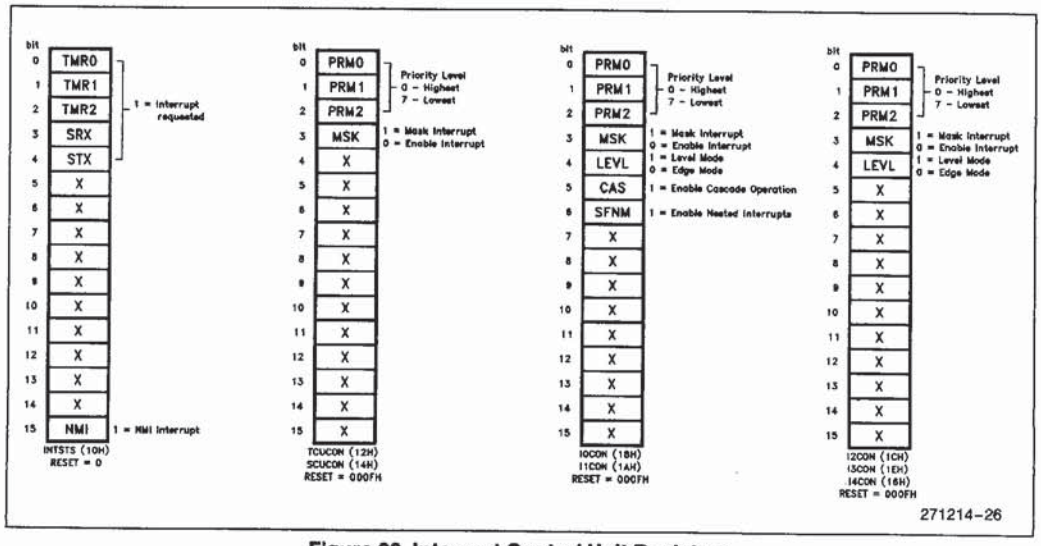


Figure 28. Interrupt Control Unit Registers

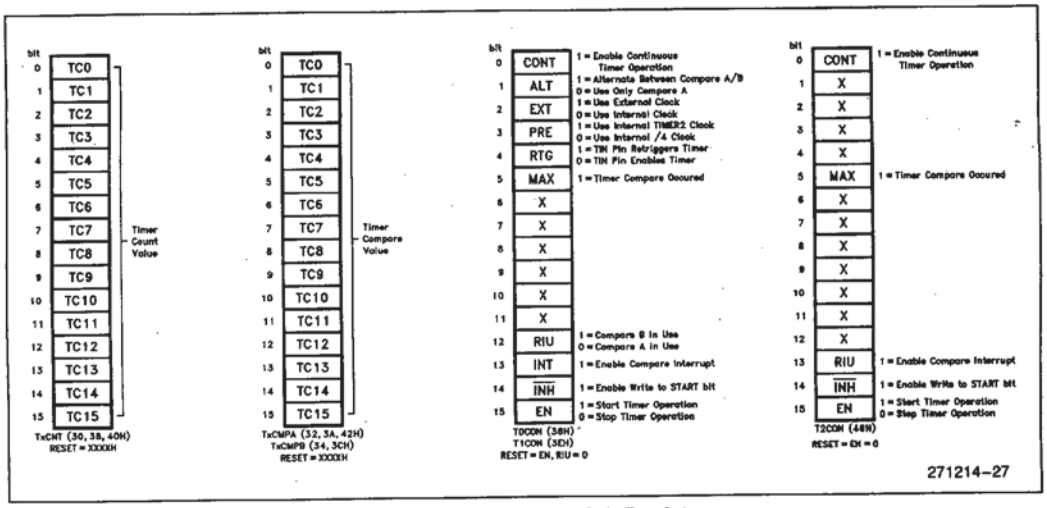


Figure 29. Timer Control Unit Registers

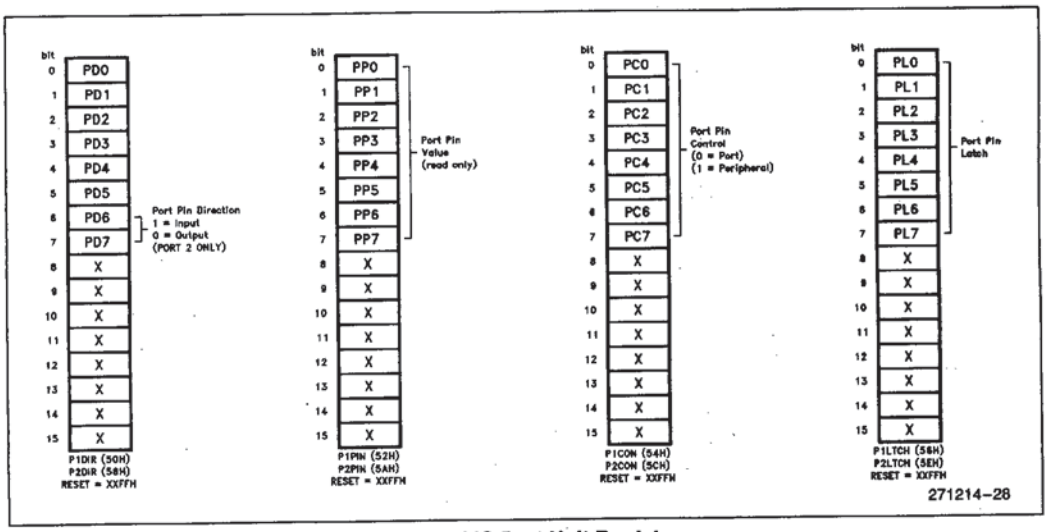


Figure 30. I/O Port Unit Registers

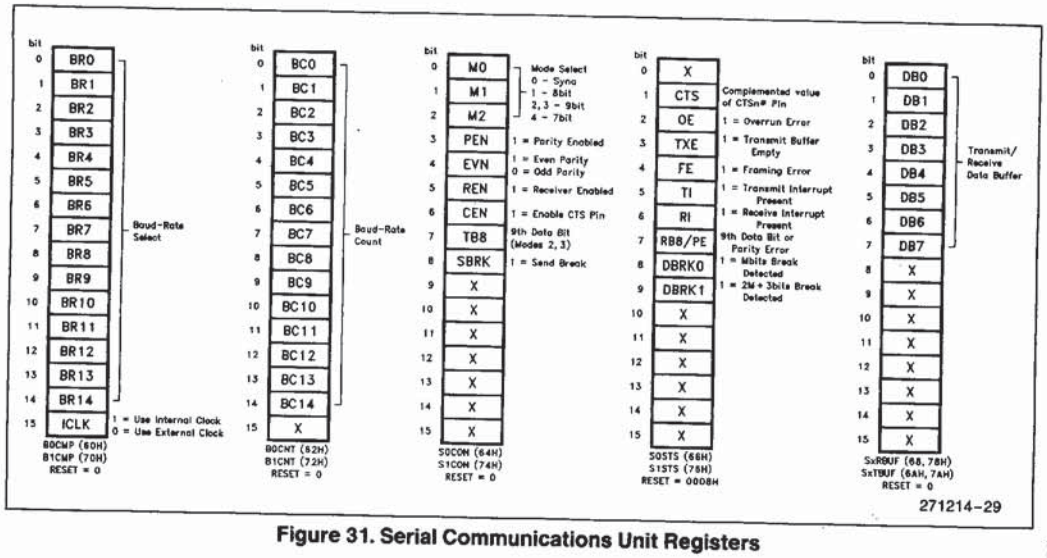


Figure 31. Serial Communications Unit Registers

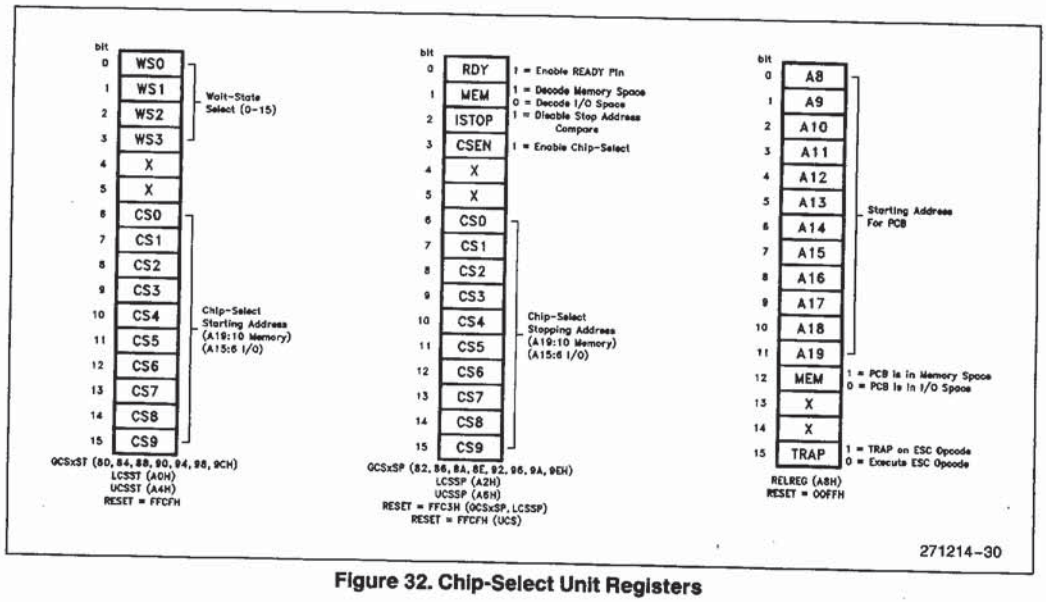


Figure 32. Chip-Select Unit Registers

3

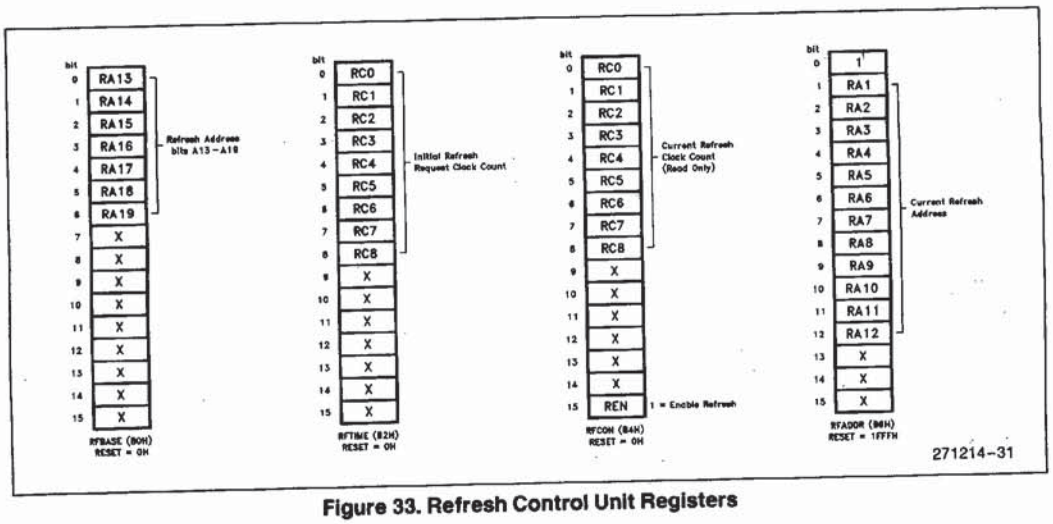


Figure 33. Refresh Control Unit Registers

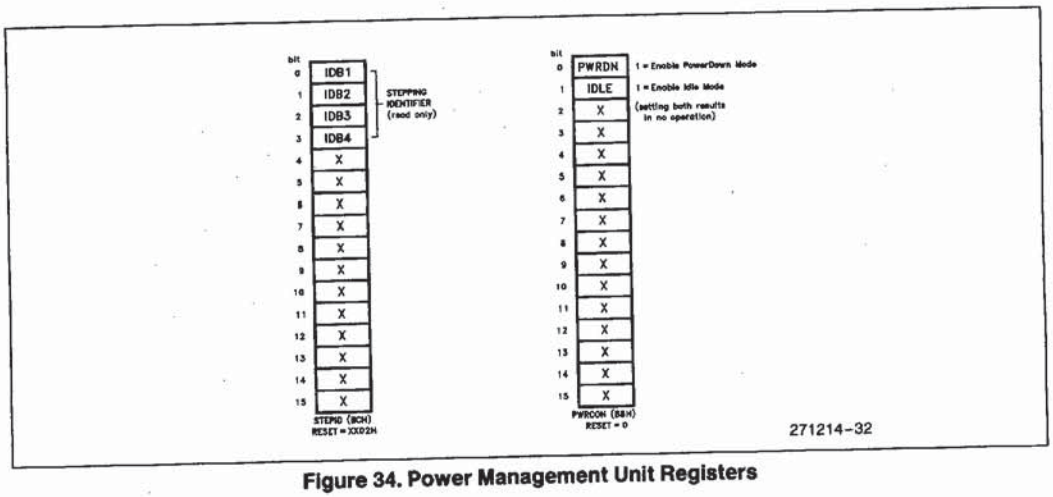


Figure 34. Power Management Unit Registers

M80C186EB EXECUTION TIMINGS

A determination of M80C186EB program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the M80C186EB has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format	Clock Cycles	Comments
DATA TRANSFER			
MOV = Move:			
Register to Register/Memory	1000100w mod reg r/m	2/12	
Register/memory to register	1000101w mod reg r/m	2/9	
Immediate to register/memory	1100011w mod 000 r/m data data if w=1	12–13	8/16-bit
Immediate to register	1011w reg data data if w=1	3–4	8/16-bit
Memory to accumulator	1010000w addr-low addr-high	8	
Accumulator to memory	1010001w addr-low addr-high	9	
Register/memory to segment register	10001110 mod 0 reg r/m	2/9	
Segment register to register/memory	10001100 mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	11111111 mod 110 r/m	16	
Register	01010 reg	10	
Segment register	000reg110	9	
Immediate	011010s0 data data if s=0	10	
PUSHA = Push All	01100000	36	
POP = Pop:			
Memory	10001111 mod000 r/m	20	
Register	01011 reg	10	
Segment register	000reg111 (reg≠01)	8	
POPA = Pop All	01100001	51	
XCHG = Exchange:			
Register/memory with register	1000011w mod reg r/m	4/17	
Register with accumulator	10010 reg	3	
IN = Input from:			
Fixed port	1110010w port	10	
Variable port	1110110w	8	
OUT = Output to:			
Fixed port	1110011w port	9	
Variable port	1110111w	7	
XLAT = Translate byte to AL	11010111	11	
LEA = Load EA to register	10001101 mod reg r/m	6	
LDS = Load pointer to DS	11000101 mod reg r/m (mod≠11)	18	
LES = Load pointer to ES	11000100 mod reg r/m (mod≠11)	18	
LAHF = Load AH with flags	10011111	2	
SAHF = Store AH into flags	10011110	3	
PUSHF = Push flags	10011100	9	
POPF = Pop flags	10011101	8	

Shaded areas indicate instructions not available in M8086/M8088 microsystems.

3

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
DATA TRANSFER (Continued)			
SEGMENT = Segment Override:			
CS	00101110	2	
SS	00110110	2	
DS	00111110	2	
ES	00100110	2	
ARITHMETIC			
ADD = Add:			
Reg/memory with register to either	000000dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 000 r/m | data | data if s w=01	4/16	
Immediate to accumulator	0000010w | data | data if w=1	3/4	8/16-bit
ADC = Add with carry:			
Reg/memory with register to either	000100dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w=01	4/16	
Immediate to accumulator	0001010w | data | data if w=1	3/4	8/16-bit
INC = Increment:			
Register/memory	1111111w | mod 000 r/m	3/15	
Register	01000 reg	3	
SUB = Subtract:			
Reg/memory and register to either	001010dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 101 r/m | data | data if s w=01	4/16	
Immediate from accumulator	0010110w | data | data if w=1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg/memory and register to either	000110dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w=01	4/16	
Immediate from accumulator	0001110w | data | data if w=1	3/4	8/16-bit
DEC = Decrement			
Register/memory	1111111w | mod 001 r/m	3/15	
Register	01001 reg	3	
CMP = Compare:			
Register/memory with register	0011101w | mod reg r/m	3/10	
Register with register/memory	0011100w | mod reg r/m	3/10	
Immediate with register/memory	100000sw | mod 111 r/m | data | data if s w=01	3/10	
Immediate with accumulator	0011110w | data | data if w=1	3/4	8/16-bit
NEG = Change sign register/memory	1111011w | mod 011 r/m	3/10	
AAA = ASCII adjust for add	00110111	8	
DAA = Decimal adjust for add	00100111	4	
AAS = ASCII adjust for subtract	00111111	7	
DAS = Decimal adjust for subtract	00101111	4	
MUL = Multiply (unsigned):	1111011w | mod 100 r/m		
Register-Byte		26–28	
Register-Word		35–37	
Memory-Byte		32–34	
Memory-Word		41–43	

Shaded areas indicate instructions not available in M8086/M8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
IMUL = Integer multiply (signed):	1111011w | mod101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43	
IMUL = Integer immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1111011w | mod111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = **And:**			
Reg/memory and register to either	001000dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod100 r/m | data | data if w=1	4/16	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1000010w | mod reg r/m	3/10	
Immediate data and register/memory	1111011w | mod000 r/m | data | data if w=1	4/10	
Immediate data and accumulator	1010100w | data | data if w=1	3/4	8/16-bit
OR = **Or:**			
Reg/memory and register to either	000010dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod001 r/m | data | data if w=1	4/16	
Immediate to accumulator	0000110w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in M8086/M8088 microsystems.

3

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
LOGIC (Continued)			
XOR = Exclusive or:			
Reg/memory and register to either	001100dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod 110 r/m | data | data if w=1	4/16	
Immediate to accumulator	0011010w | data | data if w=1	3/4	8/16-bit
NOT = Invert register/memory	1111011w | mod 010 r/m	3/10	
STRING MANIPULATION			
MOVS = Move byte/word	1010010w	14	
CMPS = Compare byte/word	1010011w	22	
SCAS = Scan byte/word	1010111w	15	
LODS = Load byte/wd to AL/AX	1010110w	12	
STOS = Store byte/wd from AL/AX	1010101w	10	
INS = Input byte/wd from DX port	0110110w	14	
OUTS = Output byte/wd to DX port	0110111w	14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)			
MOVS = Move string	11110010 | 1010010w	8+8n	
CMPS = Compare string	1111001z | 1010011w	5+22n	
SCAS = Scan string	1111001z | 1010111w	5+15n	
LODS = Load string	11110010 | 1010110w	6+11n	
STOS = Store string	11110010 | 1010101w	6+9n	
INS = Input string	11110010 | 0110110w	8+8n	
OUTS = Output string	11110010 | 0110111w	8+8n	
CONTROL TRANSFER			
CALL = Call:			
Direct within segment	11101000 | disp-low | disp-high	15	
Register/memory indirect within segment	11111111 | mod 010 r/m	13/19	
Direct intersegment	10011010 | segment offset | segment selector	23	
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	38	
JMP = Unconditional jump:			
Short/long	11101011 | disp-low	14	
Direct within segment	11101001 | disp-low | disp-high	14	
Register/memory indirect within segment	11111111 | mod 100 r/m	11/17	
Direct intersegment	11101010 | segment offset | segment selector	14	
Indirect intersegment	11111111 | mod 101 r/m (mod ≠ 11)	26	

Shaded areas indicate instructions not available in M8086/M8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = Return from CALL:						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110 000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22 + 16(n − 1)	
LEAVE = Leave Procedure	11001001				8	
INT = Interrupt:						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in M8086/M8088 microsystems.

3

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if TEST = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in M8086/M8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

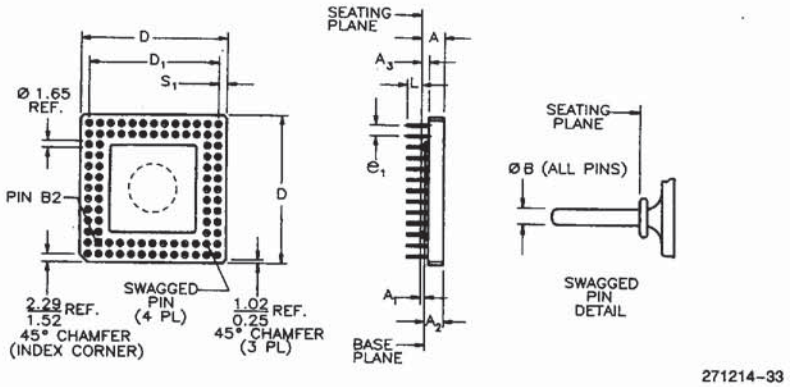
reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

88-LEAD CERAMIC PIN GRID ARRAY PACKAGE



271214-33

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	33.91	34.67		1.335	1.365	
D_1	30.35	30.61		1.195	1.205	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	88			88		
S_1	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

3

ERRATA

The current stepping (B step) of the M80C186EB has the following known functional anomaly.

An internal problem with the interrupt controller may prevent an acknowledge cycle from occurring on the INTA1 line after an interrupt on INT1. This error only occurs when INT1 is configured in cascaded mode and a higher priority interrupt exists.

Problem:

An interrupt acknowledge for INT1 is not generated on INTA1 in some conditions.

Condition:

Another interrupt of higher priority occurs after the decision is made to service Interrupt 1, but before the expected acknowledge cycle on INTA1.

Configuration:

1. Master mode
2. INT1 is in cascade mode and is enabled.
3. An interrupt of higher priority than INT1 is enabled (i.e., DMA, timers, serial ports, INT lines).

Workaround:

There are only two possible situations that might cause this problem. These, with their corresponding workarounds are described in the table below.

	Condition	Workaround
1.	Only INT1 is configured in cascade mode and is also a lower priority than another interrupt.	Use INT0 in cascaded mode instead, or make INT1 the highest priority interrupt.
2.	INT1 and INT0 are both in cascade mode and INT1 is of lower priority than another interrupt.	Change the priority of INT1 to the highest priority of all interrupts.

REVISION HISTORY

The first revision of this data sheet (271214-001) indicated only 8 MHz and 13 MHz availability. The M80C186EB will also be available in a 16 MHz version. The cover and various other locations in the data sheet reflect the additional product speed offering.

The following list reflects the changes made between the -001 version and this -002 version of the M80C186EB data sheet.

1. Operating Conditions section updated to reflect 16 MHz Input clock frequency limits.
2. DC Specifications section: Added notes regarding untested values: added/changed input leakage current and input current symbols and values; added 16 MHz I_{CC}, I_{ID} and I_{PD} values.
3. AC Specifications section: Added full 16 MHz AC Characteristics; added note about untested values and reduced minimum output delays (T_{CHOV} and T_{CLOV}) for all speeds.
4. Modified Errata section to reflect B-step known errata (INT1 acknowledge anomaly).